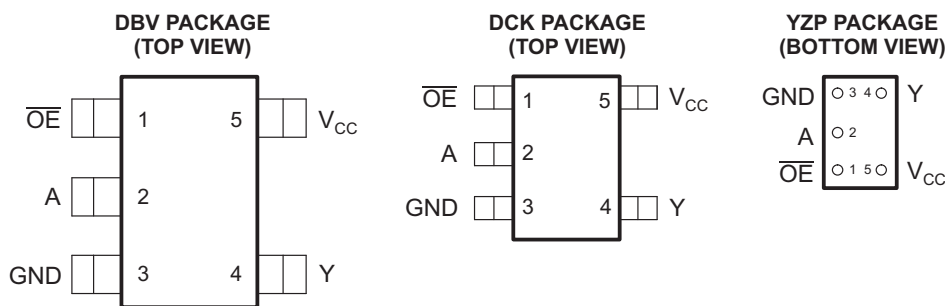


具有三态输出的单通道缓冲器/驱动器

 查询样品: [SN74AUC1G240](#)

特性

- 采用德州仪器的 **NanoFree™** 封装
- 专为 **1.8V** 工作电压而优化并具有 **3.6V I/O** 的电压容忍范围, 旨在支持混合模式信号操作
- **I_{off}** 支持部分断电模式操作
- 可在低于 **1V** 的电压下操作
- 最大 **t_{pd}** 为 **2.5ns** (在 **1.8V** 时)
- 低功耗: **10μA** 最大 **I_{CC}**
- **±8mA** 输出驱动 (在 **1.8V** 时)
- 高速操作 (典型)
 - **350 Mhz at 2.5 V**
 - **300 Mhz at 1.8 V**
 - **250 Mhz at 1.5 V**
 - **100 Mhz at 0.8 V**
- 锁断性能超过 **100mA** (符合 **JESD 78 Class II** 规范的要求)
- **ESD** 保护等级超过 **JESD 22** 标准的要求
 - **2000-V** 人体模型 (**A114-A**)
 - **200-V** 机器模型 (**A115-A**)
 - **1000 V** 充电器件模型 (**C101**)



See mechanical drawings for dimensions.

说明/订购信息

该总线缓冲器门电路虽然专门针对 1.65V 至 1.95V V_{CC} 工作范围而特别设计, 但可以在 0.8V 至 2.7V V_{CC} 的范围内工作。

SN74AUC1G240 是一款具有一个三态输出的单通道线路驱动器。当输出使能 ($\overline{\text{OE}}$) 输入为高电平时, 输出被停用。

为了确保上电或断电期间的高阻抗状态, $\overline{\text{OE}}$ 应通过一个上拉电阻器连接至 V_{CC}; 该电阻器的最小值由驱动器的电流吸收能力来决定。

NanoFree™ 封装技术是 IC 封装概念的一项重大突破, 它将硅晶片用作封装。

该器件的技术规格针对采用 I_{off} 的部分断电应用而全面拟订。I_{off} 电路负责停用输出, 从而可防止破坏性的电流在其断电时通过器件回流。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: [SCES384I](#)

订购信息

T _A	封装 ⁽¹⁾		可订购部件号	正面标记 ⁽²⁾
-40°C 至 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	3000 卷带	SN74AUC1G240YZPR	_ _ _UK_
	SOT (SOT-23) – DBV	3000 卷带	SN74AUC1G240DBVR	U40_
	SOT (SC-70) – DCK	3000 卷带	SN74AUC1G240DCKR	UK_

(1) 封装图示、标准包装数量、散热数据、符号以及 PCB 设计指南：www.ti.com/sc/package。

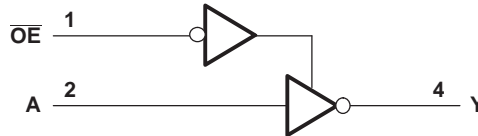
(2) DBV / DCK：实际的顶端标记具有一个用于标明装配/测试场所的附加字符。

YZP：实际的顶端标记具有3个用于表示年、月和序列码的前置字符，以及1个用于标明装配/测试场所的后置字符。

FUNCTION TABLE

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	L
L	L	H
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	3.6	V
V _I	Input voltage range ⁽²⁾	-0.5	3.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	3.6	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±20 mA
	Continuous current through V _{CC} or GND			±100 mA
θ _{JA}	Package thermal impedance ⁽³⁾	DBV package		206
		DCK package		252
		YZP package		132
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8\text{ V}$	V_{CC}	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \blacklozenge V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \blacklozenge V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8\text{ V}$	-0.7	mA
		$V_{CC} = 1.1\text{ V}$	-3	
		$V_{CC} = 1.4\text{ V}$	-5	
		$V_{CC} = 1.65\text{ V}$	-8	
		$V_{CC} = 2.3\text{ V}$	-9	
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	0.7	mA
		$V_{CC} = 1.1\text{ V}$	3	
		$V_{CC} = 1.4\text{ V}$	5	
		$V_{CC} = 1.65\text{ V}$	8	
		$V_{CC} = 2.3\text{ V}$	9	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }1.6\text{ V}$	20	ns/V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	10	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	3	
T_A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} - 0.1			V
		I _{OH} = -0.7 mA	0.8 V	0.55			
		I _{OH} = -3 mA	1.1 V	0.8			
		I _{OH} = -5 mA	1.4 V	1			
		I _{OH} = -8 mA	1.65 V	1.2			
		I _{OH} = -9 mA	2.3 V	1.8			
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V	0.2			V
		I _{OL} = 0.7 mA	0.8 V	0.25			
		I _{OL} = 3 mA	1.1 V	0.3			
		I _{OL} = 5 mA	1.4 V	0.4			
		I _{OL} = 8 mA	1.65 V	0.45			
		I _{OL} = 9 mA	2.3 V	0.6			
I _I	A or \overline{OE} input	V _I = V _{CC} or GND	0 to 2.7 V	±5			μA
I _{off}		V _I or V _O = 2.7 V	0	±10			μA
I _{OZ}		V _O = V _{CC} or GND	2.7 V	±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V	10			μA
C _I		V _I = V _{CC} or GND	2.5 V	2.5			pF
C _O		V _O = V _{CC} or GND	2.5 V	5.5			pF

(1) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	4.5	0.6	3.3	0.7	2.2	0.6	1	1.7	0.4	1.4	ns
t _{en}	\overline{OE}	Y	5.5	0.7	4.1	0.5	2.6	0.5	1.2	1.9	0.5	1.6	ns
t _{dis}	\overline{OE}	Y	5	1.5	4.3	0.9	4.1	1.2	2.3	3.3	0.8	2.3	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 1)

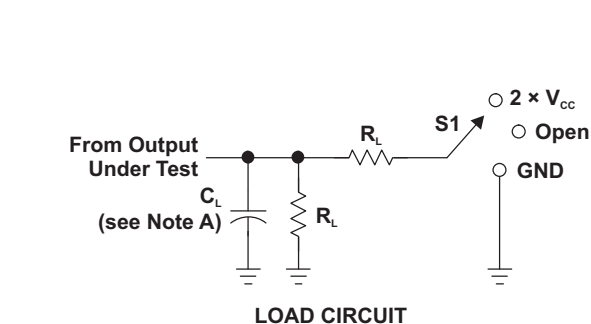
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	0.5	1.5	2.5	0.8	1.7	ns
t _{en}	\overline{OE}	Y	0.7	1.6	2.6	0.6	1.9	ns
t _{dis}	\overline{OE}	Y	2	2.4	3.1	0.8	1.7	ns

Operating Characteristics

 $T_A = 25^\circ\text{C}$

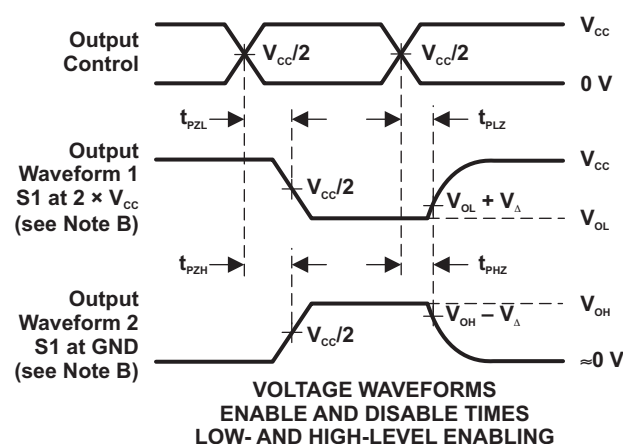
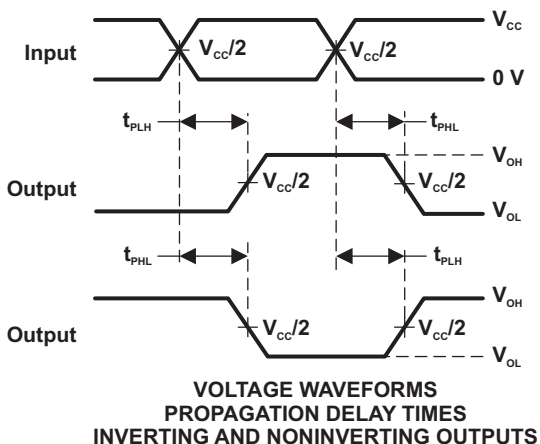
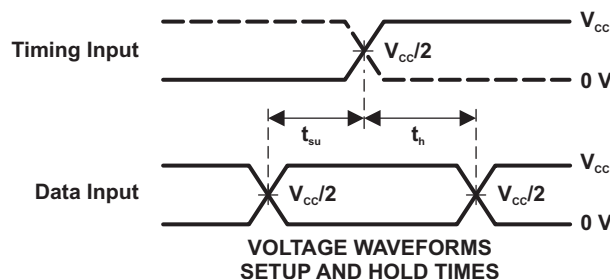
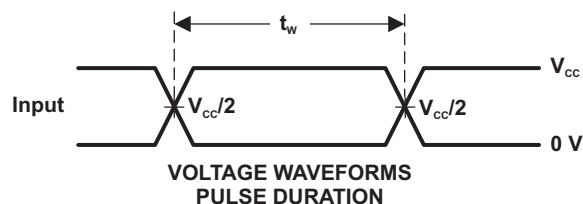
PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT	
			TYP	TYP	TYP	TYP	TYP		
C_{pd}	Power dissipation capacitance	Outputs enabled Outputs disabled	f = 10 MHz	14	14	14	14	15	pF
				1	1	1	1	2	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_A
0.8 V	15 pF	2 kΩ	0.1 V
$1.2 V \pm 0.1 V$	15 pF	2 kΩ	0.1 V
$1.5 V \pm 0.1 V$	15 pF	2 kΩ	0.1 V
$1.8 V \pm 0.15 V$	15 pF	2 kΩ	0.15 V
$2.5 V \pm 0.2 V$	15 pF	2 kΩ	0.15 V
$1.8 V \pm 0.15 V$	30 pF	1 kΩ	0.15 V
$2.5 V \pm 0.2 V$	30 pF	500 Ω	0.15 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUC1G240DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U40R
SN74AUC1G240DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U40R
SN74AUC1G240DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(UK5, UKR)
SN74AUC1G240DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(UK5, UKR)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G240DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC1G240DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G240DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUC1G240DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

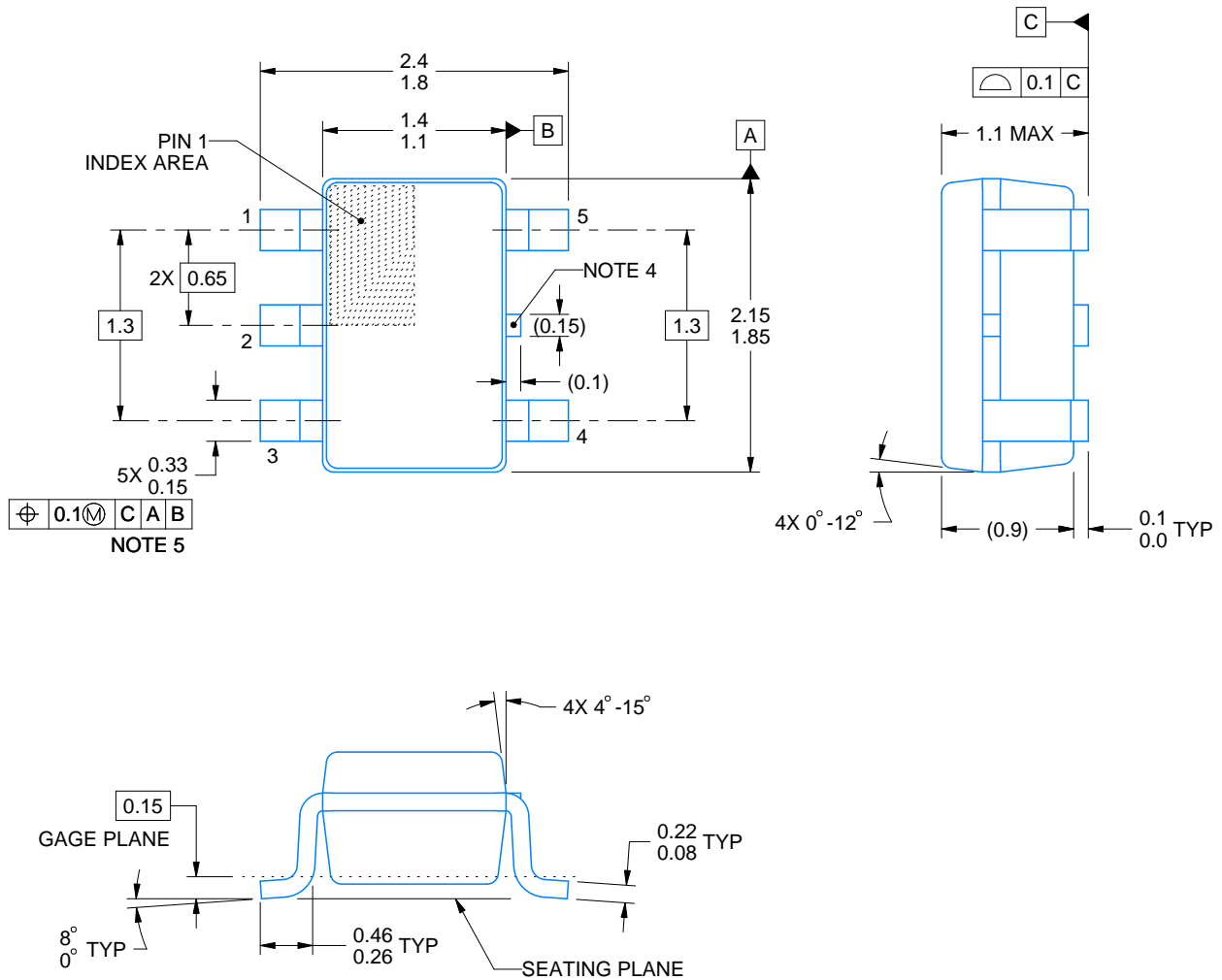
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

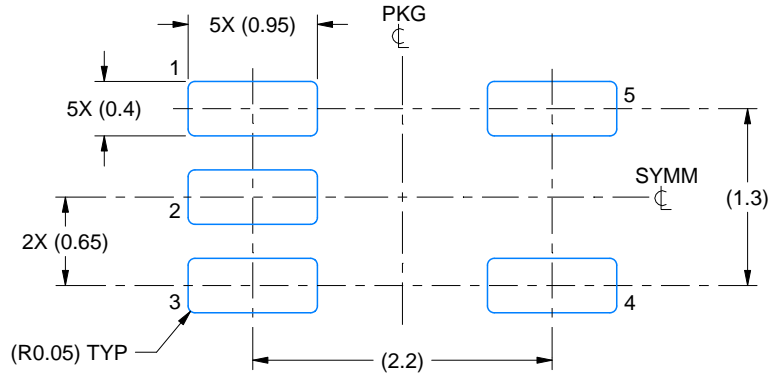
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

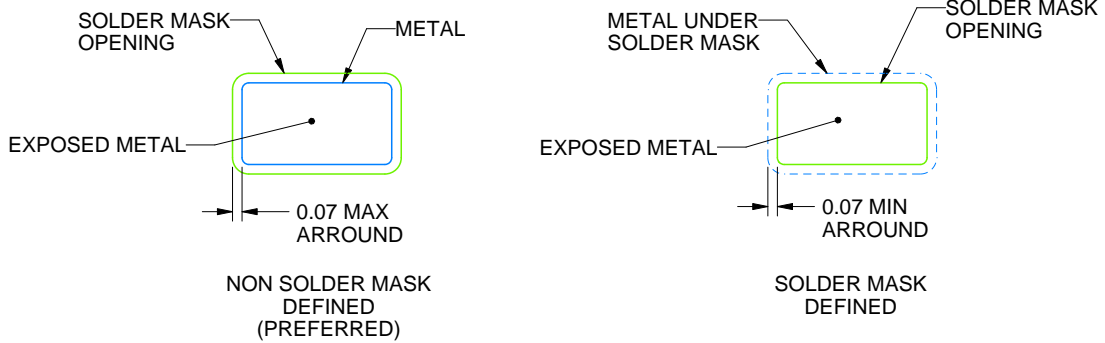
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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