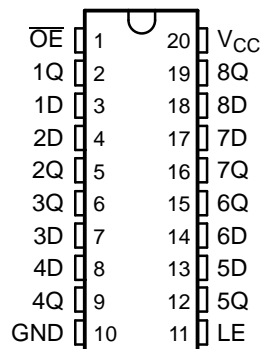


FEATURES

- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 3.3 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DG, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SOIC - DW | Tube | SN74ALVCH373DW | ALVCH373 |
| | | Tape and reel | SN74ALVCH373DWR | |
| | TSSOP - PW | Tape and reel | SN74ALVCH373PWR | VB373 |
| | TVSOP - DGV | Tape and reel | SN74ALVCH373DGVR | VB373 |
| | VFBGA - GQN | Tape and reel | SN74ALVCH373GQNR | VB373 |
| | VFBGA - ZQN (Pb-free) | | SN74ALVCH373ZQNR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

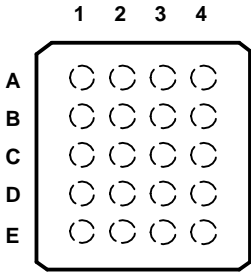


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74ALVCH373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES116H–JULY 1997–REVISED OCTOBER 2004

GQN OR ZQN PACKAGE
(TOP VIEW)



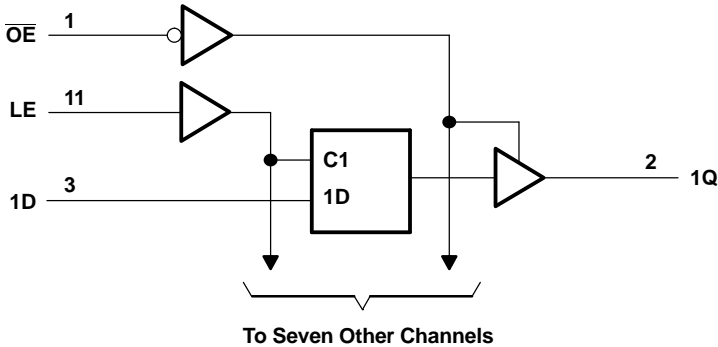
TERMINAL ASSIGNMENTS

| | 1 | 2 | 3 | 4 |
|---|-----|-----------------|----------|----|
| A | 1Q | \overline{OE} | V_{CC} | 8Q |
| B | 2D | 7D | 1D | 8D |
| C | 3Q | 2Q | 6Q | 7Q |
| D | 4D | 5D | 3D | 6D |
| E | GND | 4Q | LE | 5Q |

FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT Q |
|-----------------|----|---|-------------|
| \overline{OE} | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGV, DW, and PW packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|-----------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 4.6 | V |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGV package | 92 | °C/W |
| | | DW package | 58 | |
| | | GQN/ZQN package | 78 | |
| | | PW package | 83 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|--|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 0.7 | |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 0.8 | |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 1.65 \text{ V}$ | -4 | mA |
| | | $V_{CC} = 2.3 \text{ V}$ | -12 | |
| | | $V_{CC} = 2.7 \text{ V}$ | -12 | |
| | | $V_{CC} = 3 \text{ V}$ | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65 \text{ V}$ | 4 | mA |
| | | $V_{CC} = 2.3 \text{ V}$ | 12 | |
| | | $V_{CC} = 2.7 \text{ V}$ | 12 | |
| | | $V_{CC} = 3 \text{ V}$ | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 5 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH373

OCTAL TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCES116H–JULY 1997–REVISED OCTOBER 2004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------------|----------------|---|-----------------|----------------|--------------------|-----------|---------|
| V_{OH} | | $I_{OH} = -100 \mu A$ | 1.65 V to 3.6 V | $V_{CC} - 0.2$ | | | V |
| | | $I_{OH} = -4 \text{ mA}$ | 1.65 V | 1.2 | | | |
| | | $I_{OH} = -6 \text{ mA}$ | 2.3 V | 2 | | | |
| | | $I_{OH} = -12 \text{ mA}$ | 2.3 V | 1.7 | | | |
| | | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | | $I_{OH} = -24 \text{ mA}$ | 3 V | 2 | | | |
| V_{OL} | | $I_{OL} = 100 \mu A$ | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL} = 4 \text{ mA}$ | 1.65 V | | | 0.45 | |
| | | $I_{OL} = 6 \text{ mA}$ | 2.3 V | | | 0.4 | |
| | | $I_{OL} = 12 \text{ mA}$ | 2.3 V | | | 0.7 | |
| | | | 2.7 V | | | 0.4 | |
| | | $I_{OL} = 24 \text{ mA}$ | 3 V | | | 0.55 | |
| I_I | | $V_I = V_{CC} \text{ or GND}$ | 3.6 V | | | ± 5 | μA |
| $I_{I(hold)}$ | | $V_I = 0.58 \text{ V}$ | 1.65 V | 25 | | | μA |
| | | $V_I = 1.07 \text{ V}$ | 1.65 V | -25 | | | |
| | | $V_I = 0.7 \text{ V}$ | 2.3 V | 45 | | | |
| | | $V_I = 1.7 \text{ V}$ | 2.3 V | -45 | | | |
| | | $V_I = 0.8 \text{ V}$ | 3 V | 75 | | | |
| | | $V_I = 2 \text{ V}$ | 3 V | -75 | | | |
| | | $V_I = 0 \text{ to } 3.6 \text{ V}^{(2)}$ | 3.6 V | | | ± 500 | |
| I_{OZ} | | $V_O = V_{CC} \text{ or GND}$ | 3.6 V | | | ± 10 | μA |
| I_{CC} | | $V_I = V_{CC} \text{ or GND}, I_O = 0$ | 3.6 V | | | 20 | μA |
| ΔI_{CC} | | One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$ | 3 V to 3.6 V | | | 750 | μA |
| C_i | Control inputs | $V_I = V_{CC} \text{ or GND}$ | 3.3 V | 4.5 | | | pF |
| | Data inputs | | | 5 | | | |
| C_o | Outputs | $V_O = V_{CC} \text{ or GND}$ | 3.3 V | 7.5 | | | pF |

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC} = 1.8 \text{ V}$ | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CC} = 2.7 \text{ V}$ | | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | UNIT |
|----------|-----------------------------|--------------------------|-----|--|-----|--------------------------|-----|--|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration, LE high | 3.8 | | 3.3 | | 3.3 | | 3.3 | | ns |
| t_{su} | Setup time, data before LE↓ | 1.3 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t_h | Hold time, data after LE↓ | 0.5 | | 1.3 | | 1.7 | | 1.2 | | ns |

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|-----|---|-----|-------------------------|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | D | Q | 1.7 | 6.3 | 1 | 4 | | 4 | 1 | 3.6 | ns |
| | LE | | 2 | 6.1 | 1 | 3.8 | | 3.7 | 1 | 3.3 | |
| t_{en} | \overline{OE} | Q | 3.4 | 8.3 | 1.9 | 5.4 | | 5.4 | 1.6 | 4.8 | ns |
| t_{dis} | \overline{OE} | Q | 1.6 | 7 | 1 | 4.4 | | 4.4 | 1 | 4.4 | ns |

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

| PARAMETER | | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|--|------------------|--------------------------------|-------------------------|-------------------------|-------------------------|------|
| | | | | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per latch | Outputs enabled | C _L = 0, f = 10 MHz | 31 | 33 | 37 | pF |
| | | Outputs disabled | | 7 | 7 | 9 | |

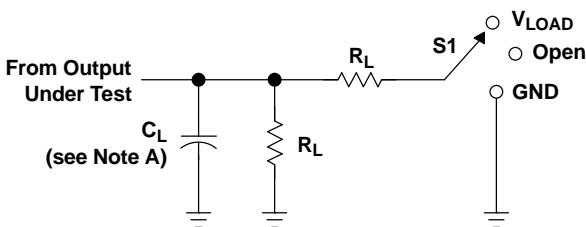
SN74ALVCH373

OCTAL TRANSPARENT D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCES116H–JULY 1997–REVISED OCTOBER 2004

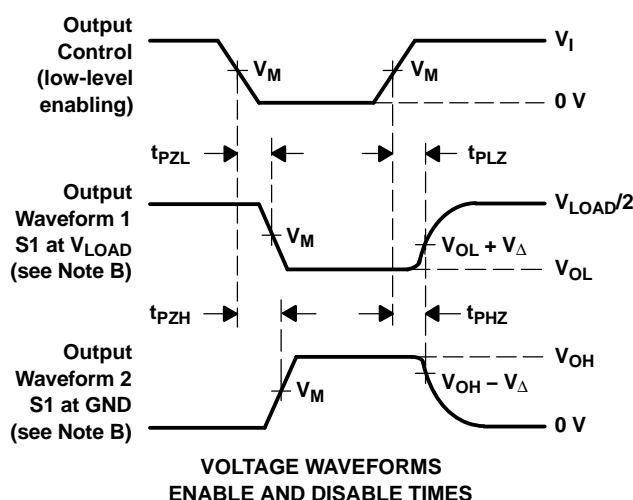
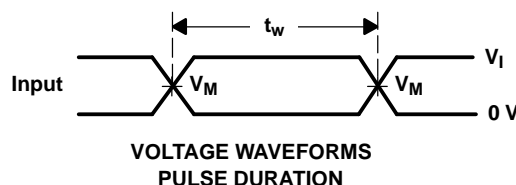
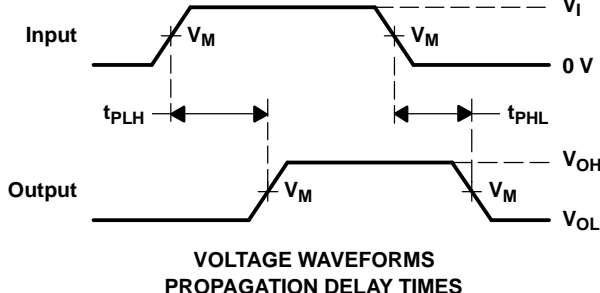
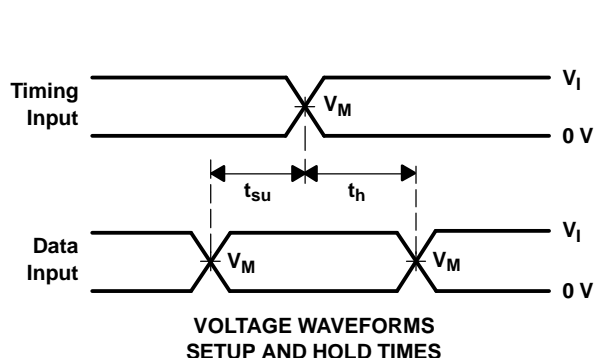
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST | S1 |
|--|---------------------------|
| t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH} | Open V_{LOAD} GND |

| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74ALVCH373DGVR | Active | Production | TVSOP (DGV) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VB373 |
| SN74ALVCH373DGVR.B | Active | Production | TVSOP (DGV) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VB373 |
| SN74ALVCH373DW | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH373 |
| SN74ALVCH373DW.B | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH373 |
| SN74ALVCH373DWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH373 |
| SN74ALVCH373DWR.B | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH373 |
| SN74ALVCH373PWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VB373 |
| SN74ALVCH373PWR.B | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VB373 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVCH373DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74ALVCH373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ALVCH373PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

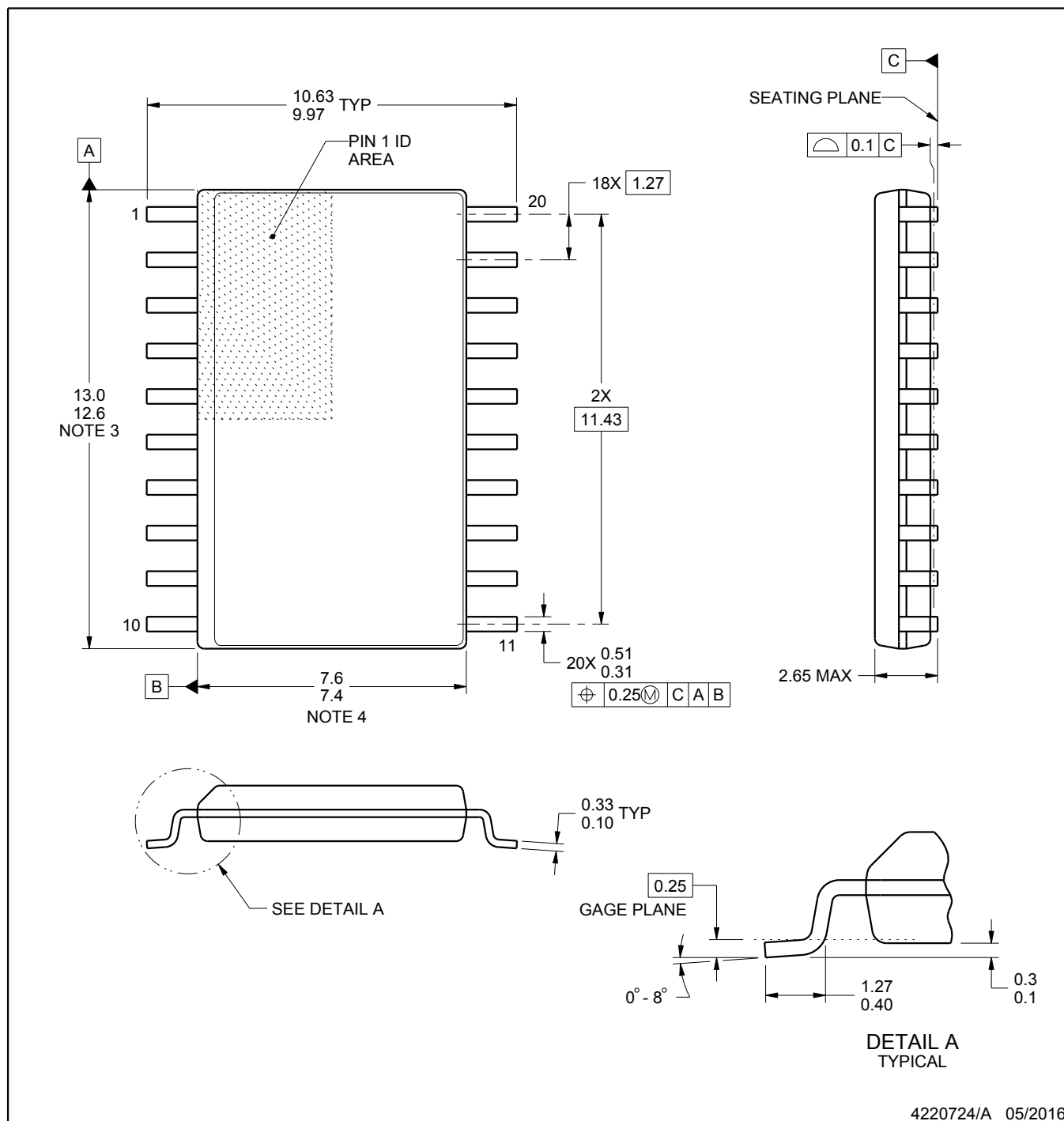
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVCH373DGVR | TVSOP | DGV | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74ALVCH373DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74ALVCH373PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALVCH373DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74ALVCH373DW.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated