SN74ALS29863
9-BIT TRANSCEIVER
WITH 3-STATE OUTPUTS

- **Functionally Equivalent to AMD's AM29863**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)

|			
$\overline{OEBA1}$	1	24	V_{CC}
A1	2	23	B1
A2	3	22	B2
A3	4	21	B3
A4	5	20	B4
A5	6	19	B5
A6	7	18	B6
A7	8	17	B7
A8	9	16	B8
A9	10	15	B9
$\overline{OEBA2}$	11	14	$\overline{OEAB2}$
GND	12	13	$\overline{OEAB1}$

description

This 9-bit transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ($\overline{OEAB1}$, $\overline{OEAB2}$, $\overline{OEBA1}$, and $\overline{OEBA2}$) inputs.

The SN74ALS29863 is characterized for operation from 0°C to 70°C.
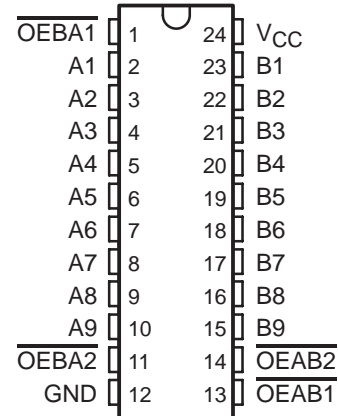
FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

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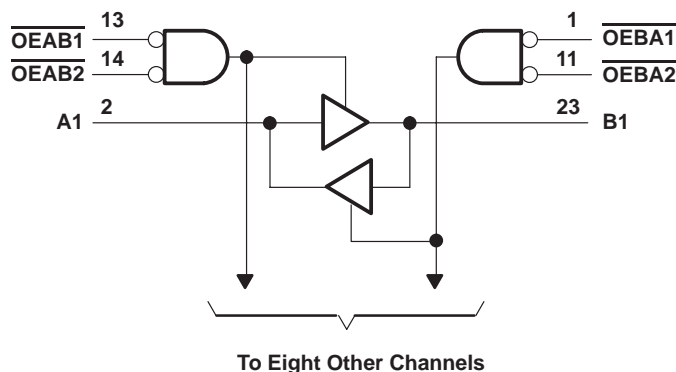
TEXAS INSTRUMENTS

1

SN74ALS29863
9-BIT TRANSCEIVER
WITH 3-STATE OUTPUTS

SDAS096C – JANUARY 1986 – REVISED JANUARY 1995

logic symbol†
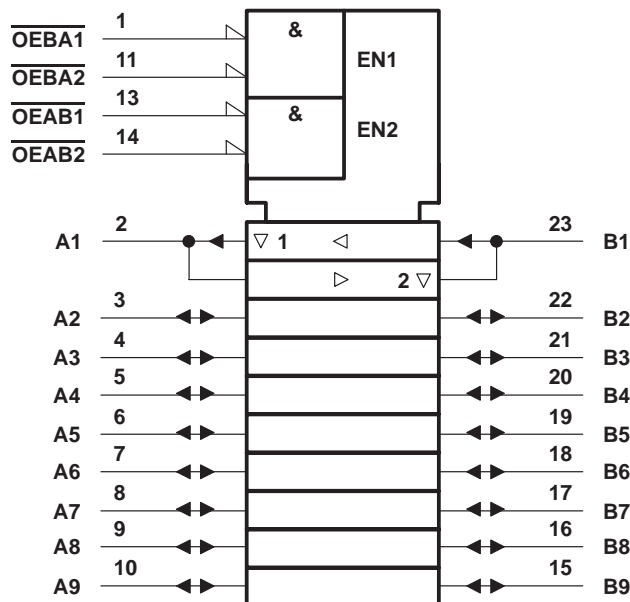
logic diagram (positive logic)

To Eight Other Channels

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . 7 V
Input voltage, V_I (all inputs and I/O ports) . . . . 5.5 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = – 18 mA			– 1.2	V
V_{OH}		V_{CC} = 4.75 V	I_{OH} = – 15 mA	2.4			V
			I_{OH} = – 24 mA	2			
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	Control inputs	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
	A or B ports‡					20	
I_{IL}	Control inputs	V_{CC} = 5.25 V,	V_I = 0.4 V			– 0.1	mA
	A or B ports‡					– 0.1	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0	– 75		– 250	mA
I_{CC}		V_{CC} = 5.25 V			40	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.75 V to 5.25 V		UNIT
				MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 300 pF		15	ns
t_{PHL}					15	
t_{PLH}	A or B	B or A	C_L = 50 pF		8	ns
t_{PHL}					8	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C_L = 300 pF		20	ns
t_{PZL}					23	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C_L = 50 pF		15	ns
t_{PZL}					15	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C_L = 50 pF		17	ns
t_{PLZ}					12	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C_L = 5 pF		9	ns
t_{PLZ}					9	

PARAMETER MEASUREMENT INFORMATION

SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS
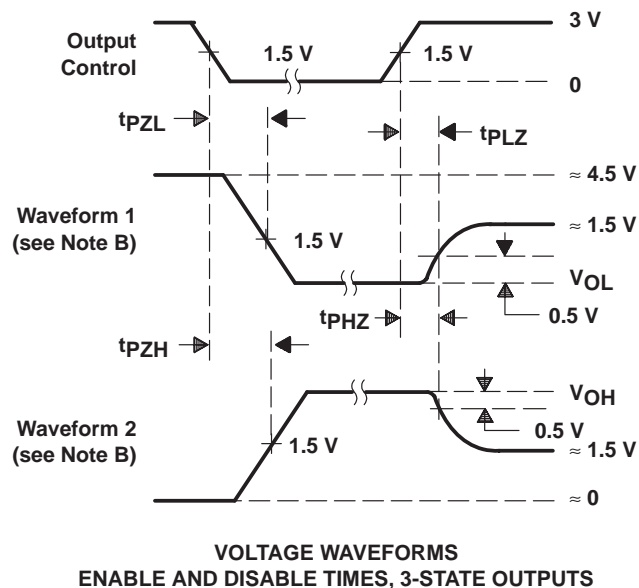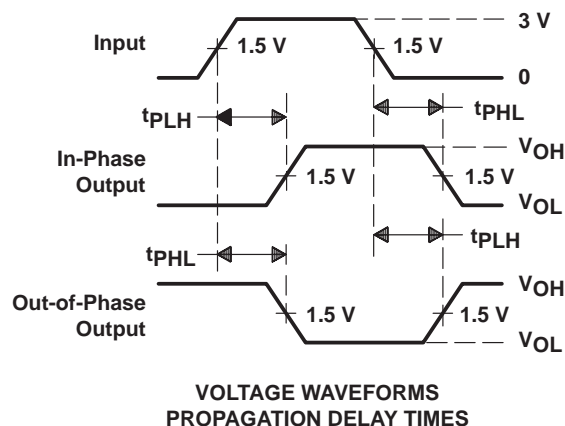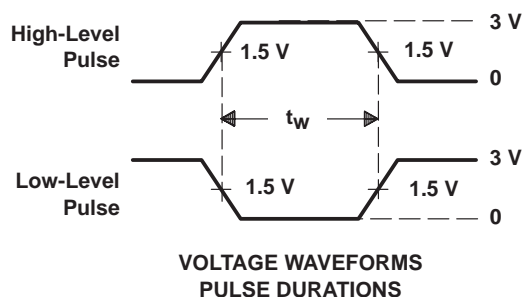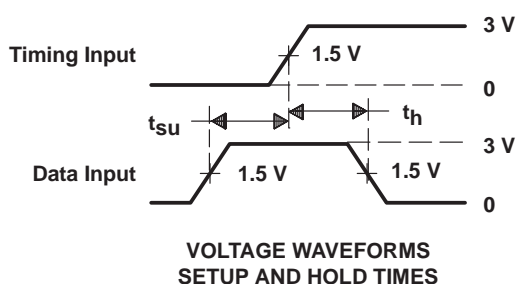
NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS29863DW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS29863
SN74ALS29863DW.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS29863

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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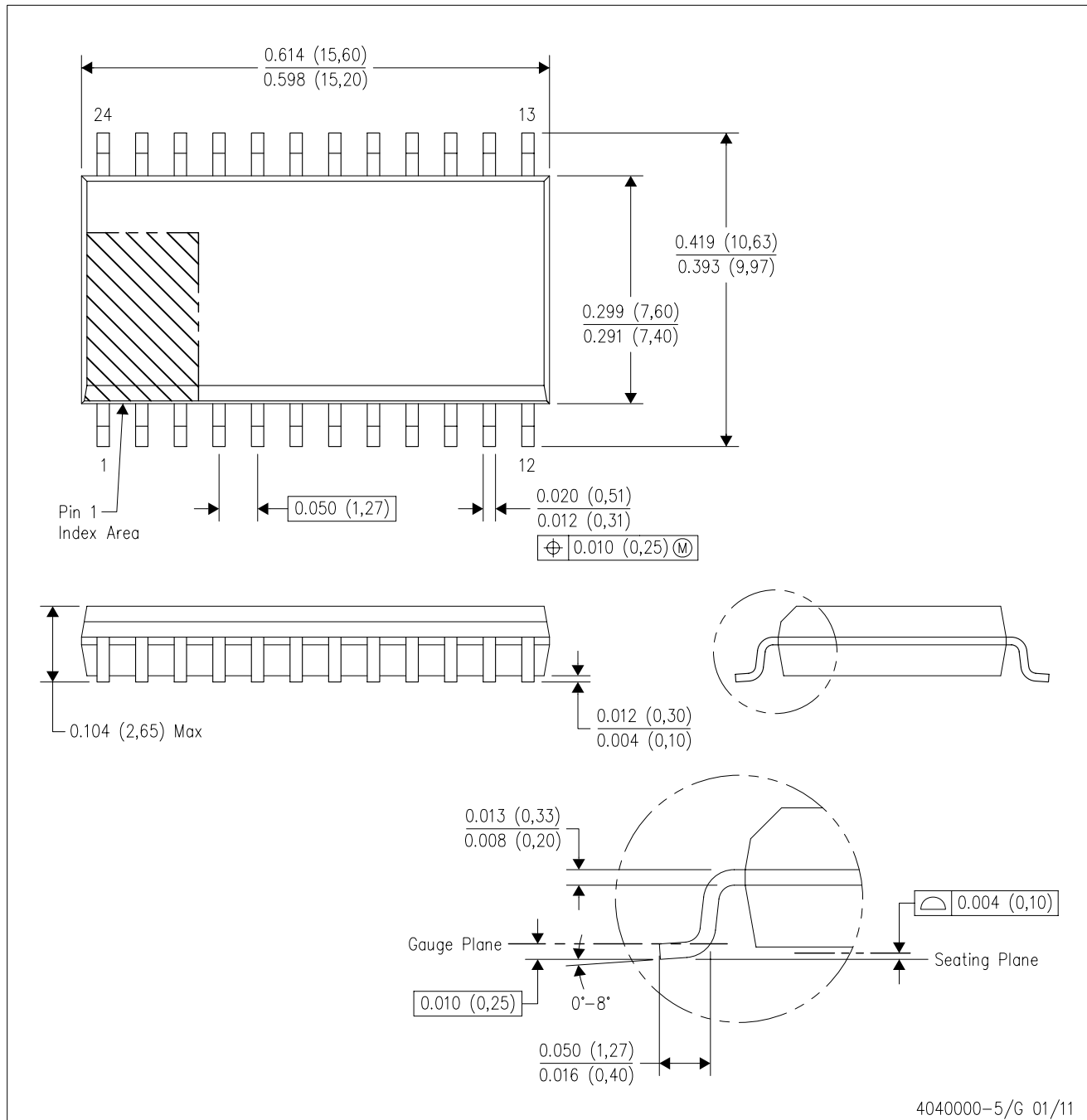
PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
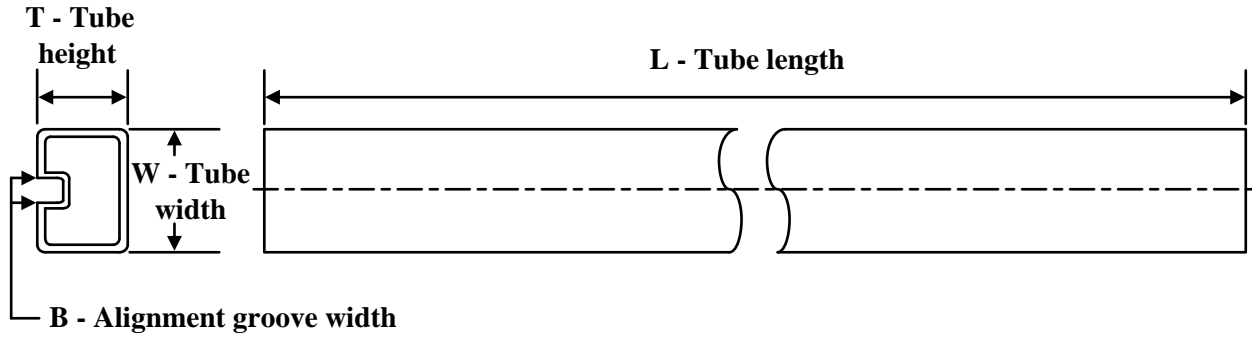
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS29863DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS29863DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AD.

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