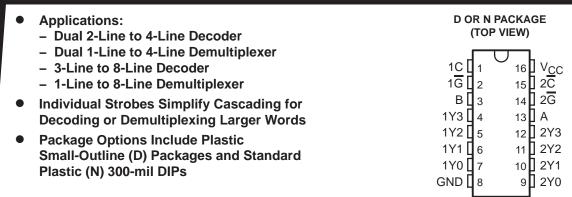
## SN74ALS156 DECODER/DEMULTIPLEXER WITH OPEN-COLLECTOR OUTPUTS

SDAS099C - JUNE 1986 - REVISED MAY 1996



### description

One of the main applications of the SN74ALS156 is as a dual 1-line to 4-line decoder/demultiplexer with individual strobes  $(\overline{G})$  and common binary-address inputs in a single 16-pin package. When both sections are enabled, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit enabling or disabling each of the 4-bit sections, as desired.

Data applied to input 1C is inverted at its outputs and data applied at input  $2\overline{C}$  is not inverted through its outputs. The inverter following the 1C data input permits use of the SN74ALS156 as a 3-line to 8-line demultiplexer without external gating. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN74ALS156 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



### **Function Tables**

### 2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER

	I	NPUTS			OUT	DUTC				
SEL	ECT	STROBE	DATA	OUTPUTS						
В	Α	1G	1C	1Y0	1Y1	1Y2	1Y3			
Х	Χ	Н	Х	Н	Н	Н	Н			
L	L	L	Н	L	Н	Н	Н			
L	Н	L	Н	Н	L	Н	Н			
Н	L	L	Н	Н	Н	L	Н			
Н	Н	L	Н	Н	Н	Н	L			
Х	Χ	Х	L	Н	Н	Н	Н			

### 2-LINE TO 4-LINE DECODER OR **1-LINE TO 4-LINE DEMULTIPLEXER**

	I	NPUTS		OUTPUTS					
SEL	ECT	STROBE	DATA	OUTPUTS		PU15			
В	Α	2G	2C	2Y0	2Y1	2Y2	2Y3		
Х	Х	Н	Х	Н	Н	Н	Н		
L	L	L	L	L	Н	Н	Н		
L	Н	L	L	Н	L	Н	Н		
Н	L	L	L	Н	Н	L	Н		
Н	Н	L	L	Н	Н	Н	L		
Х	Χ	Х	Н	Н	Н	Н	Н		

### 3-LINE TO 8-LINE DECODER OR **1-LINE TO 8-LINE DEMULTIPLEXER**

	INF	UTS					OUT	PUTS			
	SELECT		STROBE OR	0	1	2	3	4	5	6	7
c†	В	Α	DATA G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
Х	Х	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	Н	L	Н	Н	Н
L	L	Н	L	Н	L	Н	Н	Н	L	Н	Н
L	Н	L	L	Н	Н	L	Н	Н	Н	Н	Н
L	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	Н	Н	Н	Н	Н	L	Н	Н
Н	Н	L	L	Н	Н	L	Н	Н	Н	L	Н
Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	L

†  $\underline{C}$  = inputs 1 $\underline{C}$  and 2 $\underline{\overline{C}}$  connected together ‡  $\overline{G}$  = inputs 1 $\overline{G}$  and 2 $\overline{G}$  connected together

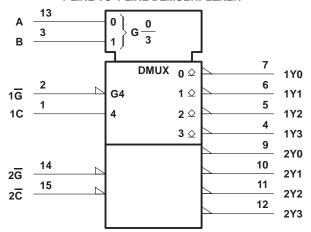


## logic symbols<sup>†</sup> (alternatives)

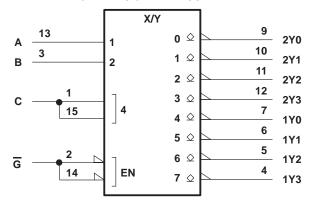
### 2-LINE TO 4-LINE DECODER

#### X/Y 7 0 α ♀ 1Y0 2 6 1<u>G</u> 1 α ◊ 1Y1 ΕN 1 5 1C 2 α ◊ 1Y2 4 13 3 α ◊ 1Y3 9 3 0 β ♀ 2Y0 В 2 10 1 β ◊ 2Y1 11 14 & 2G 2 β ♀ 2Y2 15 12 ΕN 2<u>C</u> 3 β ☆ 2Y3

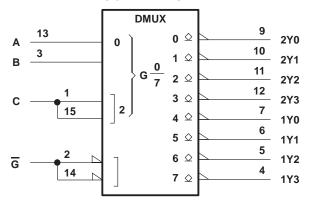
### 1-LINE TO 4-LINE DEMULTIPLEXER



### **3-LINE TO 8-LINE DECODER**



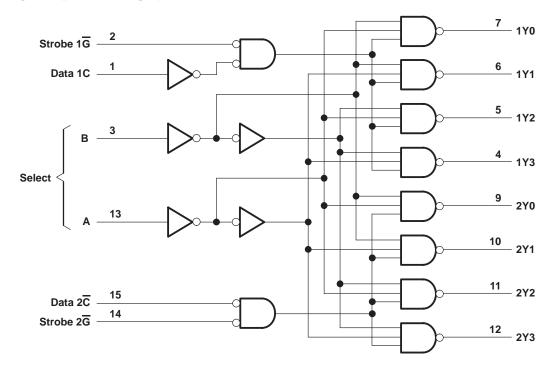
### 1-LINE TO 8-LINE DEMULTIPLEXER



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Operating free-air temperature range, T <sub>A</sub>	
Storage temperature range, T <sub>stg</sub>	°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			8.0	V
Vон	High-level output voltage			5.5	V
lOL	Low-level output current			8	mA
TA	Operating free-air temperature	0		70	°C



## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	DITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I <sub>I</sub> = –18 mA			-1.5	V
.,	V 45V	$I_{OL} = 4 \text{ mA}$		0.25	0.4	.,
V <sub>OL</sub>	$V_{CC} = 4.5 V$	$I_{OL} = 8 \text{ mA}$		0.35	0.5	V
ГОН	$V_{CC} = 4.5 V,$	V <sub>OH</sub> = 5.5 V			0.1	mA
IĮ	$V_{CC} = 5.5 V$ ,	V <sub>I</sub> = 7 V			0.1	mA
lін	$V_{CC} = 5.5 V,$	V <sub>I</sub> = 2.7 V			20	μΑ
Ι <sub>ΙL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.1	μΑ
ICCL	V <sub>CC</sub> = 5.5 V			5	9	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

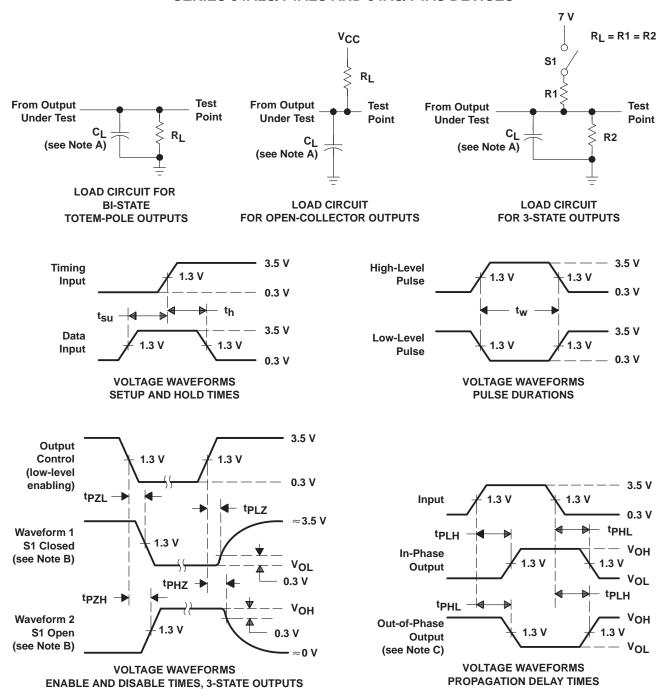
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 C <sub>L</sub> = 50 pl R <sub>L</sub> = 500 g T <sub>A</sub> = MIN	UNIT	
			MIN	MAX	
t <sub>PLH</sub>	A B	47/ 27/	7	55	
<sup>t</sup> PHL	A, B	1Y, 2Y	6	25	ns
<sup>t</sup> PLH	40	47	7	50	
<sup>t</sup> PHL	1C	1Y	6	23	ns
<sup>t</sup> PLH	, <del>,</del>	47/	7	38	
<sup>t</sup> PHL	1 <del>G</del>	1Y	6	22	ns
t <sub>PLH</sub>	2 <del>C</del> , 2 <del>G</del>	2Y	7	38	ns
t <sub>PHL</sub>	2C, 2G	Z Ť	6	22	

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  - D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_{\Gamma} = t_{\Gamma} = 2$  ns, duty cycle = 50%.
  - E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74ALS156D	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	ALS156
SN74ALS156DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS156
SN74ALS156DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS156
SN74ALS156DRE4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS156
SN74ALS156N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS156N
SN74ALS156N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS156N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

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## **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS156DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	SN74ALS156DR	SOIC	D	16	2500	340.5	336.1	32.0	

## **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS156N	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS156N	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS156N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS156N.A	N	PDIP	16	25	506	13.97	11230	4.32

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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