

# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

- Fully Buffered to Offer Maximum Isolation From External Disturbance
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

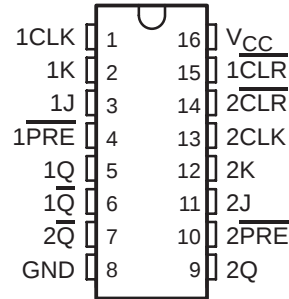
| TYPE     | TYPICAL MAXIMUM<br>CLOCK<br>FREQUENCY<br>(MHz) | TYPICAL POWER<br>DISSIPATION<br>PER FLIP-FLOP<br>(mW) |
|----------|------------------------------------------------|-------------------------------------------------------|
| 'ALS112A | 50                                             | 6                                                     |

## description

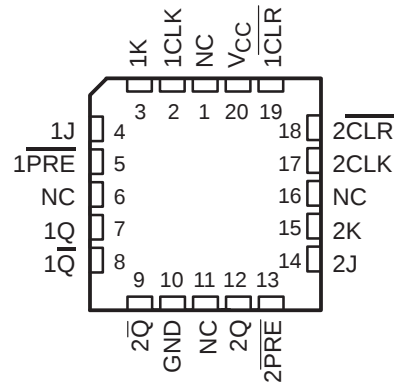
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS112A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS112A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS112A . . . J PACKAGE  
SN74ALS112A . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS112A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each flip-flop)

| INPUTS           |                  |     |   |   | OUTPUTS        |                  |
|------------------|------------------|-----|---|---|----------------|------------------|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q              | $\overline{Q}$   |
| L                | H                | X   | X | X | H              | L                |
| H                | L                | X   | X | X | L              | H                |
| L                | L                | X   | X | X | H <sup>†</sup> | H <sup>†</sup>   |
| H                | H                | ↓   | L | L | Q <sub>0</sub> | $\overline{Q}_0$ |
| H                | H                | ↓   | H | L | H              | L                |
| H                | H                | ↓   | L | H | L              | H                |
| H                | H                | ↓   | H | H | Toggle         |                  |
| H                | H                | H   | X | X | Q <sub>0</sub> | $\overline{Q}_0$ |

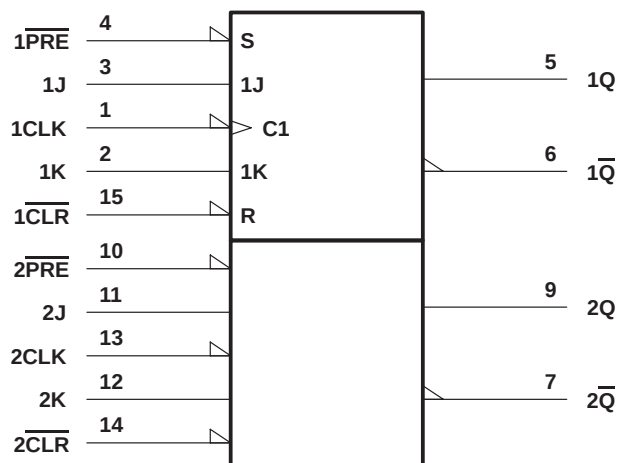
<sup>†</sup> The output levels in this configuration may not meet the minimum levels for  $V_{OH}$ . Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

# SN54ALS112A, SN74ALS112A

## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

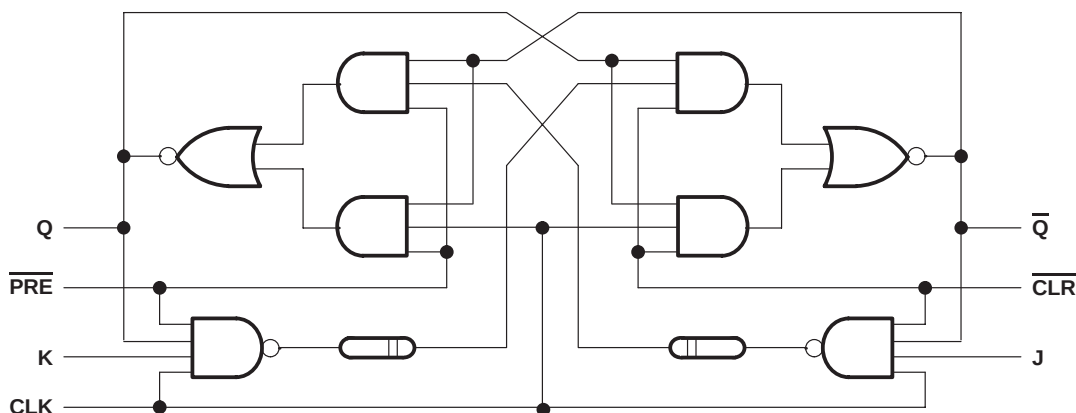
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|                                                           |                |
|-----------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$                                  | 7 V            |
| Input voltage, $V_I$                                      | 7 V            |
| Operating free-air temperature range, $T_A$ : SN54ALS112A | -55°C to 125°C |
| SN74ALS112A                                               | 0°C to 70°C    |
| Storage temperature range                                 | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## recommended operating conditions

|                    |                                |                                                             | SN54ALS112A |     |     | SN74ALS112A |     |     | UNIT |
|--------------------|--------------------------------|-------------------------------------------------------------|-------------|-----|-----|-------------|-----|-----|------|
|                    |                                |                                                             | MIN         | NOM | MAX | MIN         | NOM | MAX |      |
| V <sub>CC</sub>    | Supply voltage                 |                                                             | 4.5         | 5   | 5.5 | 4.5         | 5   | 5.5 | V    |
| V <sub>IH</sub>    | High-level input voltage       |                                                             | 2           |     |     | 2           |     |     | V    |
| V <sub>IL</sub>    | Low-level input voltage        |                                                             | 0.7         |     |     | 0.8         |     |     | V    |
| I <sub>OH</sub>    | High-level output current      |                                                             | −0.4        |     |     | −0.4        |     |     | mA   |
| I <sub>OL</sub>    | Low-level output current       |                                                             | 4           |     |     | 8           |     |     | mA   |
| f <sub>clock</sub> | Clock frequency                |                                                             | 0           | 25  |     | 0           | 30  |     | MHz  |
| t <sub>w</sub>     | Pulse duration                 | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low      | 15          |     |     | 10          |     |     | ns   |
|                    |                                | CLK high                                                    | 20          |     |     | 16.5        |     |     |      |
|                    |                                | CLK low                                                     | 20          |     |     | 16.5        |     |     |      |
| t <sub>su</sub>    | Setup time before CLK↓         | Data                                                        | 25          |     |     | 22          |     |     | ns   |
|                    |                                | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 22          |     |     | 20          |     |     |      |
| t <sub>h</sub>     | Hold time after CLK↓           | Data                                                        | 0           |     |     | 0           |     |     | ns   |
| T <sub>A</sub>     | Operating free-air temperature |                                                             | −55         | 125 |     | 0           | 70  |     | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                                    | TEST CONDITIONS                                             |                        | SN54ALS112A         |      | SN74ALS112A         |     | UNIT |
|------------------|----------------------------------------------------|-------------------------------------------------------------|------------------------|---------------------|------|---------------------|-----|------|
|                  |                                                    |                                                             |                        | MIN                 | TYP† | MAX                 | MIN |      |
| V <sub>IK</sub>  |                                                    | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA            |                        | -1.5                |      | -1.5                |     | V    |
| V <sub>OH</sub>  |                                                    | V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA |                        | V <sub>CC</sub> - 2 |      | V <sub>CC</sub> - 2 |     | V    |
| V <sub>OL</sub>  |                                                    | V <sub>CC</sub> = 4.5 V                                     | I <sub>OL</sub> = 4 mA | 0.25                | 0.4  | 0.25                | 0.4 | V    |
|                  |                                                    |                                                             | I <sub>OL</sub> = 8 mA |                     |      | 0.35                | 0.5 |      |
| I <sub>I</sub>   | J, K, or CLK                                       | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V               |                        | 0.1                 |      | 0.1                 |     | mA   |
|                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ |                                                             |                        | 0.2                 |      | 0.2                 |     |      |
| I <sub>IH</sub>  | J, K, or CLK                                       | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V             |                        | 20                  |      | 20                  |     | μA   |
|                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ |                                                             |                        | 40                  |      | 40                  |     |      |
| I <sub>IL</sub>  | J, K, or CLK                                       | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V             |                        | -0.2                |      | -0.2                |     | mA   |
|                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ |                                                             |                        | -0.4                |      | -0.4                |     |      |
| I <sub>O</sub> † |                                                    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V            | -20                    | -112                | -30  | -112                | mA  |      |
| I <sub>CC</sub>  |                                                    | V <sub>CC</sub> = 5.5 V, See Note 1                         | 2.5                    | 4.5                 | 2.5  | 4.5                 | mA  |      |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J, K, CLK, and  $\overline{PRE}$  grounded, then with J, K, CLK, and  $\overline{CLR}$  grounded.



# SN54ALS112A, SN74ALS112A

## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

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#### switching characteristics (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)                                    | TO<br>(OUTPUT)             | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX† |     |             |     | UNIT |
|------------------|----------------------------------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------|-----|-------------|-----|------|
|                  |                                                    |                            | SN54ALS112A                                                                                                             |     | SN74ALS112A |     |      |
|                  |                                                    |                            | MIN                                                                                                                     | MAX | MIN         | MAX |      |
| f <sub>max</sub> |                                                    |                            | 25                                                                                                                      |     | 30          |     | MHz  |
| t <sub>PLH</sub> | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | 3                                                                                                                       | 26  | 3           | 15  | ns   |
| t <sub>PHL</sub> |                                                    |                            | 4                                                                                                                       | 23  | 4           | 18  |      |
| t <sub>PLH</sub> | CLK                                                | Q or $\overline{\text{Q}}$ | 3                                                                                                                       | 23  | 3           | 15  | ns   |
| t <sub>PHL</sub> |                                                    |                            | 5                                                                                                                       | 24  | 5           | 19  |      |

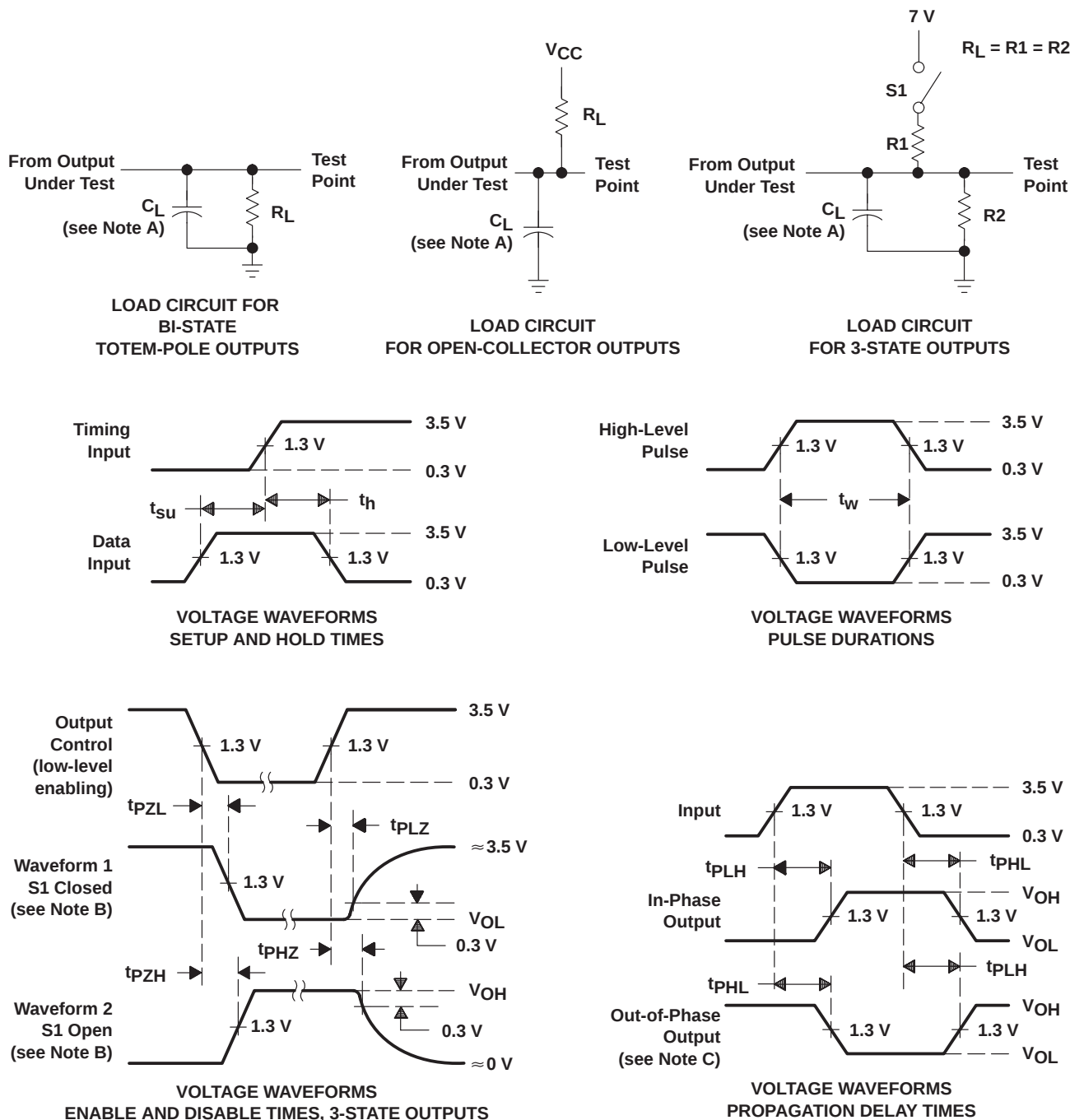
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| <a href="#">8400002EA</a>        | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8400002EA<br>SNJ54ALS112AJ |
| <a href="#">JM38510/37103B2A</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>37103B2A       |
| JM38510/37103B2A.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>37103B2A       |
| <a href="#">JM38510/37103BEA</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>37103BEA       |
| JM38510/37103BEA.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>37103BEA       |
| <a href="#">M38510/37103B2A</a>  | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>37103B2A       |
| <a href="#">M38510/37103BEA</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>37103BEA       |
| <a href="#">SN54ALS112AJ</a>     | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54ALS112AJ               |
| SN54ALS112AJ.A                   | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54ALS112AJ               |
| <a href="#">SN74ALS112AD</a>     | Active        | Production           | SOIC (D)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS112A                    |
| SN74ALS112AD.A                   | Active        | Production           | SOIC (D)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS112A                    |
| <a href="#">SN74ALS112AN</a>     | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74ALS112AN               |
| SN74ALS112AN.A                   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74ALS112AN               |
| <a href="#">SN74ALS112ANSR</a>   | Active        | Production           | SOP (NS)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS112A                    |
| SN74ALS112ANSR.A                 | Active        | Production           | SOP (NS)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS112A                    |
| <a href="#">SNJ54ALS112AJ</a>    | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8400002EA<br>SNJ54ALS112AJ |
| SNJ54ALS112AJ.A                  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8400002EA<br>SNJ54ALS112AJ |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54ALS112A, SN74ALS112A :**

- Catalog : [SN74ALS112A](#)
- Military : [SN54ALS112A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

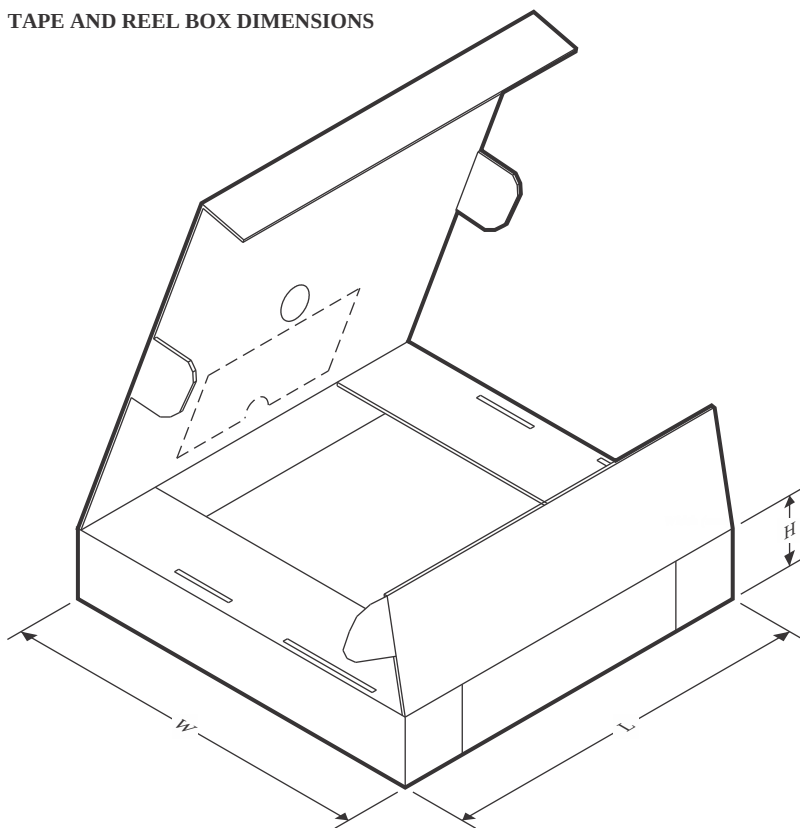
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS112ANSR | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS112ANSR | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| JM38510/37103B2A   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| JM38510/37103B2A.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| M38510/37103B2A    | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SN74ALS112AD       | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| SN74ALS112AD.A     | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| SN74ALS112AN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74ALS112AN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74ALS112AN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74ALS112AN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

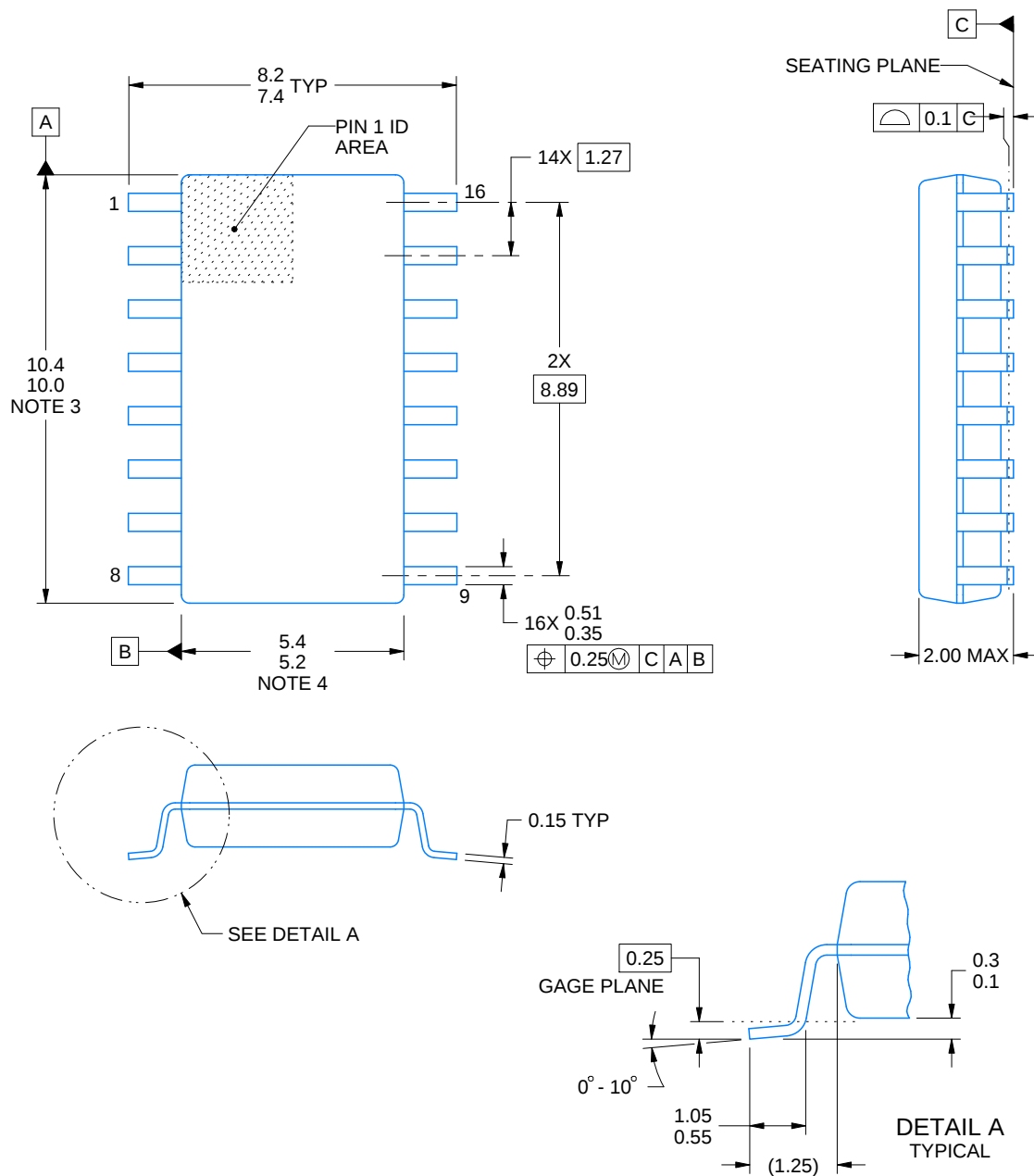


# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

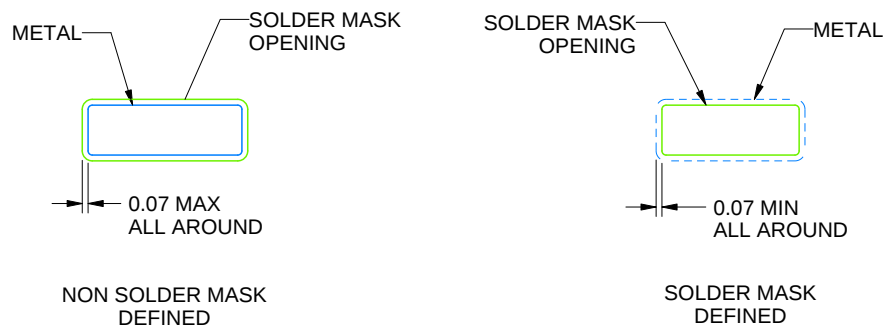
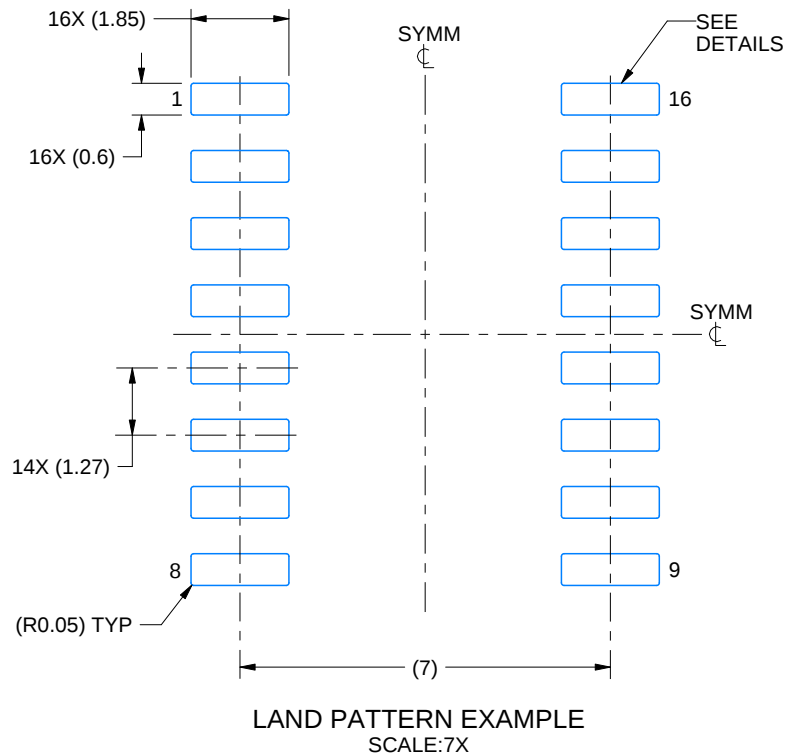
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

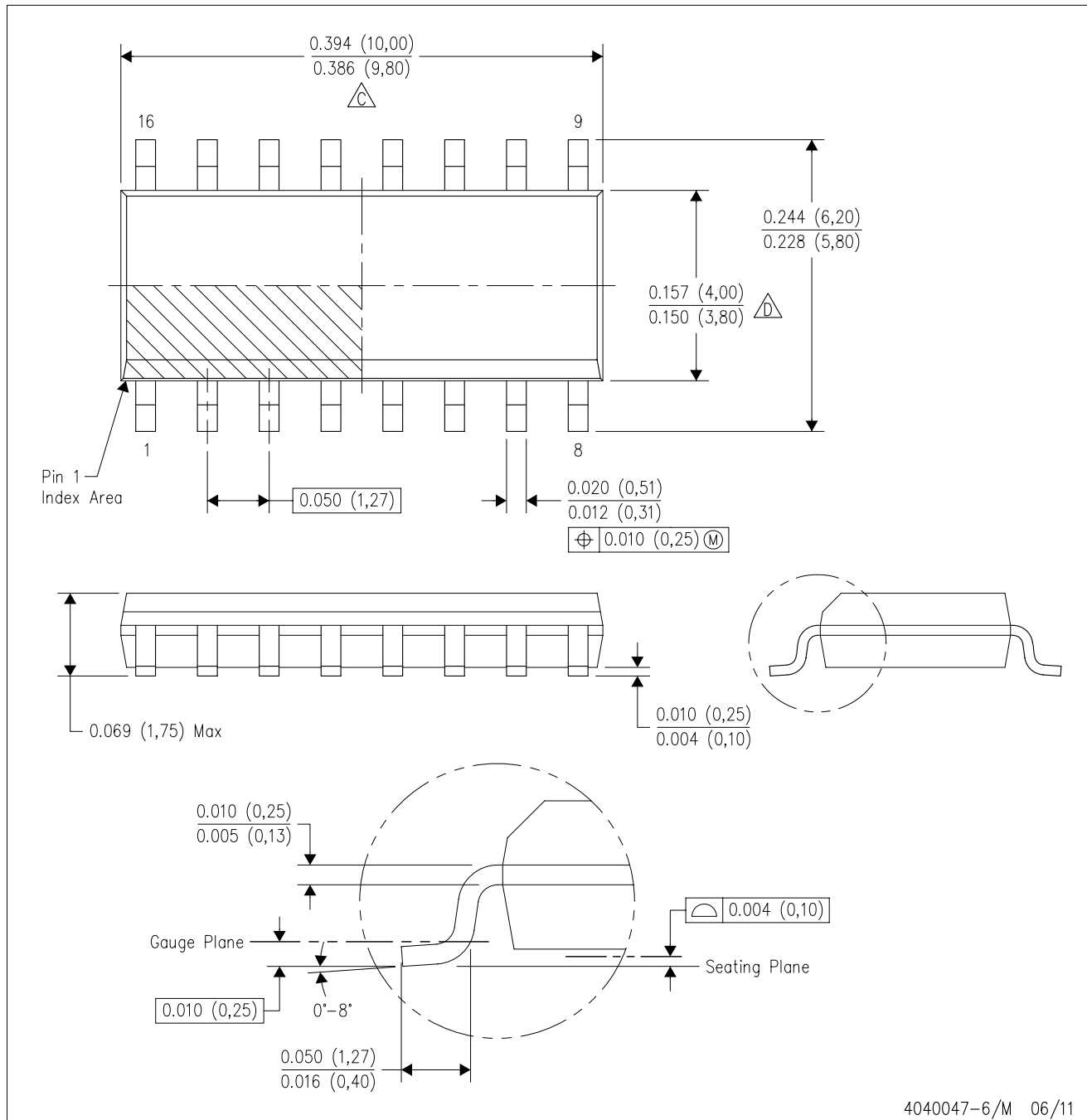
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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



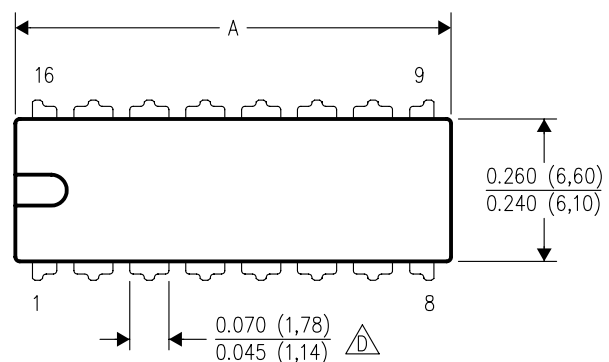
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

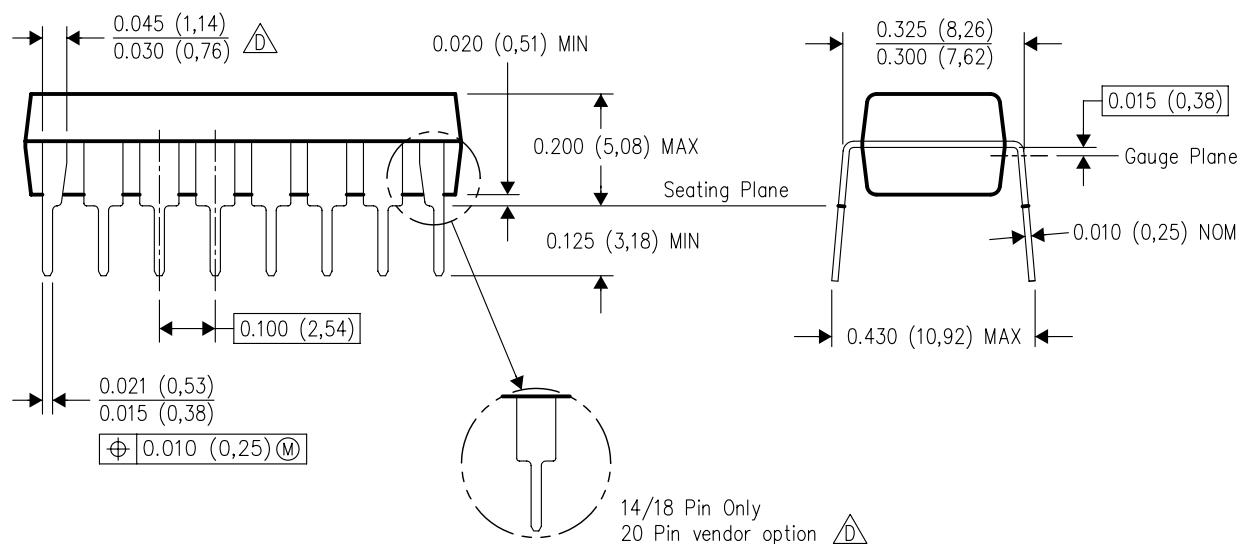
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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