

SN74AHC04-Q1 汽车类六路逆变器

1 特性

- 符合汽车应用要求
- EPIC™ (增强性能植入式 CMOS) 工艺
- 工作电压范围为 2V 至 5.5V V_{CC}

2 应用

- 同步反相时钟输入
- 对开关进行去抖
- 对数字信号进行反相

3 说明

SN74AHC04 包含六个独立的反相器。该器件执行布尔函数 $Y = \overline{A}$ 。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ²
SN74AHC04-Q1	D (SOIC , 14)	8.65mm x 6mm
	PW (TSSOP , 14)	5mm x 6.4mm
	BQA (WQFN , 14)	3mm x 2.5mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 (长 x 宽) 为标称值，并包括引脚 (如适用)。

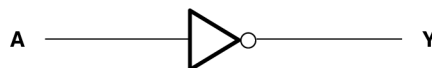


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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (April 2023) to Revision D (June 2023)	Page
• 向封装信息表中添加了 BQA 封装.....	1
• Updated thermal values for PW package from $R_{\theta JA} = 113$ to 147.7 , all values in $^{\circ}\text{C/W}$	5
• Added thermal value for $R_{\theta JA}$: BQA = 88.3 , all values in $^{\circ}\text{C/W}$	5

Changes from Revision B (April 2008) to Revision C (April 2023)	Page
• 添加了应用、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

5 Pin Configuration and Functions

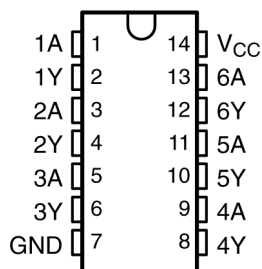


图 5-1. D or PW Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V _{CC}	14	—	Positive Supply
Thermal Pad ¹		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

1. BQA Package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ²	Input voltage range	-0.5	7	V
V _O ²	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)	-20	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})	±20	mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge Human body model (HBM) ¹	±1500	V

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 3.3 V ± 0.3 V	-4	mA
		V _{CC} = 5 V ± 0.5 V	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 3.3 V ± 0.3 V	4	mA
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC04-Q1			UNIT
		D (SOIC)	PW (TSSOP)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	86	147.7	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, ([SPRA953](#)).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5	
		4.5 V			0.36		0.5	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	μA
C _i	V _I = V _{CC} or GND	5 V		2	10			pF

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF		5	8.9	1	10.5	ns
t _{PHL}					5	8.9	1	10.5	
t _{PLH}	A	Y	C _L = 50 pF		7.5	11.4	1	13	ns
t _{PHL}					7.5	11.4	1	13	

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF		3.8	5.5	1	6.5	ns
t _{PHL}					3.8	5.5	1	6.5	
t _{PLH}	A	Y	C _L = 50 pF		5.3	7.5	1	8.5	ns
t _{PHL}					5.3	7.5	1	8.5	

6.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ¹

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

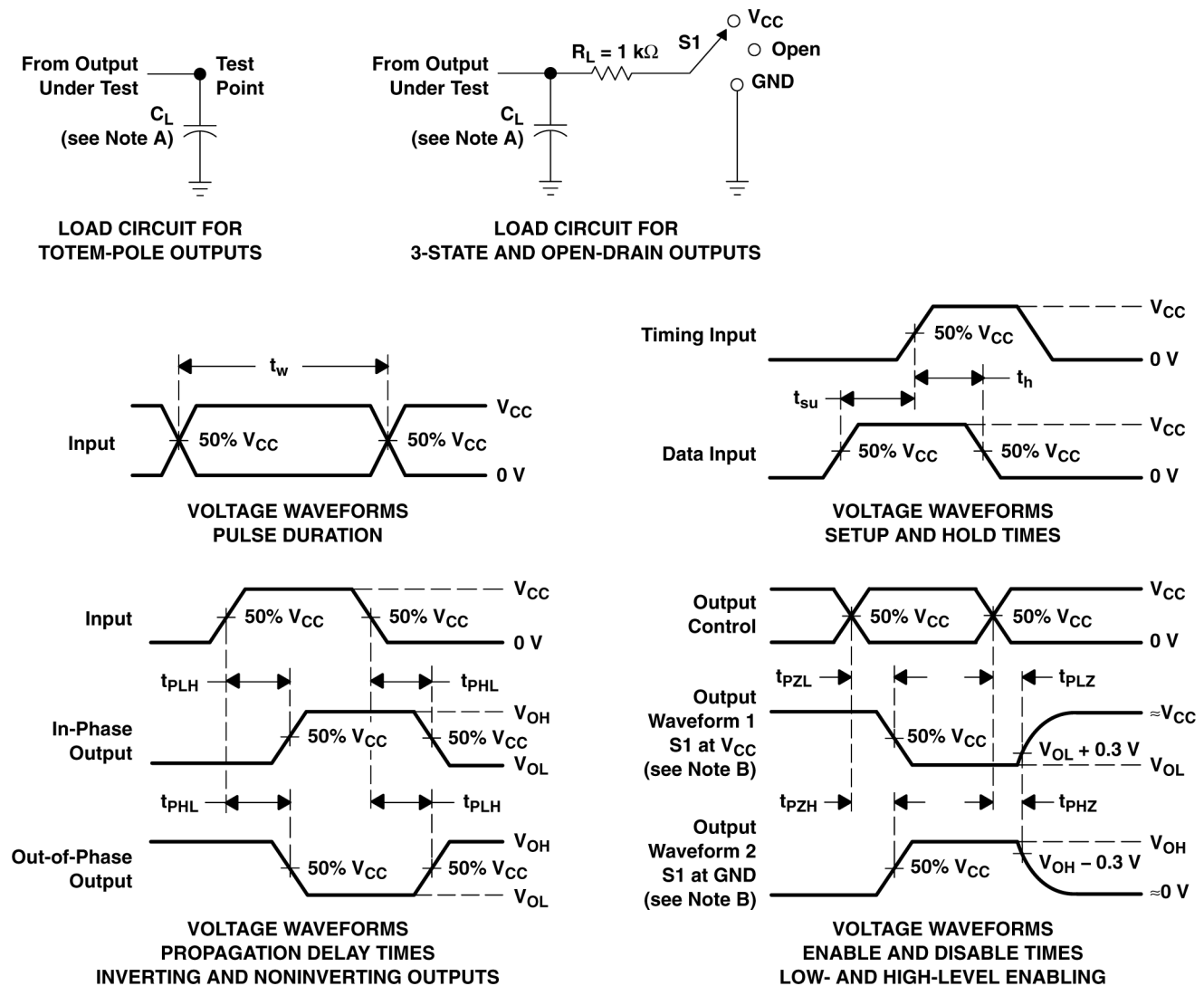
(1) Characteristics are for surface-mount packages only.

6.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

图 7-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

8 Detailed Description

8.1 Functional Block Diagram

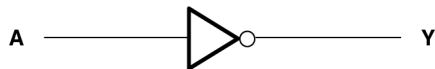


图 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.2 Device Functional Modes

表 8-1. Function Table (Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Layout Diagram](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

9.2.1.1 Layout Example

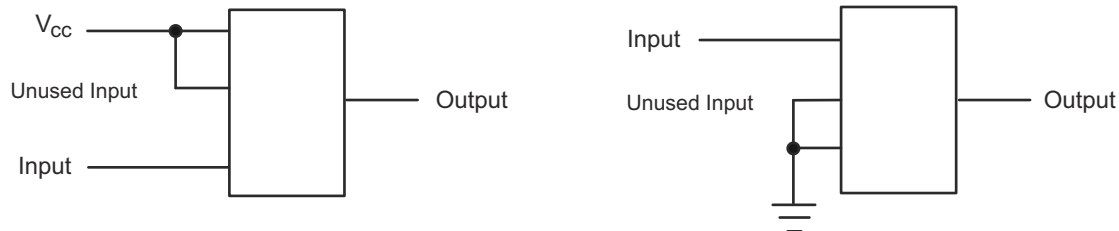


图 9-1. Layout Diagram

10 Device and Documentation Support

10.1 Document Support (Analog)

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC04-Q1	Click here	Click here	Click here	Click here	Click here

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC04QDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q
SN74AHC04QWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC04-Q1 :

- Catalog : [SN74AHC04](#)
- Enhanced Product : [SN74AHC04-EP](#)
- Military : [SN54AHC04](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

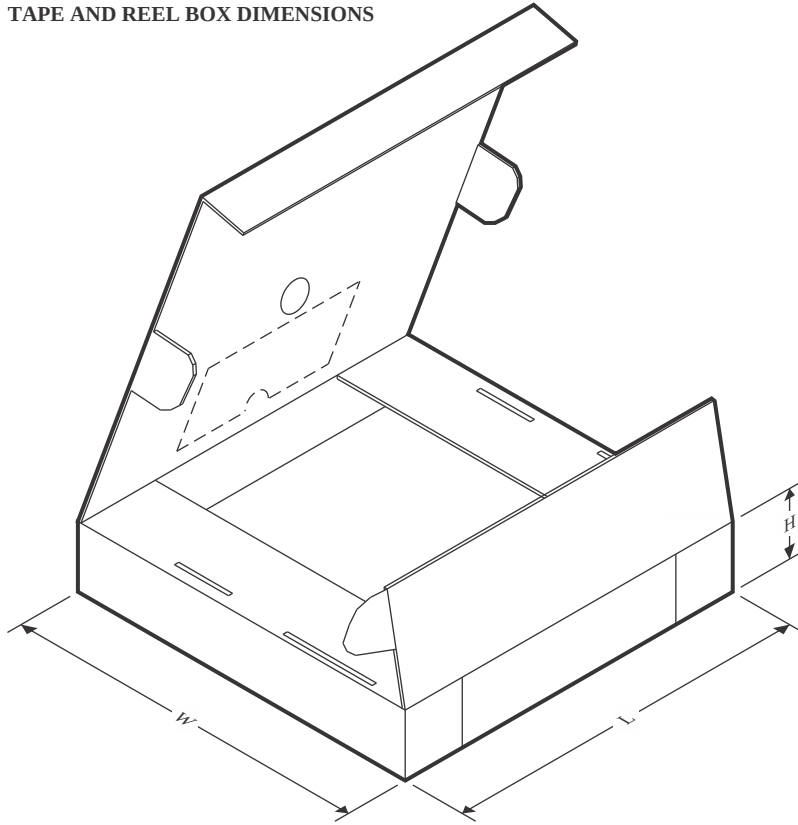
TAPE AND REEL INFORMATION



*All dimensions are nominal

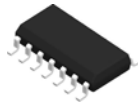
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC04QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC04QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC04QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

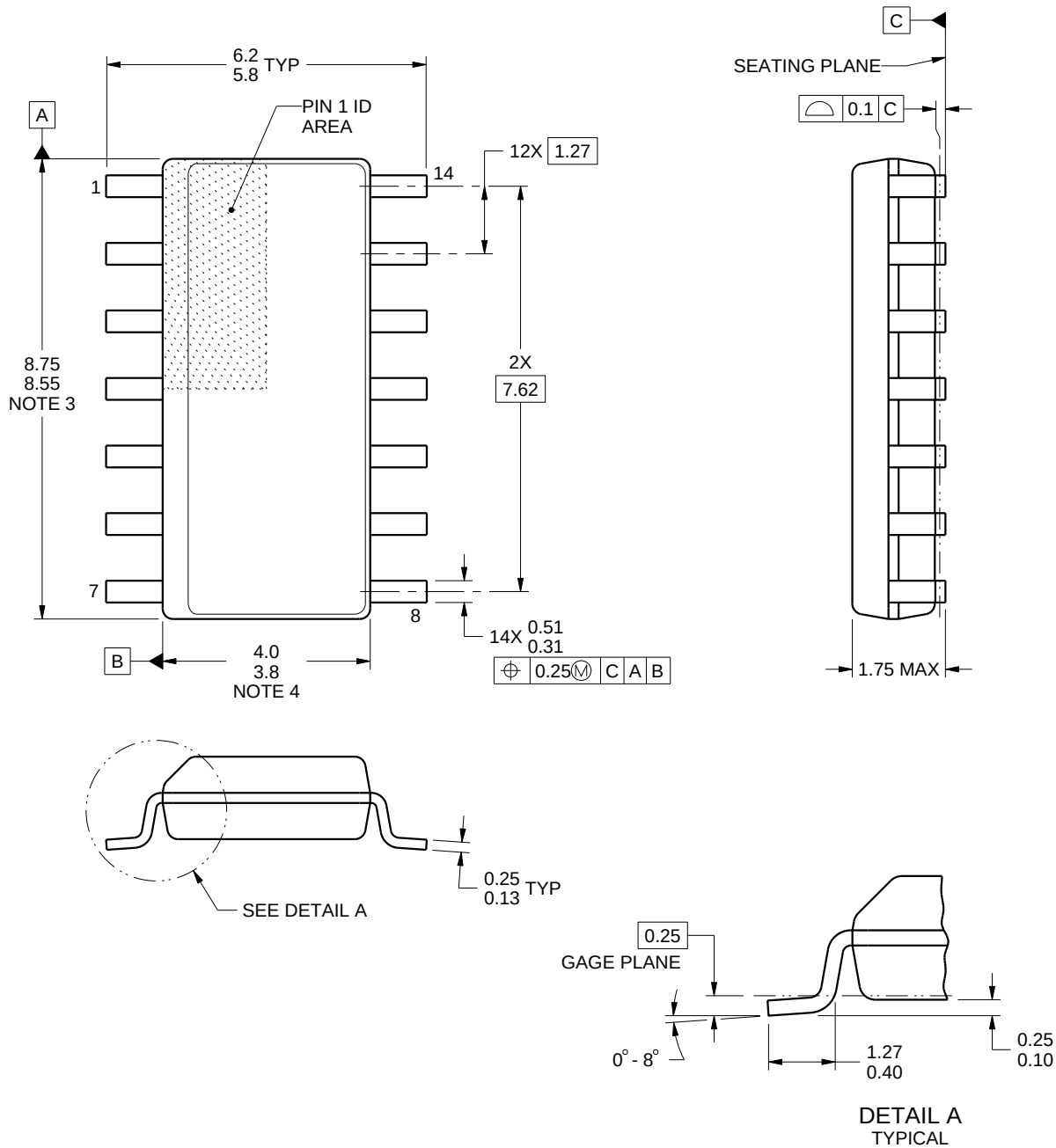


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC04QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC04QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC04QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

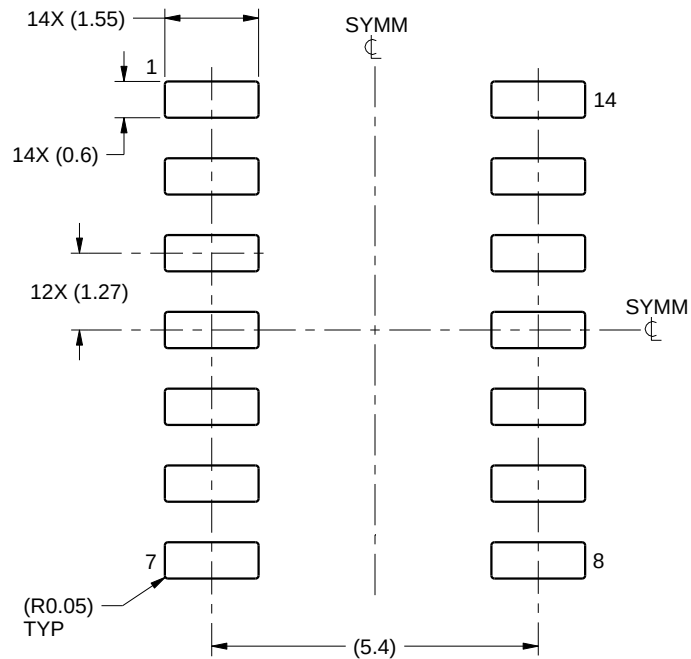
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

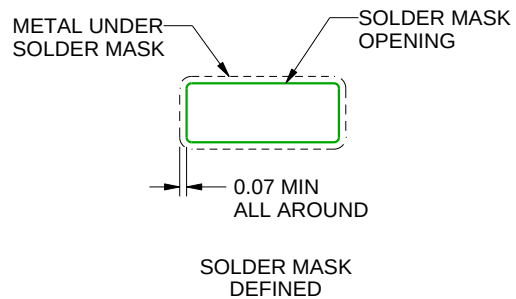
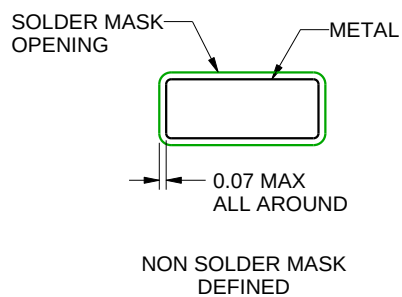
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

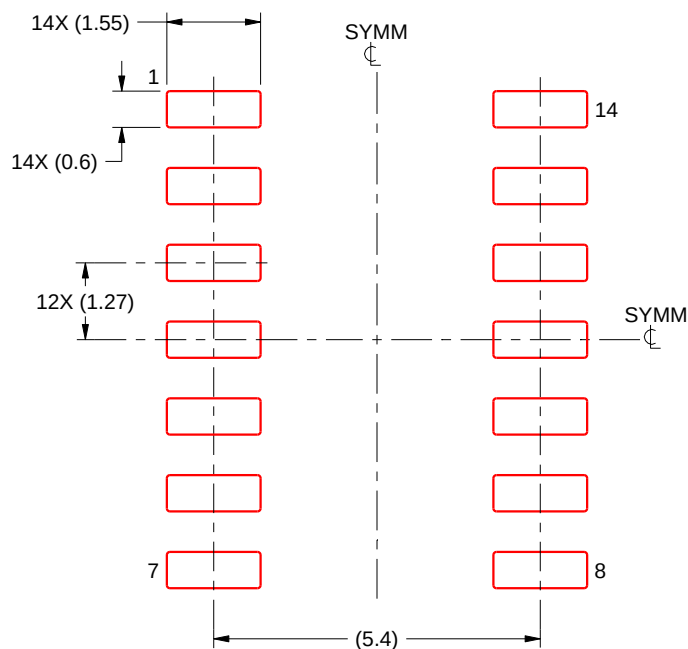
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

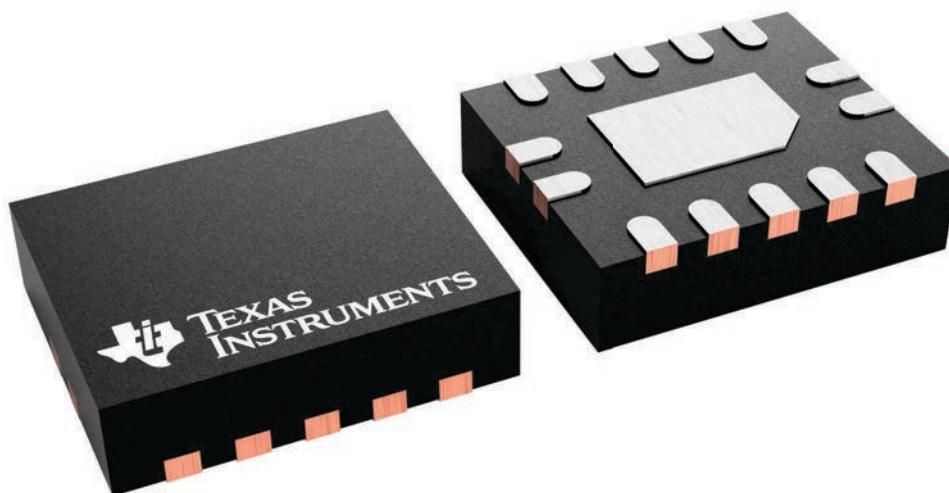
BQA 14

WQFN - 0.8 mm max height

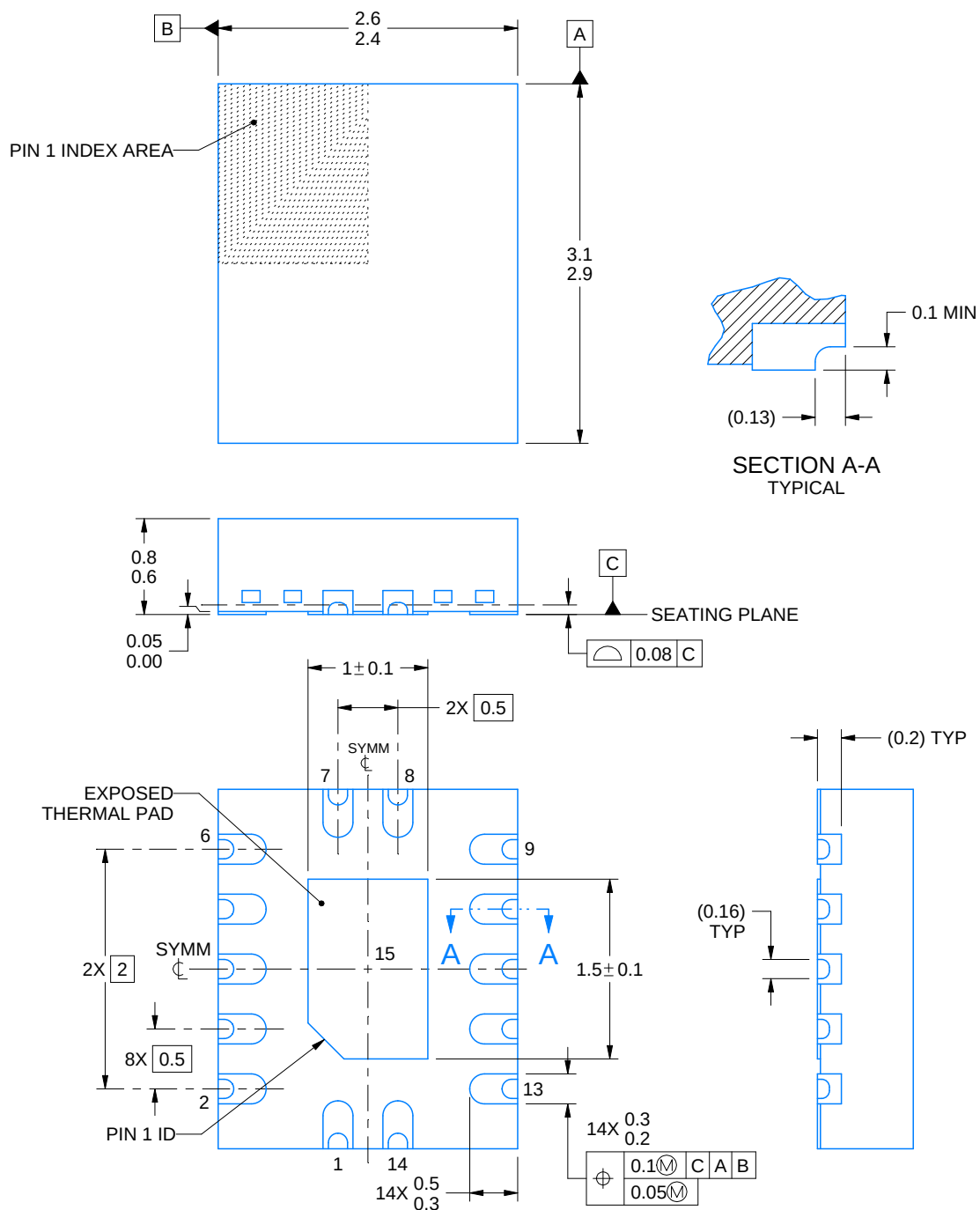
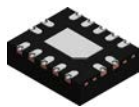
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



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NOTES:

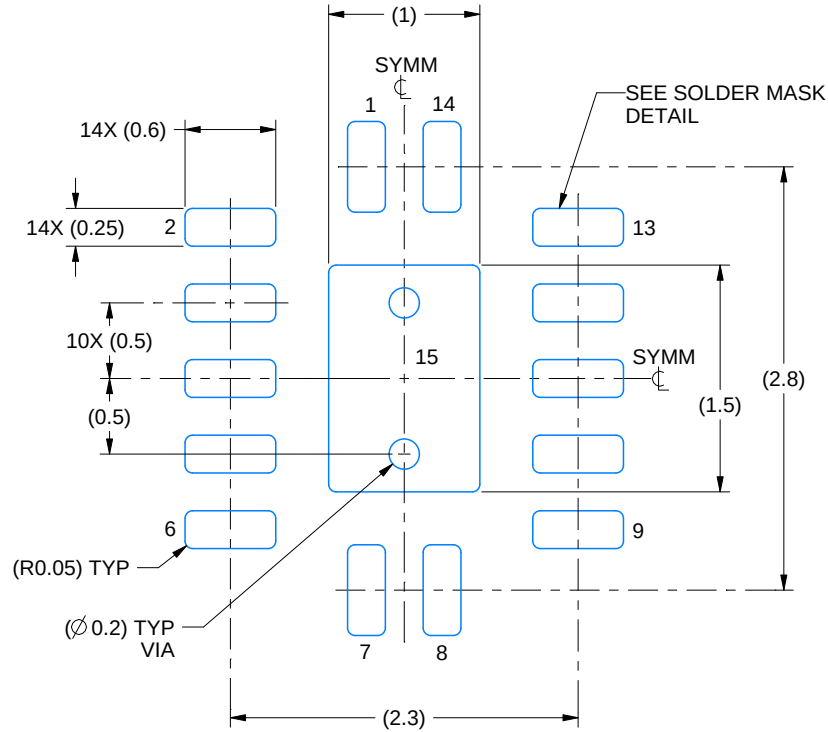
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

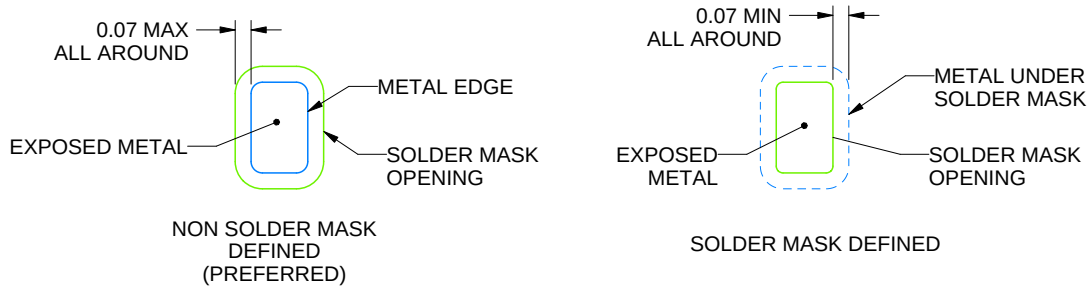
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

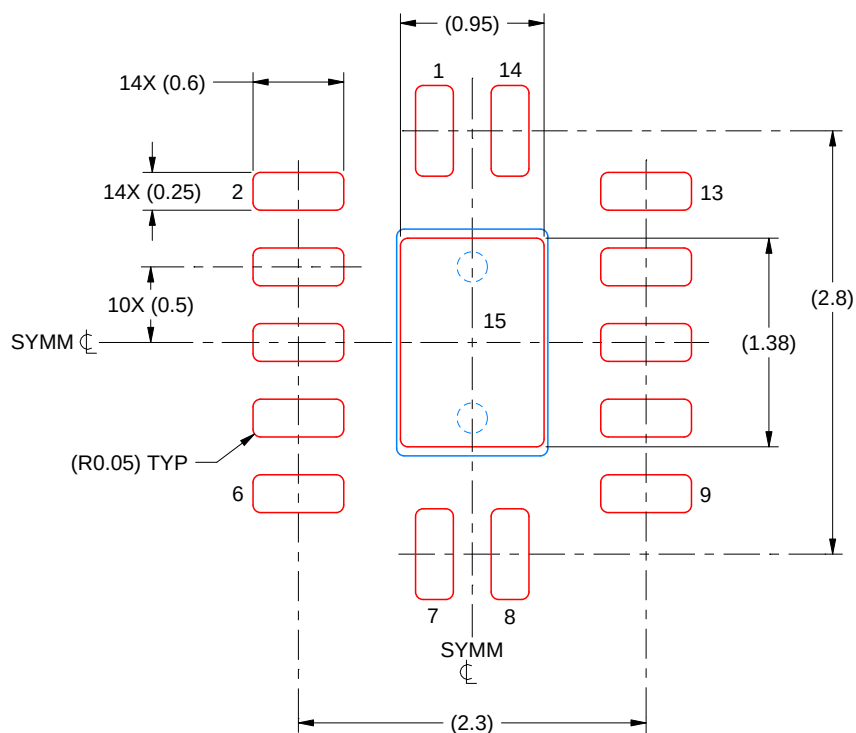
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



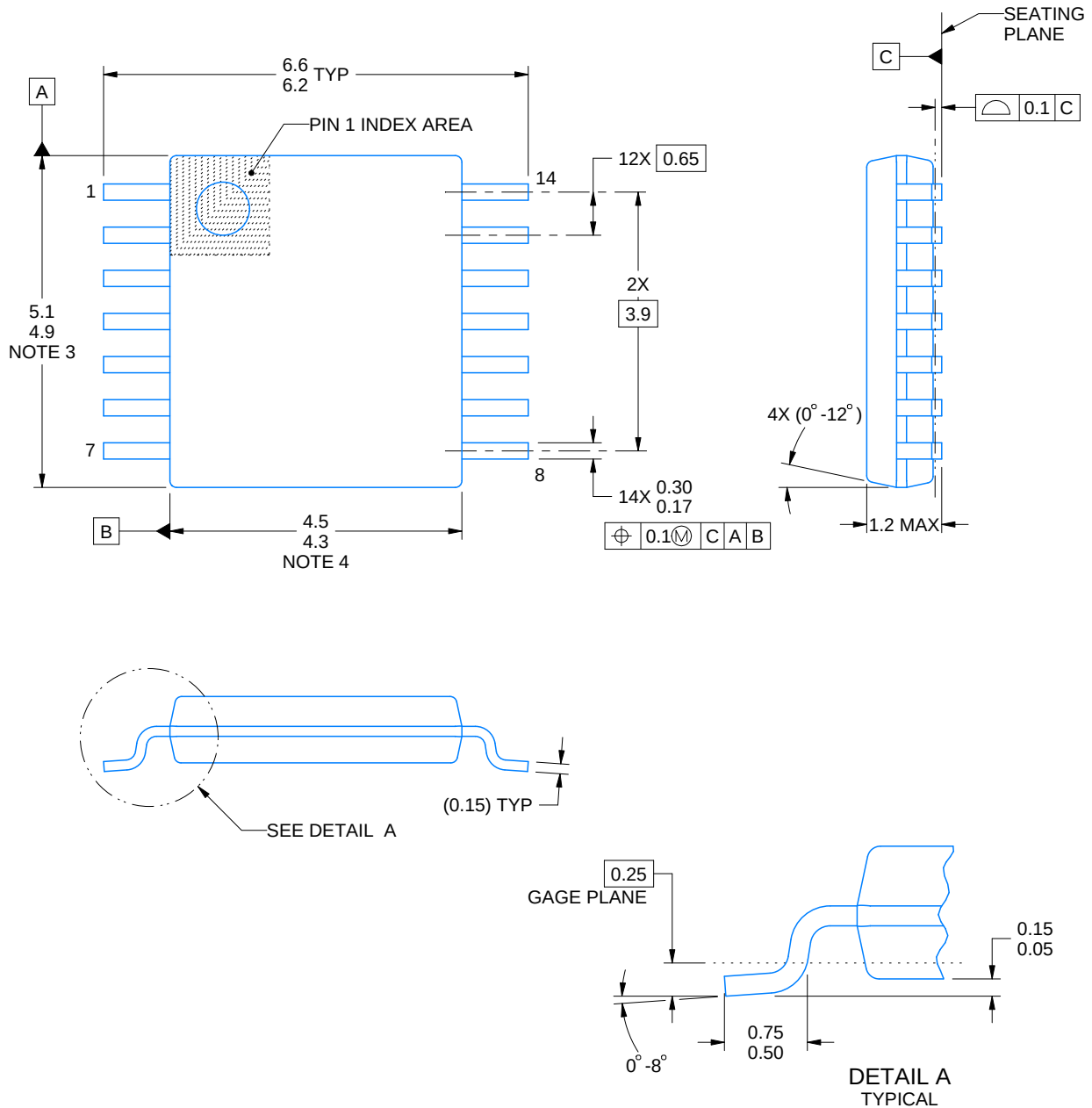
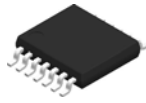
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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NOTES:

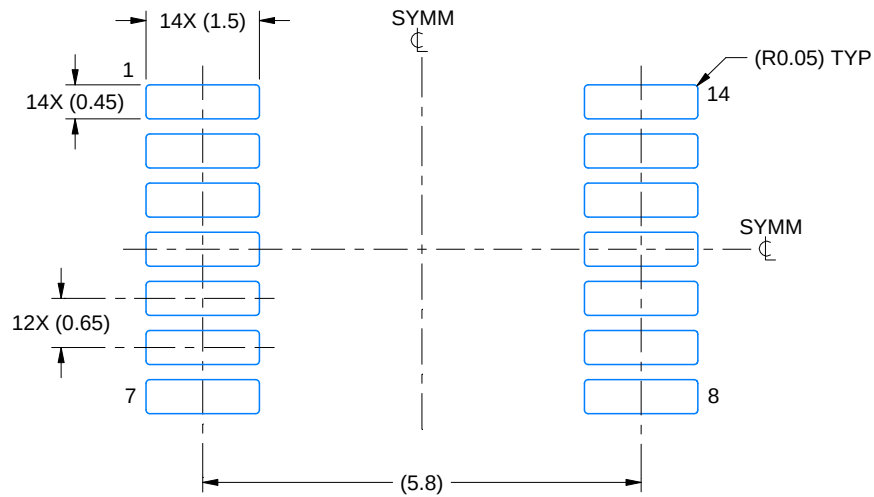
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

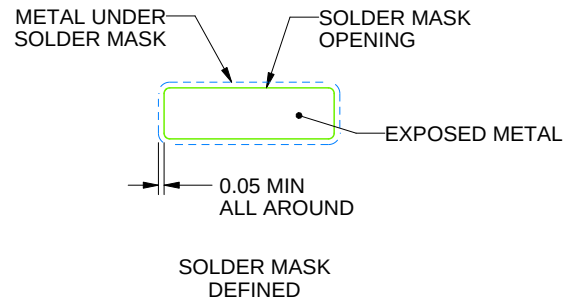
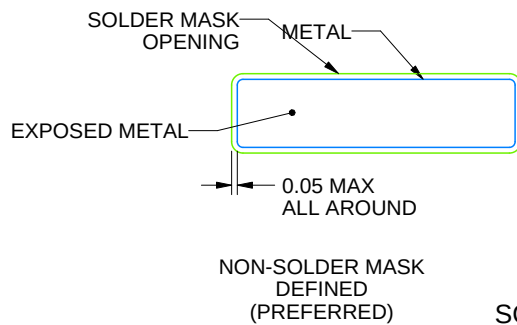
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

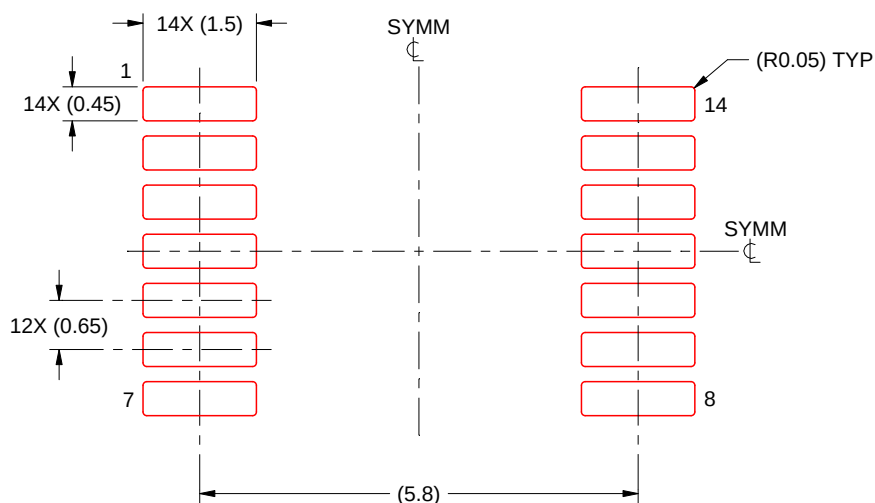
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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