SN74ACT00-Q1 四通道双输入正与非门

1 特性

- 符合汽车应用要求
- ESD 保护超过 2000V（根据 MIL-STD-883 方法 3015）；超过 200V 使用机器模型，（C = 20pF，R = 0）
- 4.5V 至 5.5V V_{CC} 运行
- 输入电压高达 5.5V
- 5V 时，t_{pd} 最大值为 8ns
- 输入兼容 TTL 电压

2 说明

SN74ACT00 包含四个独立的双输入与非门。每个逻辑门以正逻辑执行布尔函数 $Y = \overline{A\ B}$ 或 $Y = \overline{A} + \overline{B}$。

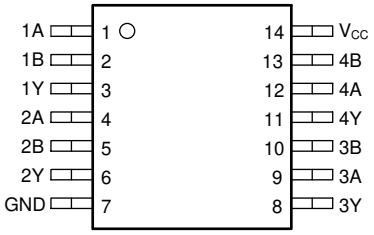
封装信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SN74ACT00-Q1	D（SOIC，14）	8.65mm × 6mm	8.65mm × 3.9mm
	PW（TSSOP，14）	5mm × 6.4mm	5mm × 4.4mm
	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm

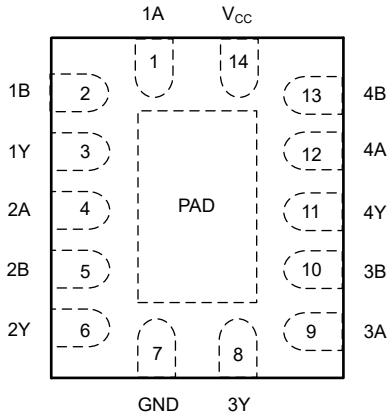
(1) 有关更多信息，请参阅 节 8。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。

功能表（每个逻辑门）

输入		输出 Y
A	B	
H	H	L
L	X	H
X	L	H



D 或 PW 封装（顶视图）



BQA 封装（顶视图）

内容

3 规格

3.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
V_{CC}	电源电压	-0.5	7	V
V_I	输入电压(2)	-0.5	V_{CC} + 0.5	V
V_O	输出电压(2)	-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳制电流（V_I < 0 或 V_I > V_{CC}）		±20	mA
I_{OK}	输出钳位电流（V_O< 0 或 V_O > V_{CC}）		±20	mA
I_O	持续输出电流（V_O = 0 至 V_{CC}）		±50	mA
	通过 V_{CC} 或 GND 的持续电流		±200	mA
T_{stg}	贮存温度	-65	150	°C

(1) 超出“绝对最大额定值”运行可能会对器件造成永久损坏。绝对最大额定值并不表示器件在这些条件下或在*建议运行条件*以外的任何其他条件下能够正常运行。如果超出“建议运行条件”但在“绝对最大额定值”范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

3.2 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
V_{CC}	电源电压	4.5	5.5	V
V_{IH}	高电平输入电压	2		V
V_{IL}	低电平输入电压		0.8	V
V_I	输入电压	0	V_{CC}	V
V_O	输出电压	0	V_{CC}	V
I_{OH}	高电平输出电流		-24	mA
I_{OL}	低电平输出电流		24	mA
Δt/Δv	输入转换上升或下降速率		8	ns/V
T_A	自然通风条件下的工作温度范围	-40	105	°C

(1) 器件的所有未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。参阅 TI *慢速或浮点 CMOS 输入影响*应用说明。

3.3 热性能信息

热指标(1)		D (SOIC)	PW (TSSOP)	BQA (WQFN)	单位
		14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	86(2)	145.7	91.3	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	—	76.5	99.4	°C/W
$R_{\theta JB}$	结至电路板热阻	—	102.0	61.0	°C/W
ψ_{JT}	结至顶部特征参数	—	18.8	14.5	°C/W
ψ_{JB}	结至电路板特征参数	—	100.7	60.8	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	—	—	37.0	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用手册。
(2) 封装热阻抗根据 JESD 51-7 计算。

3.4 电气特性

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			最小值	最大值	单位
			最小值	典型值	最大值			
V_{OH}	I_{OH} = -50μA	4.5V	4.4	4.49		4.4		V
		5.5V	5.4	5.49		5.4		
	I_{OH} = -24mA	4.5V	3.86			3.7		
		5.5V	4.86			4.7		
V_{OL}	I_{OL} = 50μA	4.5V		0.001	0.1		0.1	V
		5.5V		0.001	0.1		0.1	
	I_{OL} = 24mA	4.5V			0.36		0.5	
		5.5V			0.36		0.5	
I_I	V_I = V_{CC} 或 GND	5.5V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0	5.5V			2		40	μA
ΔI_{CC} (1)	一个输入电压为 3.4V，其他输入电压为 GND 或 V_{CC}	5.5V		0.6			1.6	mA
C_i	V_I = V_{CC} 或 GND	5V		2.6				pF

(1) 这是每个输入在指定 TTL 电压电平之一而不是 0V 或 V_{CC} 时电源电流的增加情况。

3.5 开关特性

在自然通风条件下的工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅图 4-1）

参数	从（输入）	至（输出）	T_A = 25°C			最小值	最大值	单位
			最小值	典型值	最大值			
t_{PLH}	A 或 B	Y	1.5	5.5	9	1	9.5	ns
t_{PHL}	A 或 B	Y	1.5	4	7	1	8	ns

3.6 工作特性

V_{CC} = 5V，T_A = 25°C

参数		测试条件	最小值	典型值	最大值	单位
Cpd	功率耗散电容	CL = 50pF，f = 1MHz		40		pF

4 参数测量信息

TEST	S1
t_{PLH}/t_{PHL}	Open

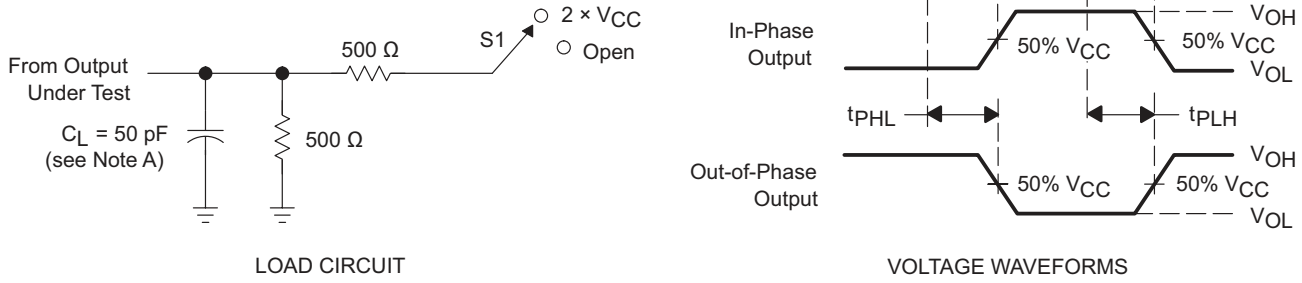
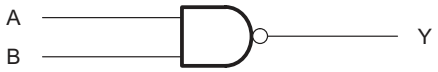


图 4-1. 负载电路和电压波形

5 详细说明

5.1 功能方框图



逻辑图，每个逻辑门（正逻辑）

6 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

6.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

7 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

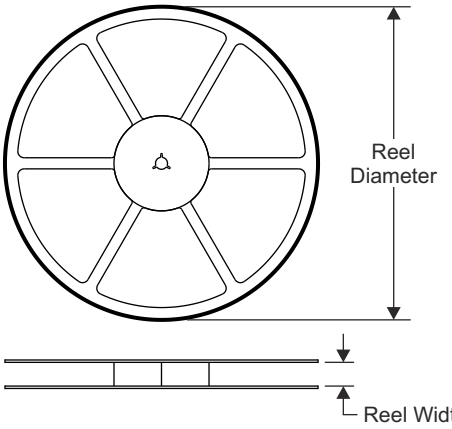
Changes from Revision A (April 2008) to Revision B (April 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更改了*封装信息* 表	1
• 向数据表添加了 PW 和 BQA 封装	1
• 新增了*热性能信息* 表	3

8 机械、封装和可订购信息

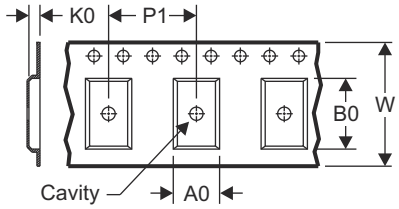
以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

8.1 卷带包装信息

REEL DIMENSIONS

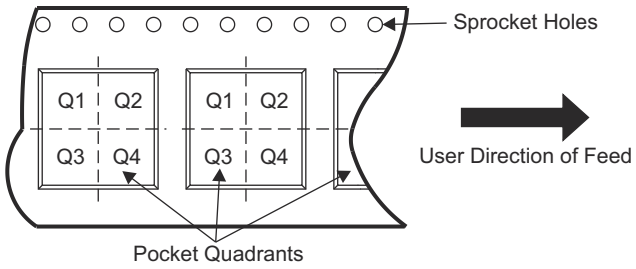


TAPE DIMENSIONS



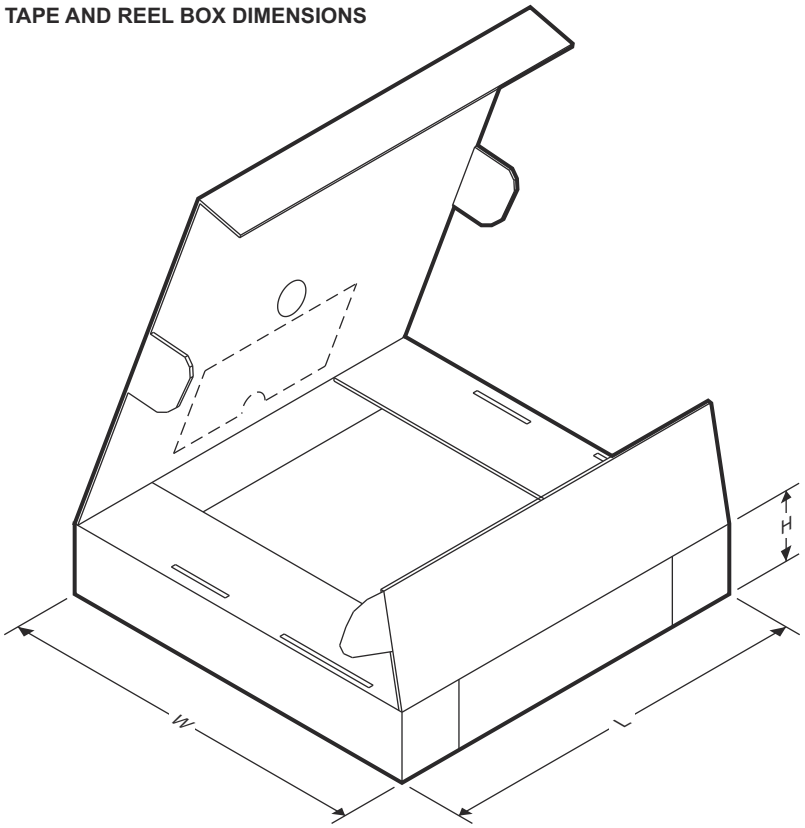
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



器件	封装类型	封装图	引脚	SPQ	卷带直径 (mm)	卷带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1象限

TAPE AND REEL BOX DIMENSIONS



器件	封装类型	封装图	引脚	SPQ	长度 (mm)	宽度 (mm)	高度 (mm)

8.2 机械数据

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT00PWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00Q
SN74ACT00PWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00Q
SN74ACT00TDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00TQ1
SN74ACT00TDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00TQ1
SN74ACT00WBQARQ1	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AD00Q
SN74ACT00WBQARQ1.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AD00Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74ACT00-Q1 :

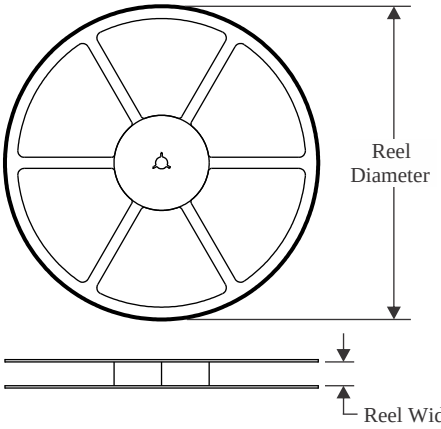
- Catalog : SN74ACT00
- Military : SN54ACT00

NOTE: Qualified Version Definitions:

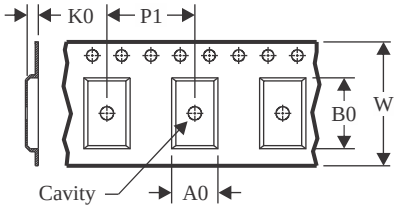
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

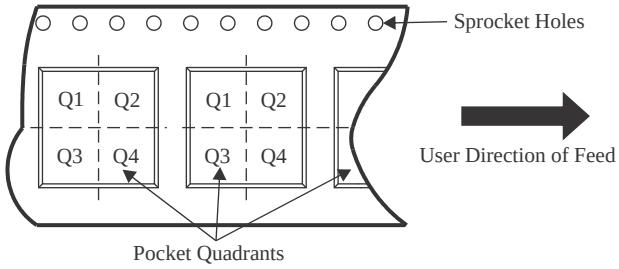


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

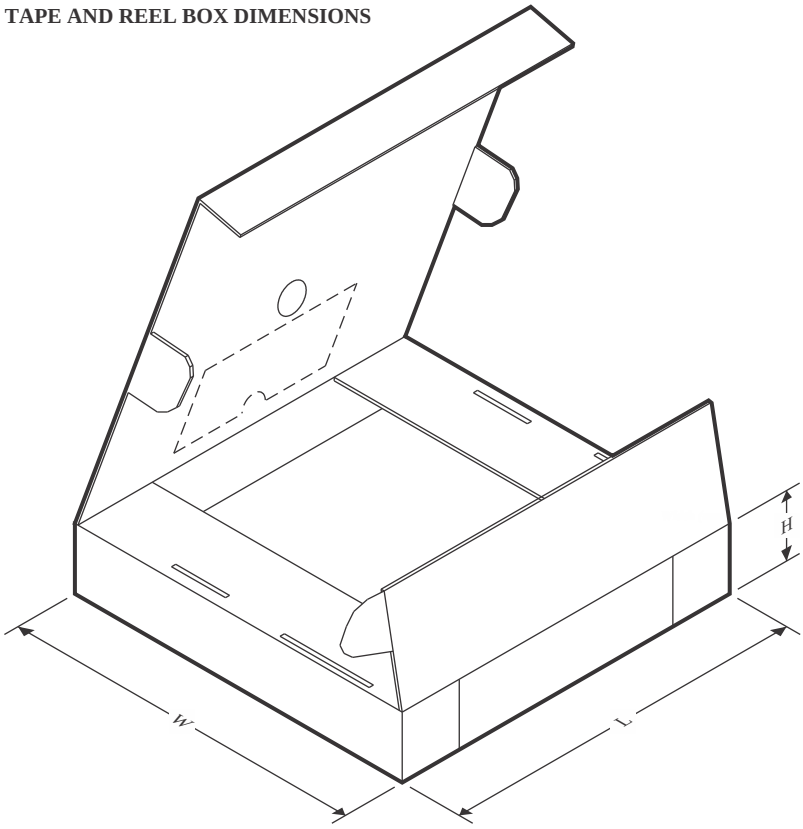
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT00PWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT00WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

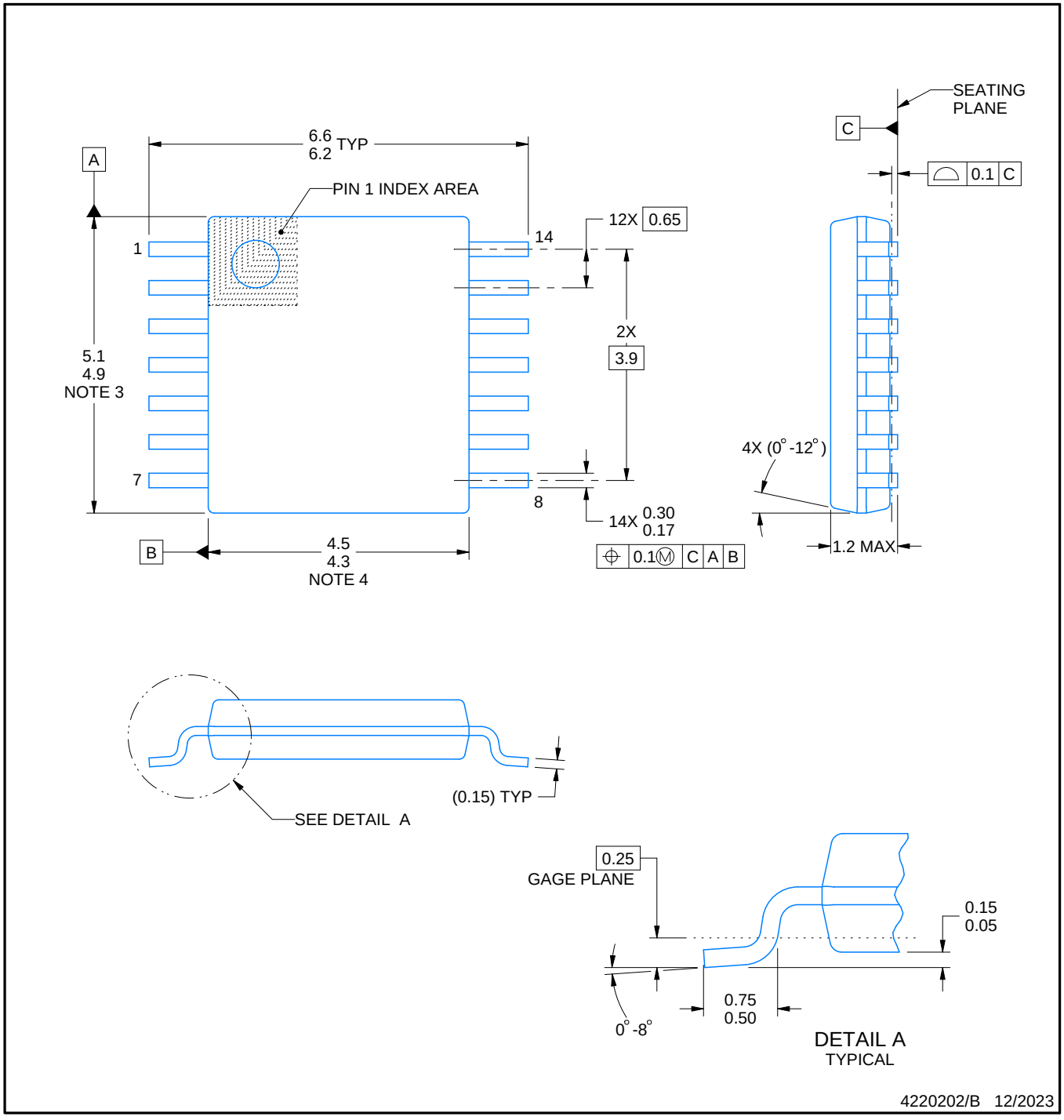
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT00PWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74ACT00WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

PACKAGE OUTLINE

PW0014A

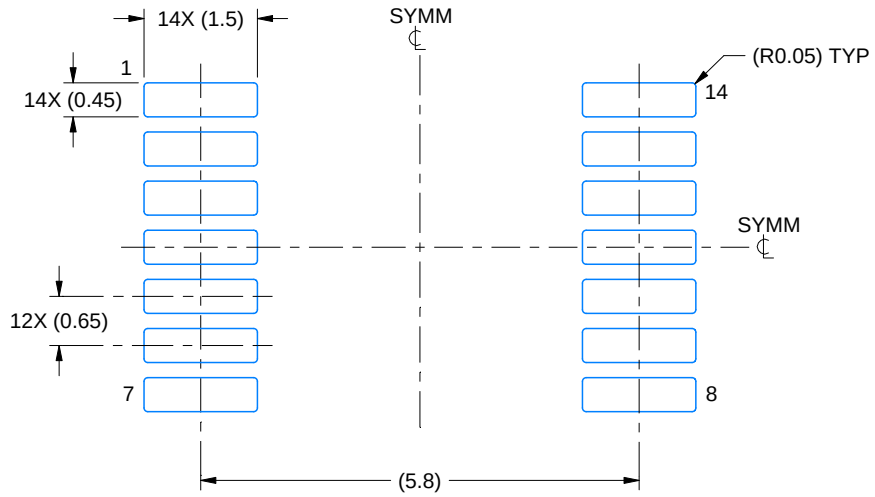
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

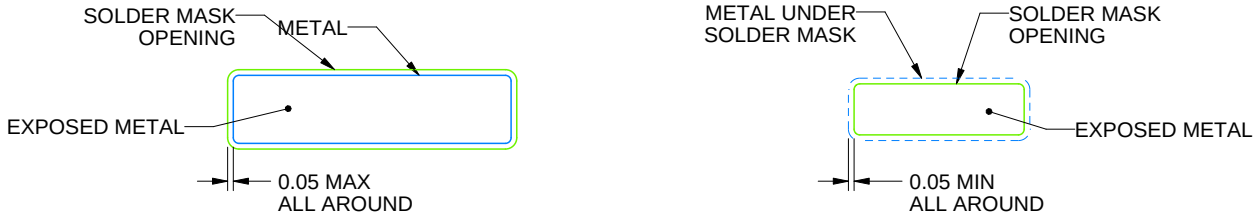


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

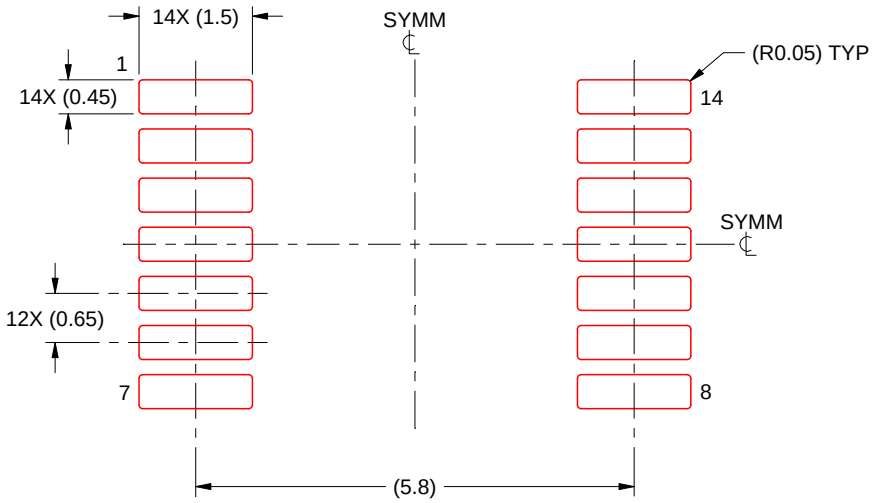


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

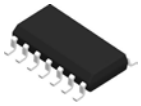


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

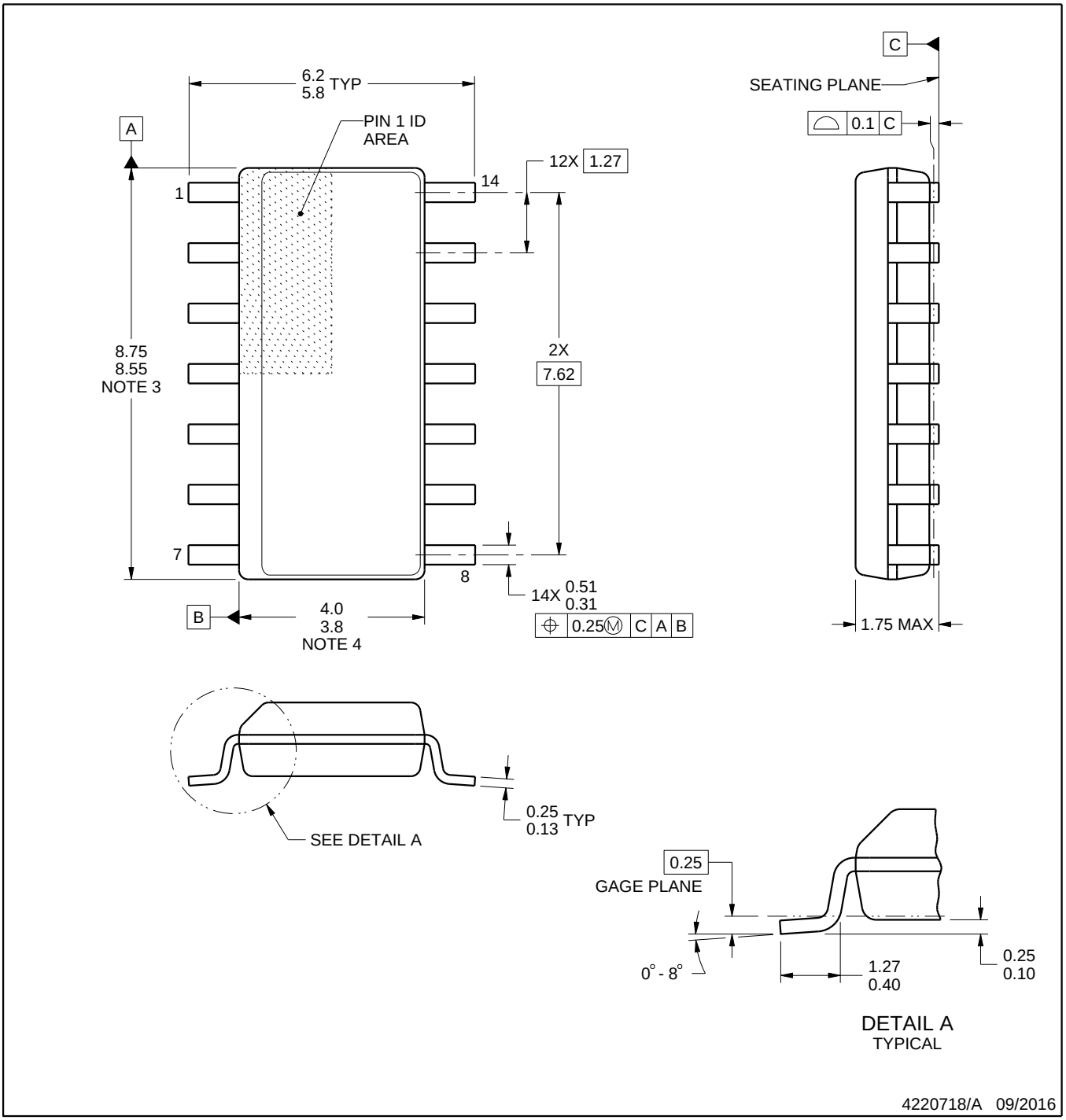


PACKAGE OUTLINE

D0014A

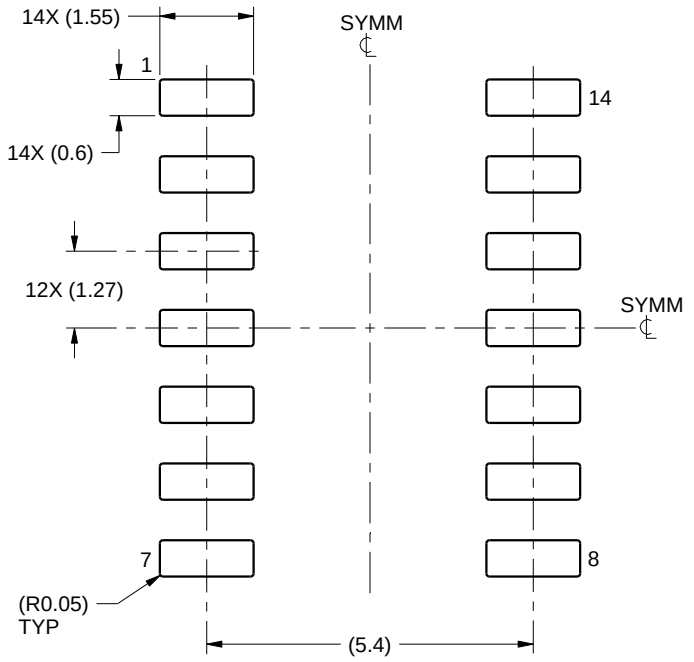
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

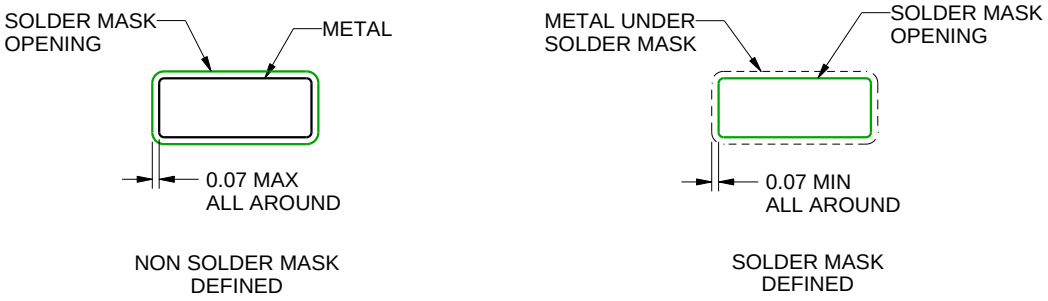


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

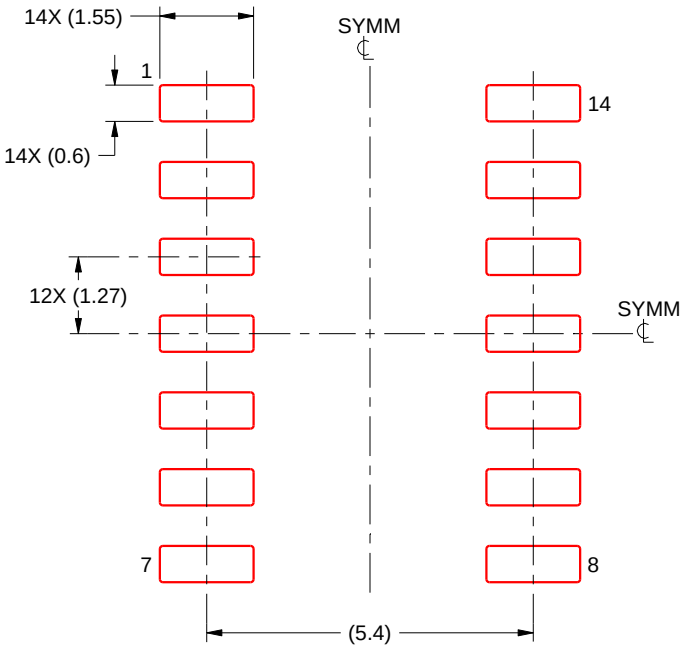
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

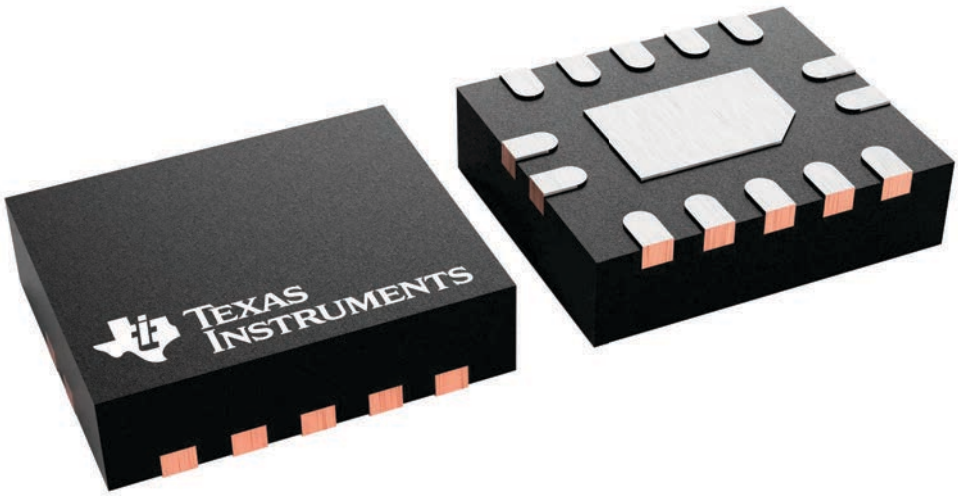
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

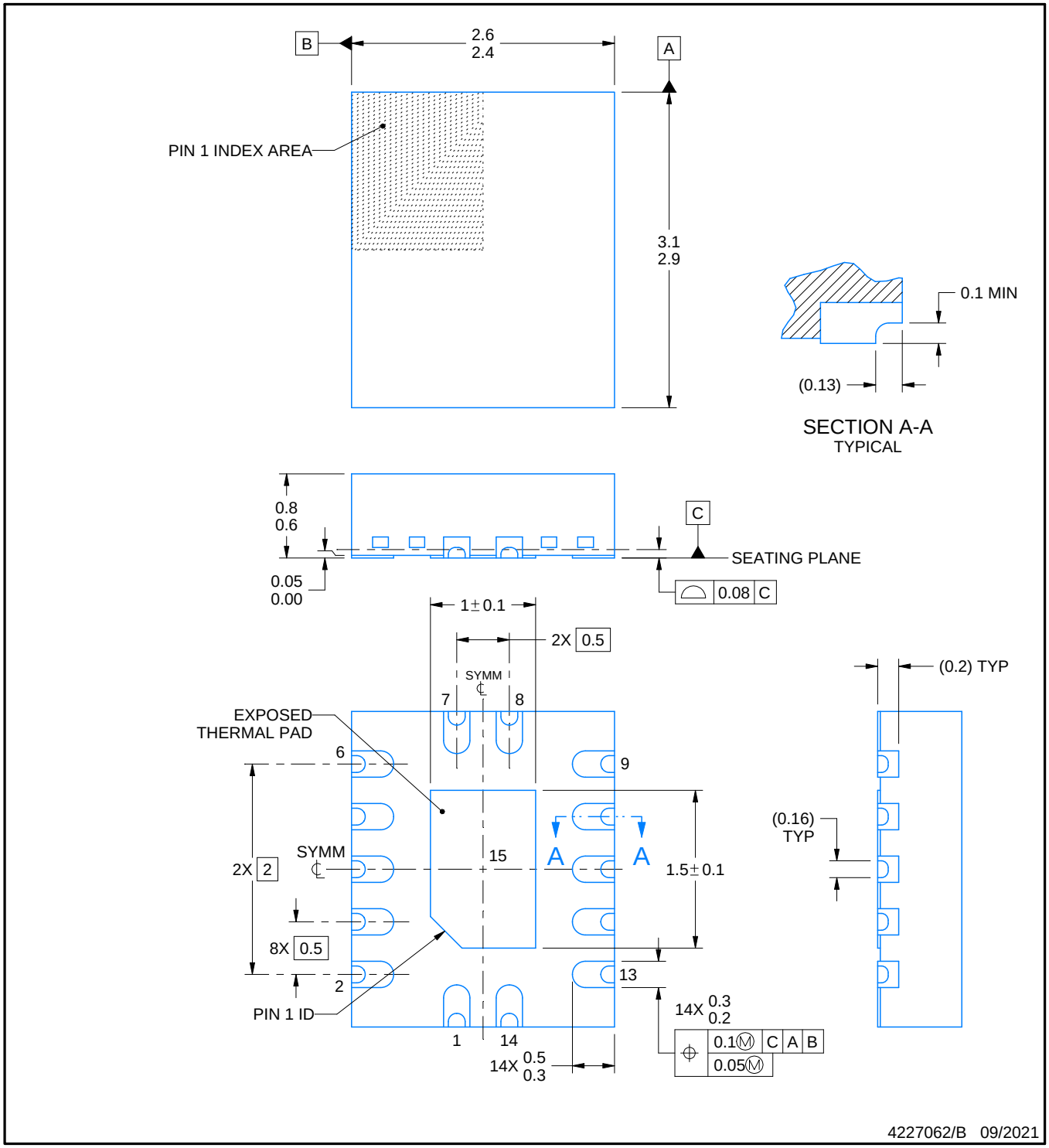


BQA0014B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

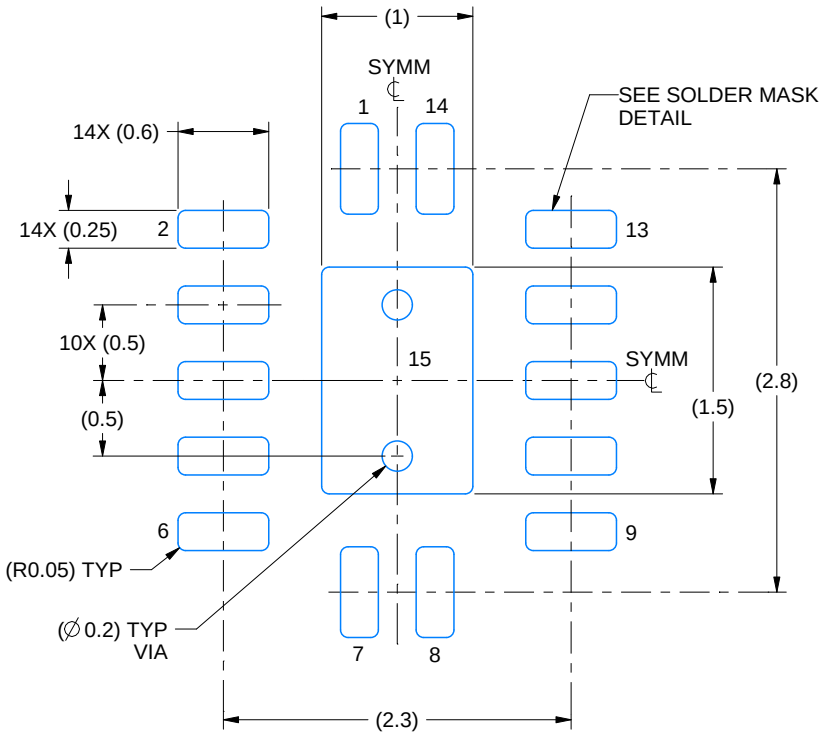
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

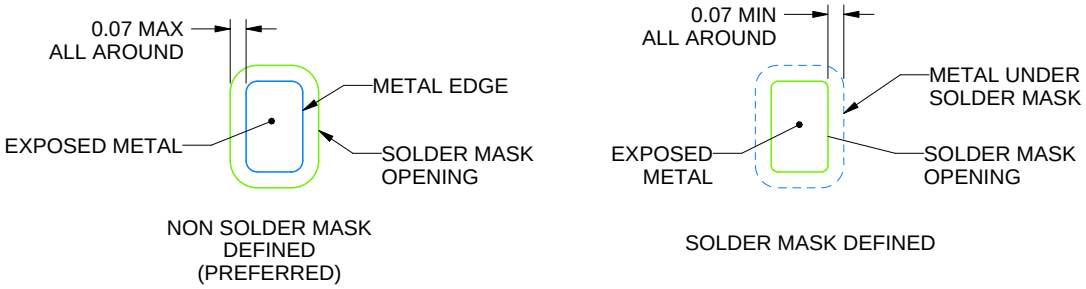
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

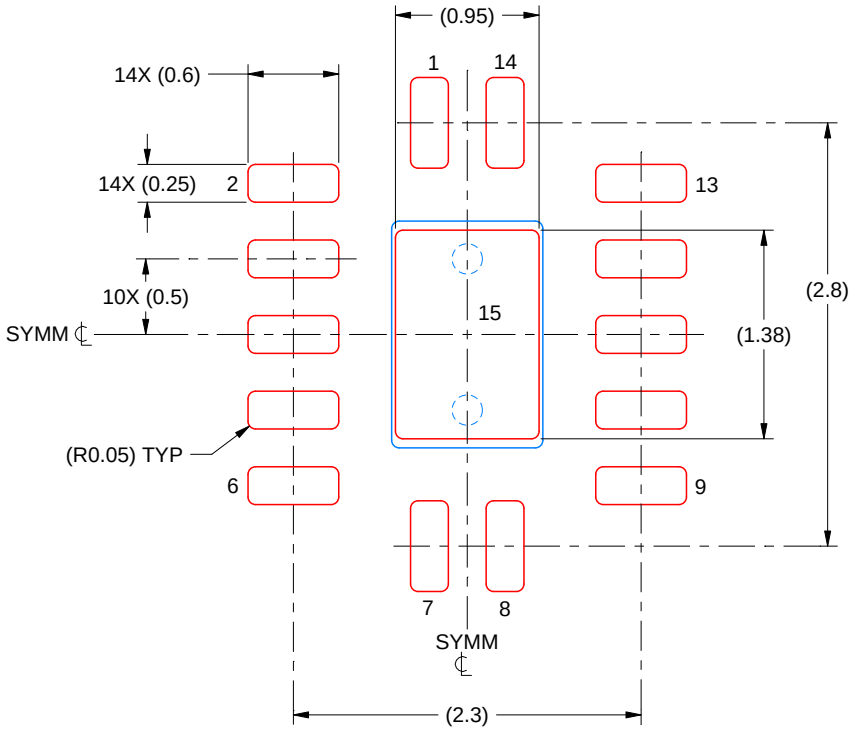


SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月