

# SN54ABT833, SN74ABT833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

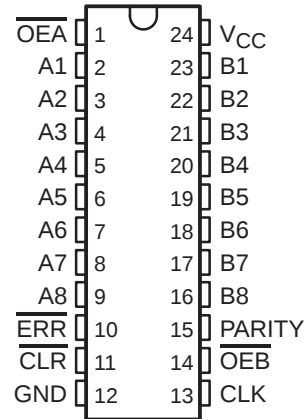
- State-of-the-Art **EPIC-II<sup>TM</sup>** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Parity Error Flag With Parity Generator/Checker
- Register for Storage of the Parity Error Flag
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

## description

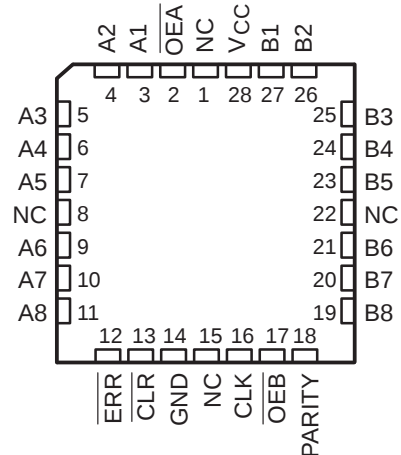
The 'ABT833 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error ( $\overline{ERR}$ ) output indicates whether or not an error in the B data has occurred. The output-enable ( $\overline{OEA}$  and  $\overline{OEB}$ ) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT833 provide true data at their outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the  $\overline{ERR}$  flag.  $\overline{ERR}$  is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear ( $\overline{CLR}$ ) input. When both  $\overline{OEA}$  and  $\overline{OEB}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

SN54ABT833 . . . JT PACKAGE  
SN74ABT833 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54ABT833 . . . FK PACKAGE  
(TOP VIEW)



SN54ABT833, SN74ABT833  
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

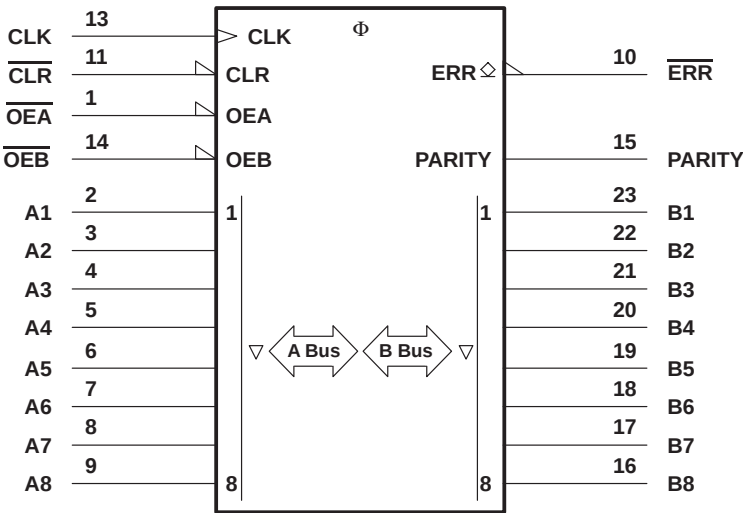
The SN54ABT833 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT833 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

| INPUTS           |                  |                  |               |                          |                                    | OUTPUT AND I/O |    |        |                             | FUNCTION                                        |
|------------------|------------------|------------------|---------------|--------------------------|------------------------------------|----------------|----|--------|-----------------------------|-------------------------------------------------|
| $\overline{OEB}$ | $\overline{OEA}$ | $\overline{CLR}$ | CLK           | $A_i$<br>$\Sigma$ OF H's | $B_i^{\dagger}$<br>$\Sigma$ OF H's | A              | B  | PARITY | $\overline{ERR}^{\ddagger}$ |                                                 |
| L                | H                | X                | X             | Odd<br>Even              | NA                                 | NA             | A  | L<br>H | NA                          | A data to B bus and<br>generate parity          |
| H                | L                | H                | $\uparrow$    | NA                       | Odd<br>Even                        | B              | NA | NA     | H<br>L                      | B data to A bus and<br>check parity             |
| X                | X                | L                | X             | X                        | X                                  | X              | NA | NA     | H                           | Check error-flag register                       |
| H                | H                | H                | No $\uparrow$ | X                        | X                                  | Z              | Z  | Z      | NC                          | Isolation $^{\S}$                               |
|                  |                  | L                | No $\uparrow$ | X                        |                                    |                |    |        | H                           |                                                 |
|                  |                  | H                | $\uparrow$    | Odd                      |                                    |                |    |        | H                           |                                                 |
| L                | L                | X                | $\uparrow$    | Even                     | NA                                 | NA             | A  | H<br>L | NA                          | A data to B bus and<br>generate inverted parity |
|                  |                  |                  | X             | Odd                      |                                    |                |    |        |                             |                                                 |

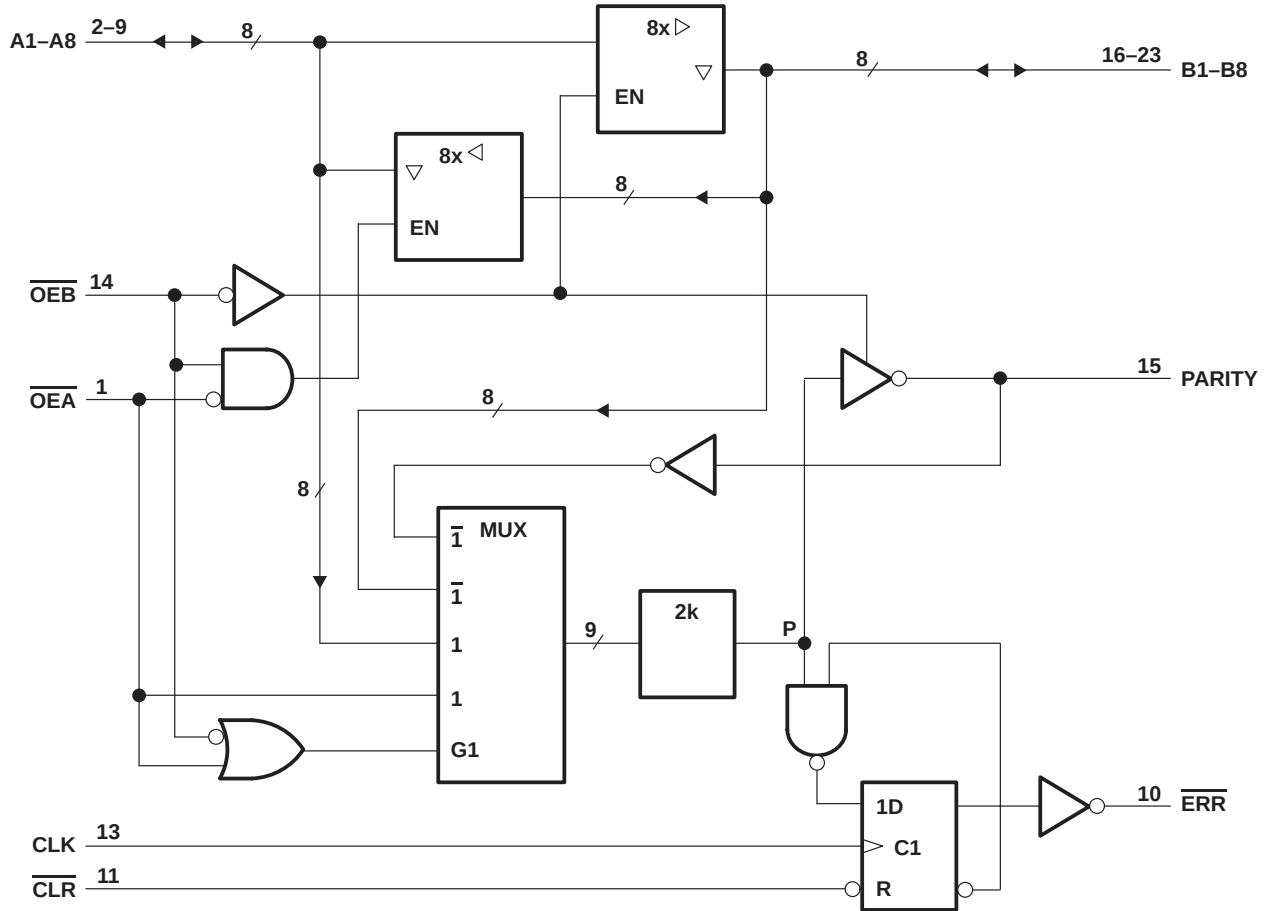
NA = not applicable, NC = no change, X = don't care  
 $^{\dagger}$  Summation of high-level inputs includes PARITY along with  $B_i$  inputs.  
 $^{\ddagger}$  Output states shown assume  $\overline{ERR}$  was previously high.  
 $^{\S}$  In this mode,  $\overline{ERR}$  (when clocked) shows inverted parity of the A bus.

logic symbol $^{\P}$



$^{\P}$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

ERROR-FLAG FUNCTION TABLE

| INPUTS                  |            | INTERNAL TO DEVICE | OUTPUT PRE-STATE                      | OUTPUT $\overline{\text{ERR}}$ | FUNCTION |
|-------------------------|------------|--------------------|---------------------------------------|--------------------------------|----------|
| $\overline{\text{CLR}}$ | CLK        | POINT P            | $\overline{\text{ERR}}_{n-1}^\dagger$ |                                |          |
| H                       | $\uparrow$ | H                  | H                                     | H                              | Sample   |
| H                       | $\uparrow$ | X                  | L                                     | L                              |          |
| H                       | $\uparrow$ | L                  | X                                     | L                              |          |
| L                       | X          | X                  | X                                     | H                              | Clear    |

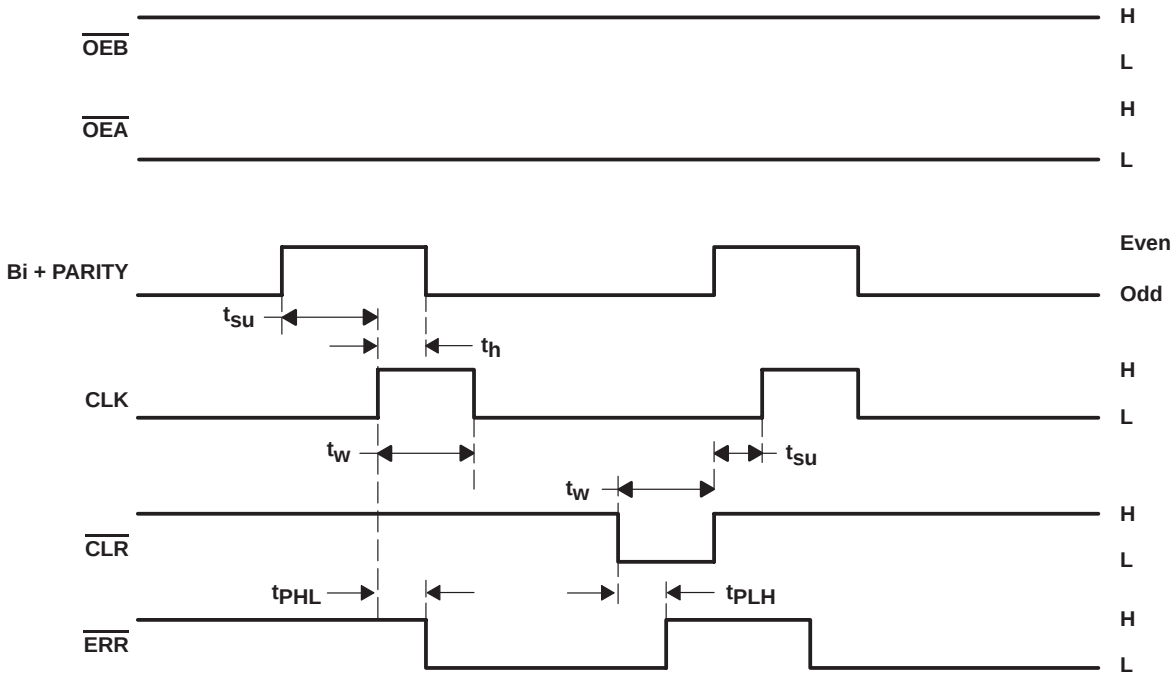
$^\dagger$  The state of ERR before any changes at CLR, CLK, or point P

# SN54ABT833, SN74ABT833

## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

### error-flag waveforms



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1)                | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT833              | 96 mA           |
| SN74ABT833                                                                | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package         | 81°C/W          |
| NT package                                                                | 67°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

# SN54ABT833, SN74ABT833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

## recommended operating conditions (see Note 3)

|                 |                                    | SN54ABT833      |                 | SN74ABT833 |                 | UNIT |
|-----------------|------------------------------------|-----------------|-----------------|------------|-----------------|------|
|                 |                                    | MIN             | MAX             | MIN        | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 4.5             | 5.5             | 4.5        | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2               |                 | 2          |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |                 | 0.8             |            | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      | 0               | V <sub>CC</sub> | 0          | V <sub>CC</sub> | V    |
| V <sub>OH</sub> | High-level output voltage          | ERR             |                 | 5.5        |                 | V    |
| I <sub>OH</sub> | High-level output current          | Except ERR      |                 | –32        |                 | mA   |
| I <sub>OL</sub> | Low-level output current           | 48              |                 | 64         |                 | mA   |
| Δt/Δv           | Input transition rise or fall rate | Outputs enabled |                 | 5          |                 | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | –55             | 125             | –40        | 85              | °C   |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

# SN54ABT833, SN74ABT833

## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          |                        | TEST CONDITIONS                                                                      |                          | T <sub>A</sub> = 25°C |      |       | SN54ABT833 |       | SN74ABT833 |       | UNIT |
|--------------------|------------------------|--------------------------------------------------------------------------------------|--------------------------|-----------------------|------|-------|------------|-------|------------|-------|------|
|                    |                        |                                                                                      |                          | MIN                   | TYP† | MAX   | MIN        | MAX   | MIN        | MAX   |      |
| V <sub>IK</sub>    |                        | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                     |                          |                       |      | -1.2  |            | -1.2  |            | -1.2  | V    |
| V <sub>OH</sub>    | All outputs except ERR | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                     |                          | 2.5                   |      |       | 2.5        |       | 2.5        |       | V    |
|                    |                        | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                       |                          | 3                     |      |       | 3          |       | 3          |       |      |
|                    |                        | V <sub>CC</sub> = 4.5 V                                                              | I <sub>OH</sub> = -24 mA | 2                     |      |       | 2          |       |            |       |      |
|                    |                        |                                                                                      | I <sub>OH</sub> = -32 mA | 2*                    |      |       |            |       | 2          |       |      |
| V <sub>OL</sub>    |                        | V <sub>CC</sub> = 4.5 V                                                              | I <sub>OL</sub> = 24 mA  |                       |      | 0.55  |            | 0.55  |            |       | V    |
|                    |                        |                                                                                      | I <sub>OL</sub> = 64 mA  |                       |      | 0.55* |            |       |            | 0.55  |      |
| V <sub>hys</sub>   |                        |                                                                                      |                          |                       | 100  |       |            |       |            |       | mV   |
| I <sub>OH</sub>    | ERR                    | V <sub>CC</sub> = 4.5 V, V <sub>OH</sub> = 5.5 V                                     |                          |                       |      | 20    |            | 20    |            | 20    | μA   |
| I <sub>I</sub>     | Control inputs         | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                     |                          |                       |      | ±1    |            | ±1    |            | ±1    | μA   |
|                    | A or B ports           |                                                                                      |                          |                       |      | ±100  |            | ±100  |            | ±100  |      |
| I <sub>IL</sub>    | A or B ports           | V <sub>CC</sub> = 0, V <sub>I</sub> = GND                                            |                          |                       |      | -50   |            | -50   |            | -50   | μA   |
| I <sub>OZH</sub> ‡ |                        | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V                                      |                          |                       |      | 50    |            | 50    |            | 50    | μA   |
| I <sub>OZL</sub> ‡ |                        | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V                                      |                          |                       |      | -50   |            | -50   |            | -50   | μA   |
| I <sub>off</sub>   |                        | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                        |                          |                       |      | ±100  |            |       |            | ±100  | μA   |
| I <sub>CEX</sub>   |                        | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      | Outputs high             |                       |      | 50    |            | 50    |            | 50    | μA   |
| I <sub>O</sub> §   |                        | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      |                          | -50                   | -100 | -200¶ | -50        | -200¶ | -50        | -200¶ | mA   |
| I <sub>CC</sub>    | A or B ports           | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | Outputs high             |                       | 1    | 250   |            | 250   |            | 250   | μA   |
|                    |                        |                                                                                      | Outputs low              |                       | 24   | 38¶   |            | 38¶   |            | 38¶   | mA   |
|                    |                        |                                                                                      | Outputs disabled         |                       | 0.5  | 250   |            | 250   |            | 250   | μA   |
| ΔI <sub>CC</sub> # | Data inputs            | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | Outputs enabled          |                       |      | 1.5   |            | 1.5   |            | 1.5   | mA   |
|                    |                        |                                                                                      | Outputs disabled         |                       |      | 50    |            | 50    |            | 50    | μA   |
|                    | Control inputs         | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                          |                       |      | 1.5   |            | 1.5   |            | 1.5   | mA   |
| C <sub>i</sub>     | Control inputs         | V <sub>I</sub> = 2.5 V or 0.5 V                                                      |                          |                       |      | 4.5   |            |       |            |       | pF   |
| C <sub>io</sub>    | A or B ports           | V <sub>O</sub> = 2.5 V or 0.5 V                                                      |                          |                       |      | 10.5  |            |       |            |       | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ These limits may vary among suppliers.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ABT833, SN74ABT833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|          |                                  |                             | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     | SN54ABT833 |     | SN74ABT833 |     | UNIT |
|----------|----------------------------------|-----------------------------|-----------------------------------------------------|-----|------------|-----|------------|-----|------|
|          |                                  |                             | MIN                                                 | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_W$    | Pulse duration                   | CLK high or low             | 3                                                   |     | 3          |     | 3          |     | ns   |
|          |                                  | $\overline{\text{CLR}}$ low | 3                                                   |     | 3          |     | 3          |     |      |
| $t_{su}$ | Setup time before CLK $\uparrow$ | B or PARITY high            | 9.8                                                 |     | 9.8        |     | 9.8        |     | ns   |
|          |                                  | B or PARITY low             | 8.1                                                 |     | 8.1        |     | 8.1        |     |      |
|          |                                  | $\overline{\text{CLR}}$     | 2                                                   |     | 2          |     | 2          |     |      |
| $t_h$    | Hold time after CLK $\uparrow$   | B or PARITY                 | 0                                                   |     | 0          |     | 0          |     | ns   |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT)         | TO<br>(OUTPUT)          | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |                |                 | SN54ABT833      |      | SN74ABT833      |                 | UNIT |
|-----------|-------------------------|-------------------------|-----------------------------------------------------|----------------|-----------------|-----------------|------|-----------------|-----------------|------|
|           |                         |                         | MIN                                                 | TYP $^\dagger$ | MAX             | MIN             | MAX  | MIN             | MAX             |      |
| $t_{PLH}$ | A or B                  | B or A                  | 1.2                                                 | 2.8            | 4.8             | 1.2             | 5.4  | 1.2             | 5.3             | ns   |
| $t_{PHL}$ |                         |                         | 1                                                   | 3              | 4.8 $^\ddagger$ | 1               | 5.4  | 1               | 5.3 $^\ddagger$ |      |
| $t_{PLH}$ | A                       | PARITY                  | 2.1                                                 | 5.5            | 9.5             | 2.1             | 11.3 | 2.1             | 11.2            | ns   |
| $t_{PHL}$ |                         |                         | 2.5                                                 | 5.3            | 9.7             | 2.5             | 11.1 | 2.5             | 11              |      |
| $t_{PZH}$ | $\overline{\text{OE}}$  | PARITY                  | 2.6                                                 | 6.2            | 8.5             | 2.6             | 10.6 | 2.6             | 10.5            | ns   |
| $t_{PZL}$ |                         |                         | 2.6 $^\ddagger$                                     | 5.8            | 8.6             | 2.6 $^\ddagger$ | 10.1 | 2.6 $^\ddagger$ | 10              |      |
| $t_{PLH}$ | $\overline{\text{CLR}}$ | $\overline{\text{ERR}}$ | 1                                                   | 3.2            | 4.8 $^\ddagger$ | 1               | 5.3  | 1               | 5.2             | ns   |
| $t_{PHL}$ | CLK                     |                         | 1.2 $^\ddagger$                                     | 2.8            | 5.7             | 1.2 $^\ddagger$ | 6.3  | 1.2 $^\ddagger$ | 6.2             |      |
| $t_{PZH}$ | $\overline{\text{OE}}$  | A, B, or PARITY         | 1                                                   | 3.7            | 5.8 $^\ddagger$ | 1               | 6.6  | 1               | 6.5 $^\ddagger$ | ns   |
| $t_{PZL}$ |                         |                         | 1.3 $^\ddagger$                                     | 3.8            | 5.8             | 1.3 $^\ddagger$ | 6.6  | 1.3 $^\ddagger$ | 6.5 $^\ddagger$ |      |
| $t_{PHZ}$ | $\overline{\text{OE}}$  | A, B, or PARITY         | 1.9 $^\ddagger$                                     | 4.4            | 7.3             | 1.9 $^\ddagger$ | 8    | 1.9 $^\ddagger$ | 7.9             | ns   |
| $t_{PLZ}$ |                         |                         | 2.2 $^\ddagger$                                     | 4.4            | 7.7             | 2.2 $^\ddagger$ | 8.2  | 2.2 $^\ddagger$ | 8.1             |      |

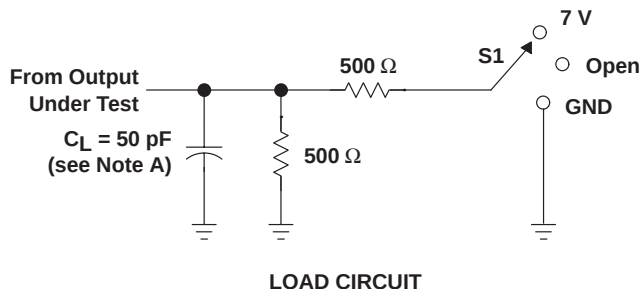
$^\dagger$  All typical values are at  $V_{CC} = 5\text{ V}$ .

$^\ddagger$  These limits may vary among suppliers.

# SN54ABT833, SN74ABT833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

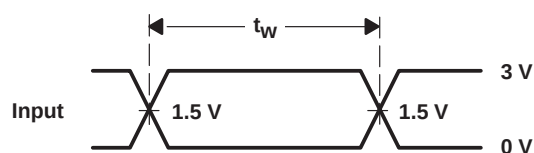
SCBS195C – FEBRUARY 1991 – REVISED JANUARY 1997

## PARAMETER MEASUREMENT INFORMATION

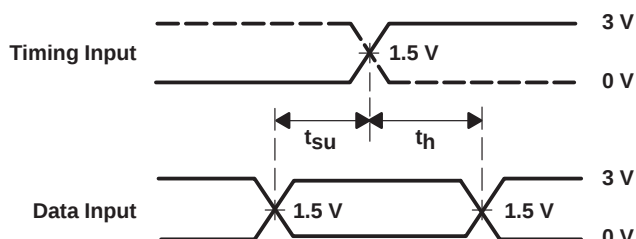


| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |

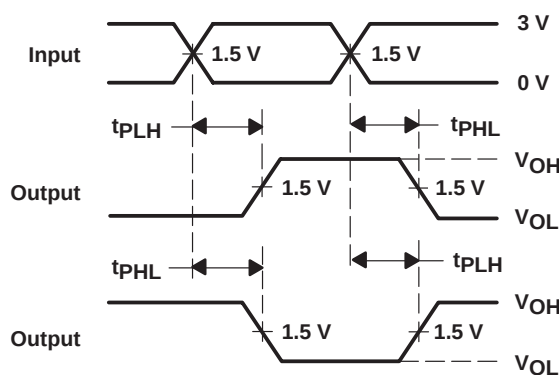
| ERR       | S1  |
|-----------|-----|
| $t_{PHL}$ | 7 V |
| $t_{PLH}$ | 7 V |



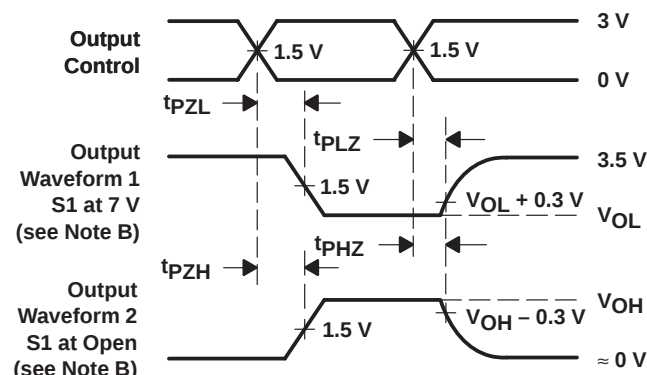
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74ABT833DW          | Active        | Production           | SOIC (DW)   24 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT833              |
| SN74ABT833DW.B        | Active        | Production           | SOIC (DW)   24 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT833              |

- <sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).
- <sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- <sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- <sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- <sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- <sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE

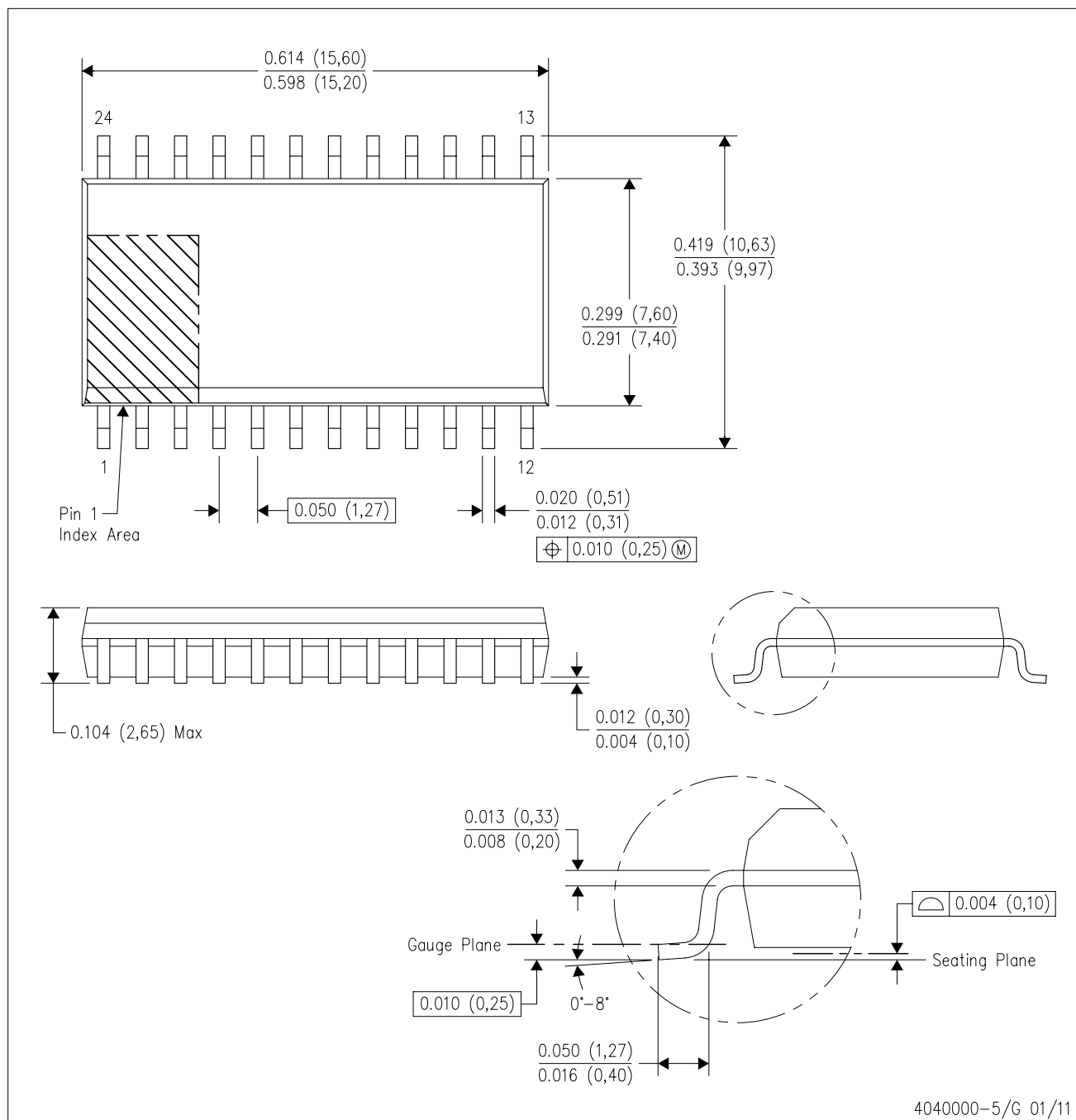


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ABT833DW   | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74ABT833DW.B | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |

DW (R-PDSO-G24)

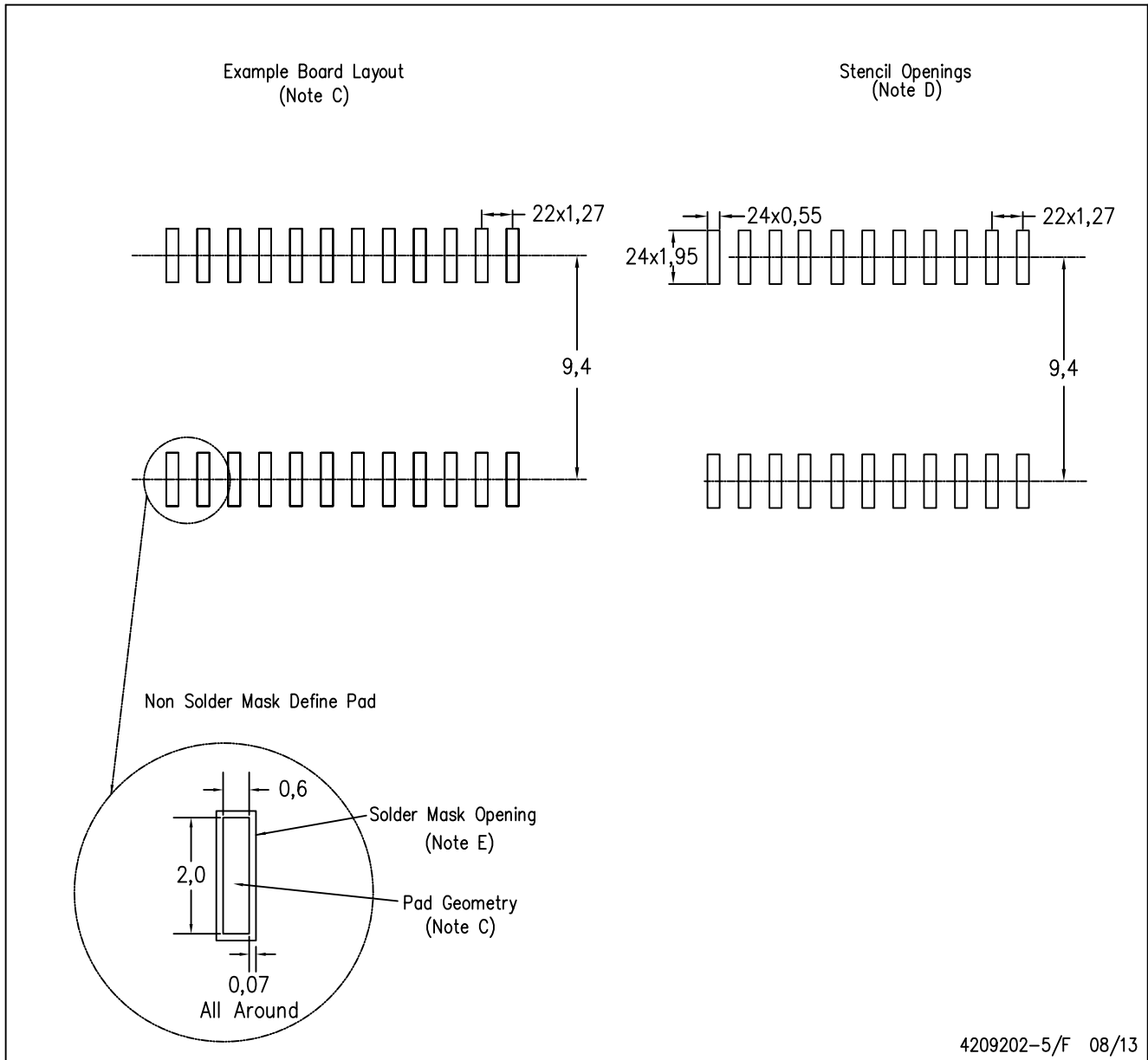
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated