

SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

- State-of-the-Art **EPIC-IITM** BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

description

These octal transparent D-type latches with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (LE) input is high, the \overline{Q} outputs follow the complements of the data (D) inputs. When LE is taken low, the \overline{Q} outputs are latched at the inverse of the levels at the D inputs.

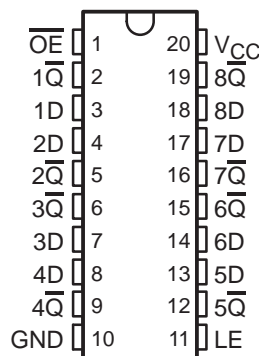
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

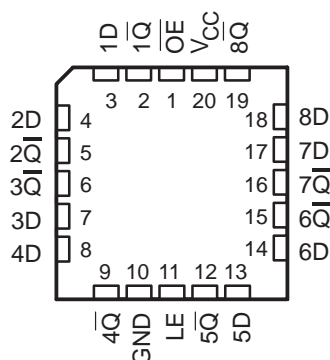
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT533 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT533A is characterized for operation from -40°C to 85°C .

SN54ABT533 . . . J OR W PACKAGE
SN74ABT533A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT533 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II^B is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

INPUTS			OUTPUT \bar{Q}
\overline{OE}	LE	D	
L	H	H	L
L	H	L	H
L	L	X	\bar{Q}_0
H	X	X	Z

Logic diagram of a 1D latch. The latch is represented by a central block labeled 'C1' and '1D'. The '1D' input is connected to a signal labeled '1D' (pin 3). The 'C1' input is connected to a signal labeled 'LE' (pin 11) through an inverter. The output of the latch is labeled '1Q' (pin 2) and is connected to an inverter. A signal labeled 'OE' (pin 1) is connected to an inverter, whose output is connected to the output of the latch. A bracket at the bottom indicates that the output is connected to seven other channels.

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT533	96 mA
SN74ABT533A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT533, SN74ABT533A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

recommended operating conditions (see Note 3)

		SN54ABT533		SN74ABT533A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–24		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT533		SN74ABT533A		UNIT
					MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = –3 mA			2.5		2.5		2.5	V
	V _{CC} = 5 V, I _{OH} = –3 mA			3		3		3	
	V _{CC} = 4.5 V			2		2			
				2*				2	
V _{OL}	V _{CC} = 4.5 V			0.55		0.55			V
				0.55*				0.55	
V _{hys}				100					mV
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10		10		10	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			–10		–10		–10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±150				±150	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high	50		50		50	μA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V	–50	–140	–180	–50	–180	–50	–180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high	1	250	250		250	μA
			Outputs low	24	30	30		30	mA
			Outputs disabled	0.5	250	250		250	μA
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		Outputs high		1.5	1.5		1.5	mA
			Outputs low		1.5	1.5		1.5	
			Outputs disabled		1.5	1.5		1.5	
C _i	V _I = 2.5 V or 0.5 V			3.5					pF
C _o	V _O = 2.5 V or 0.5 V			6.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT533, SN74ABT533A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT533		UNIT
			$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$		
			MIN	MAX	
t_w	Pulse duration, LE high		3.3	3.3	ns
t_{su}	Setup time, data before LE↓	High or low	2.1	2.1	ns
t_h	Hold time, data after LE↓	High or low	1.5	1.5	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT533A		UNIT
			$V_{CC} = 5\text{ V},$ $T_A = 25^{\circ}\text{C}$		
			MIN	MAX	
t_w	Pulse duration, LE high		3.3	3.3	ns
t_{su}	Setup time, data before LE↓	High or low	2.1	2.1	ns
t_h	Hold time, data after LE↓	High or low	2.1	2.1	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT533				UNIT	
			V _{CC} = 5 V, T _A = 25°C			MIN		MAX
			MIN	TYP	MAX			
t _{PLH}	D	\overline{Q}	1.9	4.2	5.4	1.9	6.7	ns
t _{PHL}			3.1	4.9	6.3	3.1	6.9	
t _{PLH}	LE	\overline{Q}	2.7	4.9	6.2	2.7	7.6	ns
t _{PHL}			3.5	5.4	6.8	3.5	7.5	
t _{PZH}	\overline{OE}	\overline{Q}	1.6	3.7	4.8	1.6	5.8	ns
t _{PZL}			2.4	4.2	6.2	2.4	6.9	
t _{PHZ}	\overline{OE}	\overline{Q}	2.8	5.1	6.2	2.8	7.2	ns
t _{PLZ}			2	4.1	6	2	6.9	

SN54ABT533, SN74ABT533A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT533A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	D	\overline{Q}	1.7	4.2	5.4	1.7	6.4	ns
t _{PHL}			2.6	4.9	6.3	2.6	6.6	
t _{PLH}	LE	\overline{Q}	2.7	4.9	6.2	2.7	7.3	ns
t _{PHL}			3.5	5.4	6.8	3.5	7.3	
t _{PZH}	\overline{OE}	\overline{Q}	1.6	3.7	4.8	1.6	5.7	ns
t _{PZL}			2.4	4.2	6.2	2.4	6.7	
t _{PHZ}	\overline{OE}	\overline{Q}	1.6	5.1	6.2	1.6	6.9	ns
t _{PLZ}			2	4.1	6	2	6.5	

SN54ABT533, SN74ABT533A

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



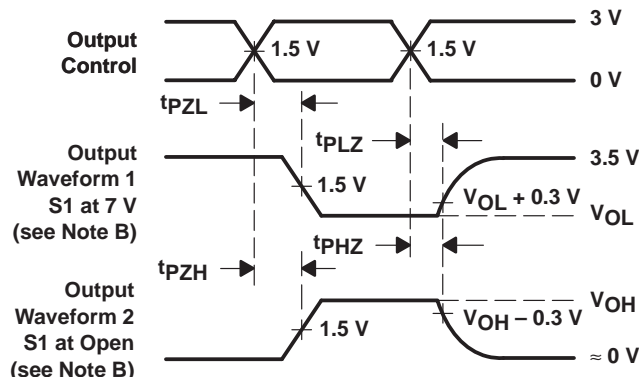
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9584301Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9584301Q2A SNJ54 ABT533FK
5962-9584301QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9584301QR A SNJ54ABT533J
SN74ABT533AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT533AN
SN74ABT533AN.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT533AN
SN74ABT533APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB533A
SN74ABT533APWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB533A
SNJ54ABT533FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9584301Q2A SNJ54 ABT533FK
SNJ54ABT533J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9584301QR A SNJ54ABT533J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT533APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT533APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9584301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ABT533AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT533AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ABT533FK	FK	LCCC	20	55	506.98	12.06	2030	NA

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated