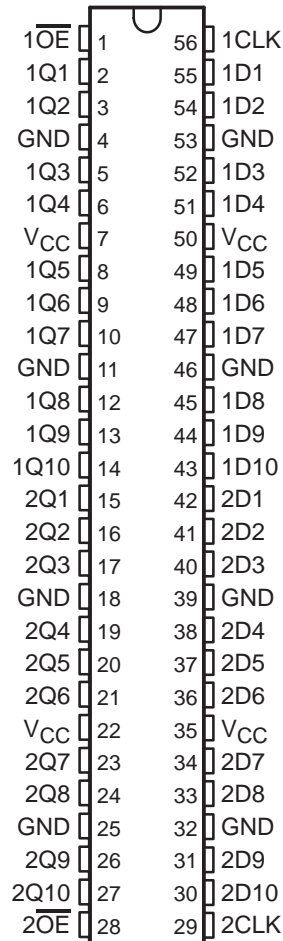


SN54ABT16821, SN74ABT16821 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), 300-mil Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16821 . . . WD PACKAGE
SN74ABT16821 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 20-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16821 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16821 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**TEXAS
INSTRUMENTS**

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INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q_0
H	X	X	Z

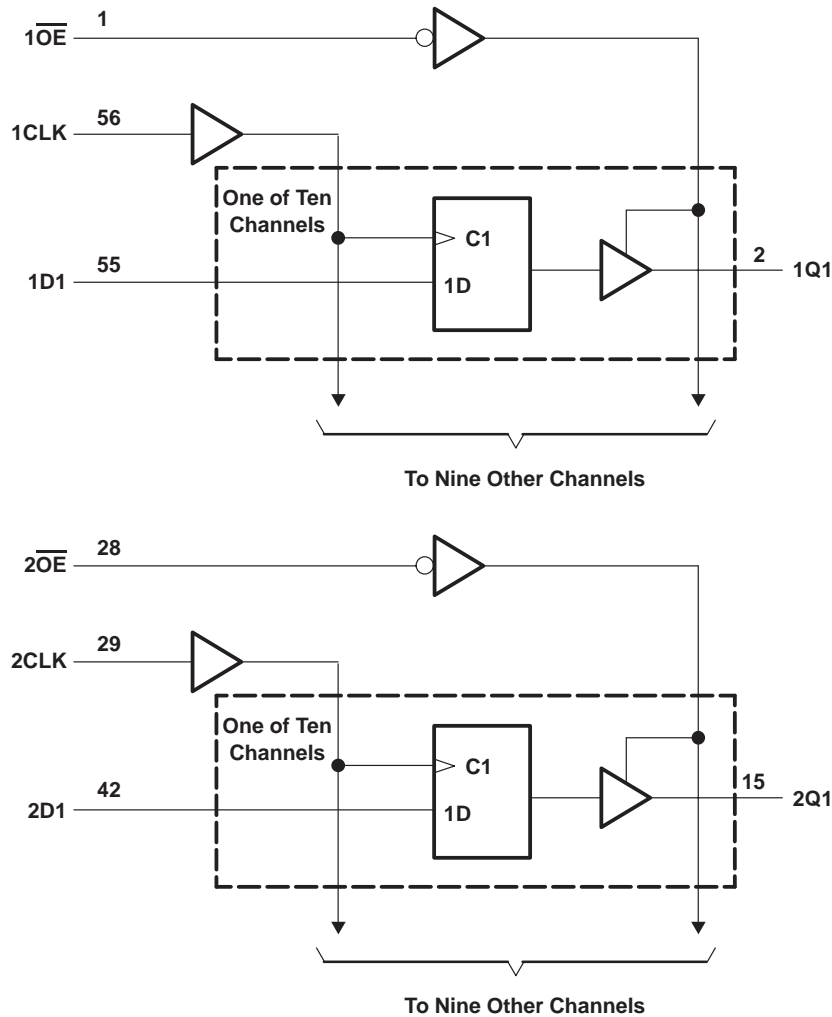
Pin diagram of the 74VHC04 hex inverters. The diagram shows a 16-pin package with pins 1 through 16. Pins 1, 5, 9, and 13 are labeled 1OE, 1CLK, 2OE, and 2CLK respectively. Pins 2, 3, 4, 10, 11, 12, 14, 15, and 16 are labeled 1Q1 through 1Q9 and 2Q1 through 2Q9. The internal circuitry shows two inverters, each with a 2-input NAND gate (EN2, EN4) and a 3-input NAND gate (C1, C3). The output of the first inverter is 1Q1 and the output of the second inverter is 2Q1.

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ABT16821, SN74ABT16821 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16821	96 mA
SN74ABT16821	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

SN54ABT16821, SN74ABT16821

20-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54ABT16821		SN74ABT16821		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25^\circ\text{C}$			SN54ABT16821		SN74ABT16821		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2		–1.2		–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$		2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$		3			3		3		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
		$I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$			0.55		0.55			V
		$I_{OL} = 64\text{ mA}$			0.55*				0.55	
V_{hys}				100						mV
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND				± 1		± 1		± 1	μA
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$				50		50		50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$				–50		–50		–50	μA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$				± 100				± 100	μA
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$ Outputs high				50		50		50	μA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$		–50	–100	–200	–50	–200	–50	–200	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			500		500		500	μA
		Outputs low			89		89		89	mA
		Outputs disabled			500		500		500	μA
$\Delta I_{CC}\S$	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	$V_I = 2.5\text{ V}$ or 0.5 V				3.5					pF
C_o	$V_O = 2.5\text{ V}$ or 0.5 V				7.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54ABT16821, SN74ABT16821 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT16821		SN74ABT16821		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK \uparrow	1.8		1.8		1.8		ns
t_h	Hold time, data after CLK \uparrow	1.3		1.3		1.3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT16821		SN74ABT16821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	1.3	3.7	5.1	1.3	6.7	1.3	6.1	ns
t_{PHL}			1.6	3.9	5.1	1.6	5.8	1.6	5.4	
t_{PZH}	$\overline{\text{OE}}$	Q	1.1	3.2	4.7	1.1	5.8	1.1	5.7	ns
t_{PZL}			1.6	3.8	5	1.6	5.7	1.6	5.6	
t_{PHZ}	$\overline{\text{OE}}$	Q	2	4.5	5.7	2	6.6	2	6.5	ns
t_{PLZ}			1.8	4.1	5.8	1.8	8.4	1.8	7.1	

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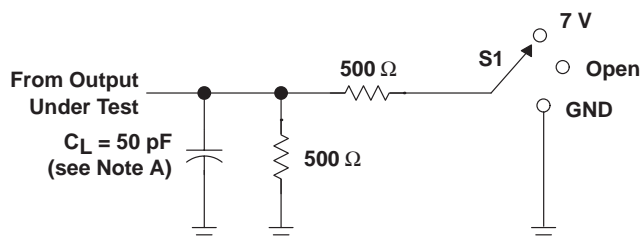


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SN54ABT16821, SN74ABT16821 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

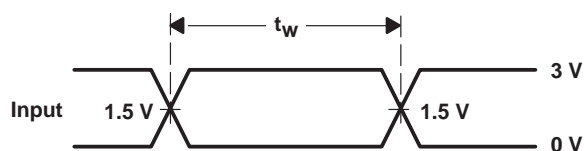
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PARAMETER MEASUREMENT INFORMATION

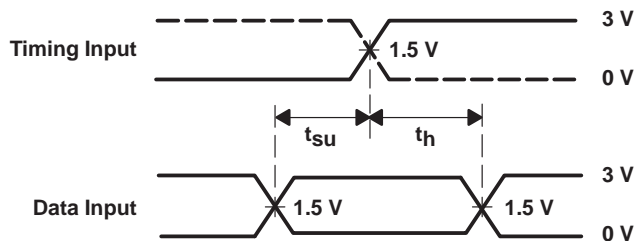


LOAD CIRCUIT

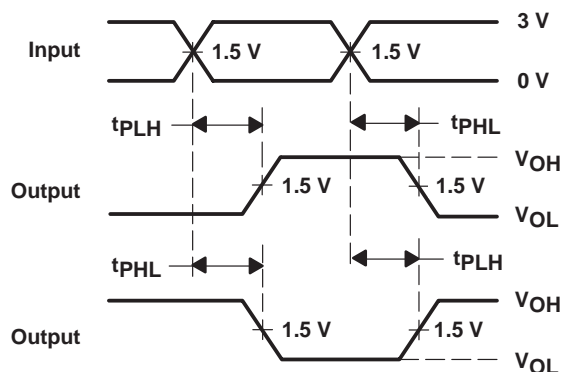
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



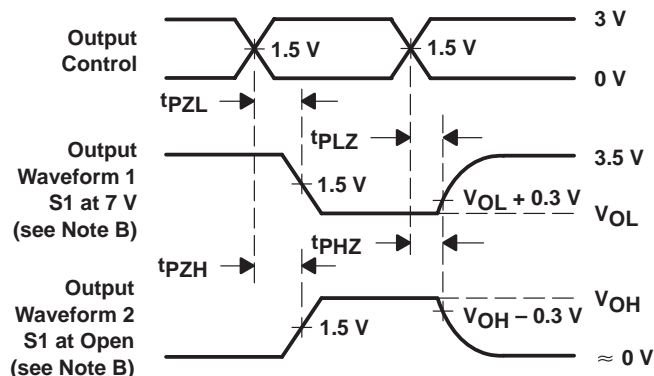
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT16821DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16821
SN74ABT16821DGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16821
SN74ABT16821DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16821
SN74ABT16821DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16821
SN74ABT16821DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16821
SN74ABT16821DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16821

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16821DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT16821DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16821DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT16821DLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE



*All dimensions are nominal

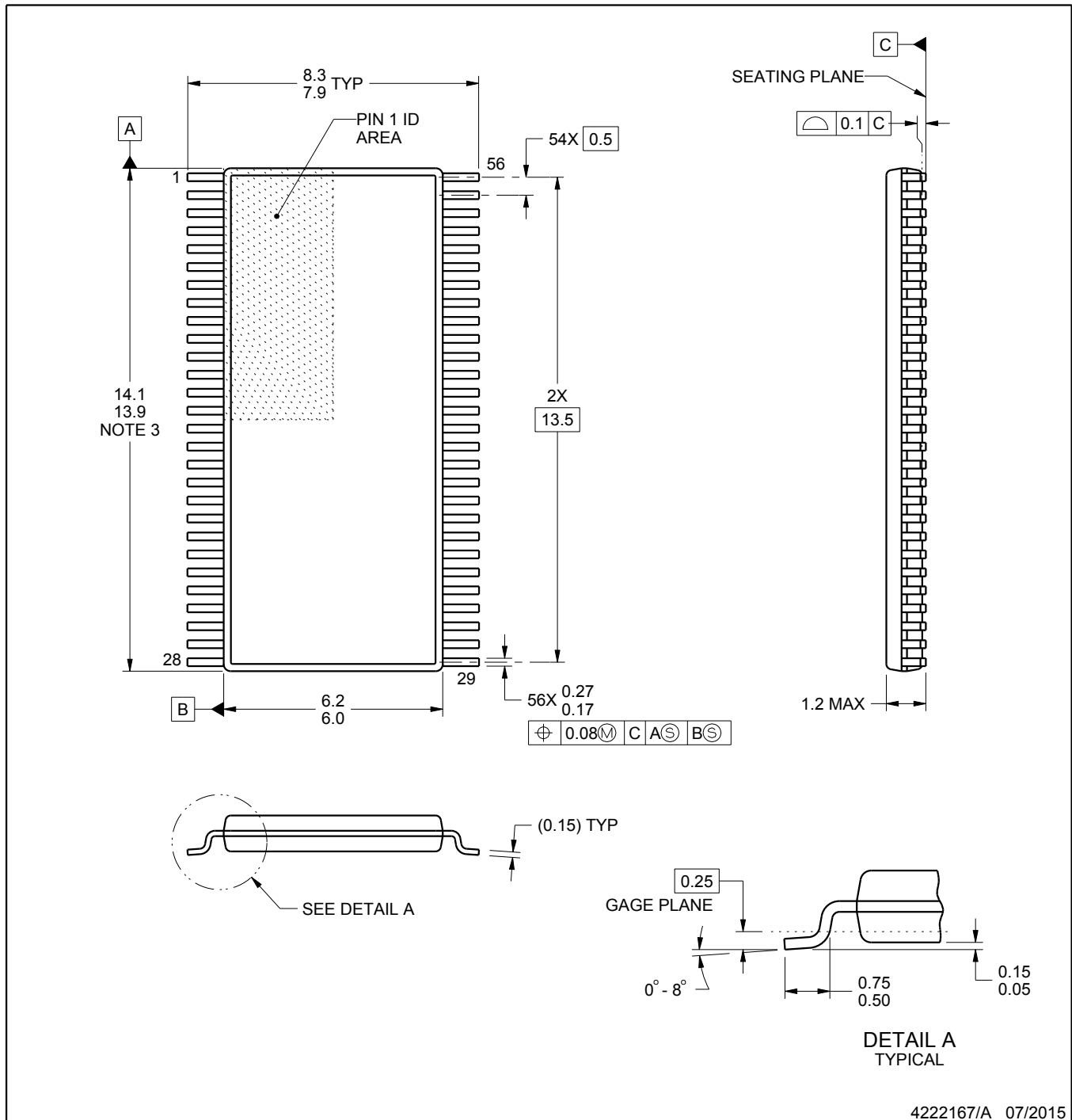
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16821DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16821DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

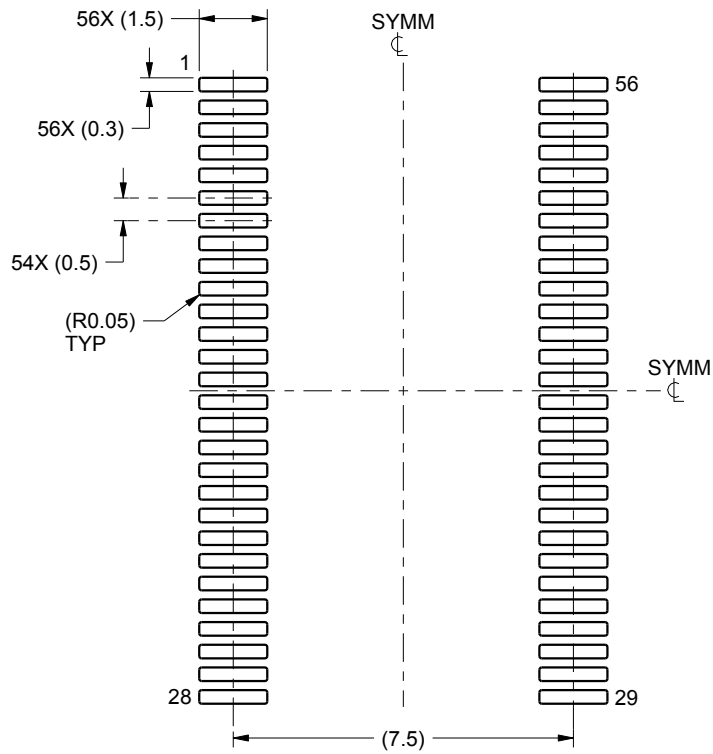
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

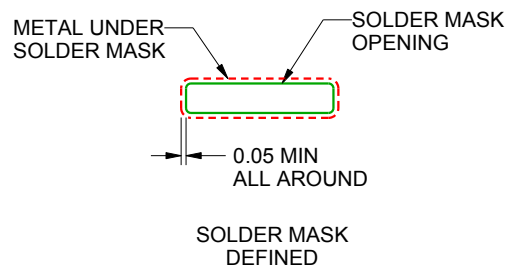
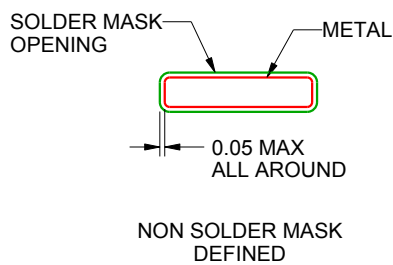
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

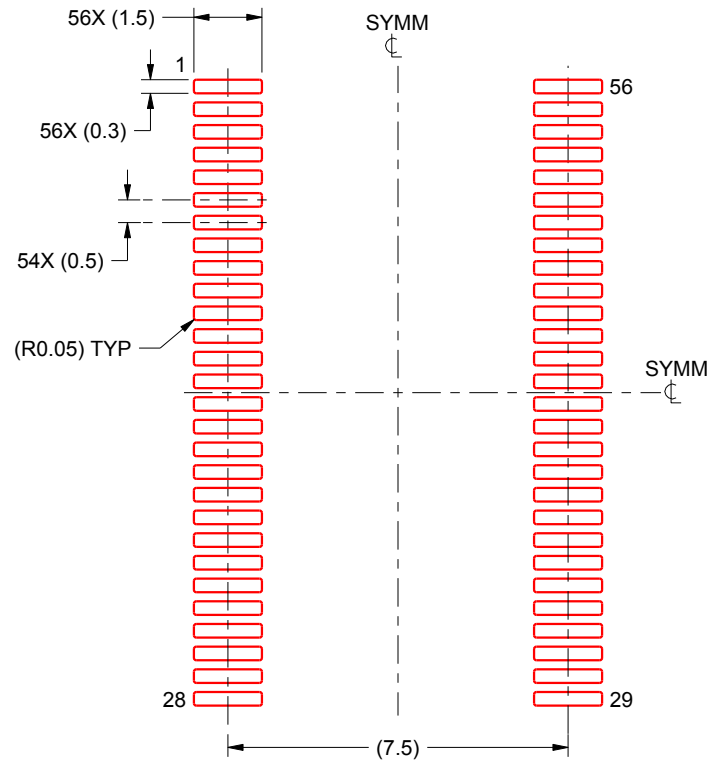
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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