

高速差分线路接收器

查询样品: [SN65LVDS31-EP](#)

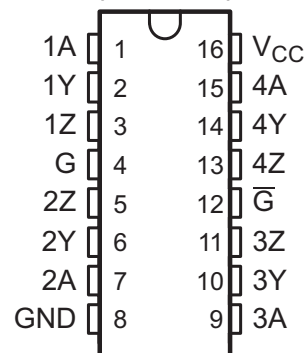
特性

- 满足或者超过**ANSI TIA/EIA-644** 标准
- 具有**350 mV** 的典型输出电压和**100-Ω** 负载的低电压差分信号传输
- 典型输出电压上升和下降次数为 **500 ps (400 Mbps时)**
- 典型传播时延 **1.7 ns**
- **3.3-V** 单电源供电下运行
- **200 MHz**时, 每个驱动器功率耗散典型值 **25 mW**
- 当被禁止或者 $V_{CC} = 0$ 时, 驱动器在高阻抗
- 总线终端**ESD**保护超过 **8 kV**
- 低电压 **TTL (LVTTTL)** 逻辑输入电平
- 与**AM26LS31**, **MC3487**, 和 **μA9638**引脚兼容
- 用于有冗余要求的空间和高可靠性应用的冷备份

支持国防、航天和医疗应用

- 受控基线
- 一个组装/测试场所
- 一个制造场所
- 在军用温度范围内 (**-55°C/125°C**)工作
- 产品生命周期有所延长
- 拓展的产品改变通知
- 产品可追溯性

**D PACKAGE
(TOP VIEW)**



说明

SN65LVDS31 是一款差分线路驱动器, 此差分驱动器具有低电压差分信号传输 (LVDS)的电气特性。此项信号传输技术降低了 5-V 差分标准电平的输出电压电平 (例如 TIA/EIA-422B) 以减少功耗, 增加交换速度并允许一个 3.3 V供电轨的操作。当被启用时, 此驱动器将向 100-Ω负载传送一个大小为 247 mV的最小差分输出电压。

这个设备和信号传输技术的目标应用是在点到点和多点间 (一个驱动器和多个接收器) 通过接近 100 Ω的受控阻抗介质传输数据。传输介质可以是印刷电路板印制线、背板或者电缆。数据传输的最终速率和距离取决于介质的衰减特性和对环境的噪声耦合。

SN65LVDS31 器件工作温度范围 -55°C 至 125°C。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: [SLLSE91](#)



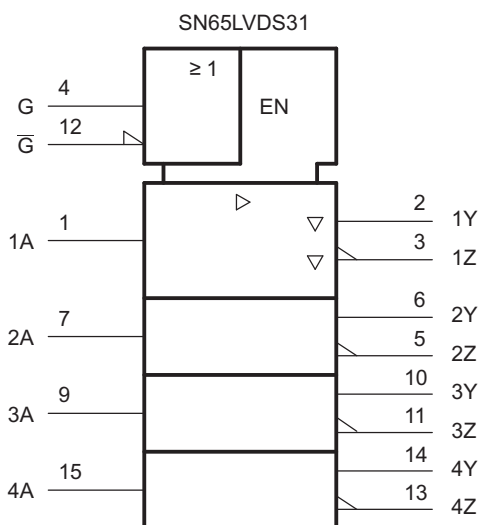
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	SOIC-D	SN65LVDS31MDREP	LVDS31EP	V62/07627-01XE

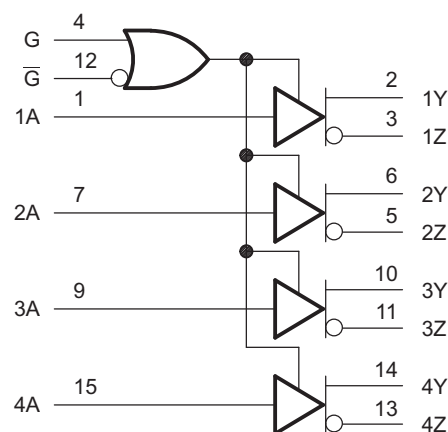
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Logic Symbol



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN65LVDS31 Logic Diagram (Positive Logic)



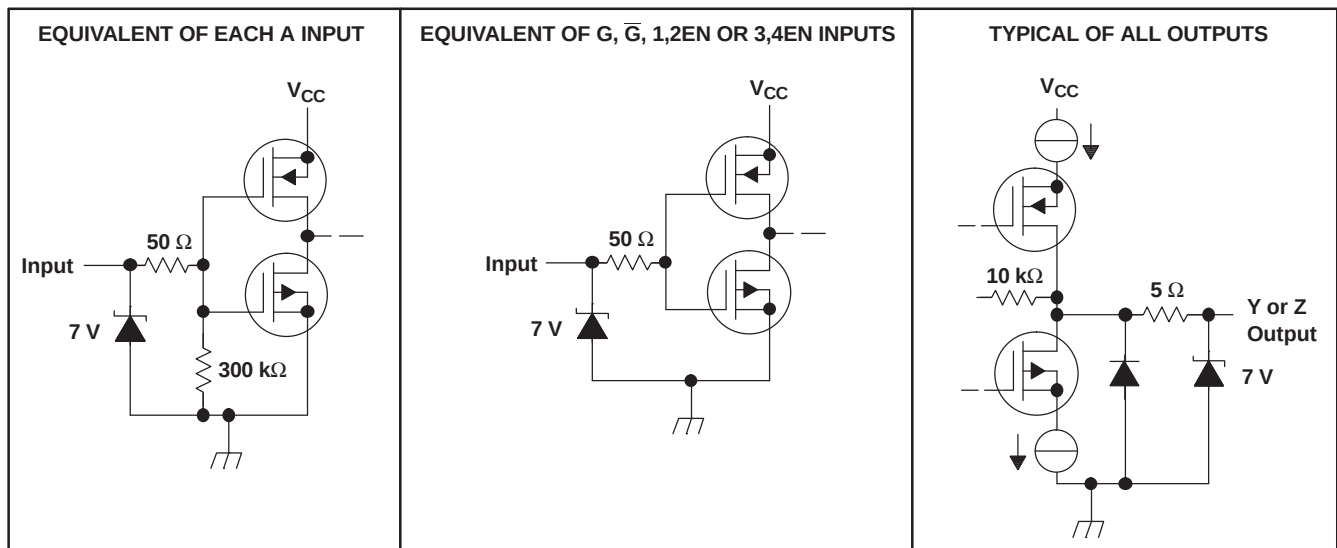
FUNCTION TABLE

Table 1. SN65LVDS31⁽¹⁾

INPUT A	ENABLES		OUTPUTS	
	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	UNIT
V _{CC} Supply voltage range ⁽²⁾	–0.5 V to 4 V
V _I Input voltage range	–0.5 V to V _{CC} + 0.5 V
Continuous total power dissipation	See Dissipation Rating Table
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
θ _{JA} Thermal resistance, junction-to-ambient	73°C/W
θ _{JC} Thermal resistance, junction-to-case	36.9°C/W
T _{stg} Storage temperature range	–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage	3	3.3	3.6	V
V _{IH} High-level input voltage	2			V
V _{IL} Low-level input voltage			0.8	V
T _A Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OD} Differential output voltage magnitude	R _L = 100 Ω, See Figure 2	247	340	454	mV
ΔV _{OD} Change in differential output voltage magnitude between logic states	R _L = 100 Ω, See Figure 2	–50		50	mV
V _{OC(SS)} Steady-state common-mode output voltage	See Figure 3	1.125	1.2	1.375	V
ΔV _{OC(SS)} Change in steady-state common-mode output voltage between logic states	See Figure 3	–50		50	mV
V _{OC(PP)} Peak-to-peak common-mode output voltage	See Figure 3		50		mV
I _{CC} Supply current	V _I = 0.8 V or 2 V, Enabled, No load		9	20	mA
	V _I = 0.8 or 2 V, R _L = 100 Ω, Enabled		25	35	
	V _I = 0 or V _{CC} , Disabled		0.25	1	
I _{IH} High-level input current	V _{IH} = 2		4	20	μA
I _{IL} Low-level input current	V _{IL} = 0.8 V		0.1	10	μA
I _{OS} Short-circuit output current	V _{O(Y)} or V _{O(Z)} = 0		–4	–24	mA
	V _{OD} = 0			±12	
I _{OZ} High-impedance output current	V _O = 0 or 2.4 V			±1	μA
I _{O(OFF)} Power-off output current	V _{CC} = 0, V _O = 2.4 V			±4	μA
C _i Input capacitance			3		pF

- (1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 100\ \Omega$, $C_L = 10\ \text{pF}$, See Figure 2	0.5	1.4	4	ns
t_{PHL} Propagation delay time, high-to-low-level output		1	1.7	4.5	ns
t_r Differential output signal rise time (20% to 80%)			0.5		ns
t_f Differential output signal fall time (80% to 20%)			0.5		ns
$t_{sk(p)}$ Pulse skew ($ t_{PHL} - t_{PLH} $)			0.3	0.6	ns
$t_{sk(o)}$ Channel-to-channel output skew ⁽²⁾			0.3	0.8	ns
t_{PZH} Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	17	ns
t_{PZL} Propagation delay time, high-impedance-to-low-level output			2.5	17	ns
t_{PHZ} Propagation delay time, high-level-to-high-impedance output			8.1	18	ns
t_{PLZ} Propagation delay time, low-level-to-high-impedance output			7.3	17	ns

(1) All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 3.3\ \text{V}$.

(2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

PARAMETER MEASUREMENT INFORMATION

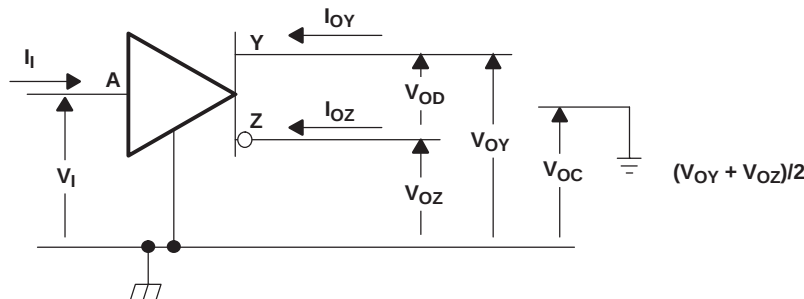
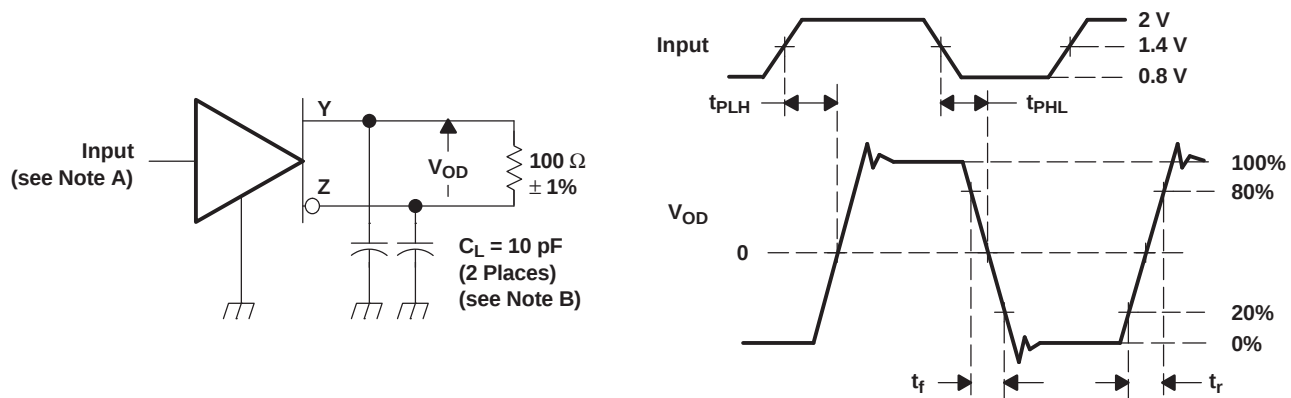


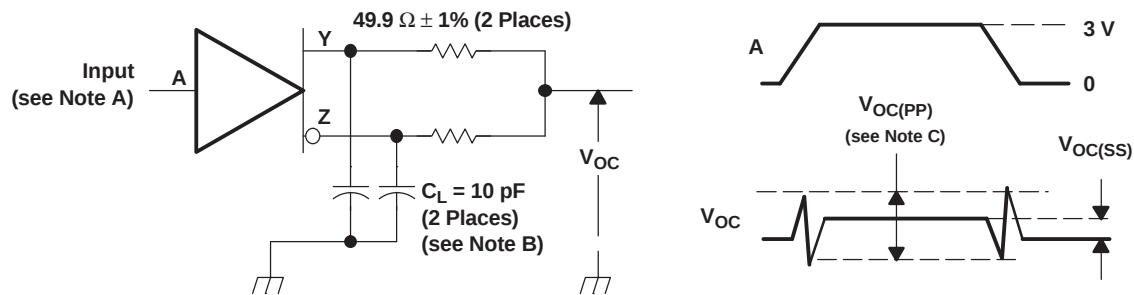
Figure 1. Voltage and Current Definitions



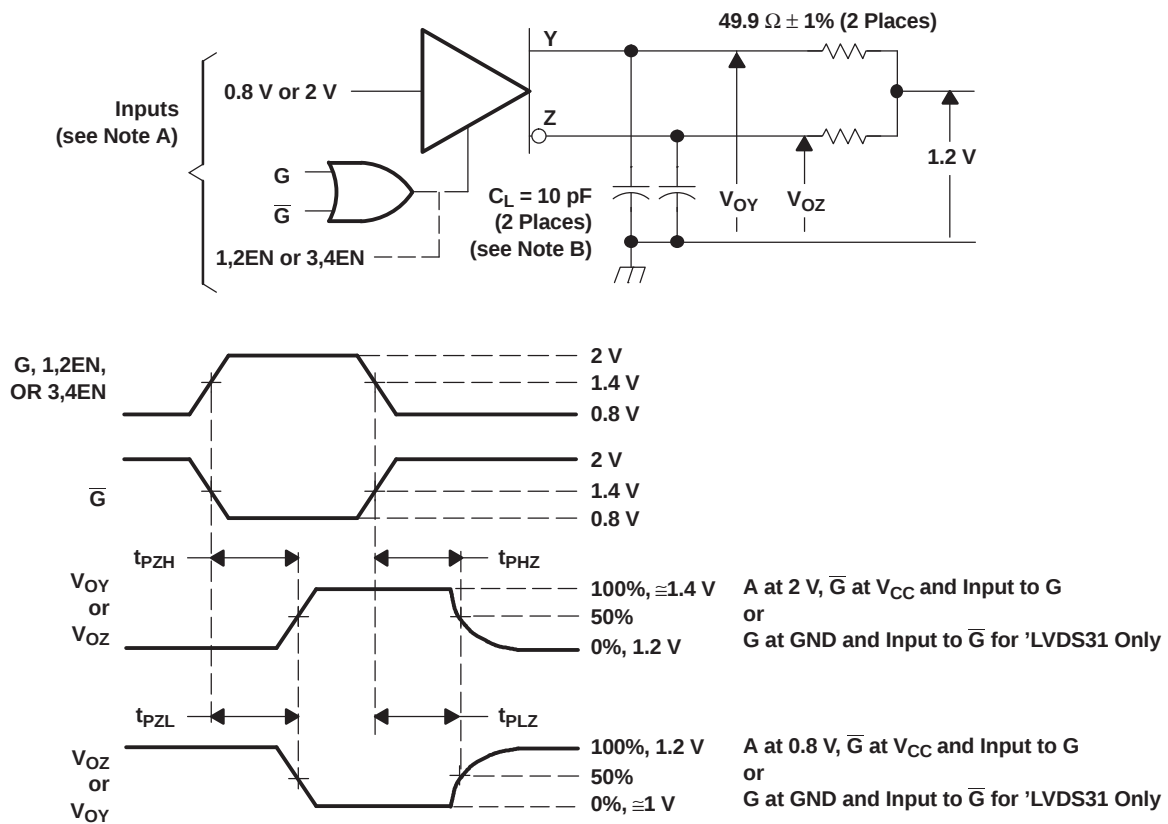
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1\ \text{ns}$, pulse repetition rate (PRR) = 50 Mpps, pulse width = $10 \pm 0.2\ \text{ns}$.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION (continued)

- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
- B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
- C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f < 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
- B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable-/Disable-Time Circuit and Definitions

TYPICAL CHARACTERISTICS

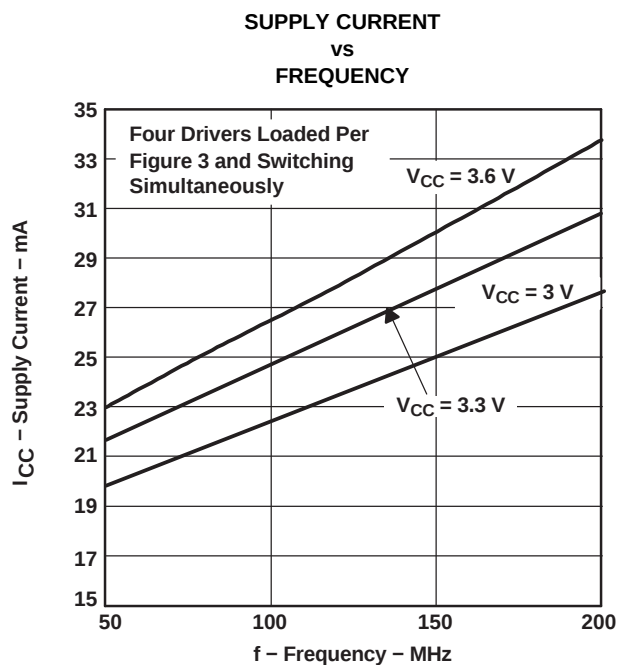


Figure 5.

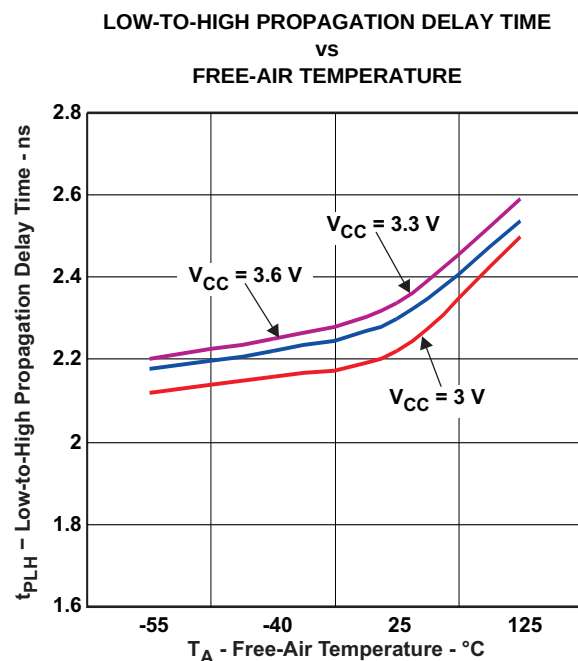


Figure 6.

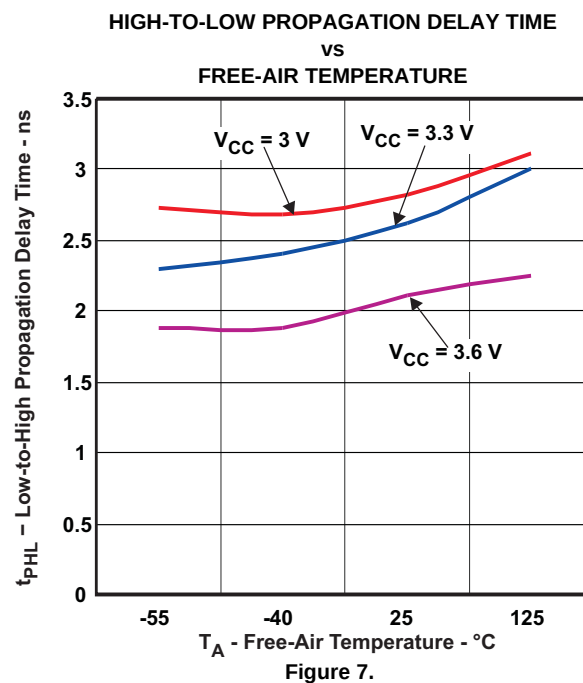
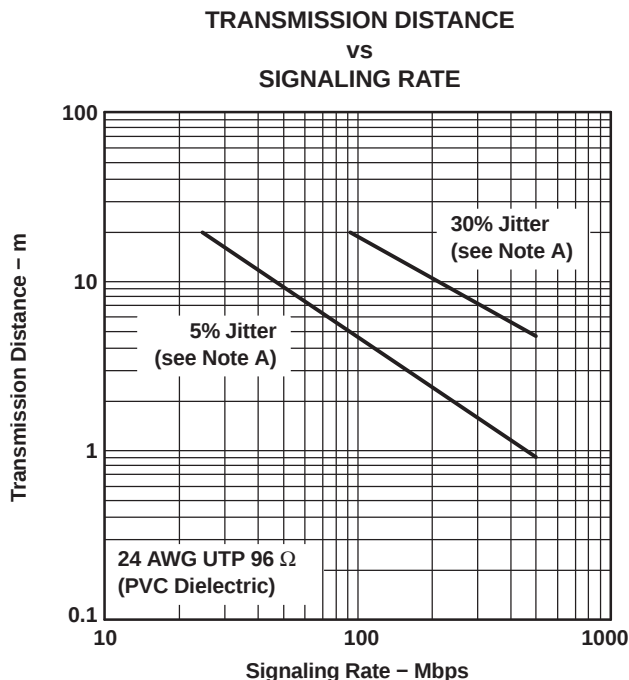


Figure 7.

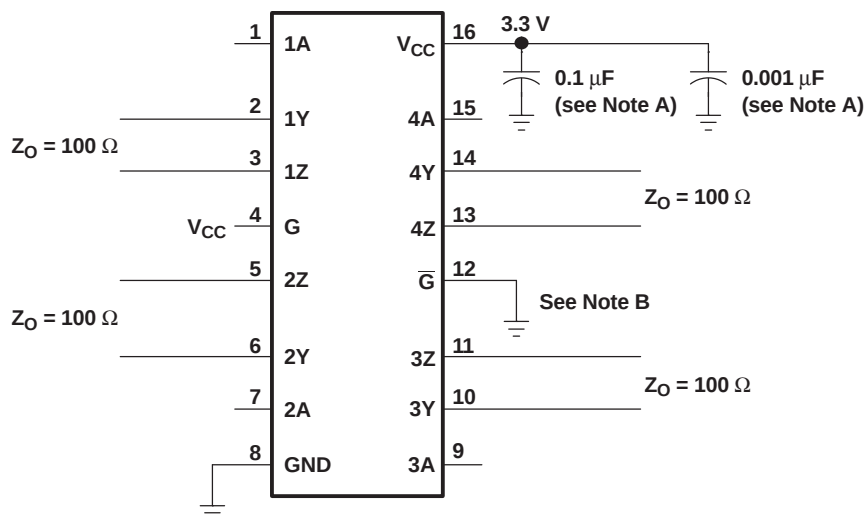
APPLICATION INFORMATION

The SN65LVDS31 is generally used as a building block for high-speed point-to-point data transmission where ground differences are less than 1 V. The SN65LVDS31 can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



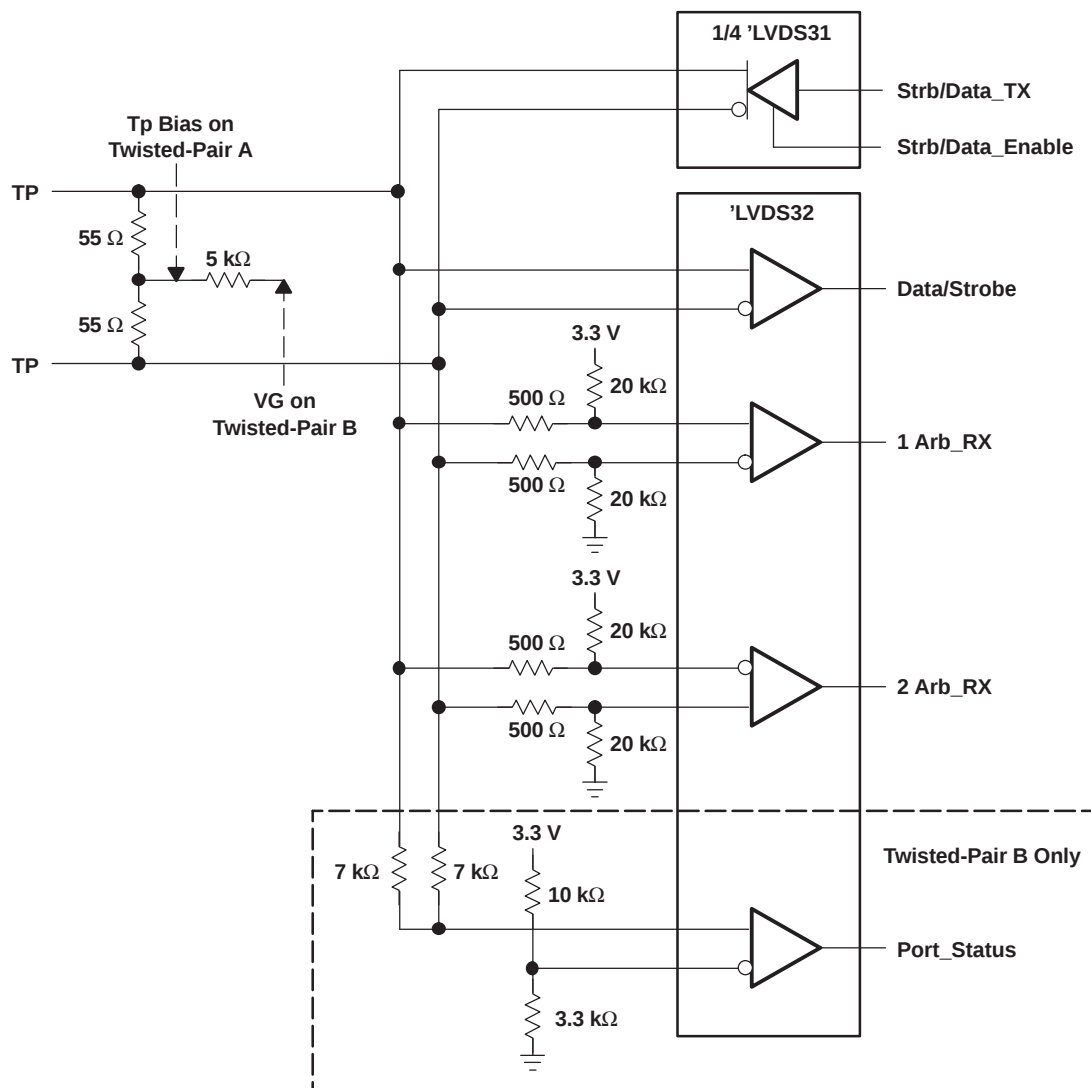
- A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 8. Typical Transmission Distance Versus Signaling Rate



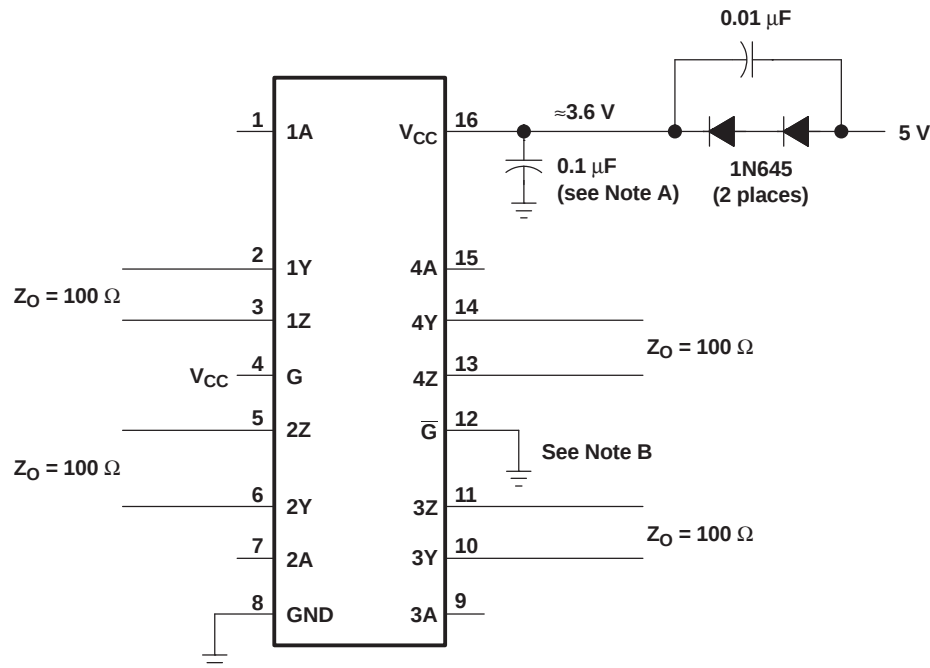
- NOTES: A. Place a 0.1- μ F and a 0.001- μ F Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
- B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 9. Typical Application Circuit Schematic



- NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
 B. Decoupling capacitance is not shown, but recommended.
 C. V_{CC} is 3 V to 3.6 V.
 D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 10. 100-Mbps IEEE 1394 Transceiver



- A. Place a 0.1-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
- B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 11. Operation With 5-V Supply

COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* ([SLLA014](#))
- *Interface Circuits for TIA/EIA-644 (LVDS)* ([SLLA038](#))
- *Reducing EMI With LVDS* ([SLLA030](#))
- *Slew Rate Control of LVDS Circuits* ([SLLA034](#))
- *Using an LVDS Receiver With RS-422 Data* ([SLLA031](#))
- *Evaluating the LVDS EVM* ([SLLA033](#))

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS31MDREP	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVDS31EP
V62/07627-01XE	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVDS31EP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65LVDS31-EP :

- Catalog : [SN65LVDS31](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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