HIGH-SPEED DIFFERENTIAL LINE TRANSCEIVERS

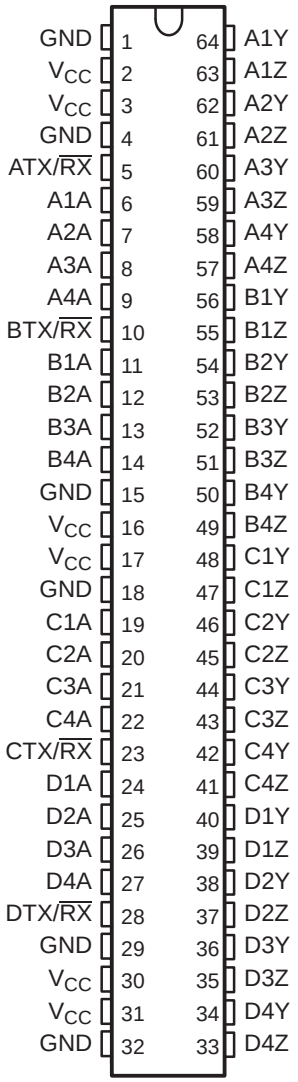
FEATURES

- **Sixteen Low-Voltage Differential Transceivers. Designed for Signaling Rates up to 200 Mbps per Receiver or 650 Mbps per Transmitter.**
- **Simplex (Point-to-Point) or Half-Duplex (Multipoint) Interface**
- **Typical Differential Output Voltage of 340 mV Into a 50-Ω Load**
- **Integrated 110-Ω Line Termination on 'LVDM1677 Product**
- **Propagation Delay Time:**
  - **Driver: 2.5 ns Typ**
  - **Receiver: 3 ns Typ**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V for Power Up/Down Glitch-Free Performance and Hot-Plugging Events**
- **Bus-Terminal ESD Protection Exceeds 12 kV**
- **Low-Voltage TTL (LVTTL) Logic Input Levels Are 5-V Tolerant**
- **Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch**

DESCRIPTION

The SN65LVDM1676 and SN65LVDM1677 (integrated termination) are sixteen differential line transmitters or receivers (tranceivers) that use low-voltage differential signaling (LVDS) to achieve signaling rates up to 200 Mbps per transceiver configured as a receiver and up to 650 Mbps per transceiver configured as a transmitter. These products are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers are doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of 100 mV with up to 1 V of ground potential difference between a transmitter and receiver.

SN65LVDM1676DGG (Marked as LVDM1676)
SN65LVDM1677DGG (Marked as LVDM1677)
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of transceivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

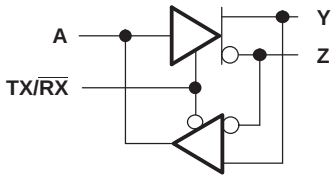
The SN65LVDM1676 and SN65LVDM1677 are characterized for operation from –40°C to 85°C.

FUNCTION TABLE(1)

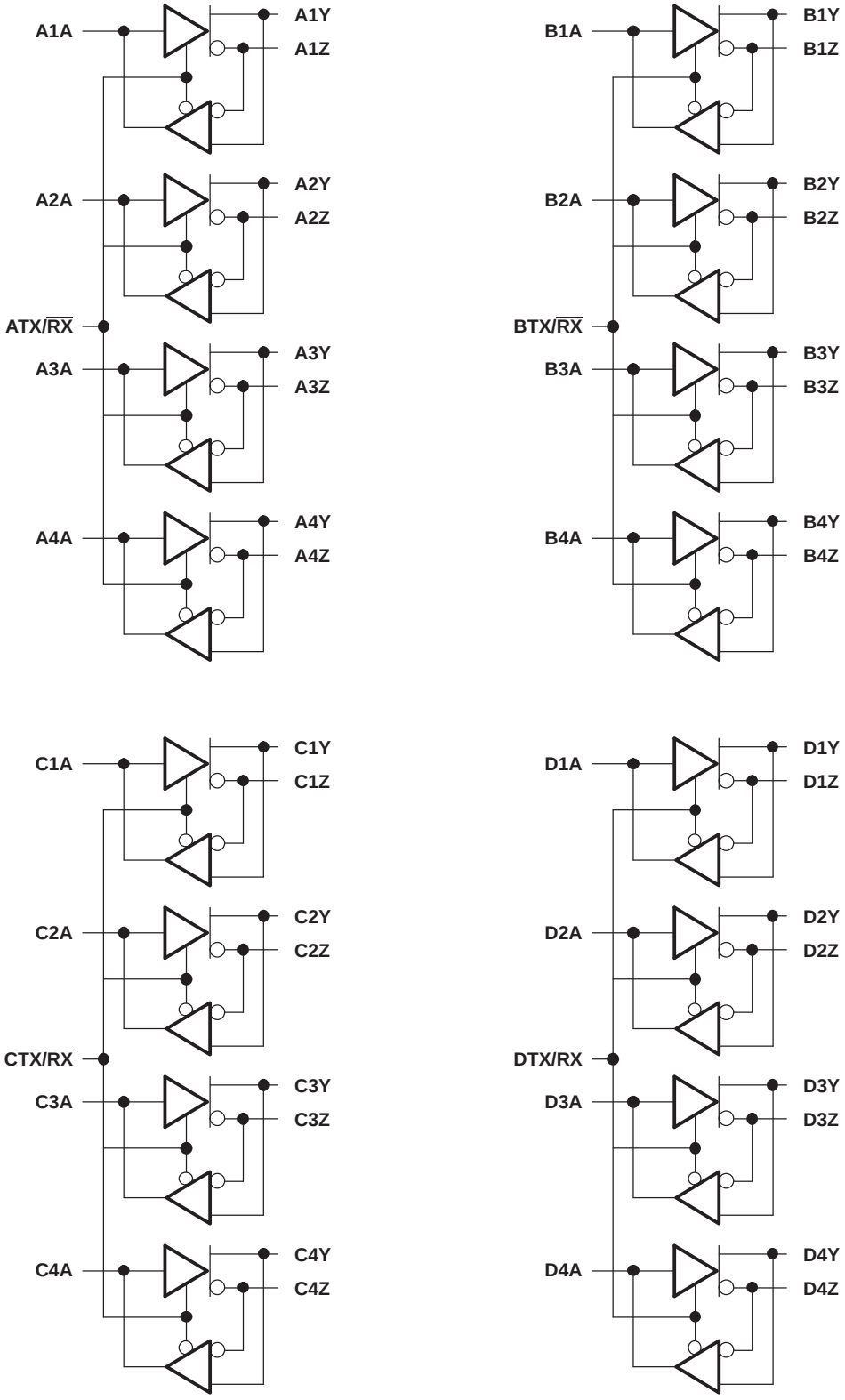
INPUTS			OUTPUTS		
(Y – Z)	TX/$\overline{RX}$	A	Y	Z	A
$V_{ID} \geq$ 100 mV	L	NA	Z	Z	H
–100 mV < V_{ID} < 100 mV	L	NA	Z	Z	?
$V_{ID} \leq$ -100 mV	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	H
NA	H	L	L	H	Z
NA	H	H	H	L	Z

(1) H = high level, L= low level, Z= high impedance, ? = indeterminate

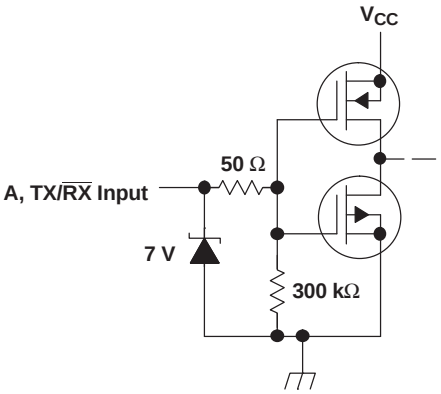
LVD Transceiver

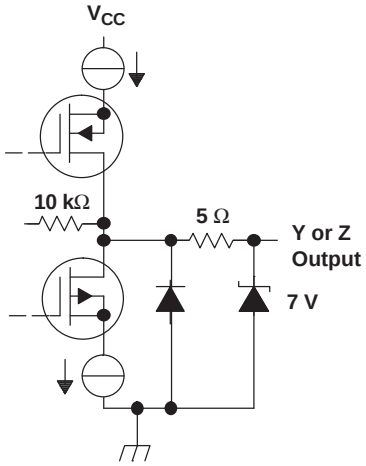


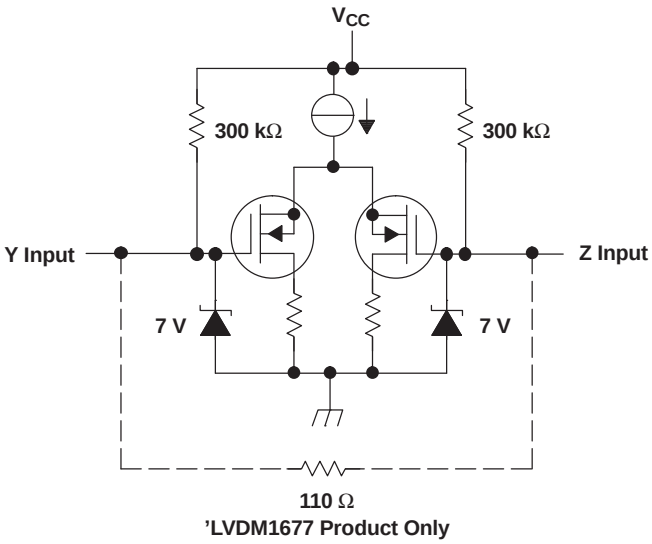
LOGIC DIAGRAM (POSITIVE LOGIC)



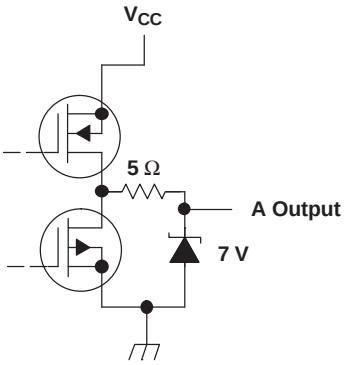
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS







'LVDM1677 Product Only



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

			RATING
V_{CC}	Supply voltage range		–0.5 V to 4 V
V_I	Input voltage range	A, TX/$\overline{RX}$	–0.5 V to 6 V
		Y or Z	–0.5 V to 4 V
$\|V_{ID}\|$	Differential input voltage magnitude, (SN65LVDM1677 only)		1 V
I_O	Receiver output current		±20 mA
P_D	Continuous power dissipation		See the Dissipation Rating Table
ESD	Electrostatic discharge (3)	Y, Z, and GND	Class 3, A: 8 kV, B: 600 V
		All Pins	Class 3, A: 7 kV, B: 500 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DGG	2094 mW	16.7 mW/°C	1089 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			
V_{IL}	Low-level input voltage			0.8	
$\|V_{ID}\|$	Magnitude of differential input voltage	0.1		0.6	
V_{IC}	Common-mode input voltage	$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	
				V_{CC}–0.8	V
I_{OL}	Receiver low-level output current			8	mA
I_{OH}	Receiver high-level output current	–8(1)			
T_A	Operating free-air temperature	–40		85	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
I_{CC}	Supply current	Driver enabled, receiver disabled R_L = 50 Ω ('LVDM1676) or R_L = 100 Ω ('LVDM1677)			140	175	mA
		Driver disabled, receiver enabled, no load			45	60	
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 50 Ω ('LVDM1676) or R_L = 100 Ω ('LVDM1677), See Figure 2 and Figure 1		247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 50 Ω ('LVDM1676) or R_L = 100 Ω ('LVDM1677), See Figure 3		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current	V_{IH} = 2 V			3	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			2	10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V				10	mA
		V_{OD} = 0 V				10	mA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V		–10		10	µA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V			5		pF
RECEIVER							
V_{IT+}	Positive-going differential input voltage threshold	See Figure 6 and Table 1				100	mV
V_{IT-}	Negative-going differential input voltage threshold			–100			
V_{OH}	High-level output voltage	I_{OH} = -8 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA				0.4	V
I_I	Input current (Y or Z inputs)	V_{IY} = V_{IZ} = 0 V		–40	–24		µA
		V_{IY} = V_{IZ} = 2.4 V			–8	–1.2	
I_{ID}	Differential input current $\|I_{IY} - I_{IZ}\|$ (inputs)	'LVDM1676	V_{IY} = 0 V and V_{IZ} = 100 mV, V_{IY} = 2.4 V and V_{IZ} = 2.3 V		5	10	µA
		'LVDM1677	V_{IY} = 0.2 V and V_{IZ} = 0 V, V_{IY} = 2.4 V and V_{IZ} = 2.2 V	1.5		2.2	mA
$I_{I(OFF)}$	Power-off input current (Y or Z inputs)	V_{CC} = 0 V, V_I = 2.4 V		–25		25	µA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DRIVER						
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω ('LVDM1676) or R_L = 100 Ω ('LVDM1677), C_L = 10 pF, See Figure 4	1.3	2.5	3.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.3	2.5	3.6	
t_r	Differential output signal rise time			0.5	1.2	
t_f	Differential output signal fall time			0.5	1.2	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.1	0.6	
$t_{sk(o)}$	Channel-to-channel output skew(2)			0.1	0.4	
$t_{sk(pp)}$	Part-to-part skew(3)				1	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		11	20	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			10	20	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3	10	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			3	10	
RECEIVER						
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 7	1.5	3	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.5	3	4.5	
t_r	Output signal rise time			0.6	1.6	
t_f	Output signal fall time			0.6	1.6	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.2	0.8	
$t_{sk(o)}$	Channel-to-channel output skew(4)			0.7	1.2	
$t_{sk(pp)}$	Part-to-part skew(5)				1	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 8		9	15	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8	15	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			12	20	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			11	20	

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
(3) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
(5) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

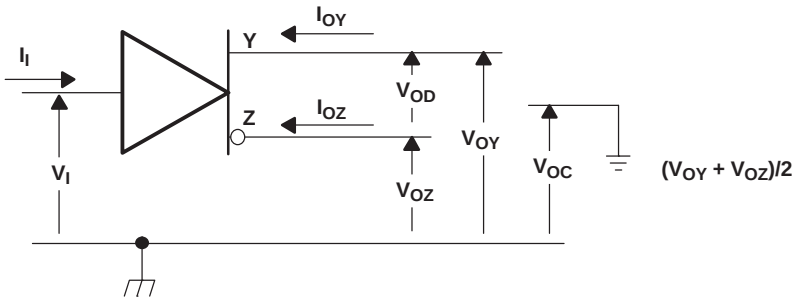


Figure 1. Driver Voltage and Current Definitions

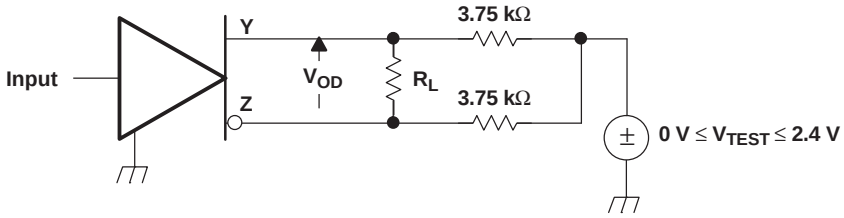
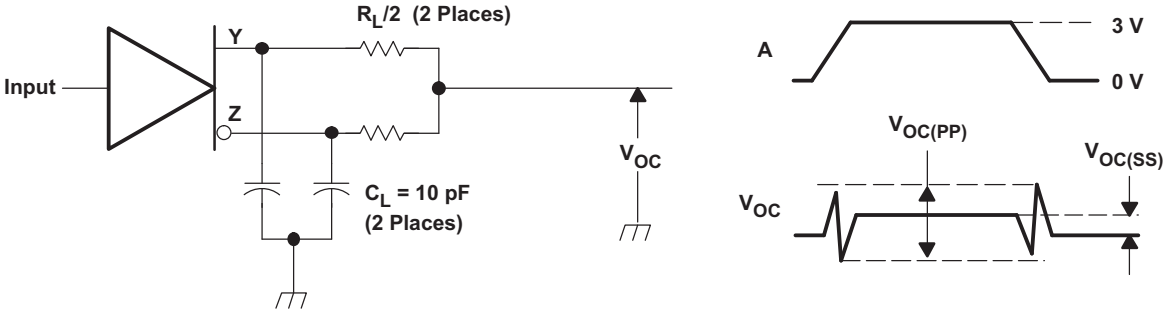


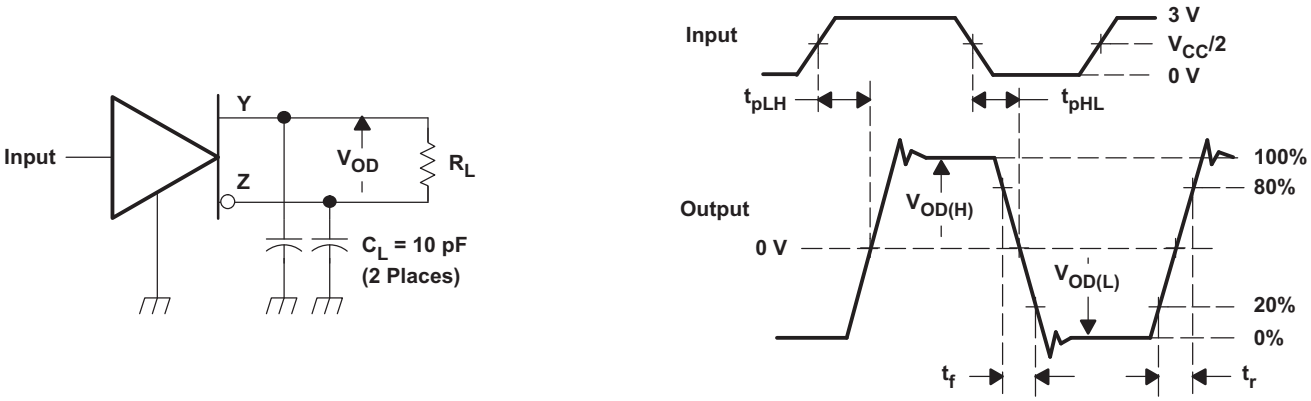
Figure 2. Driver V_{OD} Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

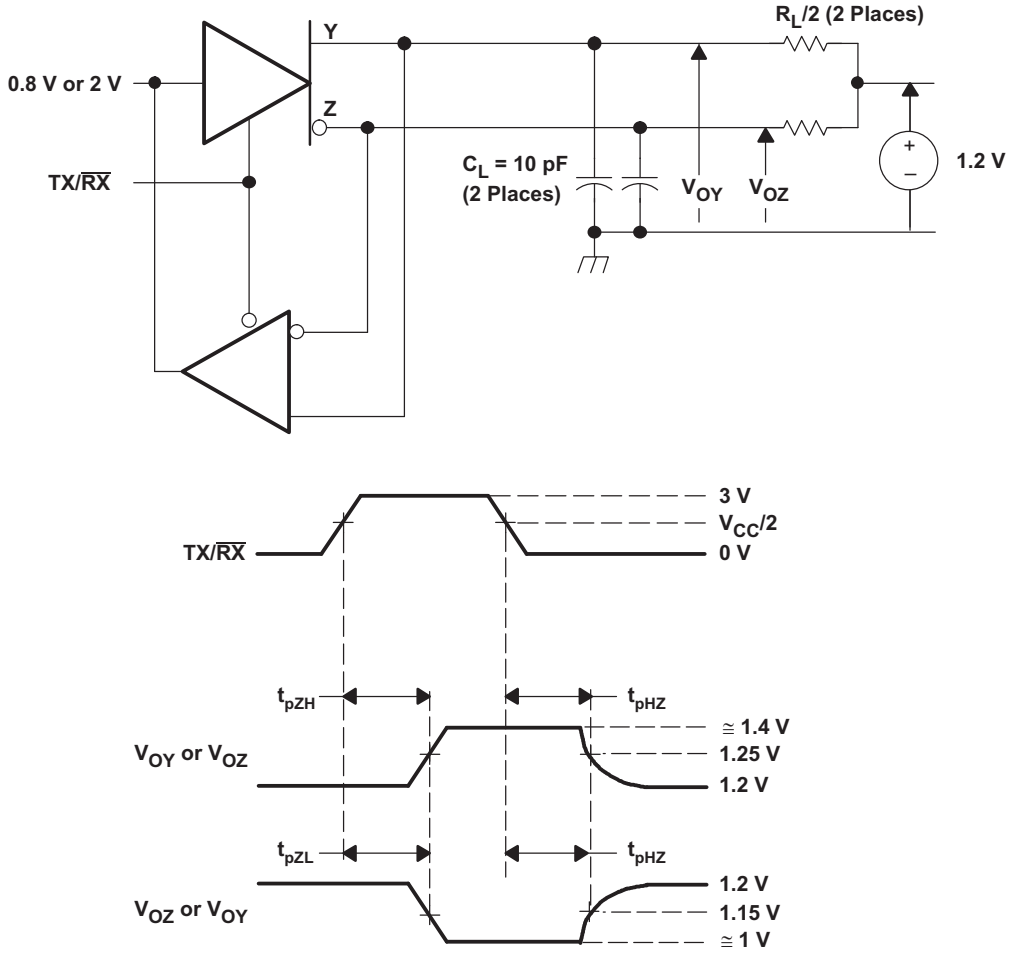
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

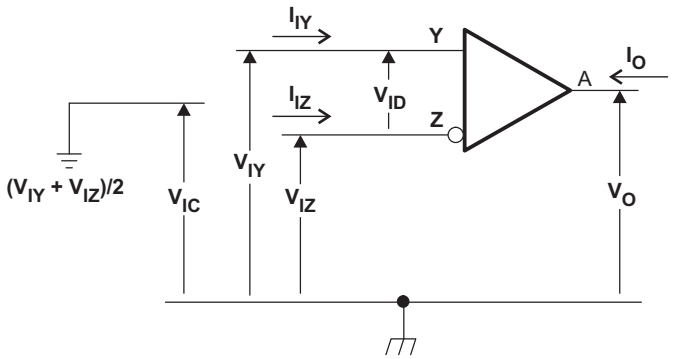
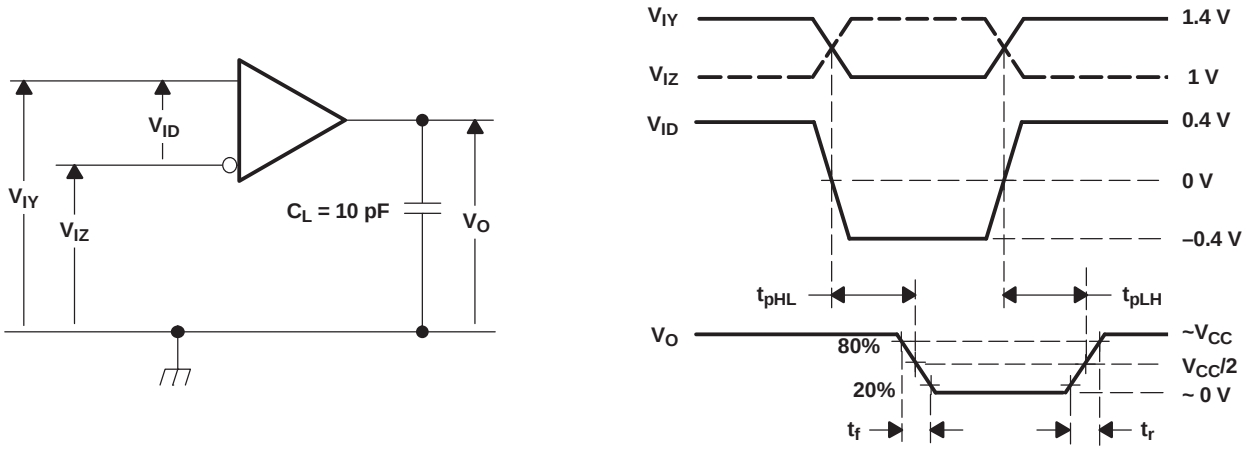


Figure 6. Voltage Definitions

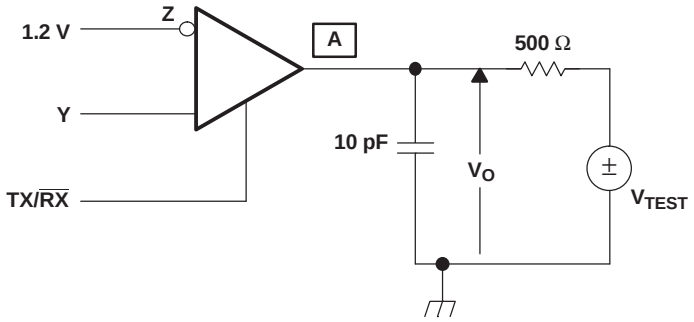
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IY}	V_{IZ}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 7. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

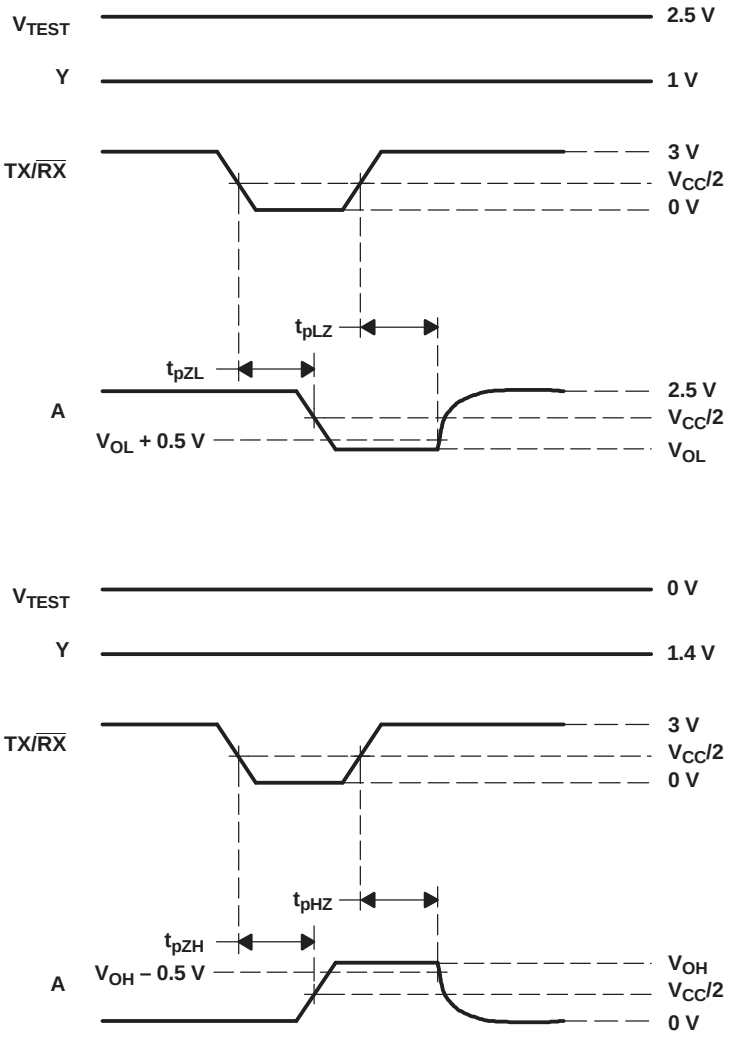


Figure 8. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

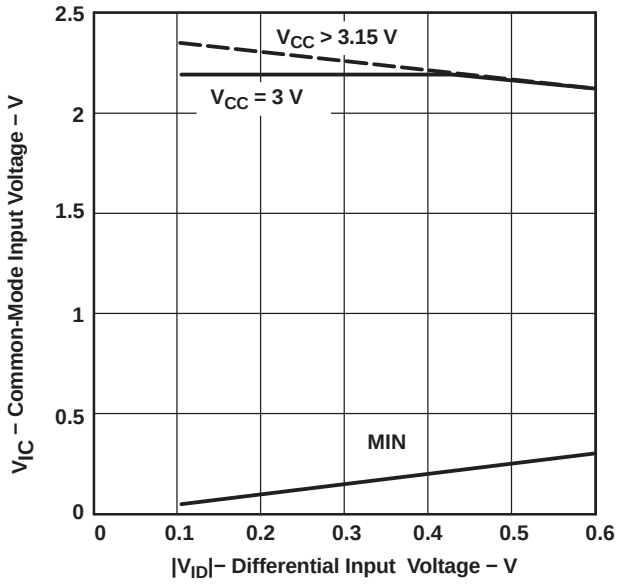


Figure 9.

DRIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

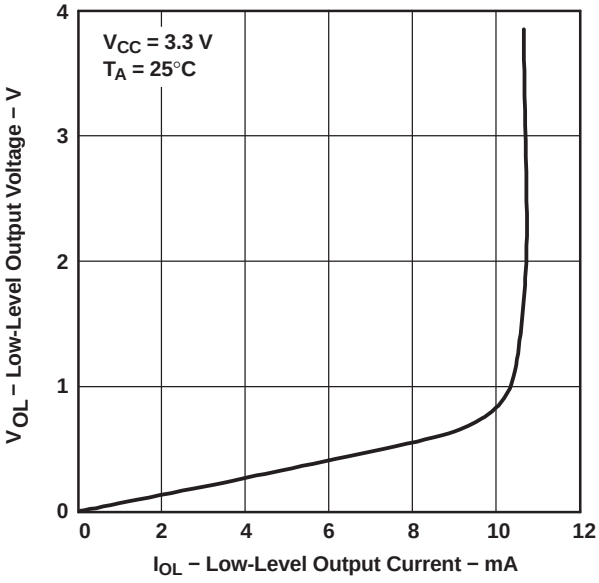


Figure 10.

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

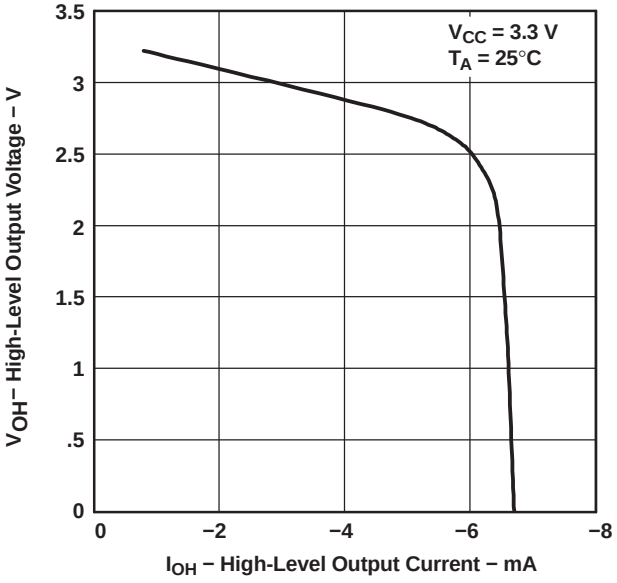


Figure 11.

TYPICAL CHARACTERISTICS (continued)

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

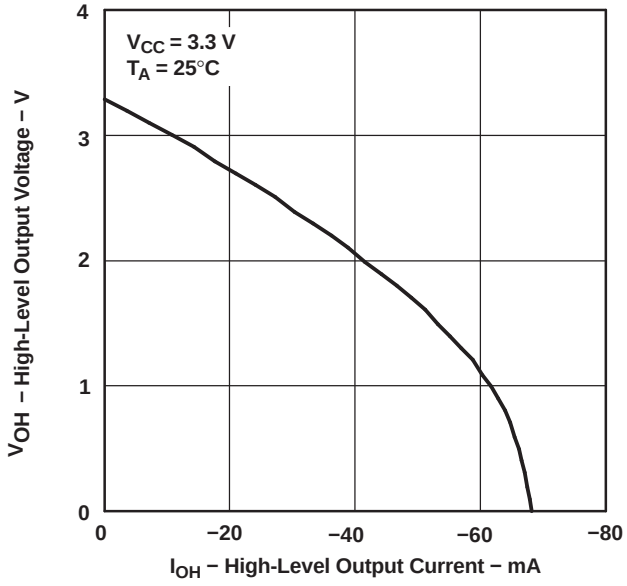


Figure 12.

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

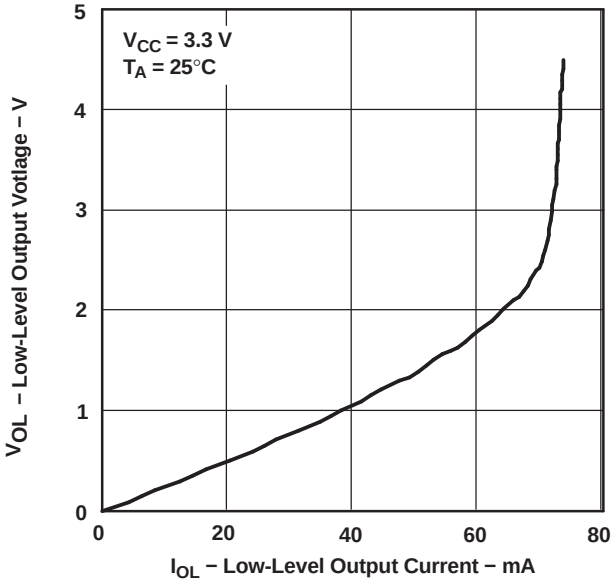


Figure 13.

TYPICAL CHARACTERISTICS (continued)

DRIVER EYE PATTERN

TEST CONDITIONS

- V_{CC} = 3.6 V
- T_A = 25°C (ambient temperature)
- All 16 channels switching simultaneously with NRZ data. Scope is triggered at the same frequency with pulse. Input signal level = 0 V to 3 V single ended.
- Resistive loading with no added capacitance

EQUIPMENT

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS6604 Digital Storage Scope
- Agilent ParBERT E4832A

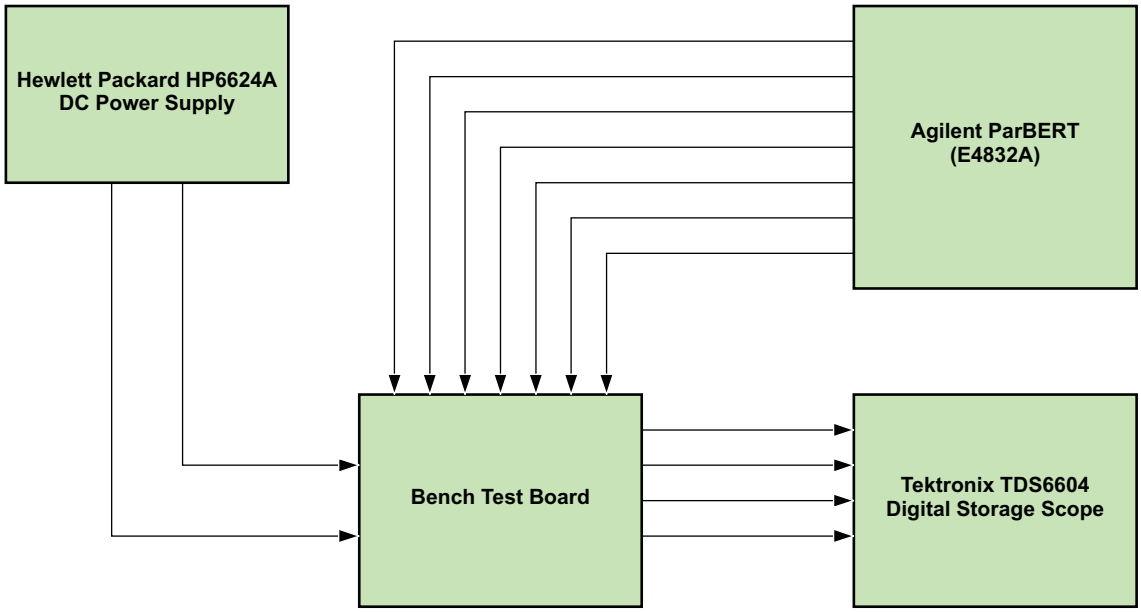
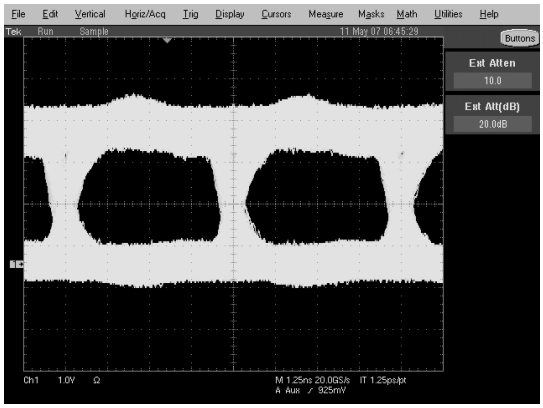
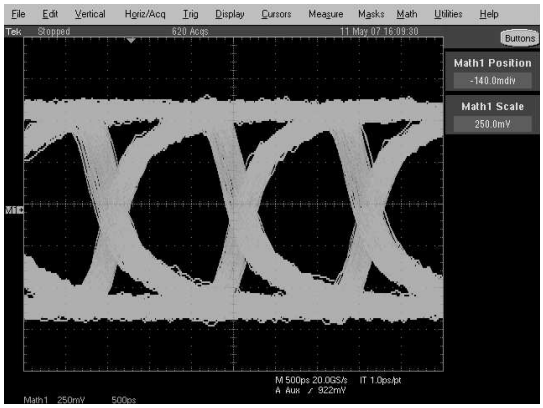


Figure 14. Equipment Setup

TYPICAL CHARACTERISTICS (continued)



(a) representative Transceiver configured as Rx @ 200 Mbps (Ch1 = xyA)



(b) representative Transceiver configured as Tx @ 650 Mbps (M1 = xyY-xyZ)

NOTE: x represents transceiver group A, B, C, or D, and y represents transceiver 1, 2, 3, or 4.

Figure 15. Typical Driver Eye Pattern for the SN65LVDM1676 With 12 Transceivers Configured as Rx and 4 Transceivers Configured as Tx all Switching Frequency Asynchronous Data (T_A = 25°C; V_{CC} = 3.6 V; PRBS = 2^{23-1})

APPLICATION INFORMATION

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different, however, in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 16. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

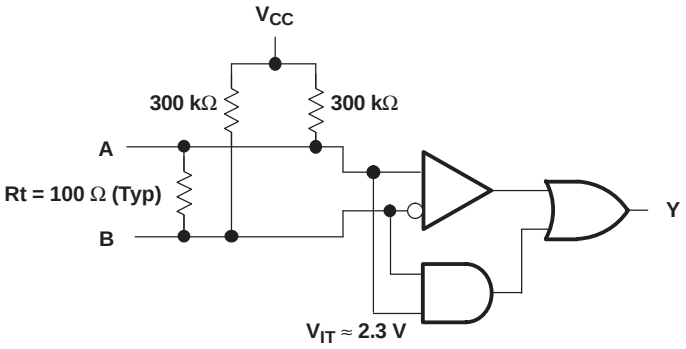


Figure 16. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDM1676DGG	Active	Production	TSSOP (DGG) | 64	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGG.B	Active	Production	TSSOP (DGG) | 64	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGG4	Active	Production	TSSOP (DGG) | 64	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGG4.B	Active	Production	TSSOP (DGG) | 64	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGR	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGR.B	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1677DGG	Active	Production	TSSOP (DGG) | 64	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGG.B	Active	Production	TSSOP (DGG) | 64	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGR	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGR.B	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGRG4	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGRG4.B	Active	Production	TSSOP (DGG) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

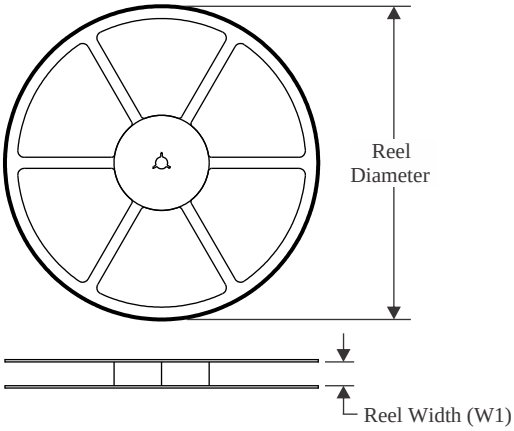
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

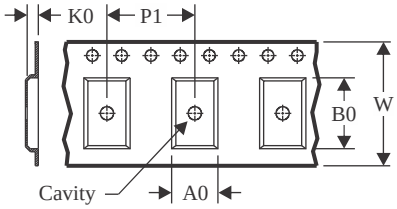
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

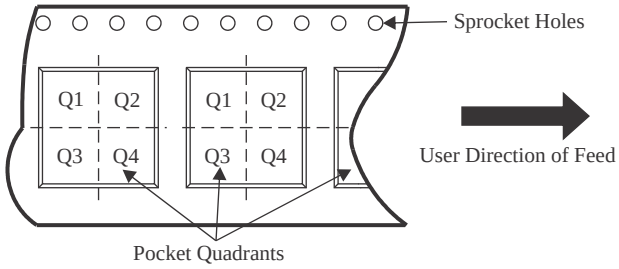


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

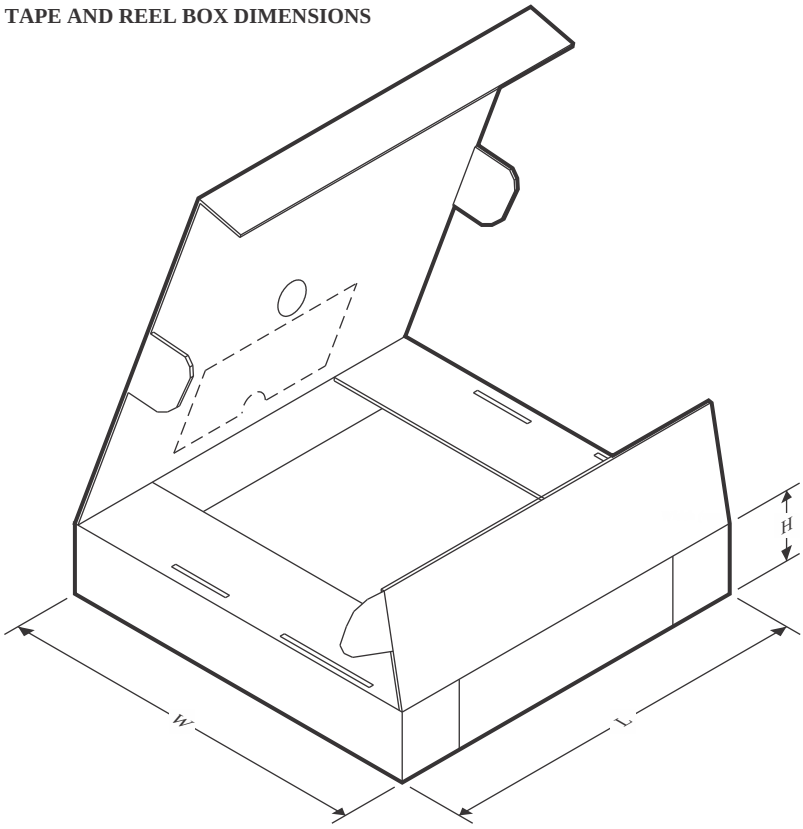
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDM1676DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDM1677DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDM1677DGGRG4	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

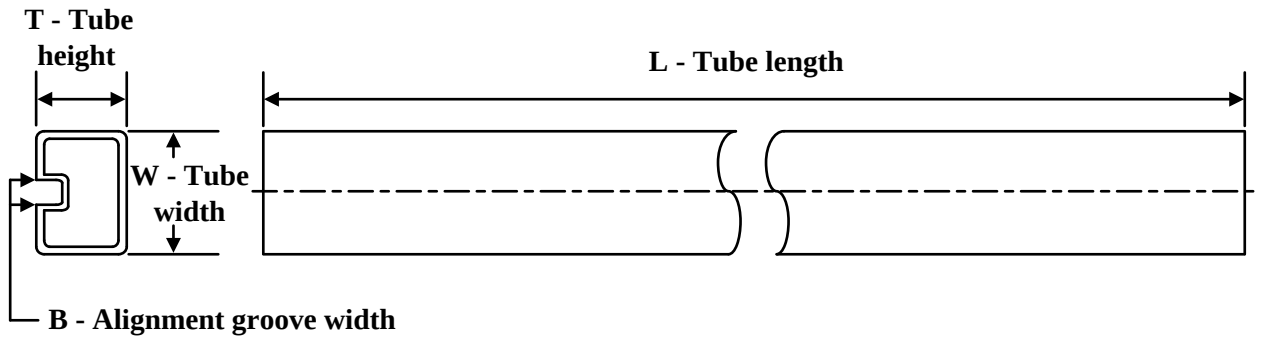
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDM1676DGGR	TSSOP	DGG	64	2000	356.0	356.0	45.0
SN65LVDM1677DGGR	TSSOP	DGG	64	2000	356.0	356.0	45.0
SN65LVDM1677DGGRG4	TSSOP	DGG	64	2000	356.0	356.0	45.0

TUBE

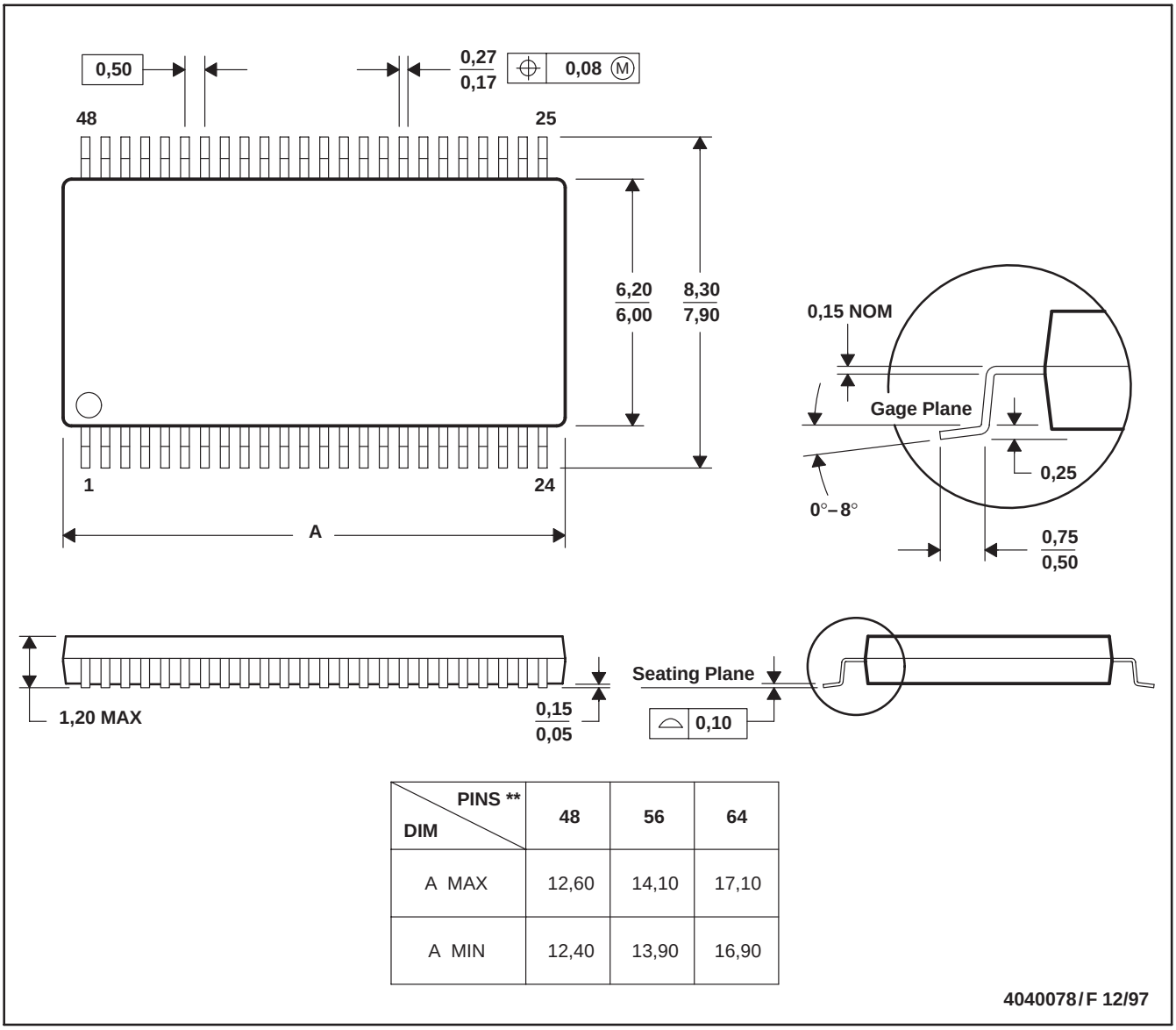


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDM1676DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1676DGG.B	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1676DGGG4	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1676DGGG4.B	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1677DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1677DGG.B	DGG	TSSOP	64	25	530	11.89	3600	4.9

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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