

SNx5LBC182 差分总线收发器

1 特性

- 四分之一单位负载允许一条总线上多达 128 个器件
- 符合或超出 ANSI 标准 TIA/EIA-485-A 和 ISO 8482 的要求：1987(E)
- 受控的驱动器输出电压摆率允许更长的电缆残桩长度
- 专门针对信号传输速率而设计。
 - 线路的信号传输速率是每秒进行电压转换的次数，以单位 bps (每秒位数) 来表示，最高 250kbps
- 低禁用电源电流：250 μ A (最大值)
- 热关断保护
- 开路失效防护接收器设计
- 接收器输入迟滞：70mV (典型值)
- 无干扰上电和断电保护

2 应用

- 公用事业计量表
- [工业过程控制](#)
- [楼宇自动化](#)

3 说明

SN65LBC182 和 SN75LBC182 是差分数据线路收发器，提供高级别的 ESD 保护，采用 SN75176 的行业标准封装。这些器件专为平衡传输线路而设计，符合 ANSI 标准 TIA/EIA-485-A 和 ISO 8482。SN65LBC182 和 SN75LBC182 整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起，用作方向控制。

驱动器输出和接收器输入在内部连接以形成差分输入/输出 (I/O) 总线端口，该端口用于为总线提供最小负载，可在宽共模电压范围内工作，使得该器件非常适合合用线应用。该器件还包含合用线数据总线的附加功能，适用于电气噪声环境应用，例如工业过程控制或电源逆变器。

SN75LBC182 和 SN65LBC182 总线引脚还具有与四分之一单位负载等效的高输入电阻，允许在总线上连接多达 128 个类似器件。高 ESD 容差可保护器件的电缆连接。(如需更高级别的保护，请参阅 SN65/75LBC184，文献编号 SLLS236。)

差动驱动器设计包含压摆率受控的输出，足以以高达 250kbps 的速率传输数据。与不受控制的电压转换相比，压摆率控制允许从主干部署更长的末端接电缆和更长的残桩线。该接收器设计可在输入保持悬空 (开路) 时提供高电平失效防护输出。可以通过禁用驱动器和接收器来实现超低的器件待机电源电流。

SN65LBC182 的额定工作温度范围为 -40°C 至 85°C ，SN75LBC182 的额定工作温度范围为 0°C 至 70°C 。

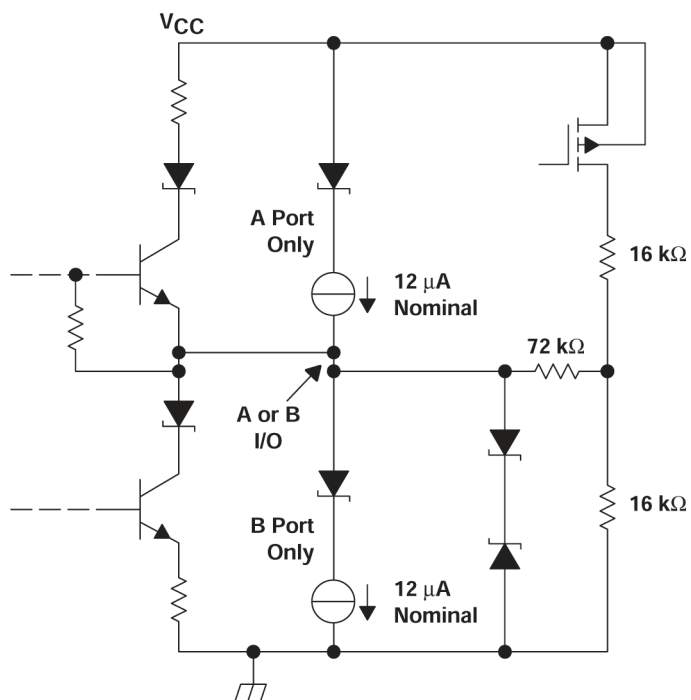
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN65LBC182、 SN75LBC182	P (PDIP , 8)	9.81mm × 9.43mm
	D (SOIC , 8)	4.9mm × 6mm

(1) 有关详细信息，请参阅 [节 11](#)。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。





输入和输出原理图

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4 Pin Configuration and Functions

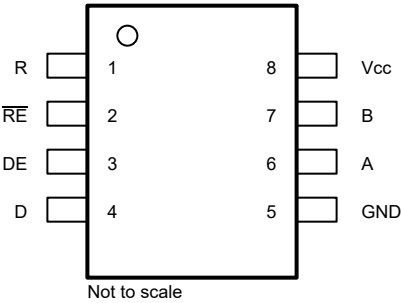


图 4-1. P (PDIP) or D (SOIC) Package
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Receiver Output
RE	2	I	Active Low Receiver Enable Input
DE	3	I	Active High Driver Enable Input
D	4	I	Driver Input
GND	5	GND	Device GND
A	6	I/O	Non-Inverting Differential Bus I/O
B	7	I/O	Inverting Differential Bus I/O
V _{CC}	8	PWR	Device VCC (4.75V to 5.25V)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range, (see ⁽²⁾)	-0.5	7	V
(A or B)	Voltage range at any bus terminal	-15	15	V
V _I (D, DE, R or RE)	Input voltage	-0.3	7	V
I _O	Receiver output current		±20	mA
	Continuous total power dissipation	See <i>Dissipation Rating</i> table		

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	A, B, GND	±15	kV
			All pins	±3	
		IEC 61000-4-2 contact discharge	A, B, GND	±8	kV
		IEC 61000-4-2 Air-gap discharge	A, B, GND	±15	kV

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Dissipation Rating

PACKAGE ⁽²⁾	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- (2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal (separately or common mode) V _I or V _{IC}		−7		12	V
High-level input voltage, V _{IH}	D, DE, RE	2		0.8	V
Low-level input voltage, V _{IL}					
Differential input voltage, V _{ID} (see ⁽¹⁾)		−12		12	V
Output current, I _O	Driver	−60		60	mA
	Receiver	−8		4	
Operating free-air temperature, T _A	SN65LBC182	−40		85	°C
	SN75LBC182	0		70	

- (1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	P (PDIP)	UNIT
		8-PINS		
R _{θJA}	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.6 Driver Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-1.5			V
V_O	Output voltage	$I_O = 0$		0		V_{CC}	V
$ V_{OD} $	Differential output voltage	$R_L = 54 \Omega$, $V_{test} = -7 \text{ V to } 12 \text{ V}$	See 图 6-1 See 图 6-2	1.5	2.2	V_{CC}	V
ΔV_{OD}	Change in magnitude of differential output voltage	See 图 6-1		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage			1		3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See 图 6-1 and 图 6-4		-0.2		0.2	
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions				0.8		V
I_{OZ}	High-impedance output current	See receiver input currents					
I_{IH}	High-level input current (D, DE)	$V_I = 2.4 \text{ V}$				50	μA
I_{IL}	Low-level input current (D, DE)	$V_I = 0.4 \text{ V}$		-50			μA
I_{OS}	Short-circuit output current	$V_O = -7 \text{ V to } 12 \text{ V}$		-250		250	mA
I_{CC}	Supply current	SN75LBC182	No load, DE at V_{CC} , $\overline{RE}$ at V_{CC}		12	25	mA
		SN65LBC182			12	30	

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage				0.2	V
V_{IT-}	Negative-going input threshold voltage		-0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			70		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18 \text{ mA}$	-1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_O = -8 \text{ mA}$, See 图 6-7	2.8			V

5.7 Receiver Electrical Characteristics (续)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OL} Low-level output voltage	V _{ID} = 200 mV, I _O = 4 mA,	See 图 6-7			0.4	V
I _{OZ} High-impedance-state output current	V _O = 0.4 to 2.4 V				±1	μ A
I _I Bus input current	V _{IH} = 12 V, V _{CC} = 5 V	Other input at 0 V			250	μ A
	V _{IH} = 12 V, V _{CC} = 0 V				250	
	V _{IH} = -7 V, V _{CC} = 5 V		-200			
	V _{IH} = -7 V, V _{CC} = 0 V		-200			
I _{IH} High-level input current ($\overline{RE}$)	V _{IH} = 2 V				50	μ A
I _{IL} Low-level input current ($\overline{RE}$)	V _{IL} = 0.8 V		-50			μ A
I _{CC} Supply current	No load	DE at 0 V, $\overline{RE}$ at 0 V			3.5	mA
		DE at 0 V, $\overline{RE}$ at V _{CC}		175	250	μ A

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _r Differential output signal rise time	R _L = 54 Ω, See 图 6-3	C _L = 50 pF,	0.25	0.72	1.2	μ s
t _f Differential output signal fall time			0.25	0.73	1.2	
t _{PLH} Propagation delay time, low-to-high-level output					1.3	
t _{PHL} Propagation delay time, high-to-low-level output					1.3	
t _{sk(p)} Pulse skew (t _{PHL} - t _{PLH})				0.075	0.15	
t _{PZH} Output enable time to high level	R _L = 110 Ω, See 图 6-5				3.5	μ s
t _{PHZ} Output disable time from high level					3.5	
t _{PZL} Output enable time to low level	R _L = 110 Ω, See 图 6-6				3.5	μ s
t _{PLZ} Output disable time from low level					3.5	

5.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _r Differential output signal rise time	C _L = 50 pF, See 图 6-7		20		ns
t _f Differential output signal fall time			20		
t _{PLH} Propagation delay time, low-to-high-level output				150	
t _{PHL} Propagation delay time, high-to-low-level output				150	
t _{PZH} Output enable time to high level	See 图 6-8			100	ns
t _{PZL} Output enable time to low level				100	
t _{PHZ} Output disable time from high level				100	ns
t _{PLZ} Output disable time from low level				100	
t _{sk(p)} Pulse skew t _{PHL} - t _{PLH}				50	ns

5.10 Typical Characteristics

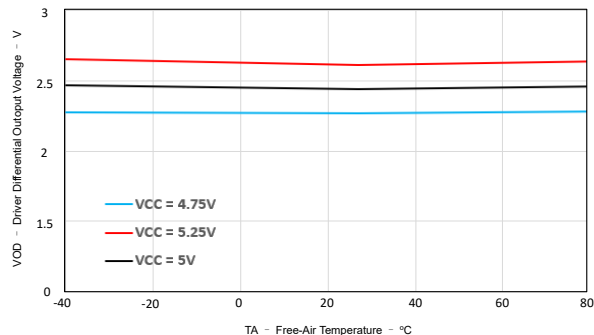


图 5-1. Driver Differential Output Voltage vs Temperature

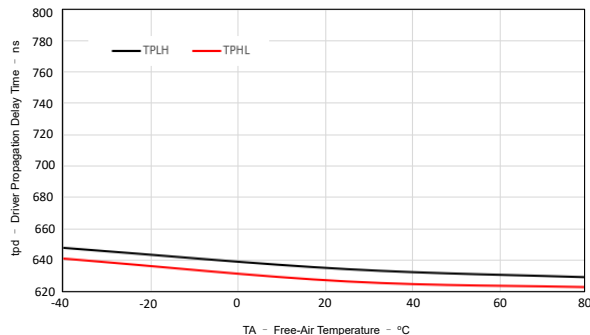


图 5-2. Driver Propagation Delay Time vs Temperature

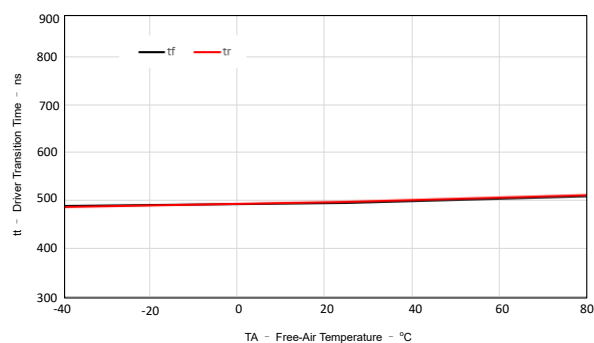


图 5-3. Driver Transition Time vs Temperature

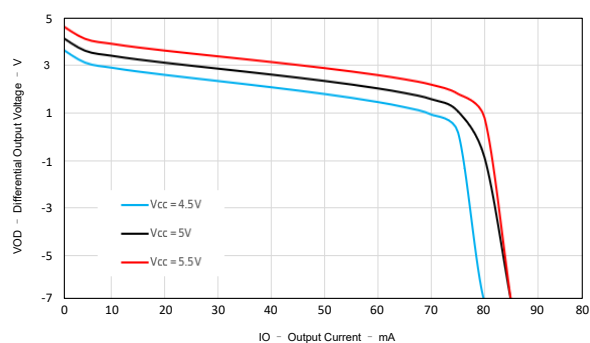


图 5-4. Differential Output Voltage vs Output Current

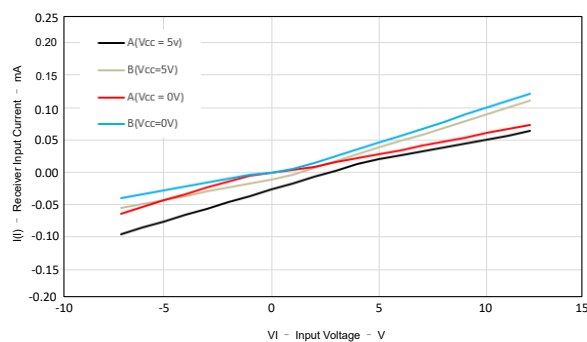
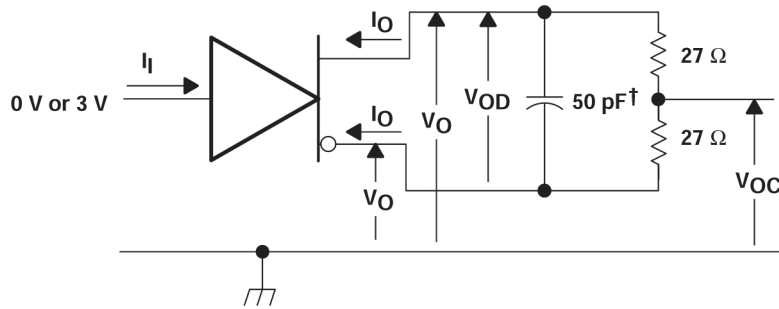


图 5-5. Receiver Input Current vs Input Voltage

6 Parameter Measurement Information



A. Includes probe and jig capacitance

图 6-1. Driver Test Circuit, v_{OD} And v_{OC} Without Common-Mode Loading

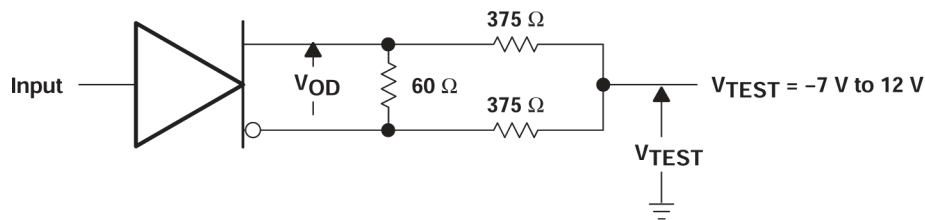
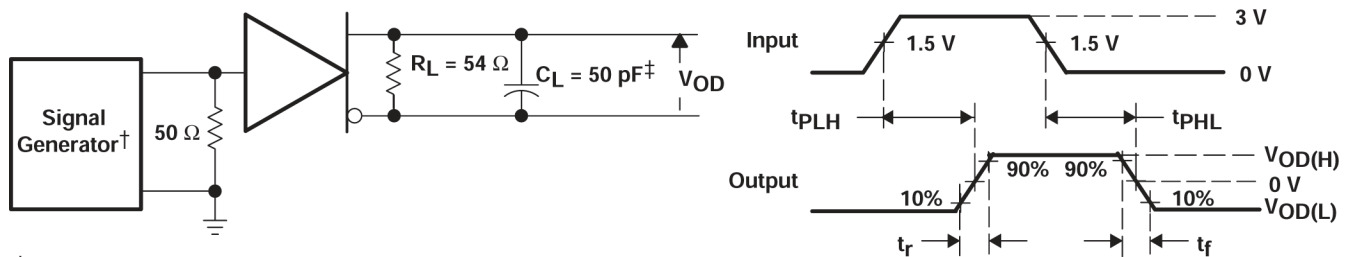


图 6-2. Driver Test Circuit, v_{OD} With Common-Mode Loading



- A. PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$
B. Includes probe and jig capacitance

图 6-3. Driver Switching Test Circuit and Waveforms

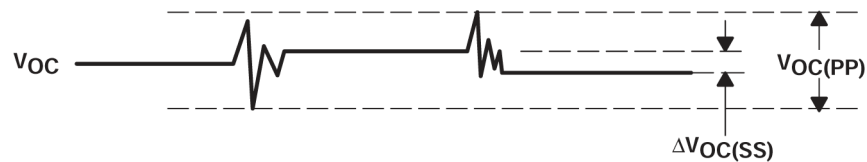
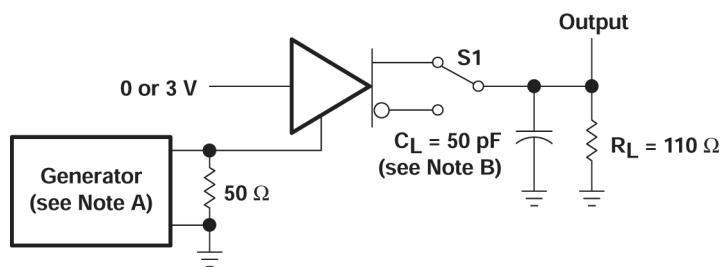
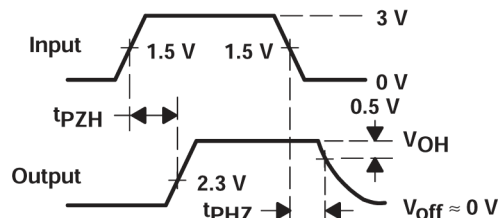


图 6-4. V_{OC} Definitions



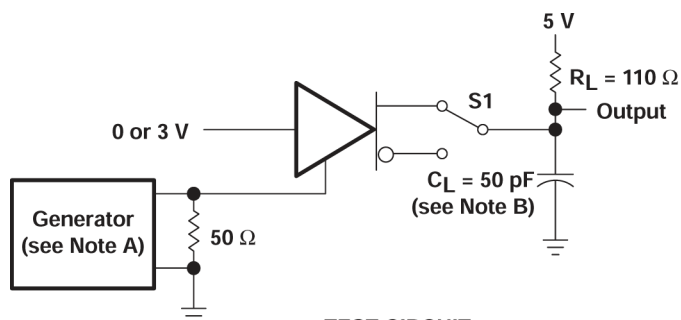
TEST CIRCUIT



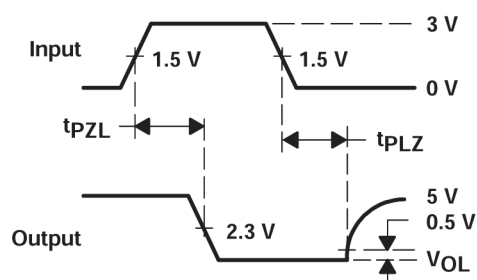
VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

图 6-5. Driver T_{PZH} And T_{PHZ} Test Circuit and Voltage Waveforms



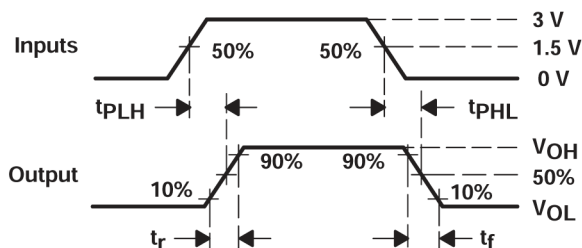
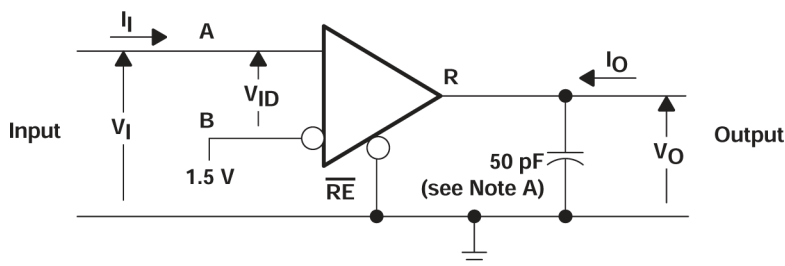
TEST CIRCUIT



VOLTAGE WAVEFORMS

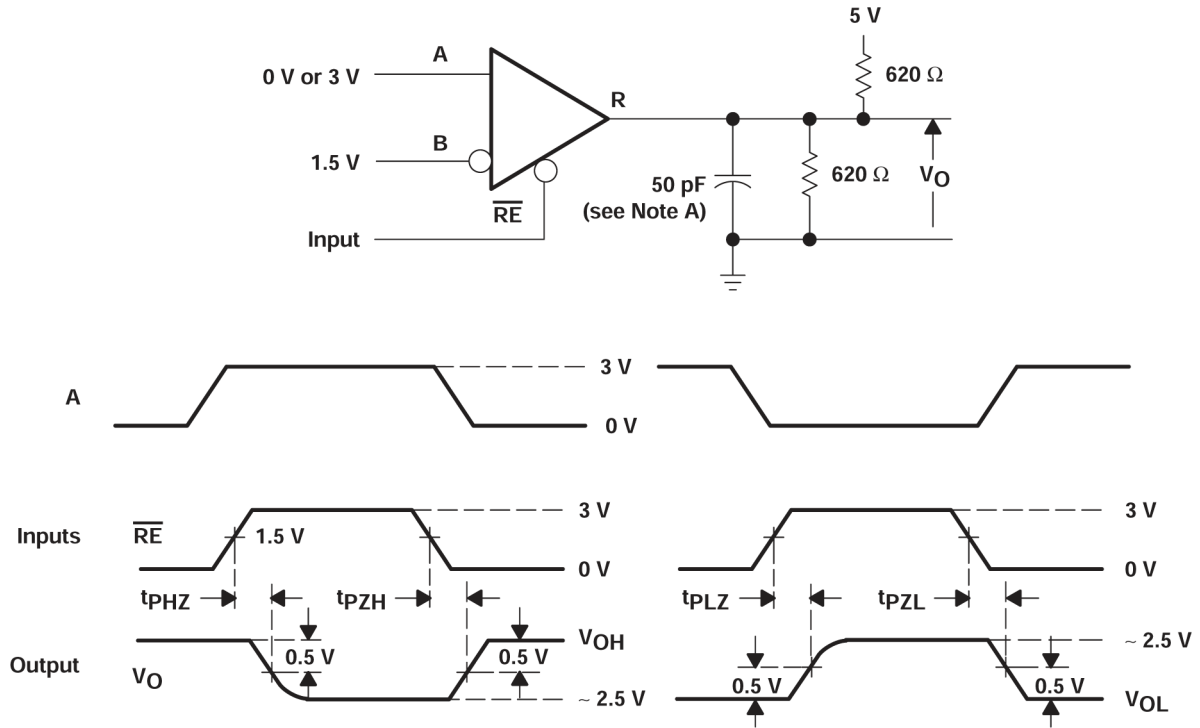
- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

图 6-6. Driver T_{PZL} And T_{PLZ} Test Circuit and Voltage Waveforms



- A. This value includes probe and jig capacitance ($\pm 10\%$).

图 6-7. Receiver T_{PLH} And T_{PHL} Test Circuit and Voltage Waveforms

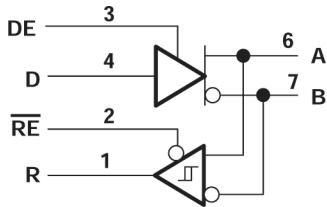


A. This value includes probe and jig capacitance ($\pm 10\%$).

图 6-8. Receiver T_{PZL} , T_{PLZ} , T_{PZH} , And T_{PHZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

表 7-1. Function Tables Driver

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

表 7-2. Function Tables Receiver

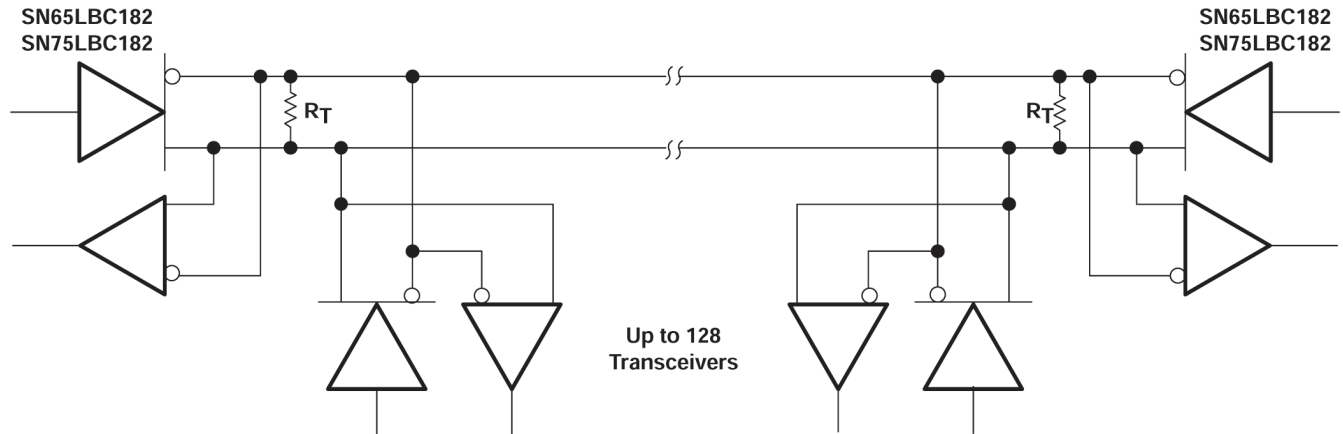
DIFFERENTIAL INPUTS	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information



- A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (March 2005) to Revision B (October 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC182D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	6LB182
SN65LBC182DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182
SN65LBC182DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182
SN65LBC182DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182
SN65LBC182P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC182
SN65LBC182P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC182
SN75LBC182D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	7LB182
SN75LBC182DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182
SN75LBC182DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182
SN75LBC182P	Obsolete	Production	PDIP (P) 8	-	-	Call TI	Call TI	0 to 70	75LBC182

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

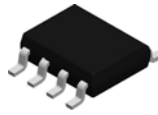
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC182DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65LBC182DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75LBC182DR	SOIC	D	8	2500	353.0	353.0	32.0
SN75LBC182DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC182P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC182P.A	P	PDIP	8	50	506	13.97	11230	4.32

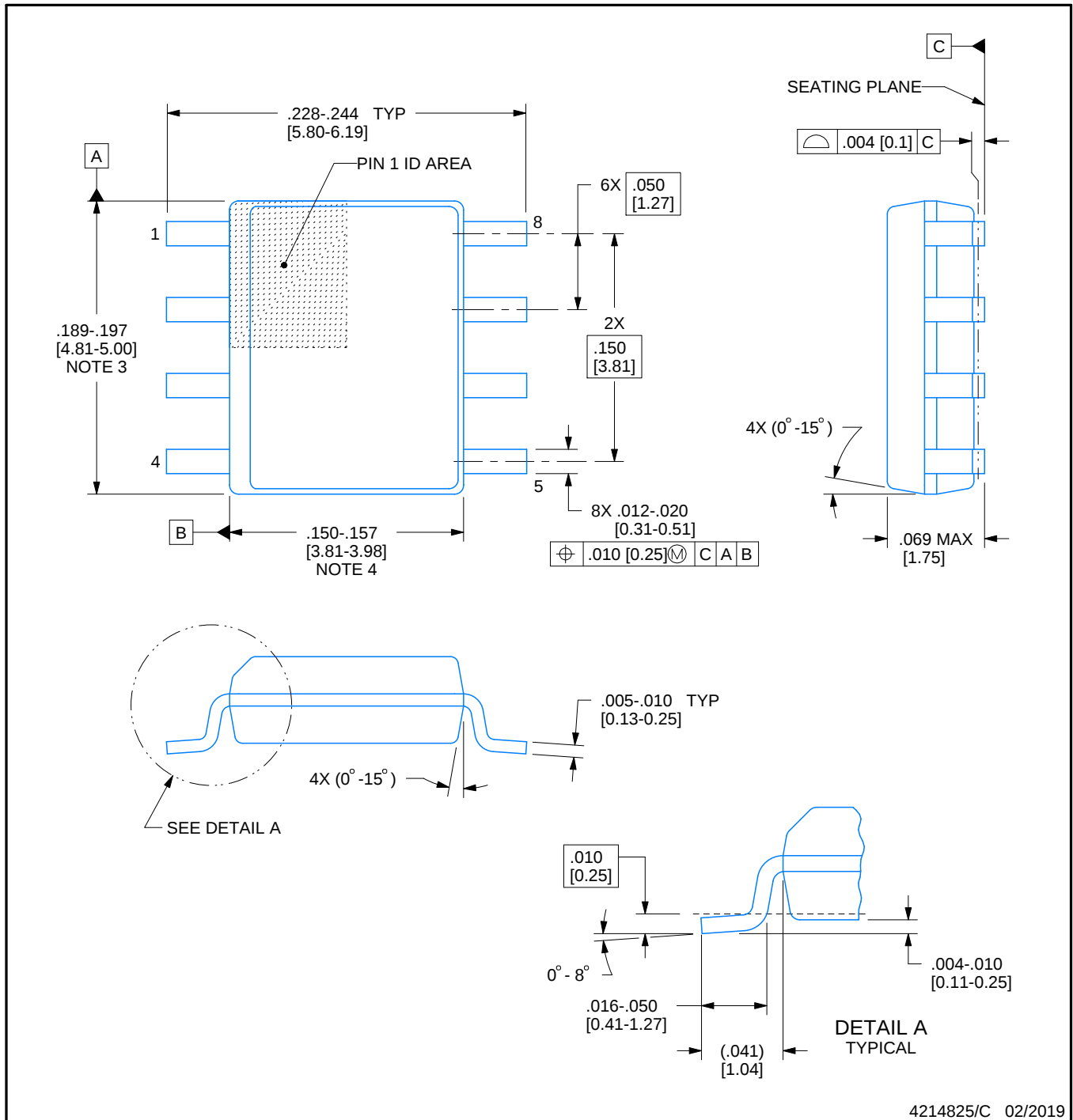


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



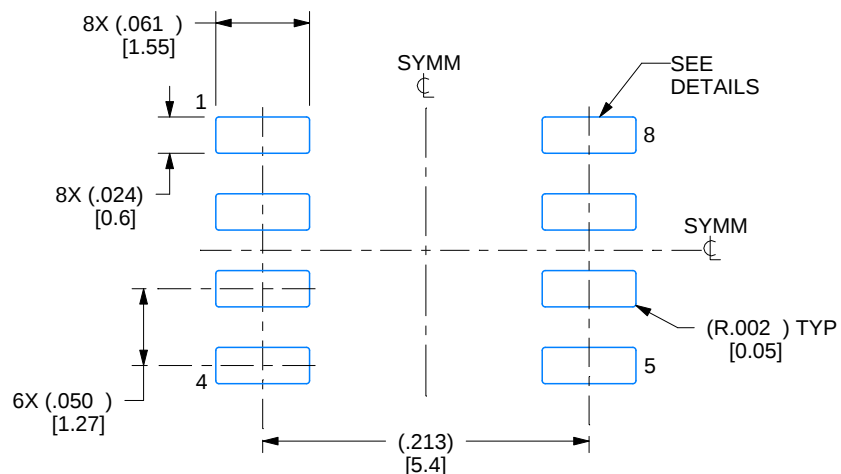
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

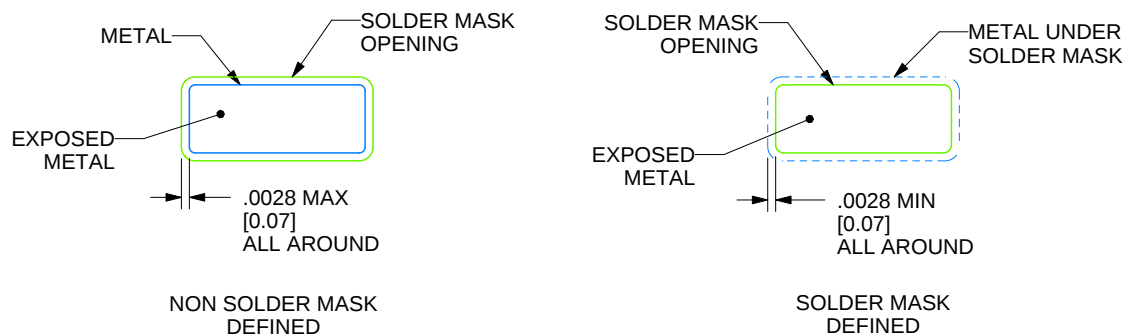
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

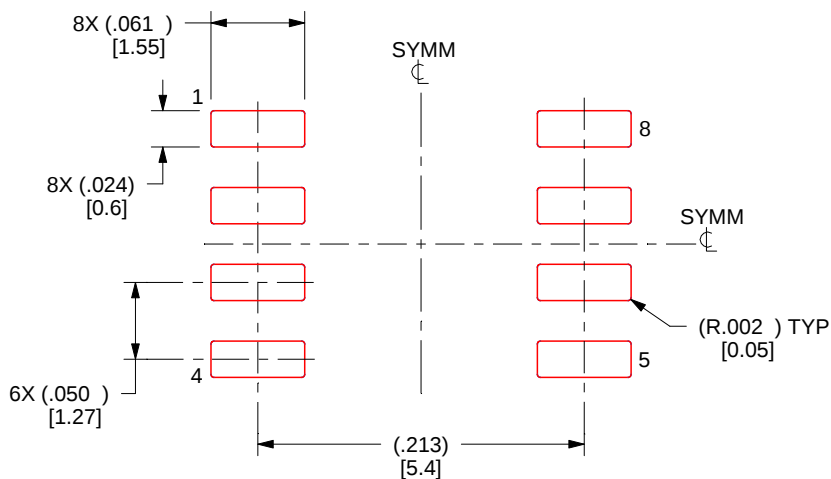
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

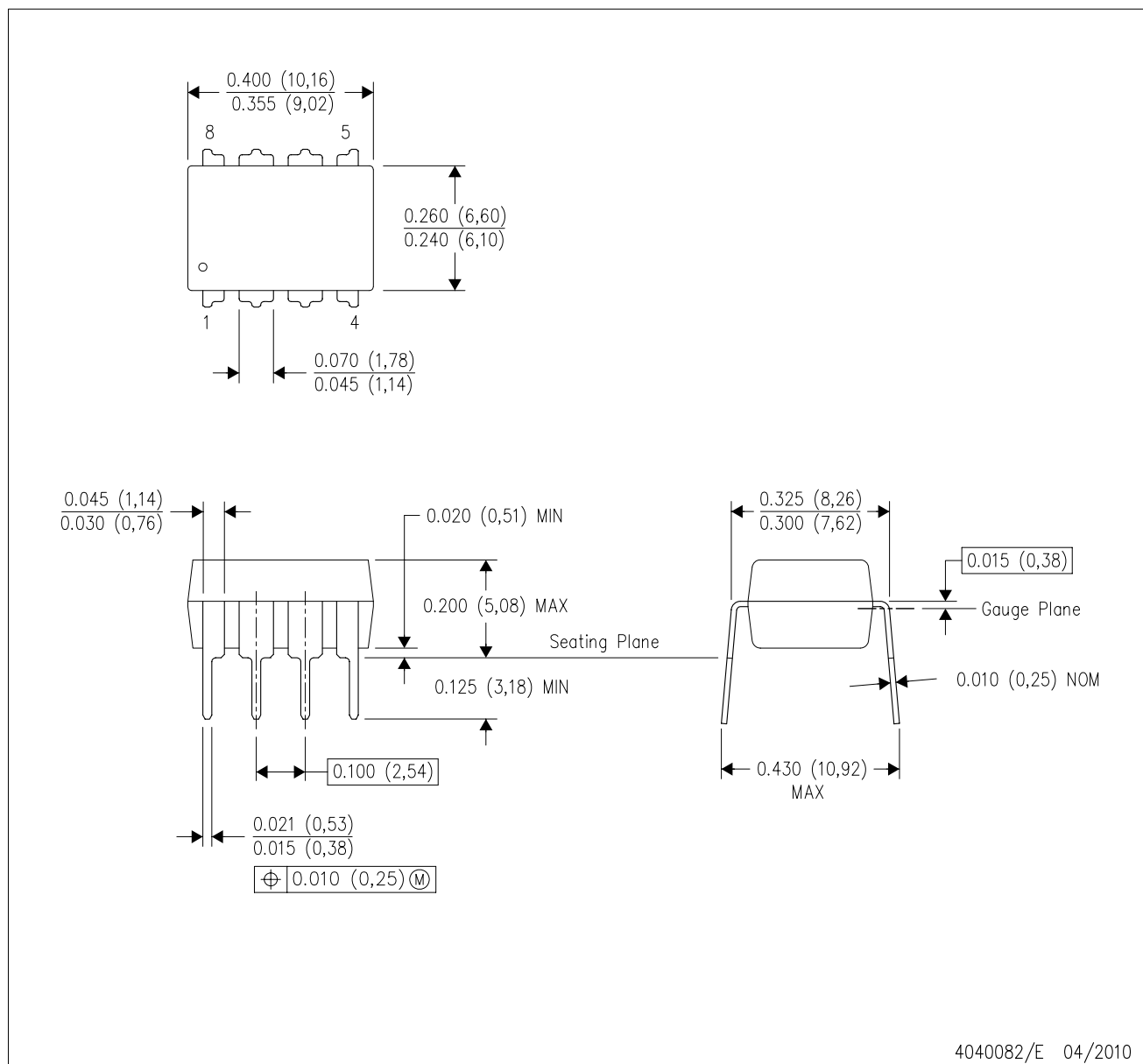
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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