INDUSTRIAL 8-DIGITAL-INPUT SERIALIZER

FEATURES

- **Eight Inputs**
  - **High Input Voltage – up to 34 V**
  - **Selectable Debounce Filters – 0 ms to 3 ms**
  - **Flexible Input Current Limit – 0.2 mA to 5.2 mA**
  - **Field Pins Protected to 15-kV HBM ESD**
- **Output Drivers for External Status LEDs**
- **Cascadable in Multiples of Eight Inputs**
- **SPI-Compatible Interface**
- **Regulated 5-V Output for External Isolator**
- **Over-Temperature Indicator**

APPLICATIONS

- **Sensor Inputs for Industrial Automation and Process Control**
- **High Channel Count Digital Input Modules for PC and PLC Systems**
- **Decentralized I/O Modules**
- **Motion Control Systems**

DESCRIPTION

The SN65HVS882 is an eight channel, digital-input serializer for high-channel density digital input modules in industrial automation. In combination with galvanic isolators the device completes the interface between the high voltage signals on the field-side and the low-voltage signals on the controller side. Input signals are current-limited and then validated by internal debounce filters.

With the addition of a few external components, the input switching characteristics can be configured in accordance with IEC61131-2 for Type 1, 2, and 3 sensor switches.

Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially.

Cascading of multiple devices is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Multiple devices can be cascaded through a single serial port, reducing both the isolation channels and controller inputs required.

Input status can be visually indicated via constant current LED outputs. The current limit on the inputs is set by a single external precision resistor. An integrated voltage regulator provides a 5-V output to supply low-power isolators. An on-chip temperature sensor provides diagnostic information for graceful shutdown and system safety.

The SN65HVS882 is available in a 28-pin PWP PowerPAD™ package, allowing for efficient heat dissipation. The device is characterized for operation at temperatures from -40°C to 125°C.

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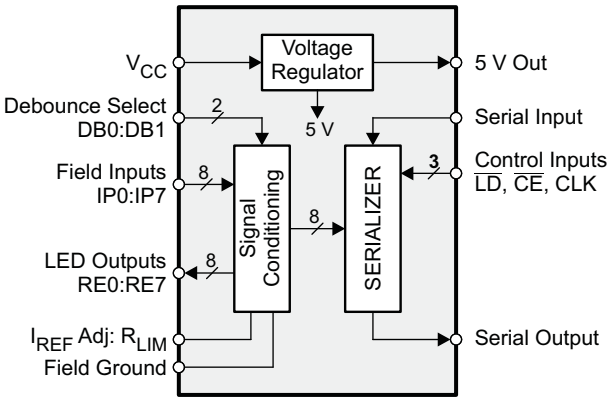
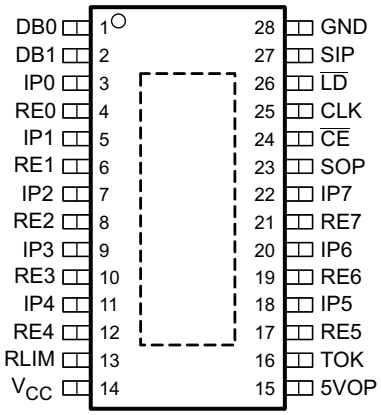
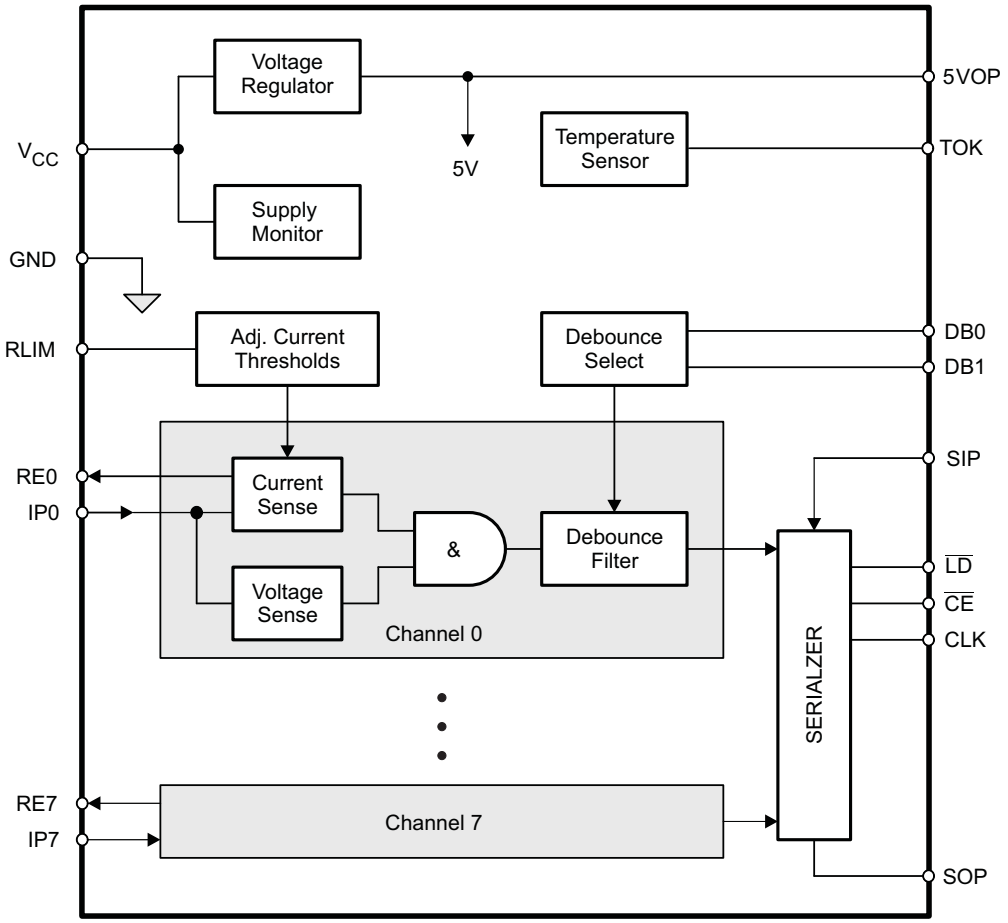




FUNCTIONAL BLOCK DIAGRAM



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TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
PIN NO.	NAME	
1, 2	DB0, DB1	Debounce select inputs
3, 5, 7, 9, 11, 18, 20, 22	IPx	Input channel x
4, 6, 8, 10, 12, 17, 19, 21	REx	Return path x (LED drive)
13	RLIM	Current limiting resistor
14	V_{CC}	Field supply voltage
15	5VOP	5-V output to supply low power isolators
16	TOK	Temperature okay
23	SOP	Serial data output
24	$\overline{CE}$	Clock enable input
25	CLK	Serial clock input
26	$\overline{LD}$	Load pulse input
27	SIP	Serial data input
28	GND	Field ground

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
V_{CC}	Field power input			–0.3 to 36	V
V_{IPx}	Field digital inputs		IPx	–0.3 to 36	V
V_{ID}	Voltage at any logic input		DB0, DB1, CLK, SIP, $\overline{CE}$, $\overline{LD}$	–0.5 to 6	V
I_O	Output current		TOK, SOP	±8	mA
V_{ESD}	Electrostatic discharge	Human-Body Model(2)	All pins	±4	kV
			IPx,V_{CC}	±15	
		Charged-Device Model(3)	All pins	±1	kV
		Machine Model(4)	All pins	±100	V
P_{TOT}	Continuous total power dissipation	See *Thermal Characteristics*			
T_J	Junction temperature			170	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) JEDEC Standard 22, Method A114-A.
(3) JEDEC Standard 22, Method C101
(4) JEDEC Standard 22, Method A115-A

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	High-K JEDEC thermal resistance model			35		°C/W
θ_{JB}	Junction-to-board thermal resistance				15		°C/W
θ_{JC}	Junction-to-case thermal resistance				4.27		°C/W
P_D	Device power dissipation	I_{CC} and $I_{IP\text{-}LIM}$ = worst case with R_{LIM} = 25 kΩ, I_{LOAD} = 50 mA on 5VOP, RE0-RE7 = GND, f_{IP} = 100 MHz	IP0-IP7 = V_{CC} = 34 V				mW
			IP0-IP7 = V_{CC} = 30 V			2600	
			IP0-IP7 = V_{CC} = 24 V				
			IP0-IP7 = V_{CC} = 12 V				

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Field supply voltage		10		34	V
V_{IPL}	Field input low-state input voltage		0		4	V
V_{IPH}	Field input high-state input voltage		5.5		34	V
V_{IL}	Logic low-state input voltage		0		0.8	V
V_{IH}	Logic high-state input voltage		2.0		5.5	V
R_{LIM}	Current limiter resistor		17	25	500	kΩ
f_{IP}(1)	Input data rate (each field input)		0		1	Mbps
T_A	Free-air temperature, see *Thermal Characteristics*	V_{CC} ≤ 34 V	–40		85	°C
		V_{CC} ≤ 27 V	–40		105	
		V_{CC} ≤ 18 V	–40		125	
T_J	Junction temperature				150	°C

(1) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = GND), and R_{IN} = 0 Ω

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ELECTRICAL CHARACTERISTICS

Over full-range of recommended operating conditions, unless otherwise noted

PARAMETER		TERMINAL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FIELD INPUTS							
$V_{TH-(IP)}$	Low-level input threshold voltage	IP0–IP7	R_{LIM} = 25 kΩ	4.0	4.3		V
$V_{TH+(IP)}$	High-level input threshold voltage				5.2	5.5	
$V_{HYS(IP)}$	Input hysteresis				0.9		
$V_{TH-(IN)}$	Low-level input threshold voltage	Measured at field side of R_{IN}	18 V < V_{CC} <30 V, R_{IN} = 1.2 kΩ ± 5%, R_{LIM} = 25 kΩ, T_A ≤ 85 °C	6	8.4		V
$V_{TH+(IN)}$	High-level input threshold voltage				9.4	10	
$V_{HYS(IN)}$	Input hysteresis				1		
R_{IP}	Input resistance	IP0–IP7	3 V < V_{IPx} < 6 V, R_{LIM} = 25 kΩ	0.2	0.63	1.1	kΩ
I_{IP-LIM}	Input current limit	IP0–IP7	R_{LIM} = 25 kΩ	3.15	3.6	4	mA
t_{DB}	Debounce times of input channels	IP0–IP7	DB0 = open, DB1 = GND		0		ms
			DB0 = GND, DB1 = open		1		
			DB0 = DB1 = open		3		
I_{RE-on}	RE on-state current	RE0–RE7	R_{LIM} = 25 kΩ, RE_x = GND	2.8	3.15	3.5	mA
FIELD SUPPLY							
$ICC_{(VCC)}$	Supply current, no load	V_{CC}	IP0 to IP7 = V_{CC}, 5VOP = open, RE_X = GND, All logic inputs open			8.7	mA
5V REGULATED OUTPUT							
$V_{O(5V)}$	Linear regulator output voltage	5VOP	10V < V_{CC} < 34V, no load	4.5	5	5.5	V
			10V < V_{CC} < 34V, $_{IL}$ = 5mA	4.5	5	5.5	
			10V < V_{CC} < 34V, I_L = 20mA, T_A ≤ 105°C	4.5	5	5.5	
			10V < V_{CC} < 34V, I_L = 50 mA, T_A ≤ 85°C	4.5	5	5.5	
$I_{LIM(5V)}$	Linear regulator output current limit				115		mA
$\Delta V_5/\Delta V_{CC}$	Linear regulation	5VOP, V_{CC}	10V < V_{CC} < 34V, I_L = 5 mA,			2	mV/V
LOGIC INPUT AND OUTPUTS							
V_{OL}	Logic low-level output voltage	SOP, TOK	I_{OL} = 20 µA			0.4	V
V_{OH}	Logic high-level output voltage		I_{OH} = –20 µA	4			V
I_{IL}	Logic input leakage current	DB0, DB1, SIP, $\overline{LD}$, $\overline{CE}$, CLK		–50		50	µA
T_{OVER}	Over-temperature indication, internal	TOK			150		°C
T_{SHDN}	Shutdown temperature, internal				170		°C

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TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t_{W1}	CLK pulse duration	See Figure 5	4			ns
t_{W2}	$\overline{LD}$ pulse duration	See Figure 3	6			ns
t_{SU1}	SIP to CLK setup time	See Figure 6	4			ns
t_{H1}	SIP to CLK hold time	See Figure 6	2			ns
t_{SU2}	Falling edge to rising edge ($\overline{CE}$ to CLK) setup time	See Figure 7	4			ns
t_{REC}	$\overline{LD}$ to CLK recovery time	See Figure 4	2			ns
f_{CLK}	Clock pulse frequency	See Figure 5	DC		100	MHz

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}, t_{PHL1}	CLK to SOP	C_L = 15 pF, see Figure 5			10	ns
t_{PLH2}, t_{PHL2}	$\overline{LD}$ to SOP	C_L = 15 pF, see Figure 3			14	ns
t_r, t_f	Rise and fall times	C_L = 15 pF, see Figure 5			5	ns

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INPUT CHARACTERISTICS

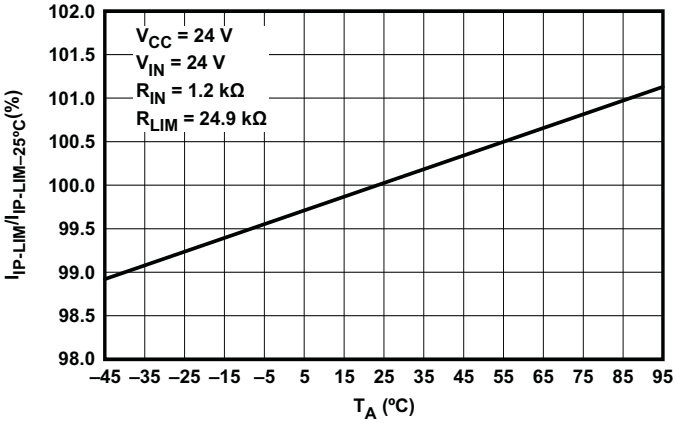

Figure 1. Typical Current Limiter Variation vs Free-Air Temperature

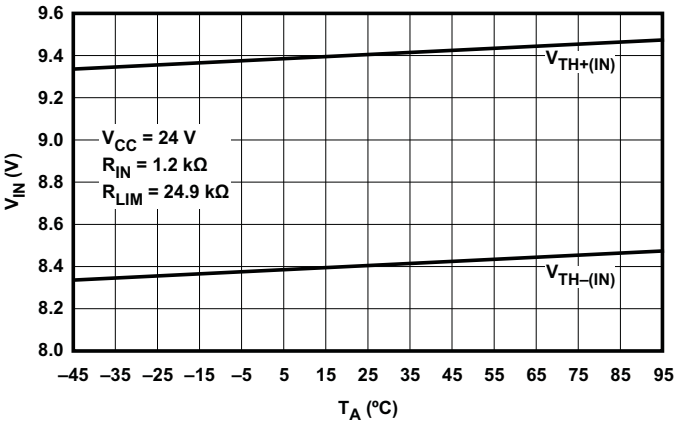

Figure 2. Typical Limiter Input Threshold Voltage Variation vs Free-Air Temperature

PARAMETER MEASUREMENT INFORMATION

Waveforms

For the complete serial interface timing, refer to Figure 19.

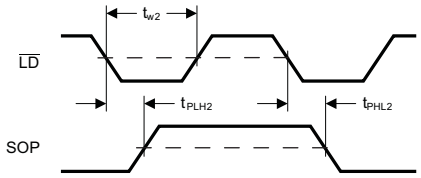

Figure 3. Parallel – Load Mode

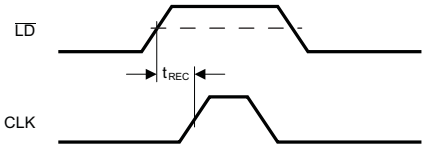

Figure 4. Serial – Shift Mode

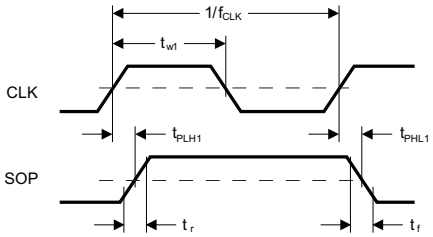

Figure 5. Serial – Shift Mode

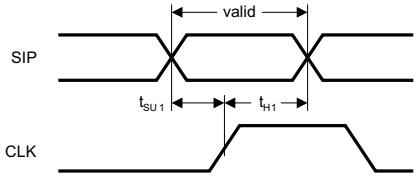

Figure 6. Serial – Shift Mode

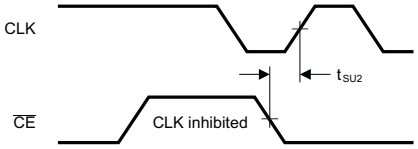

Figure 7. Serial – Shift Clock Inhibit Mode

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VOLTAGE REGULATOR PERFORMANCE CHARACTERISTICS

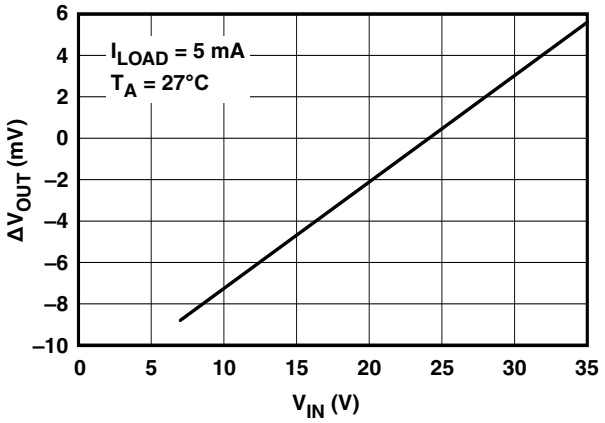

Figure 8. Line Regulation

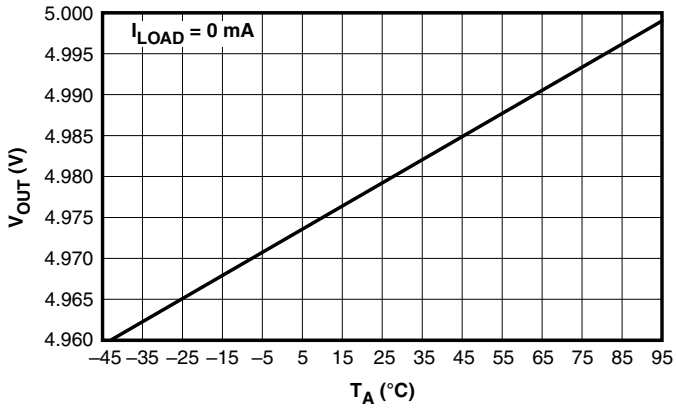

Figure 9. Output Voltage vs Free-Air Temperature

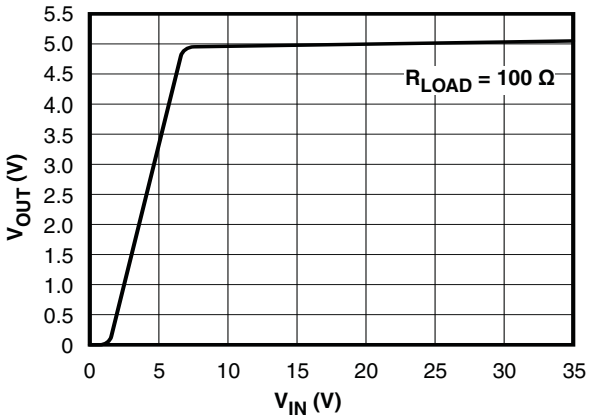

Figure 10. Output Voltage vs Input Voltage

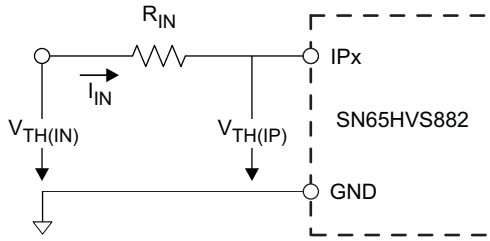

Figure 11. On/Off Threshold Voltage Measurements

DEVICE INFORMATION

Digital Inputs

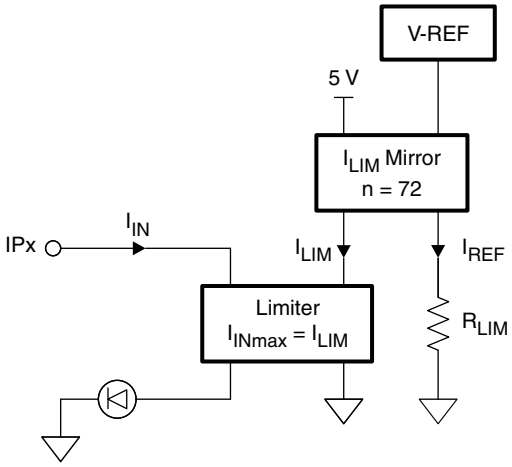

Figure 12. Digital Input Stage

Each digital input operates as a controlled current sink limiting the input current to a maximum value of I_{LIM}. The current limit is derived from the reference current via $I_{LIM} = n \times I_{REF}$, and I_{REF} is determined by $I_{REF} = V_{REF}/R_{LIM}$. Thus, changing the current limit requires the change of R_{LIM} to a different value via: $R_{LIM} = n \times V_{REF}/I_{LIM}$.

While the device is specified for a current limit of 3.6 mA, (via R_{LIM} = 25 kΩ), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of 2.5 mA simply calculate:

$$R_{LIM} = \frac{90}{I_{LIM}} = \frac{90}{2.5\ \text{mA}} = 36\ \text{k}\Omega$$

Debounce Filter

The HVS882 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table.

Table 1. Debounce Times

DB1	DB0	FUNCTION
Open	Open	3 ms delay
Open	GND	1 ms delay
GND	Open	0 ms delay (filter bypassed)
GND	GND	Reserved

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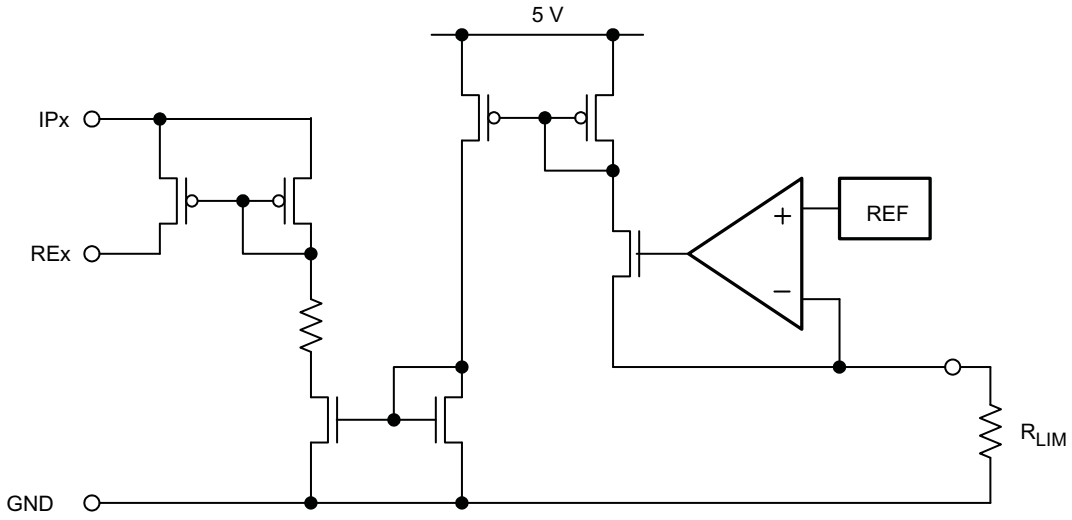

Figure 13. Equivalent Input Diagram

Shift Register

The conversion from parallel input to serial output data is performed by an eight-channel serial-in parallel-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7, that are enabled by a low level at the load input ($\overline{LD}$). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{LD}$ is held high and the clock enable ($\overline{CE}$) input is held low. Parallel loading is inhibited when $\overline{LD}$ is held high. The parallel inputs to the register are enabled while $\overline{LD}$ is low independently of the levels of the CLK, $\overline{CE}$, or serial (SIP) inputs.

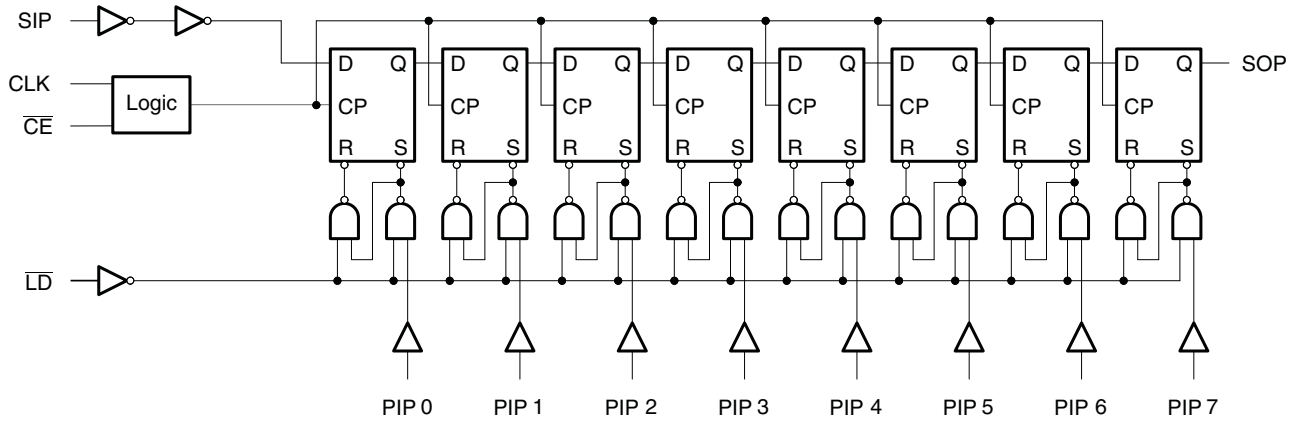

Figure 14. Shift Register Logic Structure

Table 2. Function Table

INPUTS			FUNCTION
$\overline{LD}$	CLK	$\overline{CE}$	
L	X	X	Parallel load
H	X	H	No change
H	↑	L	Shift (1)

(1) Shift = content of each internal register shifts towards serial outputs. Data at SIP is shifted into first register.

Voltage Regulator

The on-chip linear voltage regulator provides a 5-V supply to the internal and external circuitry, such as digital isolators, with an output drive capability of 50 mA and a typical current limit of 115 mA. The regulator accepts input voltages from 30 V down to 10 V. Because the regulator output is intended to supply external digital isolator circuits proper output voltage decoupling is required. For best results connect a 1-µF and a 0.1-µF ceramic capacitor as close as possible to the 5VOP output. For longer traces between the SN65HVS882 and isolators of the ISO72xx family use additional 0.1-µF and 10-pF capacitors next to the isolator supply pins. Make sure, however, that the total load capacitance does not exceed 4.7 µF.

For good stability the voltage regulator requires a minimum load current, $I_{L\text{-}MIN}$. Ensure that under any operating condition the ratio of the minimum load current in mA to the total load capacitance in µF is larger than 1:

$$\frac{I_{L\text{-}MIN}}{C_L} > \frac{1\ \text{mA}}{1\ \mu\text{F}}$$

Temperature Sensor

An on-chip temperature sensor monitors the device temperature and signals a fault condition if the internal temperature reaches 150°C. If the internal temperature exceeds this trip point, the TOK output switches to an active low state. If the internal temperature continues to rise, passing a second trip point at 170°C, all device outputs are put in a high-impedance state.

A special condition occurs, however, when the chip temperature exceeds the second temperature trip point due to an output short. Then the output buffer becomes three-state, thus separating the buffer from the external circuitry. An internal 100-kΩ pull-down resistor, connecting the TOK pin to ground, is used as a *cooling down* resistor, which continues to provide a logic low level to the external circuitry.

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APPLICATION INFORMATION

System-Level EMC

The SN65HVS882 is designed to operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards. In addition to the device internal ESD structures, external protection circuitry, as shown in Figure 15, can be used to absorb as much energy from burst- and surge-transients as possible.

R_1	56-Ω, 1/3-W MELF resistor
D_1	33–36-V fast Zener diode, ZSMB36
C_1	10-µF, 60-V ceramic capacitor
R_{IN}	1.2-kΩ, 1/4-W MELF resistor
C_{IN}	22-nF, 60-V ceramic capacitor
C_S	4.7-nF, 2-kV polypropylene capacitor
D_S	39-V transient voltage suppressor, SM15T39CA
D_2	Super rectifier: BYM10-1000 or General purpose rectifier: 1N4007

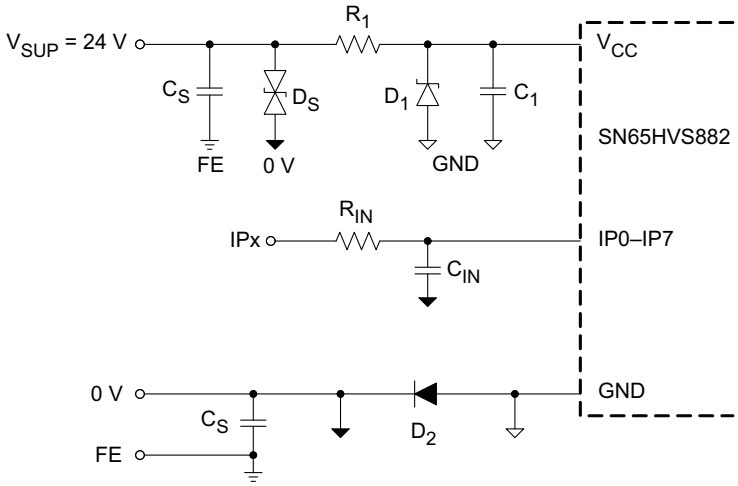

Figure 15. Typical EMC Protection Circuitry for Supply and Signal Inputs

Input Channel Switching for IEC61131-2 PLC Applications

The input stage of the SN65HVS882 is designed so that with a 24-V supply on V_{CC} and an input resistor R_{IN} = 1.2 kΩ, the trip point for signaling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 type-1 and type-3 switches.

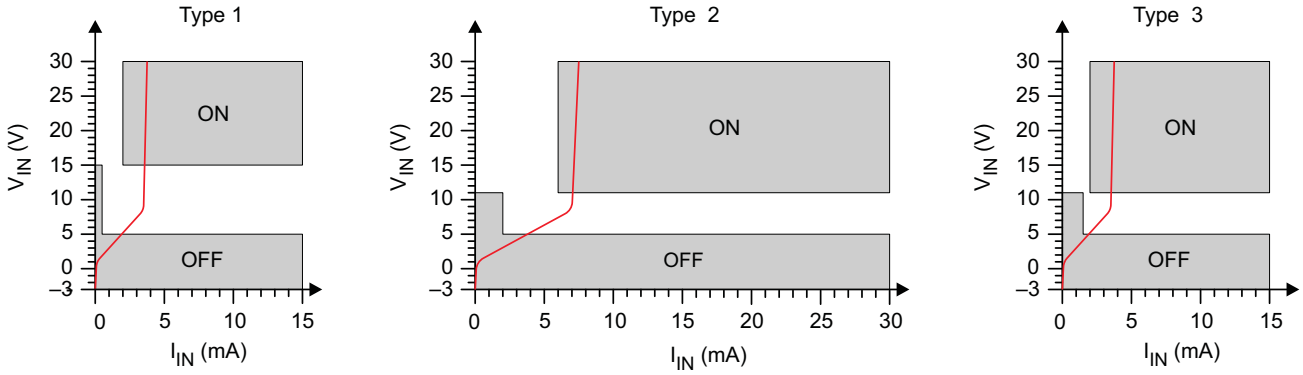

Figure 16. Switching Characteristics for IEC1131-2 Type 1, 2, and 3 Proximity Switches

For a type-2 switch application two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (GND).

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

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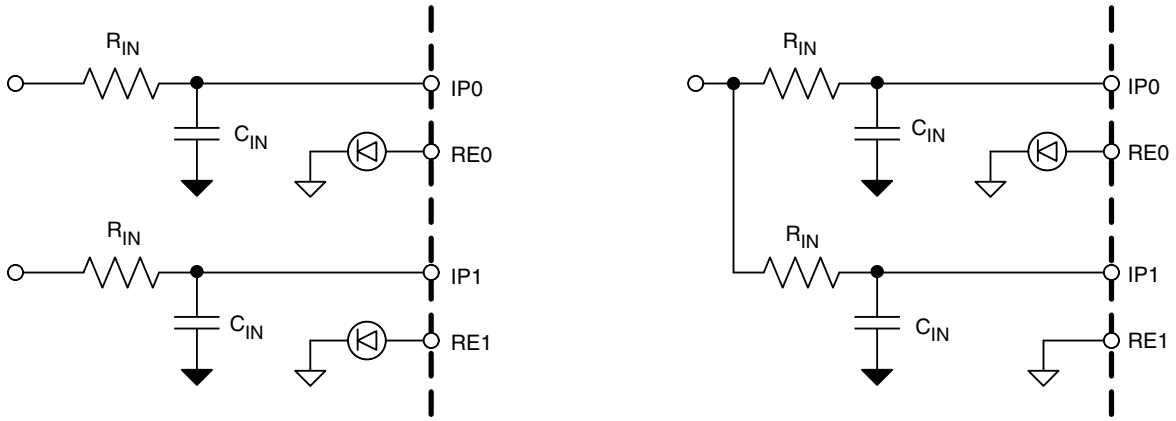

Figure 17. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input

Digital Interface Timing

The digital interface of the SN65HVS882 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard microcontrollers.

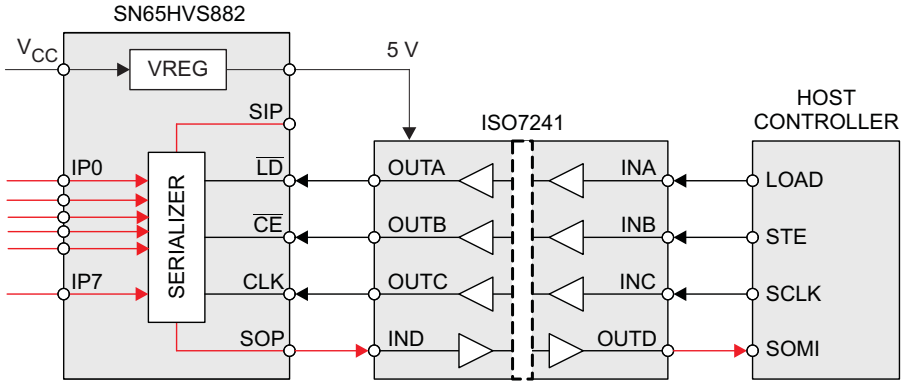

Figure 18. Simple Isolation of the Shift Register Interface

Upon a low-level at the load input, $\overline{LD}$, the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking $\overline{LD}$ high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, $\overline{CE}$, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

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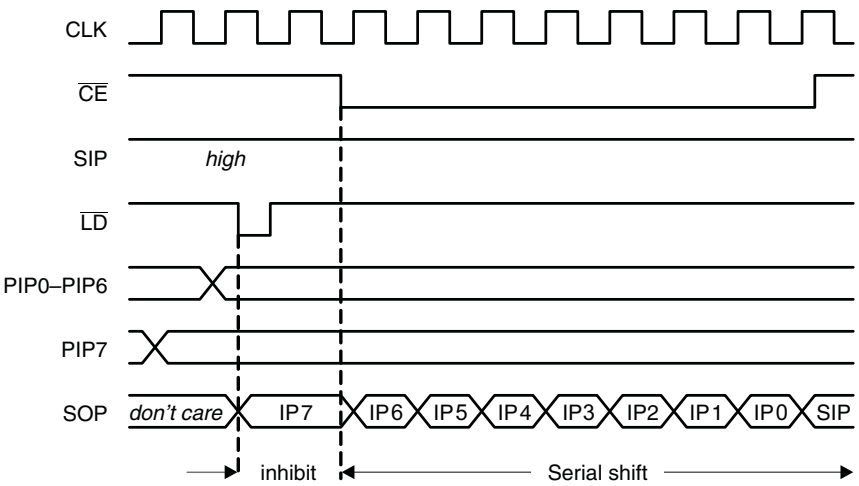

Figure 19. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register

Cascading for High Channel Count Input Modules

Designing high-channel count modules requires cascading multiple SN65HVS882 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

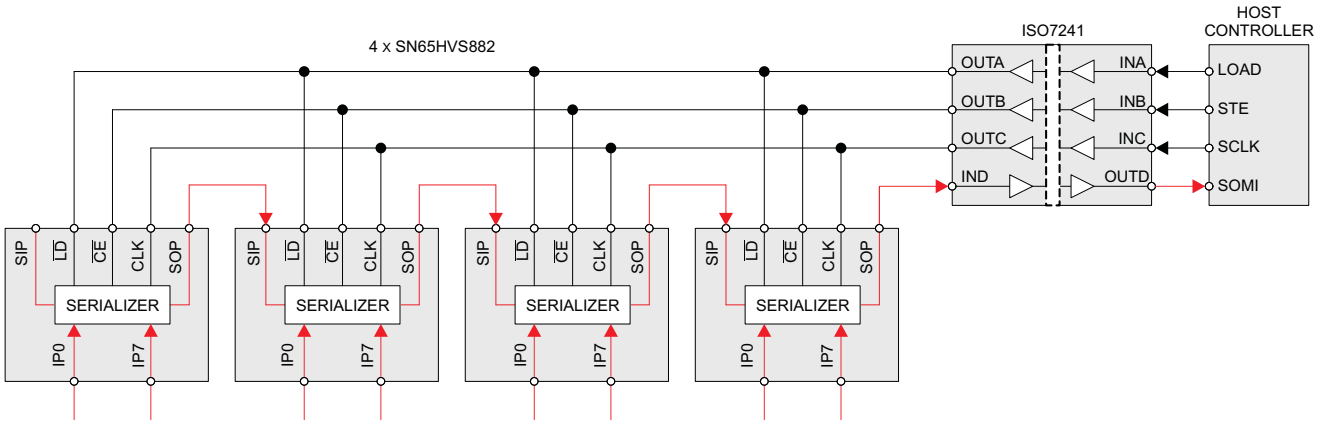

Figure 20. Cascading Four SN65HVS882 for a 32-Channel Input Module

Typical Digital Input Module Application

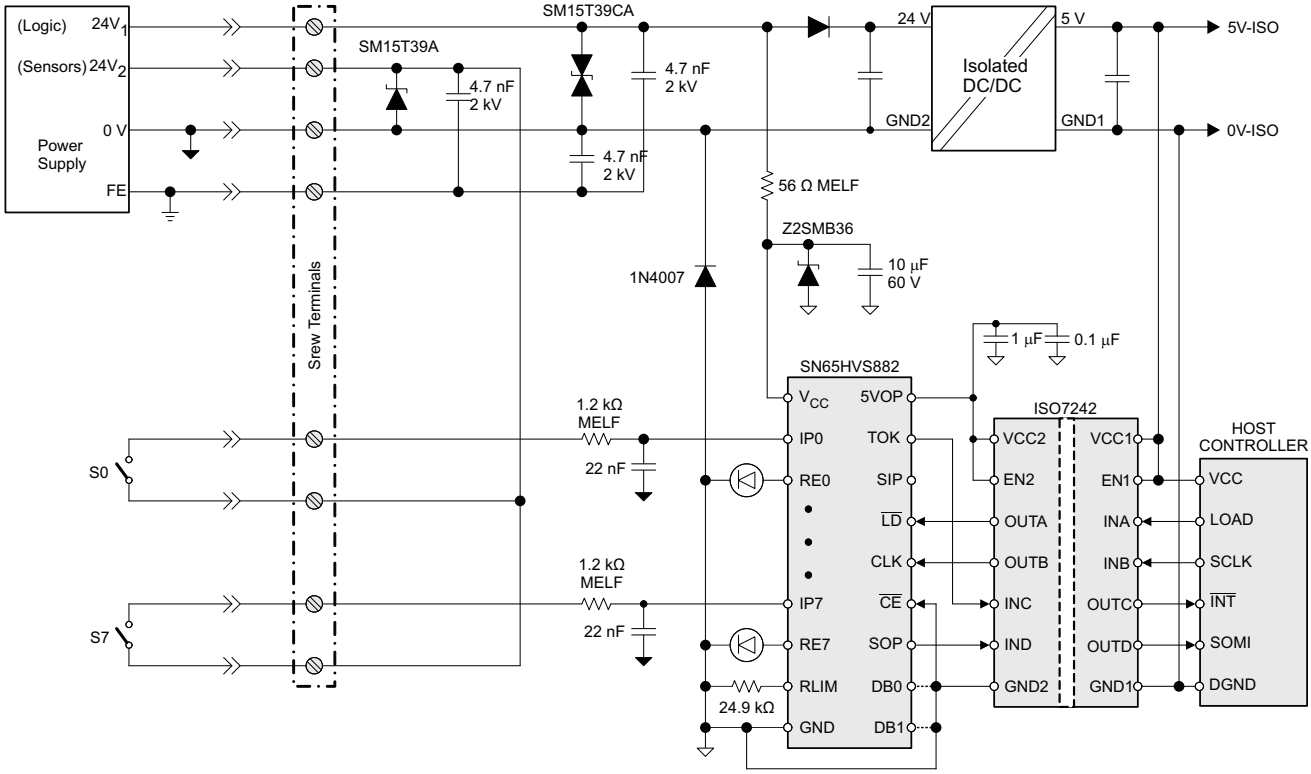

Figure 21. Typical Digital Input Module Application

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVS882PWP	Obsolete	Production	HTSSOP (PWP) | 28	-	-	Call TI	Call TI	-40 to 125	HVS882
SN65HVS882PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS882
SN65HVS882PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS882
SN65HVS882PWPRG4	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS882

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

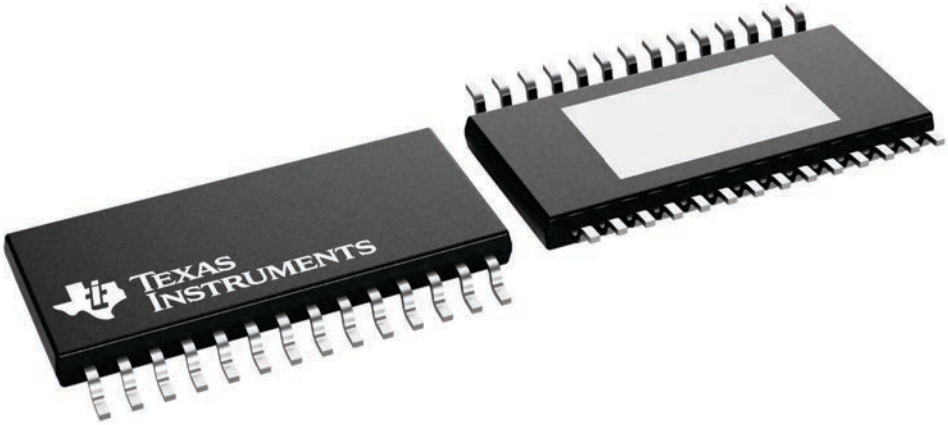
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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