

## SN65HVD888 具有 IEC-ESD 保护的总线极性校正 RS-485 收发器

### 1 特性

- 超出 EIA-485 标准要求
- 76ms ( $t_{FS}$ ) 内即可实现总线极性校准
- 数据速率: 300bps 至 250kbps
- 提供两种配置:
  - 只作为故障安全电阻器
  - 故障安全和差分端接电阻器
- 一条总线上多达 256 个节点 (1/8 单位负载)
- 小外形尺寸集成电路 (SOIC)-8 封装以实现向后兼容性
- 总线引脚保护:
  - $\pm 16\text{kV}$  的人体放电模式 (HBM) 保护
  - $\pm 12\text{kV}$  IEC61000-4-2 接触放电
  - $+4\text{kV}$  IEC61000-4-4 快速瞬态突发

### 2 应用

- 电子
- 工业自动化
- 加热, 通风和空调环境系统 (HVAC)
- DMX512 网络
- 过程控制
- 电池供电类应用
- 运动控制
- 电信设备

### 3 说明

SN65HVD888 是一款低功率 RS-485 转发器, 此转发器具有自动总线极性纠正和瞬态保护。热插拔时, 此器件在总线闲置的头 76ms 内检测并纠正总线极性。片载瞬态保护功能保护此器件不受 IEC61000 静电放电 (ESD) 和瞬态放电 (EFT) 瞬态的影响。该器件兼具驱动器和接收器功能, 稳健耐用, 可满足特定工业应用中的严格要求。这些总线引脚可耐受静电放电 (ESD) 事件, 具有对于人体放电模式 (HBM), 空气间隙放电和接触放电技术规范的高水平保护。

此器件将一个差分驱动器和一个差分接收器组合在一起, 这两个器件由一个 5V 单电源供电。驱动器差分输出和接收器差分输入在内部连接, 构成一个适用于半双工 (两线制总线) 通信的总线端口。该器件具有宽共模电压范围, 因此适用于长线缆上的多点应用。

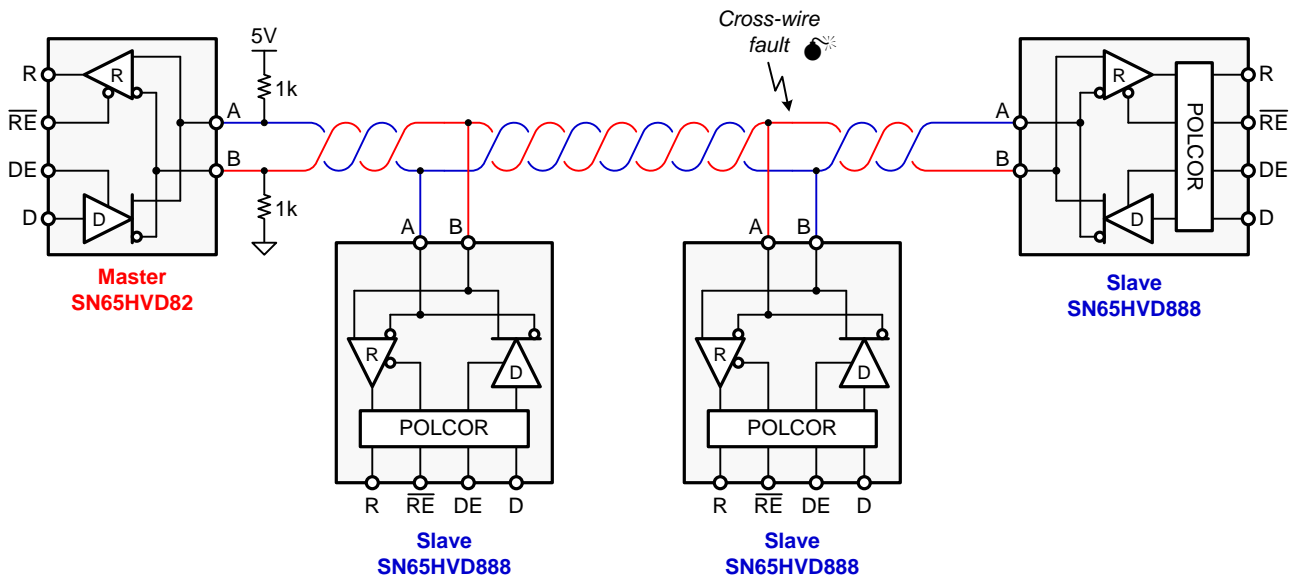
SN65HVD888 采用 SOIC-8 封装, 工作温度范围为  $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$ 。

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD888	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

#### 支持极性校正 (POLCOR) 的典型网络应用



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### 4 修订历史记录

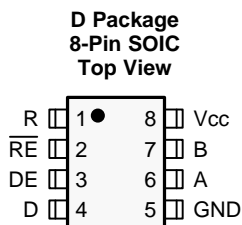
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (June 2017) to Revision C	Page
• Changed 3.3 V <sub>ISO</sub> To: 5 V <sub>ISO</sub> in <a href="#">Figure 24</a> .....	20

Changes from Revision A (September 2015) to Revision B	Page
• 将说明部分中的“工作温度范围为 -40°C 至 85°C”更改为“工作温度范围为 -40°C 至 125°C”说明中删除了锁定转子检测.....	1
• Changed the T <sub>A</sub> MAX value From: 85°C To: 125°C in the <i>Recommended Operating Conditions</i> table .....	4
• Changed I <sub>CC</sub> to show values for the temperature ranges of -40°C to 85°C and -40°C to 125°C in the <i>Electrical Characteristics</i> table .....	5

Changes from Original (July 2013) to Revision A	Page
• 已添加 引脚配置和功能部分, ESD 额定值表, 特性 描述 部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分 .....	1
• Changed JEDEC Standard 22, Test Method A114 (HBM) from ±4 to ±8 kV.....	3
• Changed JEDEC Standard 22, Test Method A115 (Machine Model) from ±100 to ±200 V. ....	3
• Changed the "D and $\overline{RE}$ Inputs" circuit and the "DE Input" circuit of <a href="#">Figure 15</a> .....	13

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V <sub>CC</sub>	8	Supply	4.5-V to 5.5-V supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

(see <sup>(1)</sup>)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
	Input voltage at any logic pin	-0.3	5.7	V
	Voltage input, transient pulse, A and B, through 100 Ω	-100	100	V
	Voltage at A or B inputs	-18	18	V
	Receiver output current	-24	24	mA
	Continuous total-power dissipation	See ( <a href="#">Thermal Information</a> ) table		
T <sub>J</sub>	Junction temperature		170	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings: JEDEC Specifications

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	
		Machine model (MM)	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings: IEC Specifications

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±12000
		IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND	±4000
		IEC 60749-26 ESD (HBM), bus terminals and GND	±16000

### 6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>ID</sub>	Differential input voltage	–12		12	V
V <sub>I</sub>	Input voltage at any bus terminal (separate or common mode) <sup>(1)</sup>	–7		12	V
V <sub>IH</sub>	High-level input voltage (driver, driver-enable, and receiver-enable inputs)	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)	0		0.8	V
I <sub>O</sub>	Output current	Driver		60	mA
		Receiver	–8	8	
C <sub>L</sub>	Differential load capacitance		50		pF
R <sub>L</sub>	Differential load resistance		60		Ω
1/t <sub>UI</sub>	Signaling rate	0.3		250	kbps
T <sub>J</sub>	Junction temperature	–40		150	°C
T <sub>A</sub> <sup>(2)</sup>	Operating free-air temperature (see <a href="#">Thermal Information</a> for additional information)	–40		125	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65HVD888	UNIT
		D (SOIC)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	116.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	60.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	57.1	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$ V_{OD} $	Driver differential-output voltage magnitude	RL = 60 $\Omega$ , 375 $\Omega$ on each output from -7 to +12 V	See Figure 4	1.5	2.5		V	
		RL = 54 $\Omega$ (RS-485)	See Figure 5	1.5	2.5			
		RL = 100 $\Omega$ (RS-422)		2	3			
$\Delta V_{OD} $	Change in magnitude of driver differential-output voltage	RL = 54 $\Omega$ , CL = 50 pF	See Figure 5	-0.2	0	0.2	V	
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27- $\Omega$ load resistors	See Figure 5	1	$V_{CC} / 2$	3	V	
$\Delta V_{OC}$	Change in differential driver common-mode output voltage	Center of two 27- $\Omega$ load resistors	See Figure 5	-0.2	0	0.2	mV	
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27- $\Omega$ load resistors	See Figure 5		850		mV	
$C_{OD}$	Differential output capacitance				8		pF	
$V_{IT+}$	Positive-going receiver differential-input voltage threshold				35	100	mV	
$V_{IT-}$	Negative-going receiver differential-input voltage threshold			-100	-35		mV	
$V_{HYS}^{(1)}$	Receiver differential-input voltage threshold hysteresis ( $V_{IT+} - V_{IT-}$ )			40	60		mV	
$V_{OH}$	Receiver high-level output voltage	$I_{OH} = -8$ mA		2.4	$V_{CC} - 0.3$		V	
$V_{OL}$	Receiver low-level output voltage	$I_{OL} = 8$ mA			0.2	0.4	V	
$I_i$	Driver input, driver enable, and receiver enable input current			-2		2	$\mu$ A	
$I_{OZ}$	Receiver high-impedance output current	$V_O = 0$ V or $V_{CC}$ , $\overline{RE}$ at $V_{CC}$		-10		10	$\mu$ A	
$ I_{OS} $	Driver short-circuit output current	$ I_{OS} $ with $V_A$ or $V_B$ from -7 to +12 V				150	mA	
$I_i$	Bus input current (driver disabled)	$V_{CC} = 4.5$ to $5.5$ V or	$V_i = 12$ V		75	125	$\mu$ A	
		$V_{CC} = 0$ V, DE at 0 V	$V_i = -7$ V	-100	-40			
$I_{CC}$	Supply current (quiescent) -40°C to 85°C	Driver and receiver enabled	DE = $V_{CC}$ , $\overline{RE} = GND$ , No load		750	900	$\mu$ A	
		Driver enabled, receiver disabled	DE = $V_{CC}$ , $\overline{RE} = V_{CC}$ , No load			650		
		Driver disabled, receiver enabled	DE = GND, $\overline{RE} = GND$ , No load					750
		Driver and receiver disabled	DE = GND, D = GND $\overline{RE} = V_{CC}$ , No load		0.4	5		
$I_{CC}$	Supply current (quiescent) -40°C to 125°C	Driver and receiver enabled	DE = $V_{CC}$ , $\overline{RE} = GND$ , No load		750	990	$\mu$ A	
		Driver enabled, receiver disabled	DE = $V_{CC}$ , $\overline{RE} = V_{CC}$ , No load			715		
		Driver disabled, receiver enabled	DE = GND, $\overline{RE} = GND$ , No load					825
Supply current (dynamic)		See Figure 3						

(1) Under any specific conditions,  $V_{IT+}$  is specified to be at least  $V_{HYS}$  higher than  $V_{IT-}$ .

## 6.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
PD	Power Dissipation driver and receiver enabled, $V_{CC} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ 50% duty cycle square-wave signal at 250 kbps signaling rate:	Unterminated	$R_L = 300\ \Omega$ , $C_L = 50\text{ pF}$ (driver)	164	mW
		RS-422 load	$R_L = 100\ \Omega$ , $C_L = 50\text{ pF}$ (driver)	247	
		RS-485 load	$R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ (driver)	316	

## 6.8 Switching Characteristics

 3.3 ms > bit time > 4  $\mu\text{s}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>DRIVER</b>							
$t_r$ , $t_f$	Driver differential-output rise and fall times	$R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$	See <a href="#">Figure 6</a>	400	700	1200	ns
$t_{PHL}$ , $t_{PLH}$	Driver propagation delay	$R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$	See <a href="#">Figure 6</a>	90	700	1000	ns
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL} - t_{PLH} $	$R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$	See <a href="#">Figure 6</a>		25	200	ns
$t_{PHZ}$ , $t_{PLZ}$	Driver disable time		See <a href="#">Figure 7</a> and <a href="#">Figure 8</a>		50	500	ns
$t_{PHZ}$ , $t_{PLZ}$	Driver enable time	Receiver enabled	See <a href="#">Figure 7</a> and <a href="#">Figure 8</a>		500	1000	ns
		Receiver disabled	See <a href="#">Figure 7</a> and <a href="#">Figure 8</a>		3	9	$\mu\text{s}$
<b>RECEIVER</b>							
$t_r$ , $t_f$	Receiver output rise and fall times	$C_L = 15\text{ pF}$	See <a href="#">Figure 9</a>		18	30	ns
$t_{PHL}$ , $t_{PLH}$	Receiver propagation delay time	$C_L = 15\text{ pF}$	See <a href="#">Figure 9</a>		85	195	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $	$C_L = 15\text{ pF}$	See <a href="#">Figure 9</a>		1	15	ns
$t_{PHZ}$ , $t_{PLZ}$	Receiver disable time				50	500	
$t_{PZL(1)}$ , $t_{PZH(1)}$ , $t_{PZL(2)}$ , $t_{PZH(2)}$	Receiver enable time	Driver enabled	See <a href="#">Figure 10</a>		20	130	ns
		Driver disabled	See <a href="#">Figure 11</a>		2	8	$\mu\text{s}$
$t_{FS}$	Bus failsafe time	Driver disabled	See <a href="#">Figure 12</a>	44	58	76	ms

### 6.9 Typical Characteristics

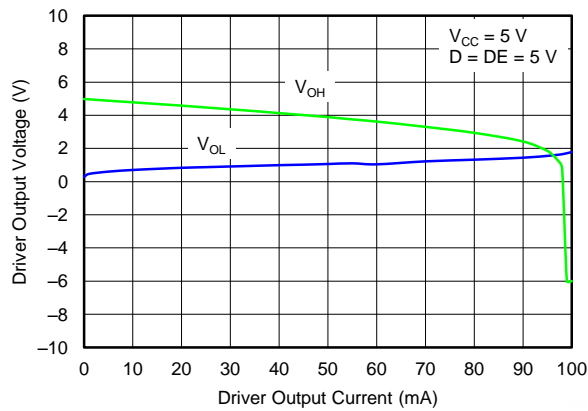


Figure 1. Driver Output Voltage vs Driver Output Current

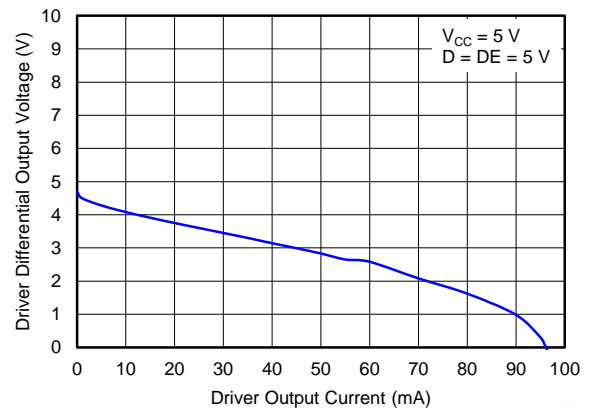


Figure 2. Driver Differential Output Voltage vs Driver Output Current

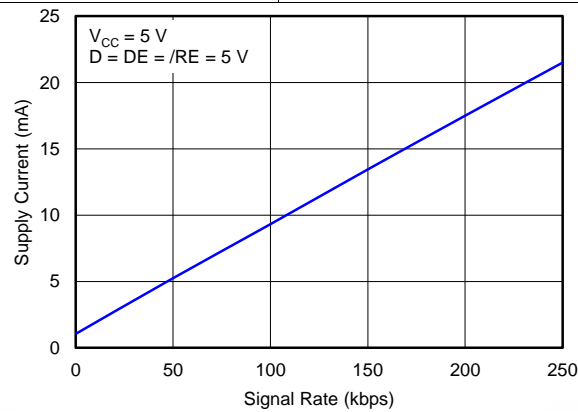


Figure 3. Supply Current vs Signaling Rate

## 7 Parameter Measurement information

### 7.1 Driver

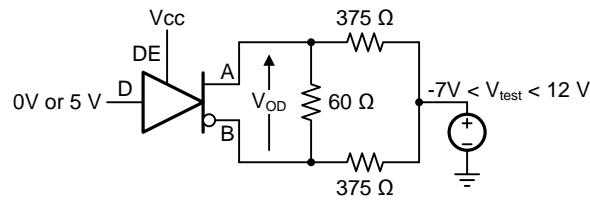


Figure 4. Measurement of Driver Differential-Output Voltage With Common-Mode Load

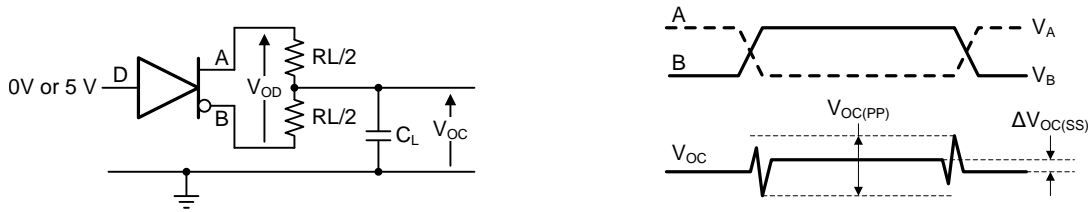


Figure 5. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

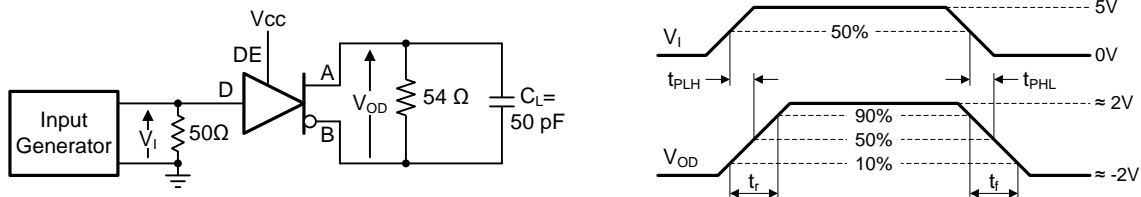


Figure 6. Measurement of Driver Differential-Output Rise and Fall Times and Propagation Delays

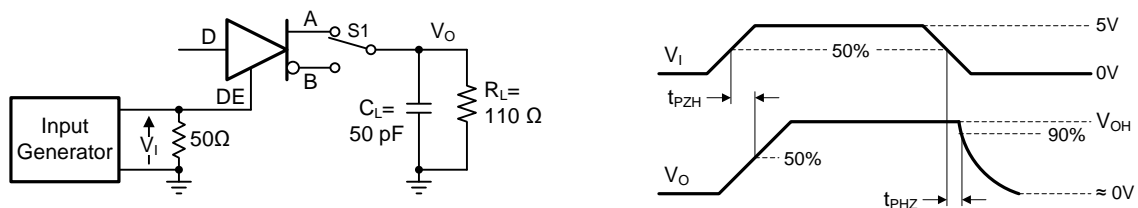


Figure 7. Measurement of Driver Enable and Disable Times With Active-High Output and Pull-Down Load

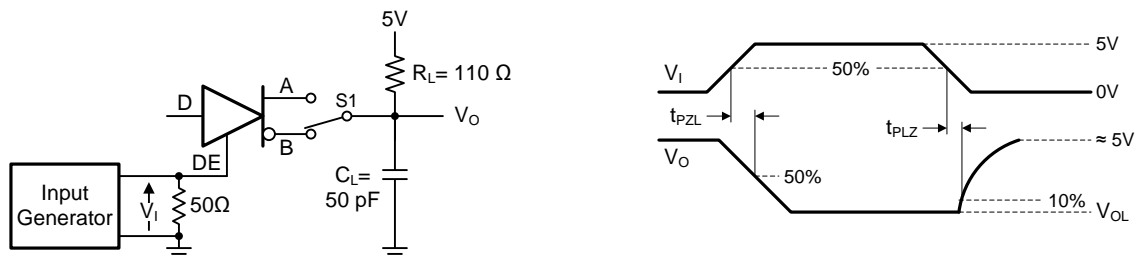


Figure 8. Measurement of Driver Enable and Disable Times With Active-Low Output and Pull-up Load



7.2 Receiver

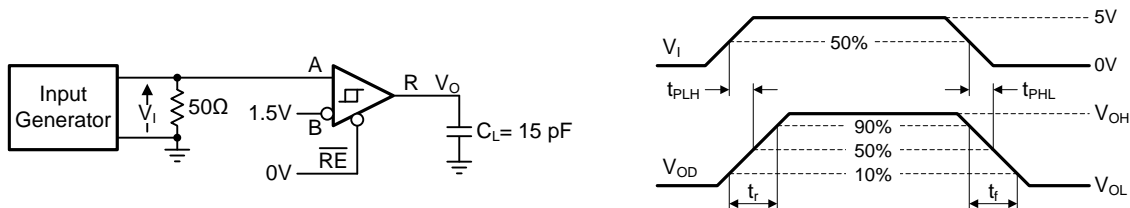


Figure 9. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

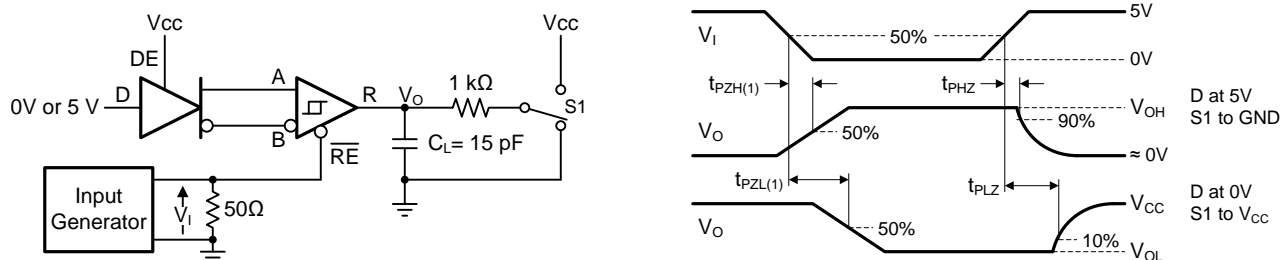


Figure 10. Measurement of Receiver Enable and Disable Times With Driver Enabled

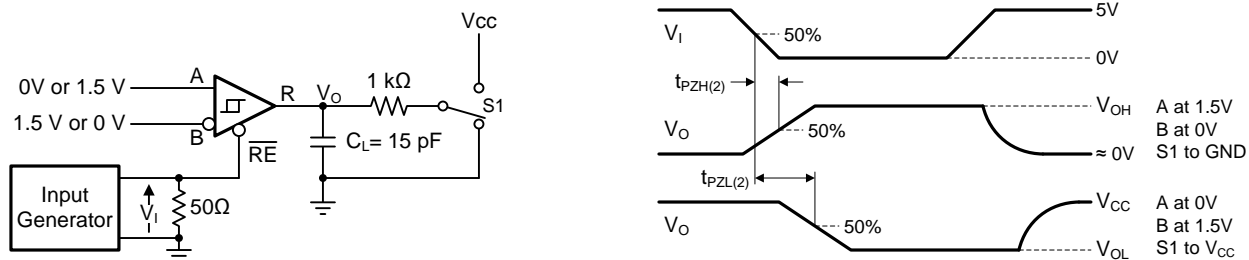


Figure 11. Measurement of Receiver Enable Times With Driver Disabled

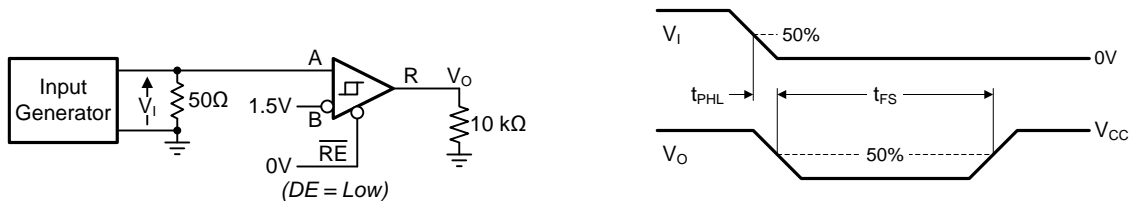


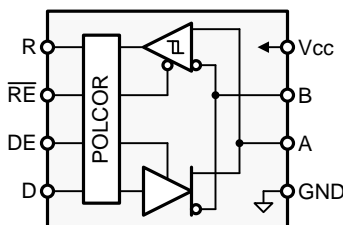
Figure 12. Measurement of Receiver Polarity-Correction Time With Driver Disabled

## 8 Detailed Description

### 8.1 Overview

The SN65HVD888 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 250 kbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand up ESD strikes up to 12 kV (per IEC 61000-4-2) and EFT transients up to 4 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of SN65HVD888 may share a common RS-485 bus due to the device's low bus input currents. The device features automatic polarity correction, which detects bus mis-wirings at start-up and then swaps the *A* and *B* halves of the bus if needed.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

#### 8.3.1 Low-Power Standby Mode

When the driver and the receiver are both disabled ( $DE = Low$  and  $RE = High$ ) the device enters standby mode. If the enable inputs are in the disabled state for only a brief time (for example: less than 100 ns), the device does not enter standby mode, preventing the SN65HVD888 from entering standby mode during driver or receiver enabling. Only when the enable inputs are held in the disabled state for a duration of 300 ns or more does the device enter low-power standby mode. In this mode most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active. During  $V_{CC}$  power-up, when the device is set for both driver and receiver disabled mode, the device may consume more than 5- $\mu A$  of  $I_{CC}$  disabled current because of capacitance charging effects. This condition occurs only during  $V_{CC}$  power up.

#### 8.3.2 Bus Polarity Correction

The SN65HVD888 automatically corrects a wrong bus-signal polarity caused by a cross-wire fault. In order to detect the bus polarity, all three of the following conditions must be met:

- A failsafe-biasing network (commonly at the master node) must define the signal polarity of the bus
- A slave node must enable the receiver and disable the driver ( $\overline{RE} = DE = Low$ )
- The bus must idle for the failsafe time,  $t_{FS-max}$

After the failsafe time has passed, the polarity correction is complete and is applied to both the receive and transmit channels. The status of the bus polarity is latched within the transceiver and is maintained for subsequent data transmissions.

#### NOTE

Data string durations of consecutive 0s or 1s exceeding  $t_{FS-min}$  can accidentally trigger a wrong polarity correction and must be avoided.

Figure 13 shows a simple point-to-point data link between a master node and a slave node. Because the master node with the failsafe biasing network determines the signal polarity on the bus, an RS-485 transceiver without polarity correction, such as SN65HVD82, suffices. All other bus nodes, typically performing as slaves, require the SN65HVD888 transceiver with polarity correction.

Feature Description (continued)

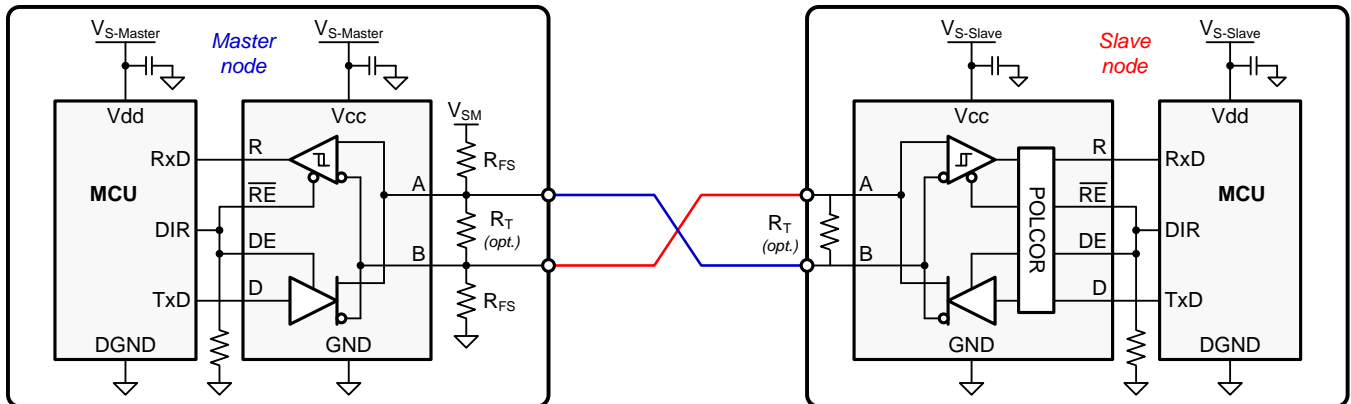


Figure 13. Point-To-Point Data Link With Cross-Wire Fault

Prior to initiating data transmission the master transceiver must idle for a time span that exceeds the maximum failsafe time,  $t_{FS-max}$ , of a slave transceiver. This idle time is accomplished by driving the direction control line, DIR, low. After a time,  $t > t_{FS-max}$ , the master begins transmitting data.

Because of the indicated cross-wire fault between master and slave, the slave node receives bus signals with reversed polarity. Assuming the slave node has just been connected to the bus, the direction-control pin is pulled-down during power-up and then is actively driven low by the slave MCU. The polarity correction begins as soon as the slave supply is established and ends after approximately 44 to 76 ms.

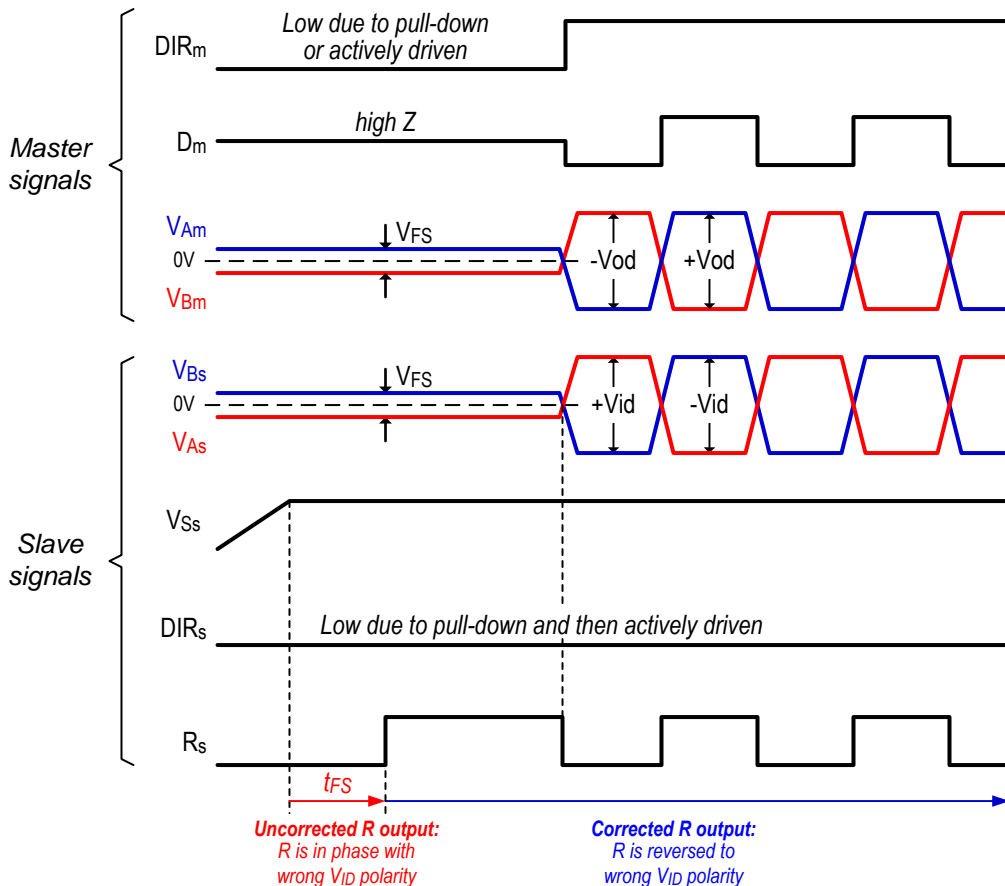


Figure 14. Polarity Correction Timing Prior to a Data Transmission

## Feature Description (continued)

Initially the slave receiver assumes that the correct bus polarity is applied to the inputs and performs no polarity reversal. Because of the reversed polarity of the bus-failsafe voltage, the output of the slave receiver,  $R_S$ , turns low. After  $t_{FS}$  has passed and the receiver has detected the wrong bus polarity, the internal POLCOR logic reverses the input signal and  $R_S$  turns high.

At this point all incoming bus data with reversed polarity are polarity corrected within the transceiver. Because polarity correction is also applied to the transmit path, the data sent by the slave MCU are reversed by the POLCOR logic and then fed into the driver.

The reversed data from the slave MCU are reversed again by the cross-wire fault in the bus, and the correct bus polarity is reestablished at the master end.

This process repeats each time the device powers up and detects an incorrect bus polarity.

## 8.4 Device Functional Modes

**Table 1. Driver Pin Functions**

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
<b>NORMAL MODE</b>				
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus High
<b>POLARITY-CORRECTING MODE<sup>(1)</sup></b>				
H	H	L	H	Actively drives bus Low
L	H	H	L	Actively drives bus High
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus Low

(1) The polarity-correcting mode is entered when  $V_{ID} < V_{IT-}$  and  $t > t_{FS}$  and  $DE = \text{low}$ . This state is latched when  $\overline{RE}$  turns from Low to High.

**Table 2. Receiver Pin Functions**

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
<b>NORMAL MODE</b>			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state
<b>POLARITY-CORRECTING MODE<sup>(1)</sup></b>			
$V_{IT+} < V_{ID}$	L	L	Receive valid bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	H	Receive polarity corrected bus High
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	?	Indeterminate bus state

(1) The polarity-correcting mode is entered when  $V_{ID} < V_{IT-}$  and  $t > t_{FS}$  and  $DE = \text{low}$ . This state is latched when  $\overline{RE}$  turns from Low to High.

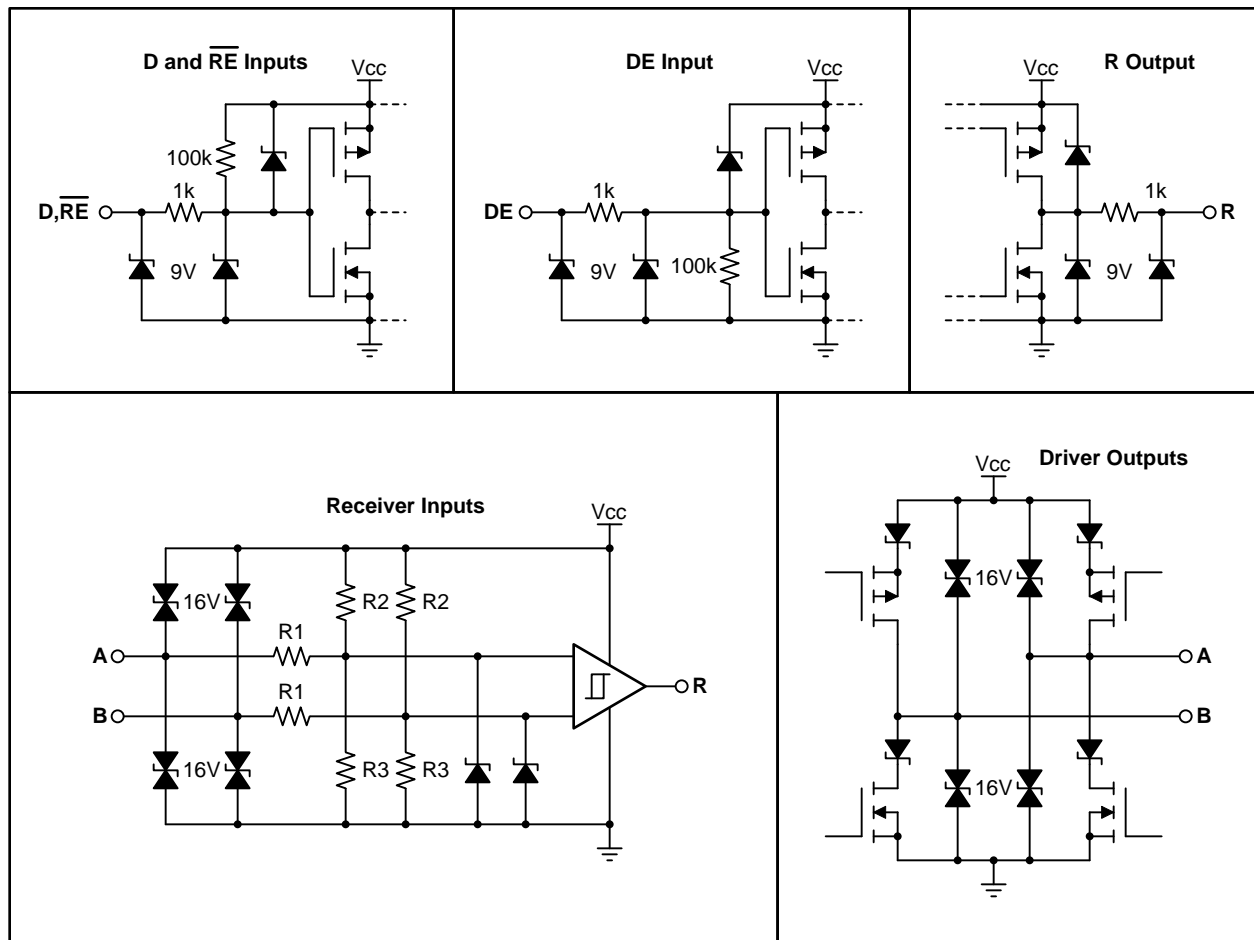


Figure 15. Equivalent Input and Output Schematic Diagrams

## 9 Application and Implementation

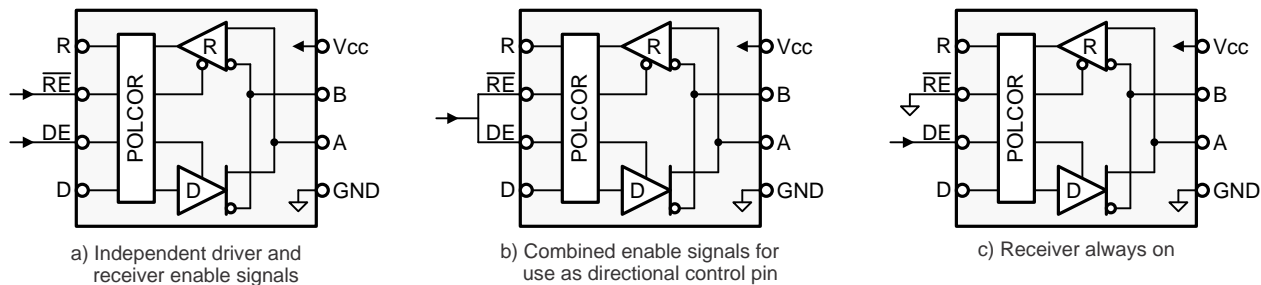
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Device Configuration

The SN65HVD888 is a half-duplex RS-485 transceiver operating from a single 5-V  $\pm 10\%$  supply. The driver and receiver enable pins allow for the configuration of different operating modes.



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**Figure 16. Transceiver Configurations**

Using independent enable lines provides the most flexible control as the lines allow for the driver and the receiver to be turned on and turned off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not. Only this configuration allows the SN65HVD888 to enter low-power standby mode because it allows both the driver and receiver to be disabled simultaneously.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver enable to ground and controlling only the driver-enable input also uses only one control line. In this configuration a node not only receives the data on the bus sent by other nodes but also receives the data sent on the bus, enabling the node to verify the correct data has been transmitted.

#### 9.1.2 Bus Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with  $Z_0 = 100 \Omega$ , and RS-485 cable with  $Z_0 = 120 \Omega$ . Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

Application Information (continued)

Table 3. VID with a Failsafe Network and Bus Termination

V <sub>CC</sub>	R <sub>L</sub> DIFFERENTIAL TERMINATION	R <sub>FS</sub> PULLUP	R <sub>FS</sub> PULLDOWN	V <sub>ID</sub>
5 V	54 Ω	560 Ω	560 Ω	230 mV
		1 KΩ	1 KΩ	131 mV
		4.7 KΩ	4.7 KΩ	29 mV
		10 KΩ	10 KΩ	13 mV

An external failsafe-resistor network must be used to ensure failsafe operation during an idle bus state. When the bus is not actively driven, the differential receiver inputs could float allowing the receiver output to assume a random output. A proper failsafe network forces the receiver inputs to exceed the V<sub>IT</sub> threshold, thus forcing the SN65HVD888 receiver output into the failsafe (high) state. Table 3 shows the differential input voltage (V<sub>ID</sub>) for various failsafe networks with a 54-Ω differential bus termination.

9.1.3 Cable Length Versus Data Rate

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

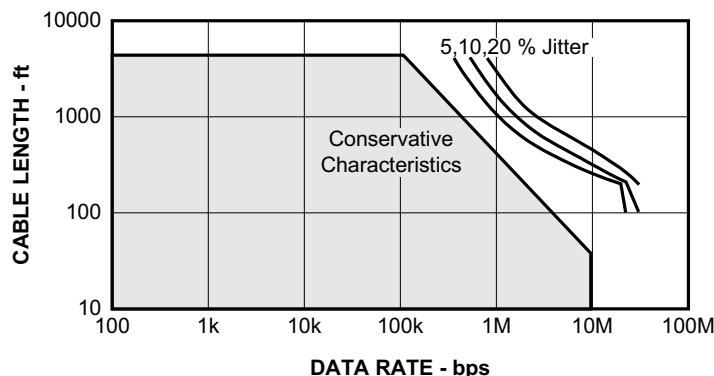


Figure 17. Cable Length vs Data Rate Characteristic

9.1.4 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for the short distance is because a stub presents a non-terminated piece of bus line which can introduce reflections if the distance is too long. As a general guideline, the electrical length or round-trip delay of a stub should be less than one-tenth of the rise time of the driver, thus leading to a maximum physical stub length of as shown in Equation 1.

$$L_{\text{Stub}} \leq 0.1 \times t_r \times v \times c$$

where

- t<sub>r</sub> is the 10/90 rise time of the driver
- c is the speed of light (3 × 10<sup>8</sup> m/s or 9.8 × 10<sup>8</sup> ft/s)
- v is the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of c

Based on Equation 1, with a minimum rise time of 400 ns, Equation 2 shows the maximum cable-stub length of the SN65HVD888.

$$L_{\text{Stub}} \leq 0.1 \times 400 \times 10^{-9} \times 3 \times 10^8 \times 0.78 = 9.4 \text{ m (or 30.6 ft)}$$

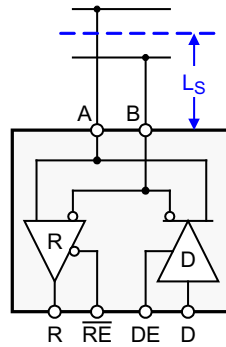


Figure 18. Stub Length

9.1.5 3- to 5-V Interface

Interfacing the SN65HVD888 to a 3-V controller is easy. Because the 5-V logic inputs of the transceiver accept 3-V input signals they can be directly connected to the controller I/O. The 5-V receiver output, R, however must be level-shifted by a Schottky diode and a 10-k resistor to connect to the controller input (see Figure 19). When R is high, the diode is reverse biased and the controller supply potential lies at the controller RxD input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2 V lies at the controller RxD input.

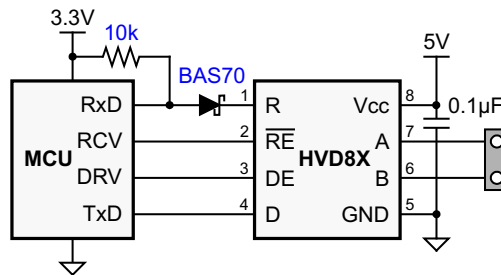


Figure 19. 3-V to 5-V Interface

9.1.6 Noise Immunity

The input sensitivity of a standard RS-485 transceiver is  $\pm 200$  mV. When the differential input voltage,  $V_{ID}$ , is greater than +200 mV, the receiver output turns high, for  $V_{ID} < -200$  mV the receiver outputs low.

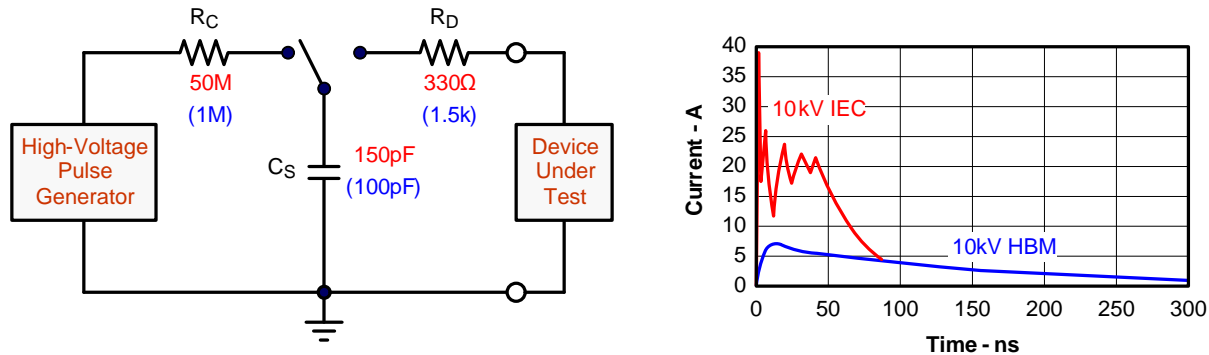
The SN65HVD888 transceiver implements high receiver noise-immunity by providing a typical positive-going input threshold of 35 mV and a minimum hysteresis of 40 mV. In the case of a noisy input condition therefore, a differential noise voltage of up to 40 mV<sub>pp</sub> can be present without causing the receiver output to change states from high to low.

9.1.7 Transient Protection

The bus terminals of the SN65HVD888 transceiver family possess on-chip ESD protection against  $\pm 16$  kV HBM and  $\pm 12$  kV IEC61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance,  $C_S$ , and 78% lower discharge resistance,  $R_D$  of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.





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**Figure 20. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)**

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients. Figure 12 suggests two circuit designs providing protection against short and long duration surge transients, in addition to ESD and Electrical Fast Transients (EFT) transients. Table 4 lists the bill of materials for the external protection devices.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 21 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. In the diagram on the left of Figure 21, the tiny blue blip in the bottom left corner represents the power of a 10-kV ESD transient, which already dwarfs against the significantly higher EFT power spike, and certainly dwarfs against the 500-V surge transient. This type of transient power is well representative of factory environments in industrial and process automation. The diagram on the right of Figure 21 compares the enormous power of a 6-kV surge transient, most likely occurring in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient.

**NOTE**

The unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost dropping off the scale.

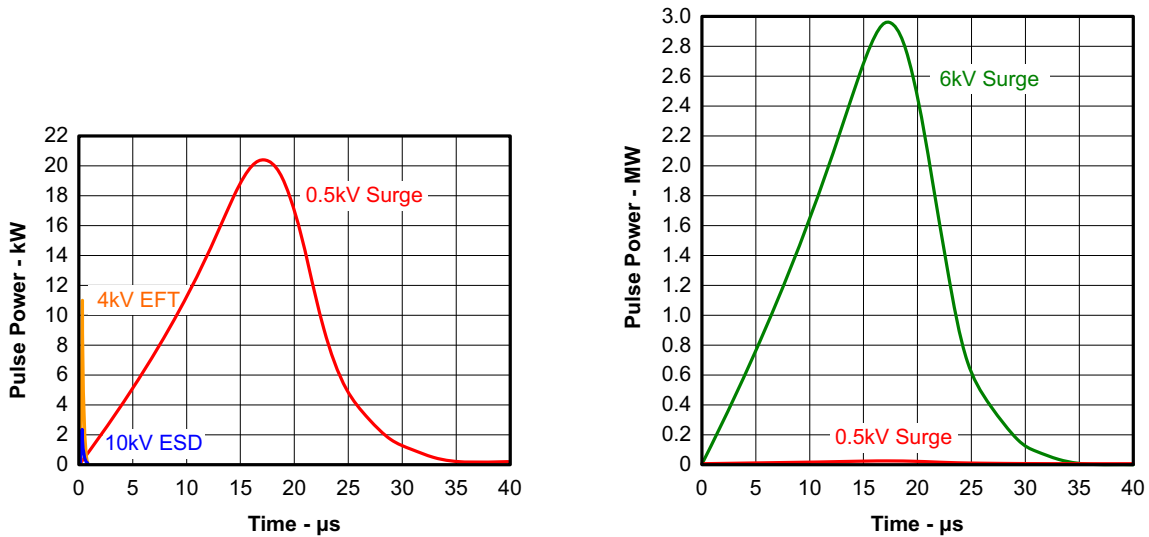


Figure 21. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is signified by long pulse duration and slow decaying pulse power

The electrical energy of a transient that is dumped into the internal protection cells of the transceiver is converted into thermal energy. This thermal energy heats the protection cells and literally destroys them, thus destroying the transceiver. Figure 22 shows the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

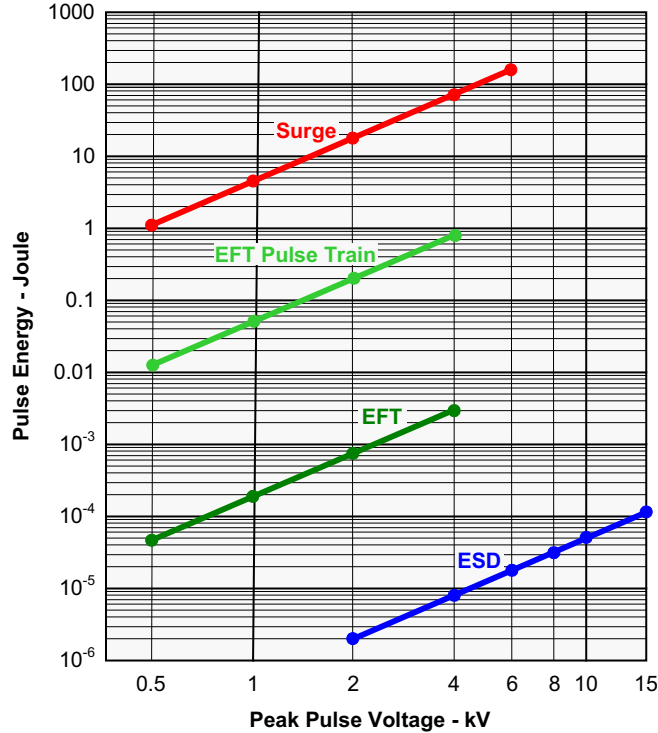
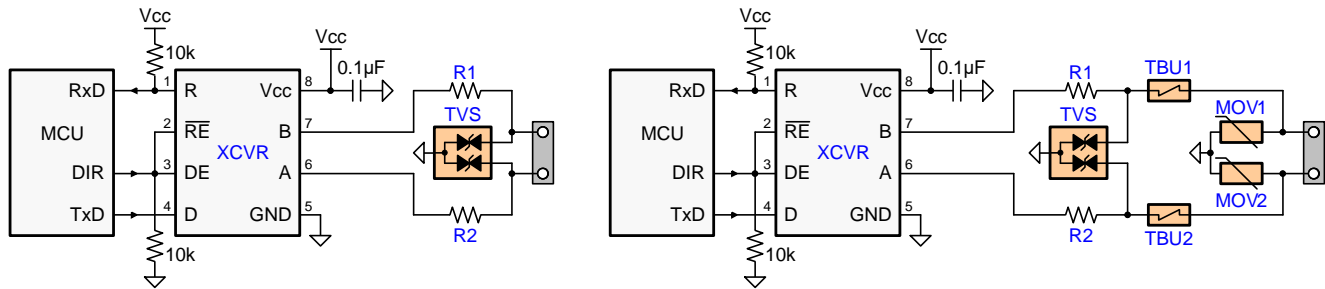


Figure 22. Comparison of Transient Energies

**Table 4. Bill of Materials**

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, 250-kbps RS-485 Transceiver	SN65HVD888	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional.	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200mA Transient Blocking Unit 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns



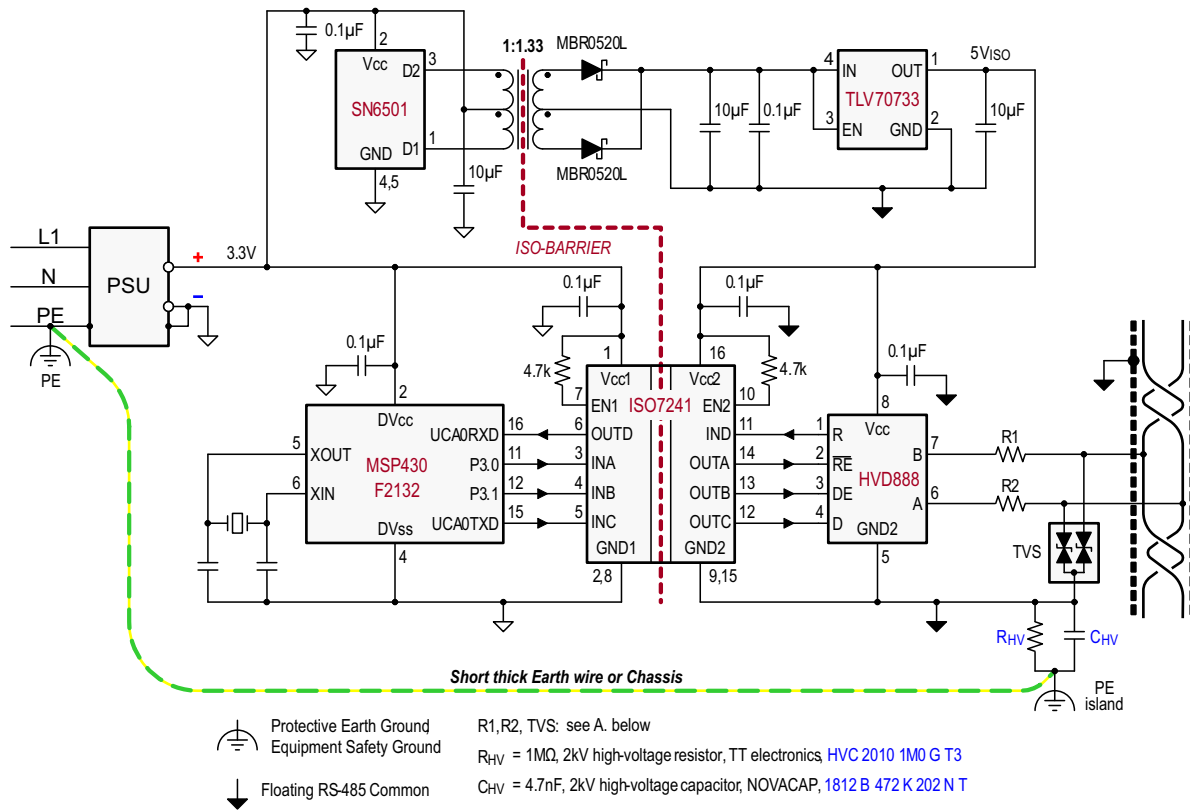
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**Figure 23. Transient Protections Against ESD, EFT, and Surge Transients**

The left circuit shown in [Figure 23](#) provides surge protection of  $\geq 500\text{-V}$  transients, while the right protection circuits can withstand surge transients of 5 kV.

## 9.2 Typical Application

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver through a multi-channel, digital isolator (Figure 24).



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A. See Table 4.

**Figure 24. Isolated Bus Node With Transient Protection**

### 9.2.1 Design Requirements

Example Application: Isolated Bus Node with Transient Protection

- RS-485-compliant bus interface (needs differential signal amplitude of at least 1.5 V under fully-loaded conditions – essentially, maximum number of nodes connected and with dual 120-Ω termination).
- Galvanic isolation of both signal and power supply lines.
- Able to withstand ESD transients up to 12 kV (per IEC 61000-4-2) and EFTs up to 4 kV (per IEC 61000-4-4).
- Full control of data flow on bus in order to prevent contention (for half-duplex communication).

### 9.2.2 Detailed Design Procedure

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-kΩ resistors to limit input currents during transient events.

While the transient protection is similar to the one in Figure 23 (left circuit), an additional high-voltage capacitor diverts transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This diversion is necessary as noise transients on the bus are usually referred to Earth potential.

R<sub>VH</sub> refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

### Typical Application (continued)

Occasionally varistors are used instead of resistors in order to rapidly discharge  $C_{HV}$ , if expected that fast transients might charge  $C_{HV}$  to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components,  $C_{HV}$  and  $R_{HV}$ , are connecting to the chassis at the other end.

### 9.2.3 Application Curve

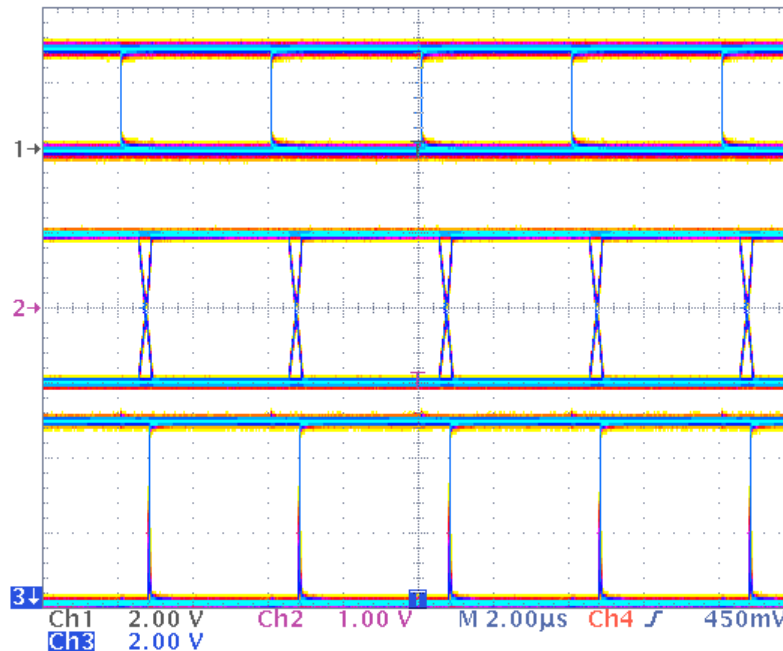


Figure 25. SN65HVD888 D Input (Top), Differential Output (Middle), and R Output (Bottom), 250 kbps Operation, PRBS Data Pattern

## 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

## 11 Layout

### 11.1 Layout Guidelines

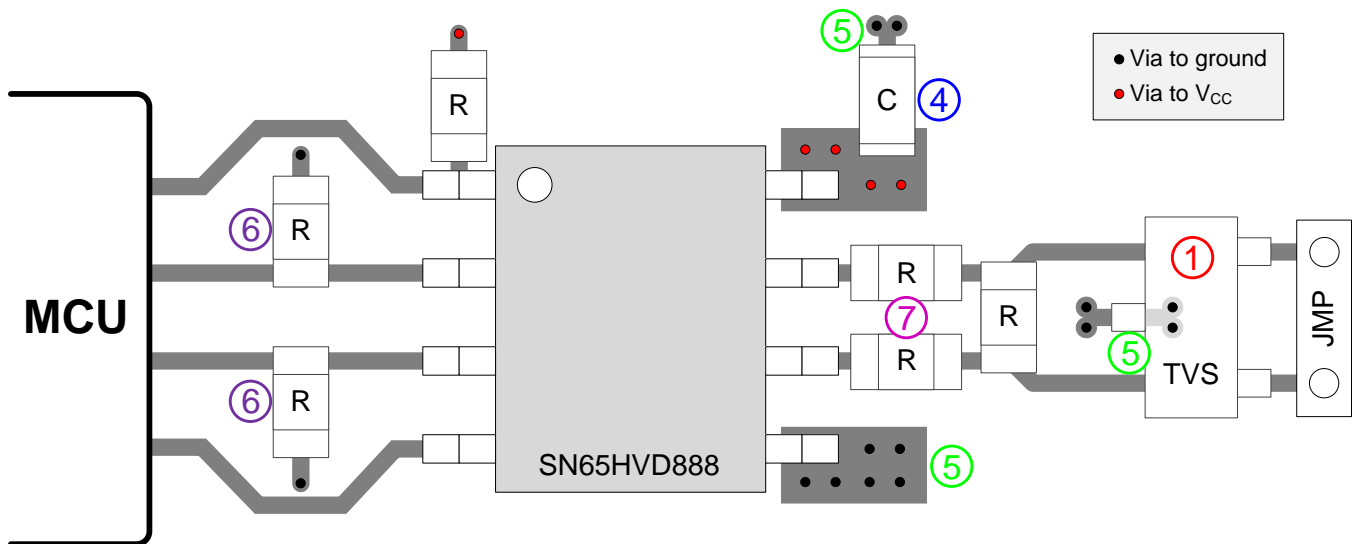
#### 11.1.1 Design and Layout Considerations For Transient Protection

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for PCB design to be successful, begin with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use  $V_{CC}$  and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100- to 220-nF bypass capacitors as close as possible to the  $V_{CC}$ -pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for  $V_{CC}$  and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1- to 10-k pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
  - While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few-hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

#### 11.2 Layout Example



**Figure 26. SN65HVD888 Layout Example**

## 12 器件和文档支持

### 12.1 器件支持

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### 12.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65HVD888D</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
SN65HVD888D.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
SN65HVD888D.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
<a href="#">SN65HVD888DR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
SN65HVD888DR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888
SN65HVD888DR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD888

**(1) Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD888DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD888DR	SOIC	D	8	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65HVD888D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD888D.A	D	SOIC	8	75	507	8	3940	4.32
SN65HVD888D.B	D	SOIC	8	75	507	8	3940	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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