SN65HVD178x-Q1 具有故障保护功能和 3.3V 至 5V 工作电压的 RS-485 收发器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性
  - 器件温度等级 1：
    - –40°C 至 125℃ 环境工作温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESG 分类等级 C3B
- 总线引脚故障保护：
  - > ±70V ('HVD1780-Q1、'HVD1781-Q1)
  - > ±30V ('HVD1782-Q1)
- 工作电源电压范围为 3.3V 至 5V
- 总线引脚上提供 ±16kV HBM 保护
- 减少高达 320 个节点的单位负载
- 针对开路、短路和空闲总线情况的失效防护接收器
- 低功耗
  - 低待机电源电流 (最大值为 1 µ A)
  - 运行期间 I_{CC} 静态电流为 4mA
- 与业界通用的 SN75176 引脚兼容
- 115kbps、1Mbps 以及高达 10Mbps 的信号传输速率

2 应用

汽车数据链路

3 说明

这些器件可在遇到过压故障 (例如电源直接短路、误接线故障、连接器故障、电缆挤压以及工具误用) 时免受损坏。它们还具有高级的人体放电模型保护规格，在静电放电 (ESD) 事件发生时依然可保持稳定。

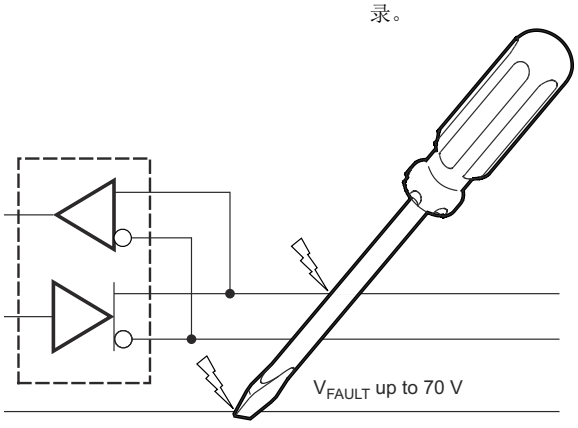
这些器件将一个差分驱动器和一个差分接收器组合在一起，这两个器件由一个单电源供电。在 'HVD1782 中，驱动器差分输出和接收器差分输入在内部进行连接，形成适用于半双工 (双线总线) 通信的总线端口。此端口具有宽共模电压范围，使得这些器件适合于长线缆上的多点应用。这些器件的额定工作温度范围为 -40°C 至 125°C。这些器件与业界通用的 SN75176 收发器引脚兼容，适合在大多数系统中直接用作升级替代器件。

这些器件采用 5V 电源，完全符合 ANSI TIA/EIA 485A 标准，并且可以使用 3.3V 电源运行，同时降低驱动器输出电压，以适用于低功耗应用。对于需要在扩展共模电压范围内运行的应用，请参阅 SN65HVD1785 (SLLS872) 数据表。

器件信息

器件型号	信号传输速率(1)	节点数量
SN65HVD1780-Q1	最高 115kbps	高达 320
SN65HVD1781-Q1	最高 1Mbps	高达 320
SN65HVD1782-Q1	最高 10Mbps	高达 64

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Pin Configuration and Functions

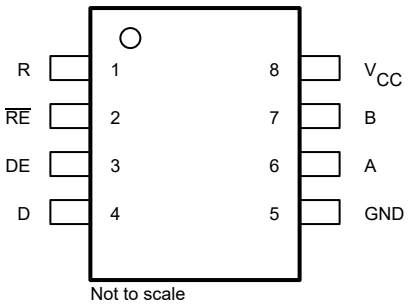


图 4-1. D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	3.15V to 5.5V supply

5 Specifications

5.1 Absolute Maximum Ratings

See Note (1).

				MIN	MAX	UNIT
V_{CC}	Supply voltage			–0.5	7	V
	Voltage range at bus pins	'HVD1780-Q1, 'HVD1781-Q1	A, B pins	–70	70	V
		'HVD1782-Q1	A, B pins	–70	30	
	Input voltage range at any logic pin			–0.3	V_{CC} + 0.3	V
	Transient overvoltage pulse through 100 Ω per TIA-485			–70	70	V
	Receiver output current			–24	24	mA
	Continuous total power dissipation			See *Power Dissipation Ratings*		
T_J	Junction temperature				170	°C
T_{stg}	Storage temperature			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings—AEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	Bus terminals and GND	±16000	V
			All pins	±4000	
		Charged-device model (CDM), per AEC Q100-011		±2000	
		Machine Model (MM), AEC-Q100-003		±400	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings—IEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per IEC 60749-26	Bus terminals and GND	±16000	V

5.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	SN65HVD1780-Q1			0.115	Mbps
		SN65HVD1781-Q1			1	
		SN65HVD1782-Q1			10	
T_A	Operating free-air temperature (See the *Thermal Information* table)	5V supply	–40		105	°C
		3.3V supply	–40		125	

5.4 Recommended Operating Conditions（续）

		MIN	NOM	MAX	UNIT
T_J	Junction Temperature	–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

5.5 Thermal Information

THERMAL METRIC(1)		SN65HVD1780-Q1 SN65HVD1781-Q1 SN65HVD1782-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC high-K model)	138	°C/W
	Junction-to-ambient thermal resistance (JEDIC low-K model)	242	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V, See 图 6-1	T_A < 85°C	1.5			V
			T_A < 125°C	1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V	T_A < 85°C	1.7	2		
			T_A < 125°C	1.5			
		R_L = 54 Ω, 3.15 V ≤ V_{CC} ≤ 3.45 V		0.8	1		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V	T_A < 85°C	2.2	2.5		
			T_A < 125°C	2			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω		–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage			1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See 图 6-2			500		mV
C_{OD}	Differential output capacitance				23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				–100	–35	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–180	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – V_{IT-})(1)			30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	T_A < 85°C		0.2	0.4	V
			T_A < 125°C			0.5	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current			–50		50	μA

5.6 Electrical Characteristics（续）

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	μA
I_{OS}	Driver short-circuit output current				–200		200	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V	HVD1780-Q1, HVD1781-Q1		75	100	μA
				HVD1782-Q1		400	500	
			V_I = –7 V	HVD1780-Q1, HVD1781-Q1	–60	–40		
				HVD1782-Q1	-400	-300		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load			4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load			3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4	
		Driver and receiver disabled, standby mode	DE = GND, D = open, RE = V_{CC}, no load, T_A < 85°C			0.15	1	μA
			DE = GND, D = open, RE = V_{CC}, no load, T_A < 125°C				12	
	Supply current (dynamic)	See the *Typical Characteristics* section						

(1) Specified by design. Not production tested.

5.7 Power Dissipation Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Power dissipation	V_{CC} = 3.6 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, unterminated(1)	75	mW
		V_{CC} = 3.6 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-422 load(1)	95	
		V_{CC} = 3.6 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-485 load(1)	115	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)	320	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
T_{SD}	Thermal-shutdown junction temperature		170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

5.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (SN65HVD1780)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See 图 6-3	3.15 V < V_{CC} < 3.45 V	0.4	1.4	1.8	µs
			3.15 V < V_{CC} < 5.5 V	0.4	1.7	2.6	µs
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See 图 6-3			0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See 图 6-3			20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See 图 6-4 and 图 6-5			0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See 图 6-4 and 图 6-5		0.2	3	µs
		Receiver disabled			3	12	
DRIVER (SN65HVD1781)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See 图 6-3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See 图 6-3				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See 图 6-3				25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See 图 6-4 and 图 6-5				3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See 图 6-4 and 图 6-5			300	ns
		Receiver disabled				10	µs
DRIVER (SN65HVD1782)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	All V_{CC} and Temp			50	ns
			V_{CC} > 4.5V and T < 105°C		16		
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See 图 6-3				55	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See 图 6-3				10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See 图 6-4 and 图 6-5				3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See 图 6-4 and 图 6-5			300	ns
		Receiver disabled				9	µs
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time (1)	C_L = 15 pF, See 图 6-6	All devices		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L = 15 pF, See 图 6-6	HVD1780-Q1, HVD1781-Q1		100	200	ns
			HVD1782-Q1			80	
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} - t_{PLH}\|$	C_L = 15 pF, See 图 6-6	HVD1780-Q1, HVD1781-Q1		6	20	ns
			HVD1782-Q1			5	
t_{PLZ}, t_{PHZ}	Receiver disable time (1)	Driver enabled, See 图 6-7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See 图 6-7			80	300	ns
		Driver disabled, See 图 6-8			3	9	µs

(1) Specified by design. Not production tested.

5.9 Package Dissipation Ratings

PACKAGE(1)	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING	T_A = 125°C RATING (3.3 V ONLY)
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW	180 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW	103 mW

(1) For the most current package and ordering information, see the *Mechanical, Packaging, and Orderable Information* section, or see the TI website at www.ti.com.

5.10 Typical Characteristics

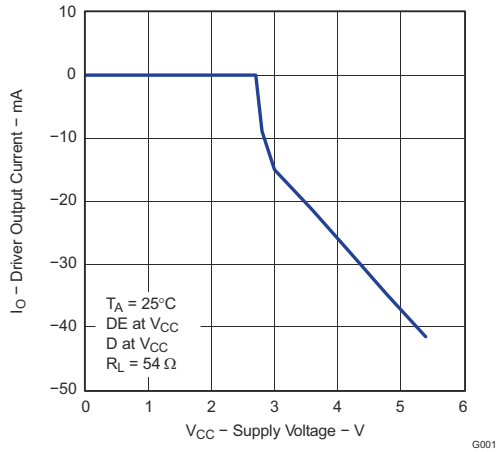


图 5-1. Driver Output Current vs Supply Voltage

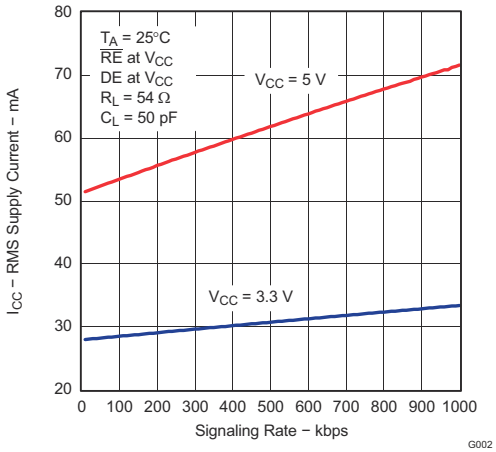


图 5-2. RMS Supply Current vs Signaling Rate

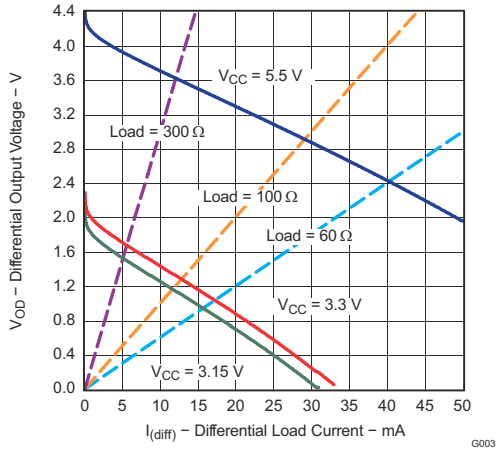


图 5-3. Differential Output Voltage vs Differential Load Current

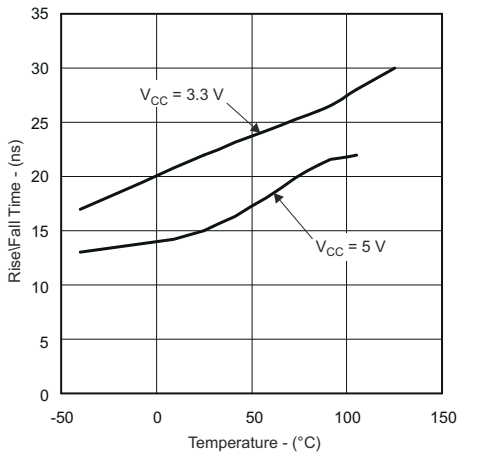


图 5-4. SN65HVD1782 Rise and Fall Time

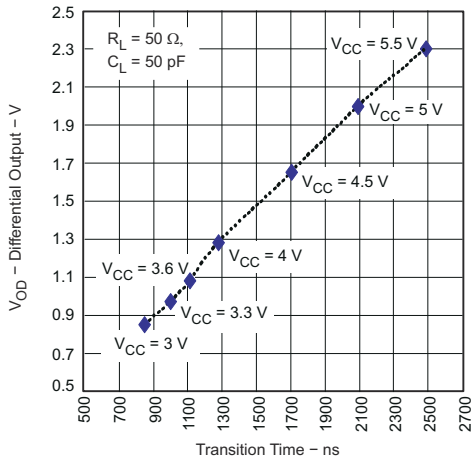


图 5-5. SN65HVD1780 Differential Output Amplitude and Transition Time vs Supply Voltage

6 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 ns, output impedance 50 Ω.

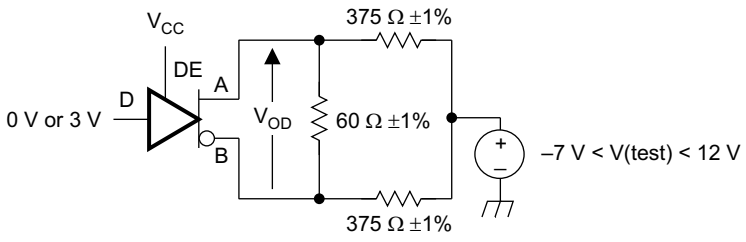
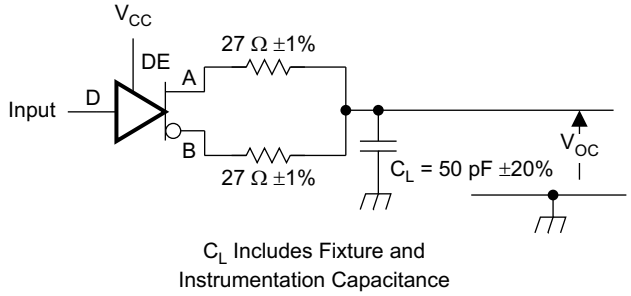


图 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load



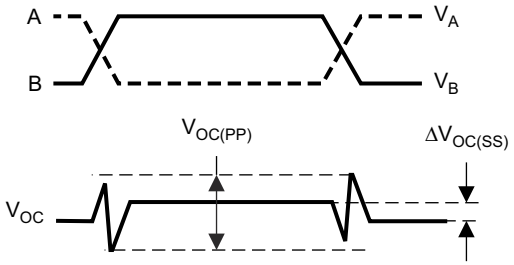
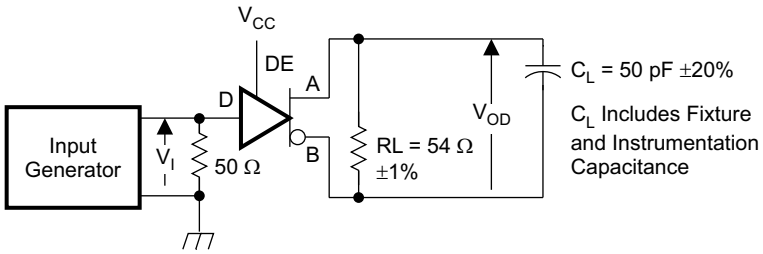


图 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



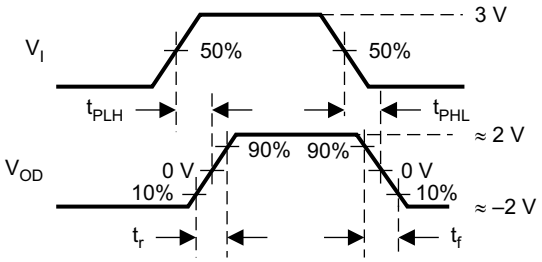
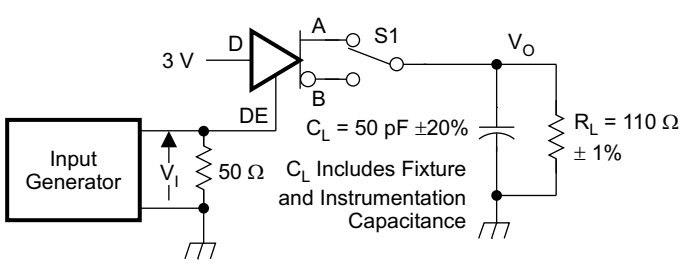
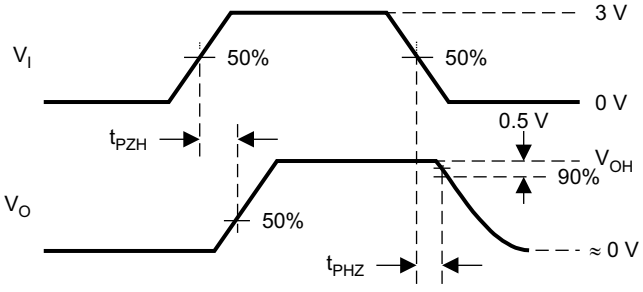


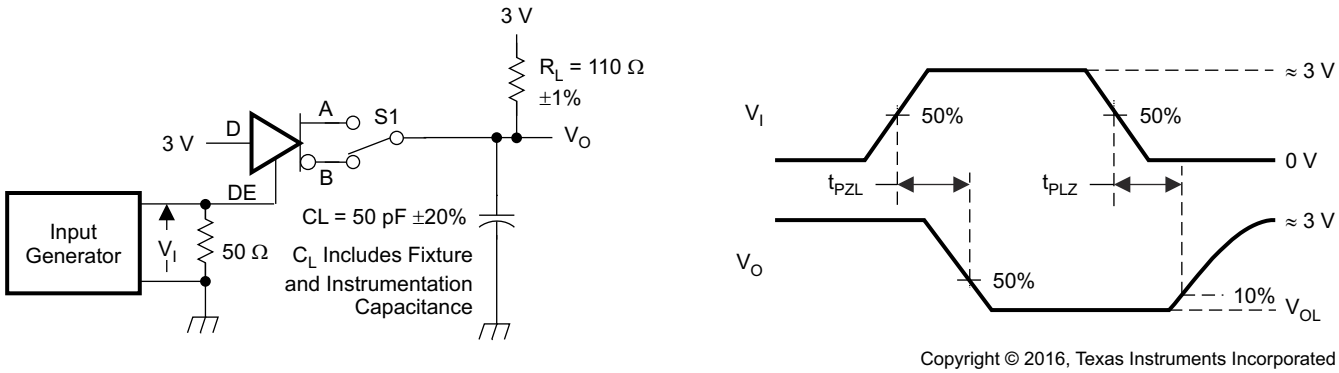
图 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays





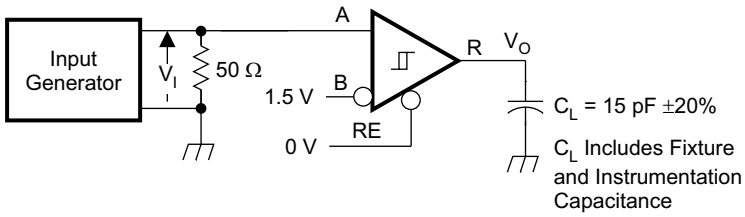
D at 3 V to test non-inverting output, D at 0 V to test inverting output.

图 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

图 6-5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load



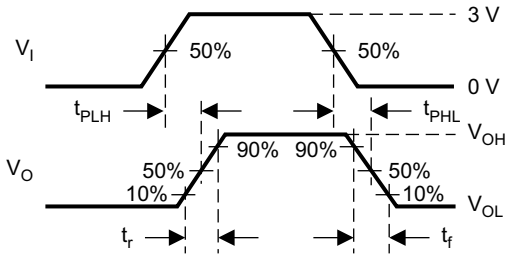


图 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

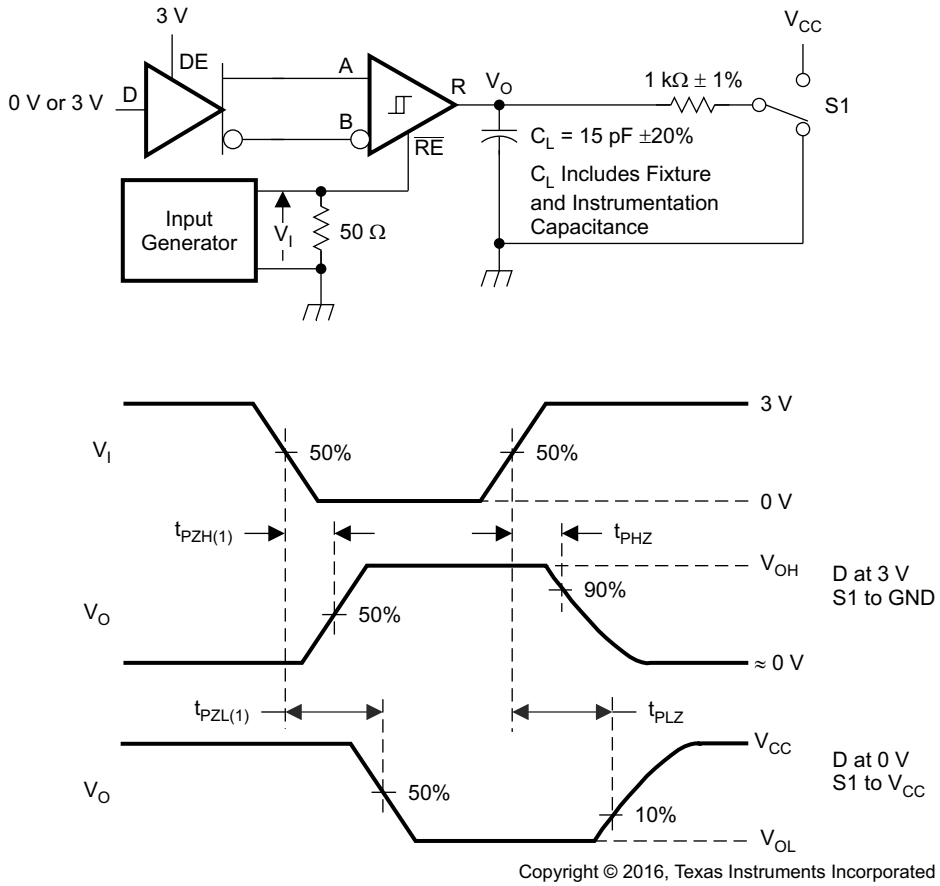


图 6-7. Measurement of Receiver Enable and Disable Times With Driver Enabled

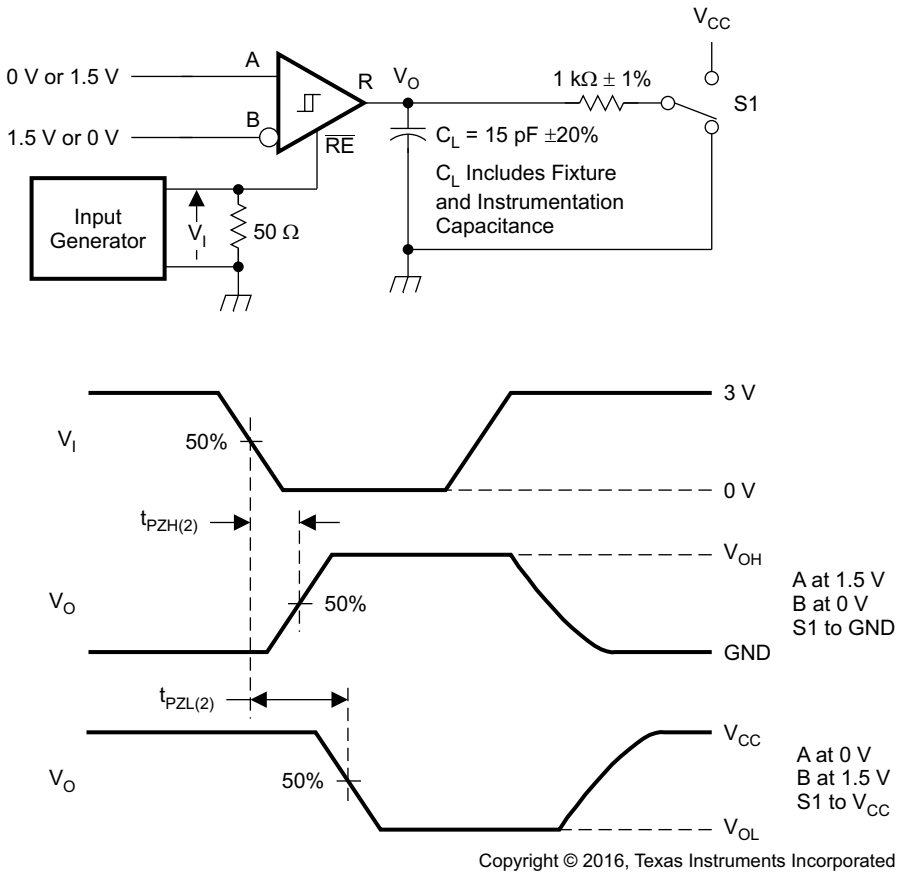


图 6-8. SN65HVD1781 Measurement of Receiver Enable Times With Driver Disabled

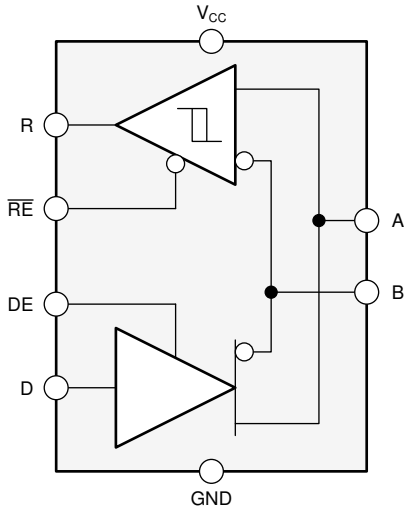
7 Detailed Description

7.1 Overview

The SN65HVD1780-Q1, SN65HVD1781-Q1, and SN65HVD1782-Q1 devices are half-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 115kbps, 1Mbps, and 10Mbps.

These devices feature a wide common-mode operating range and bus-pin fault protection up to ±70V. Each device has an active-high driver enable and active-low receiver enable. A standby current of less than 1µA can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagram



7.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16kV Human Body Model (HBM) electrostatic discharges.

Device operation is specified over a wide temperature range from –40°C to 125°C.

7.3.1 Bus Fault Conditions

The SN65HVD178x-Q1 family of RS-485 transceivers is designed to survive bus pin faults up to ±70V. The SN65HVD1782-Q1 device will not survive a bus pin fault with a direct short to voltages above 30V when all of the following occurs:

- The device is powered on
- The driver is enabled (DE = HIGH), and one of the following is true
  - D = HIGH AND the bus fault is applied to the A pin
  - D = LOW AND the bus fault is applied to the B pin

Under other conditions, the device survives shorts to bus pin faults up to ±70V. 表 7-1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

表 7-1. Bus Fault Conditions for the HVD1782

POWER	DE	D	A	B	RESULTS
OFF	X	X	–70V < V_A < 70V	–70V < V_B < 70V	Device survives
ON	LO	X	–70V < V_A < 70V	–70V < V_B < 70V	Device survives
ON	HI	L	–70V < V_A < 70V	–70V < V_B < 30V	Device survives
ON	HI	L	–70V < V_A < 70V	30V < V_B	Damage may occur
ON	HI	H	–70V < V_A < 30V	–70 V < V_B < 30V	Device survives
ON	HI	H	30V < V_A	–70V < V_B < 30V	Damage may occur

7.3.2 Receiver Failsafe

The SN65HVD178x-Q1 family of half-duplex transceivers provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –35mV and an input hysteresis of V_{HYS} = 30mV, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to 130mV_{PP} differential noise without the need for external failsafe biasing resistors.

7.3.3 Hot-Plugging

These devices are designed to operate in *hot swap* or *hot-pluggable* applications. Key features for hot-pluggable applications are power-up and power-down glitch free operation, default disabled input and output pins, and receiver failsafe.

As shown in the *Functional Block Diagram*, an internal power-on reset circuit keeps the driver outputs in a high impedance state until the supply voltage has reached a level at which the device will reliably operate. This circuit makes sure no problems occur on the bus pin outputs as the power supply turns on or off.

As shown in *Device Functional Modes*, the driver and receiver enable inputs (DE and $\overline{RE}$) are disabled by default. This default makes sure the device neither drives the bus nor reports data on the R pin until the associated controller actively drivers the enable pins.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as V_{OD} = V_A – V_B is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 7-2. Driver Function Table

INPUT	ENABLE	OUTPUTS		DRIVER STATE
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 7-3. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	RECEIVER STATE
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN65HVD178x-Q1 family of devices is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

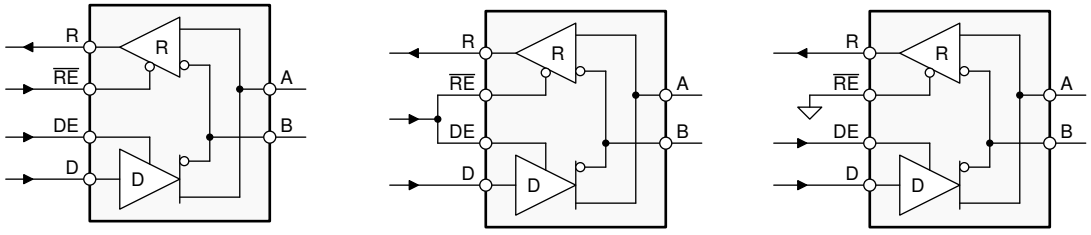


图 8-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

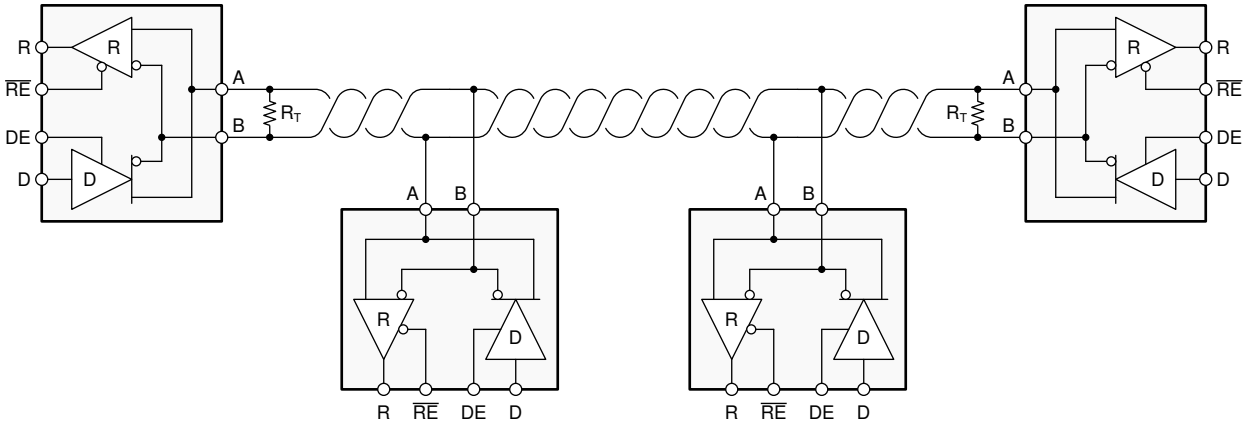


图 8-2. Typical RS-485 Network With Half-Duplex Transceivers

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

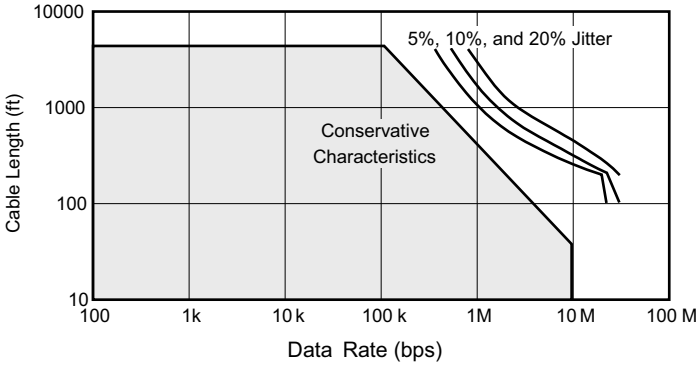


图 8-3. Cable Length vs Data Rate Characteristic

8.2.1.2 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL). Where 1 unit load represents a load impedance of approximately 12kΩ. Because the SN65HVD7x-Q1 family of devices consists of 1/10 UL transceivers, connecting up to 320 receivers to the bus is possible.

8.2.2 Detailed Design Procedure

Although the SN65HVD178x-Q1 family of devices is internally protected against human-body-model ESD strikes up to 16kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

图 8-4 shows a protection circuit intended to withstand 8kV IEC ESD (per IEC 61000-4-2) as well as 4kV EFT (per IEC 61000-4-4).

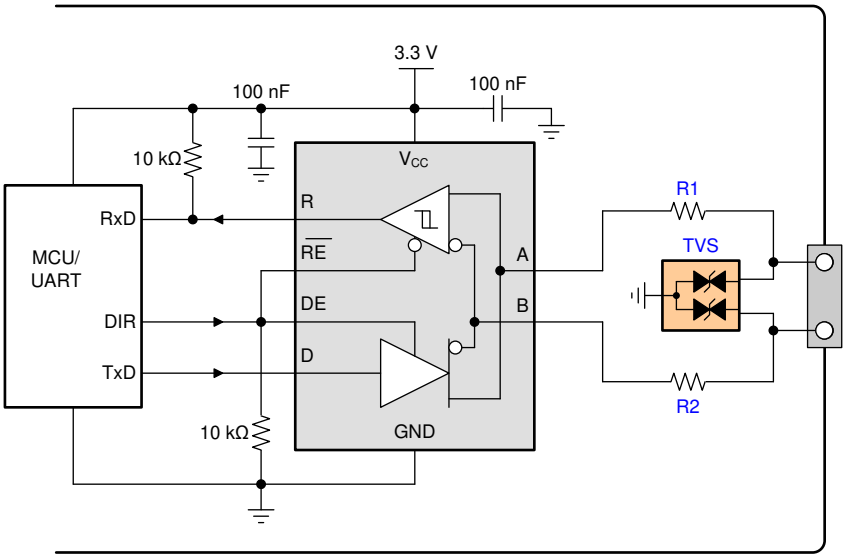


图 8-4. RS-485 Transceiver with External Transient Protection

表 8-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 Transceiver	SN65HVD178x-Q1	TI
R1, R2	10 Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 600W Transient Suppressor	SMBJ43CA	Littlefuse

(1) See Third-Party Products Disclaimer.

8.2.2.1 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{stub} \leqslant 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.2.2 Receiver Failsafe

The differential receivers of the SN65HVD178x-Q1 family have receiver input thresholds that are offset, so the receiver output state is known for the following three fault conditions:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200mV, and must output a Low when V_{ID} is more negative than –200mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$, $V_{IT(-)}$, and V_{HYS} (the separation between $V_{IT(+)}$ and $V_{IT(-)}$). As shown in the *Electrical Characteristics* table, differential signals more negative than –200mV always cause a Low receiver output, and differential signals more positive than 200mV always cause a High receiver output.

When the differential input signal is close to zero, the signal is still above the maximum $V_{IT(+)}$ threshold of –35 mV, and the receiver output is High. Only when the differential input is more than V_{HYS} below $V_{IT(+)}$ does the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS}, as well as the value of $V_{IT(+)}$.

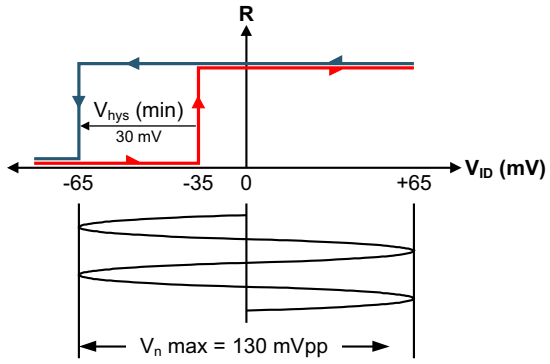
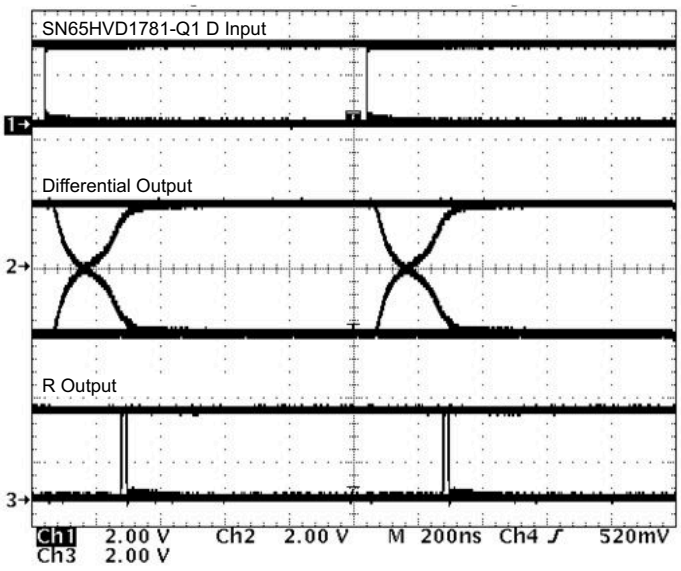


图 8-5. Noise Immunity Under Bus Fault Conditions

8.2.3 Application Curve



1-Mbps Operation

图 8-6. SN65HVD1781-Q1 PRBS Data Pattern

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be buffered with a 100nF ceramic capacitor located as close to the supply pins as possible. The device is a linear voltage regulator suitable for the 5V supply.

8.4 Layout

8.4.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1kΩ to 10kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1mA.

8.4.2 Layout Example

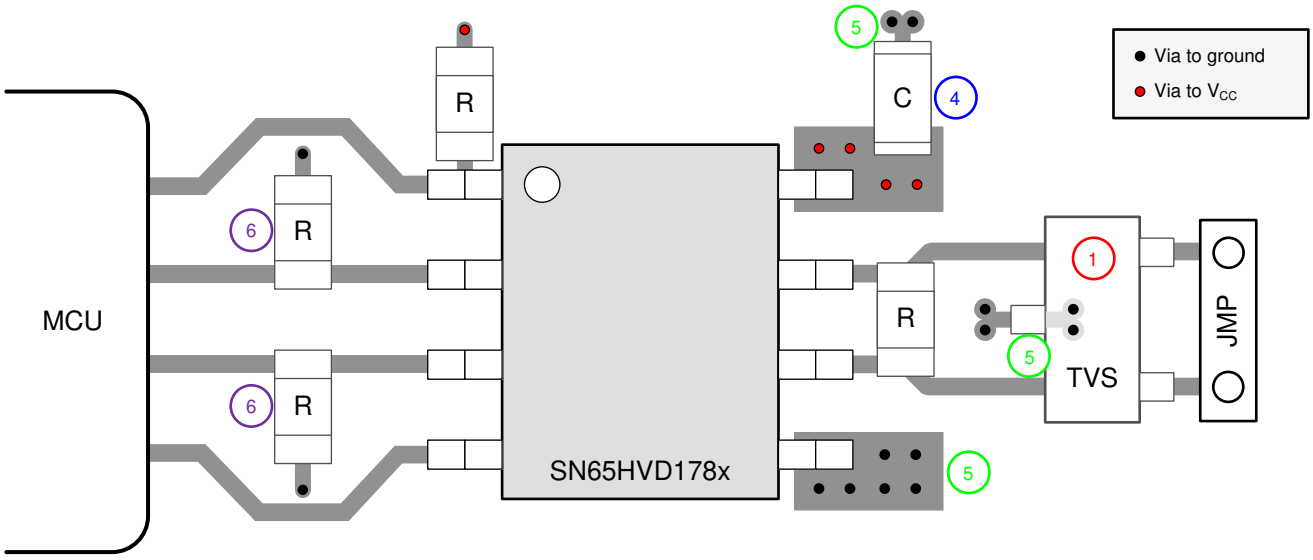


图 8-7. Half-Duplex Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- *RS-485 Half-Duplex Evaluation Module*
- *SN65HVD17xx Fault-Protected RS-485 Transceivers With Extended Common-Mode Range*
- *TPS7A6xxx-Q1 300-mA 40-V Low-Dropout Regulator With 25-µA Quiescent Current*

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (July 2017) to Revision E (October 2024) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- Changed the Storage temperature MIN value from −44°C to −55°C in the *Absolute Maximum Ratings* 4

Changes from Revision C (April 2016) to Revision D (July 2017) **Page**

- Changed the differential input to receive a valid bus high from $V_{ID} < V_{IT+}$ to $V_{ID} > V_{IT+}$ in the *Receiver Function Table* 14
- Changed the *Half-Duplex Layout Example* 20
- Added the *Receiving Notification of Documentation Updates* section.....21
- Changed the *Electrostatic Discharge Caution* statement.....21

Changes from Revision B (January 2016) to Revision C (April 2016) **Page**

- Changed the signaling rate for SN65HVD1780-Q1 from 115 to 0.115 Bin the *Recommended Operating Conditions* table 4

Changes from Revision A (August 2015) to Revision B (January 2016) **Page**

- Changed HBM and CDM back to the AEC specification and split the IEC specification into a separate table . 4
- Added the SN65HVD1780-Q1 and SN65HVD1782-Q1 devices to the *Thermal Information* table.....5

Changes from Revision * (September 2010) to Revision A (August 2015) **Page**

- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分.....1
- 向“特性”中添加了新的列表项（第二个列表项具有子列表项）.....1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1780QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1780Q
SN65HVD1780QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1780Q
SN65HVD1781QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781Q
SN65HVD1781QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781Q
SN65HVD1782QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1782Q
SN65HVD1782QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1782Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN65HVD1780-Q1, SN65HVD1781-Q1, SN65HVD1782-Q1 :

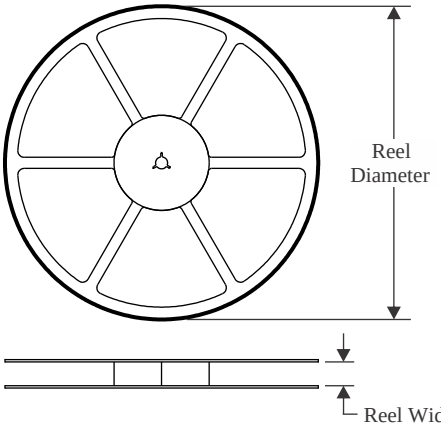
- Catalog : SN65HVD1780, SN65HVD1781, SN65HVD1782

NOTE: Qualified Version Definitions:

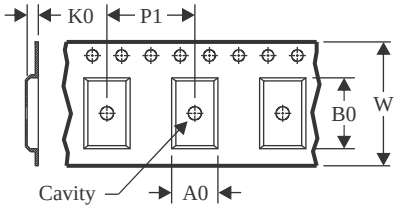
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

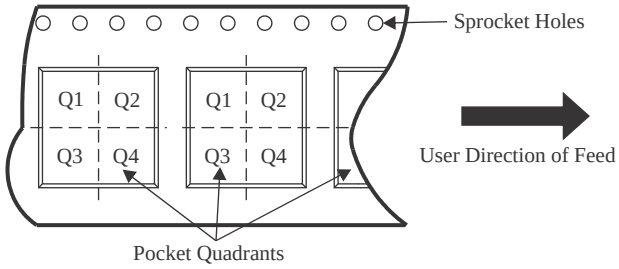


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

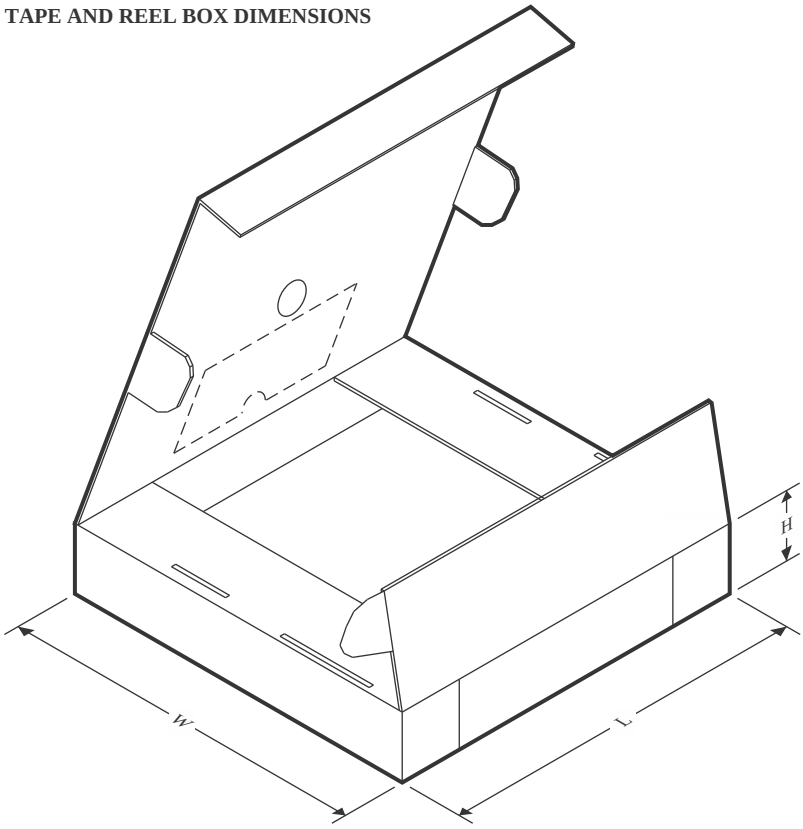
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

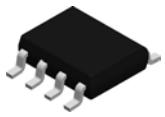
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1780QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1781QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1782QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1780QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD1781QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD1782QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

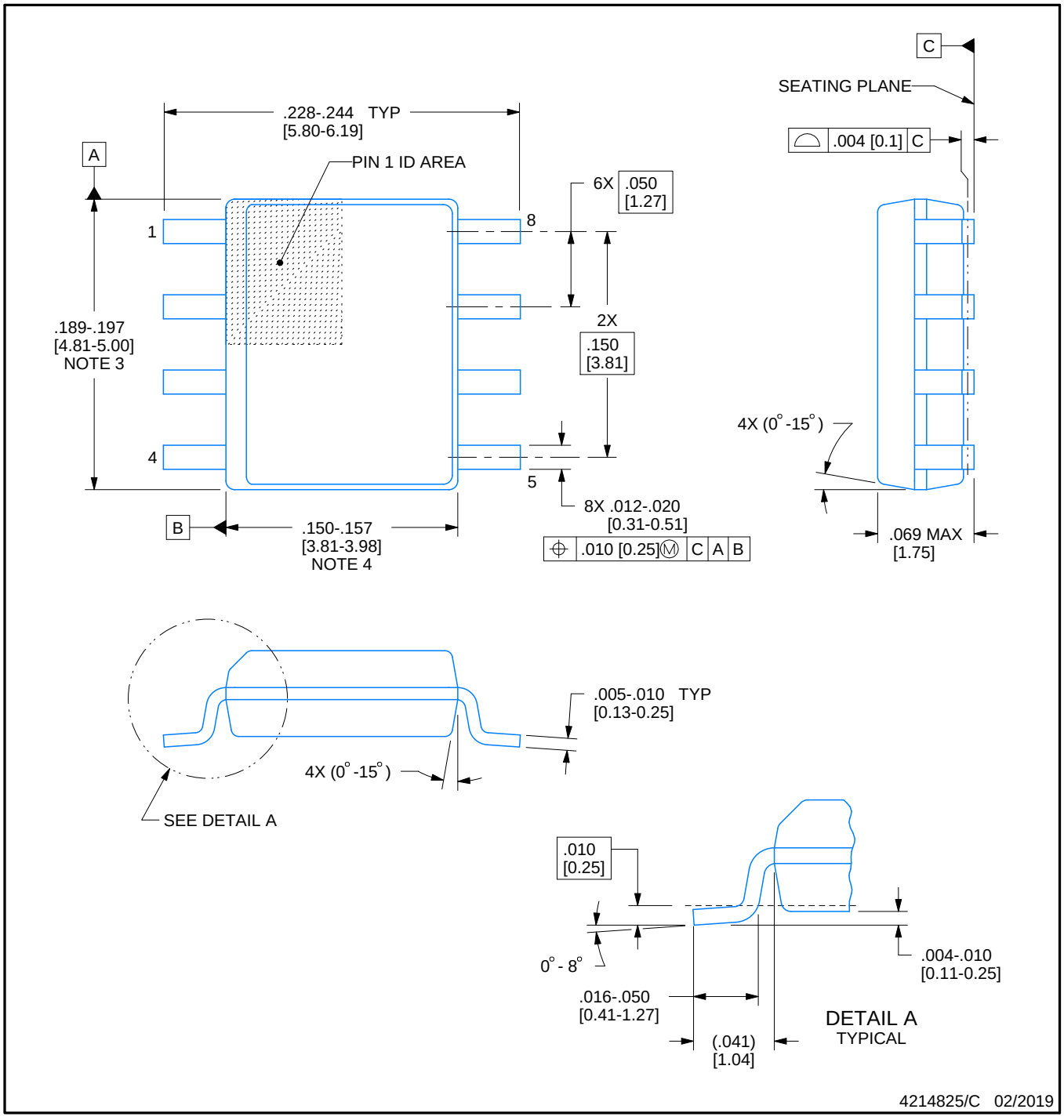


PACKAGE OUTLINE

D0008A

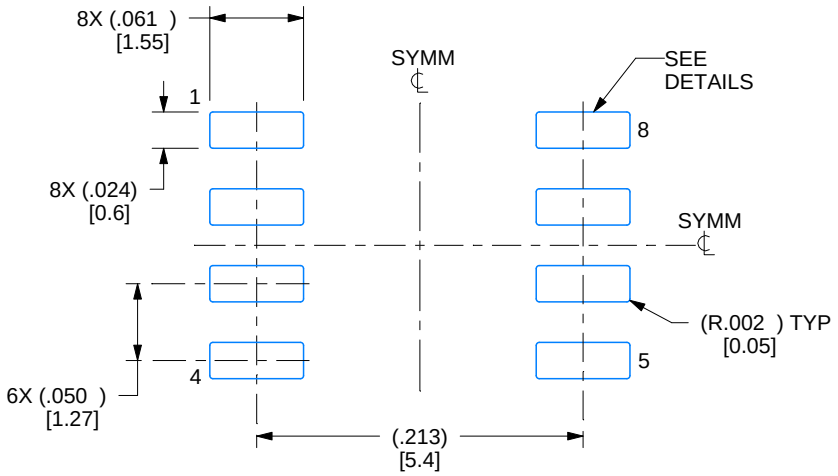
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

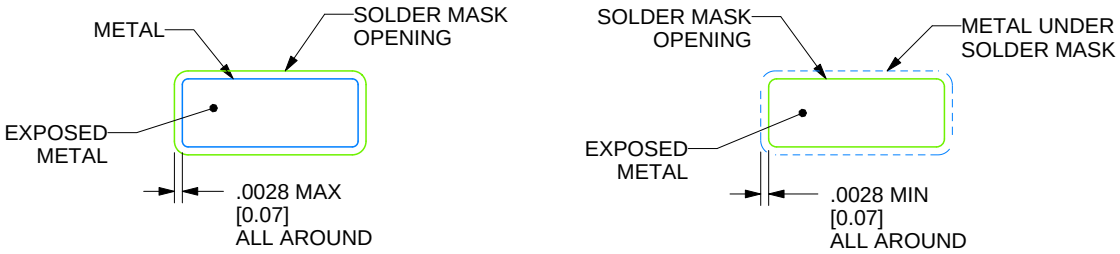


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

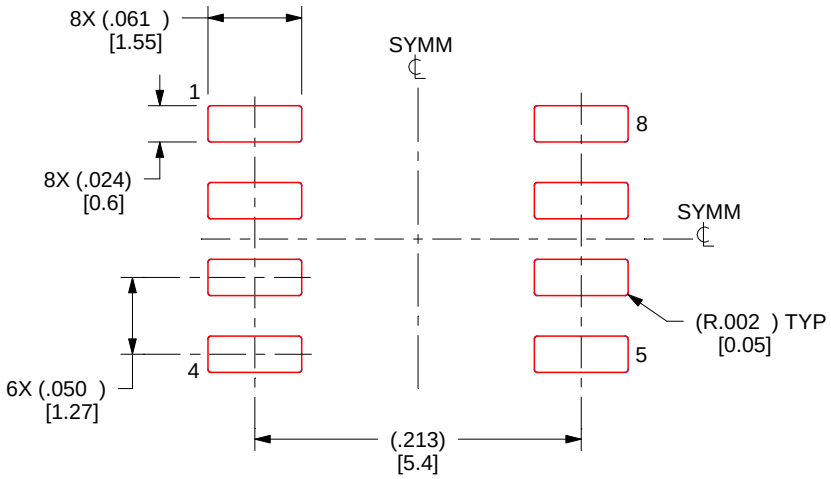
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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