

具有 $\pm 16\text{kV}$ IEC ESD 的 SN65HVD147x 3.3V 全双工 RS-485 收发器

1 特性

- 提供 1/8 单元负载选项
 - 一条总线上多达 256 个节点
- 总线 I/O 保护
 - $> \pm 30\text{kV}$ 人体放电模式 (HBM) 保护
 - $> \pm 16\text{kV}$ IEC 61000-4-2 接触放电
 - $> \pm 4\text{kV}$ IEC61000-4-4 快速瞬态突发
- 扩展的工业温度范围:
 - -40°C 至 125°C
- 用于噪声抑制的较大接收器滞后 (70mV)
- 低功耗
 - $< 1.1\text{mA}$ 的静态工作电流
 - 低待机电源电流: 典型值 10nA, 低于 $5\mu\text{A}$ (最大值)
- 针对热插拔应用的无干扰加电和断电 保护
- 与 3.3V 或 5V 控制器兼容的 5V 耐压逻辑输入
- 针对以下信号传输速率进行了优化:
 - 400 kbps (1470, 1471)、20 Mbps (1473, 1474)、50 Mbps (1476, 1477)

2 应用

- 工业自动化
- 编码器和解码器
- 楼宇自动化
- 安全和监控网络
- 电信

3 说明

SN65HVD147x 系列全双工收发器特有 RS-485 产品组合中最高静电放电 (ESD) 保护, 从而支持 $\pm 16\text{kV}$ IEC 61000-4-2 接触放电和大于 $\pm 30\text{kV}$ 的人体放电模式 (HBM) ESD 保护。这些 RS-485 收发器具有稳健耐用的 3.3V 驱动器和接收器, 并且采用标准小外形尺寸集成电路 (SOIC) 以及小型表面贴装小外形尺寸 (MSOP) 封装。SN65HVD147x 器件的较大接收器滞后提供对传导差分噪声的抗扰度, 并且较宽工作温度范围可保证器件在恶劣工作环境中实现稳定。

这些器件的每一个都组装有一个差分驱动器和一个差分接收器, 这两个器件由一个 3.3V 单电源供电运行。每个驱动器和接收器都具有用于全双工总线通信设计的独立输入和输出引脚。这些器件均具有宽共模电压范围, 因此非常适合长电缆上的多点应用。

SN65HVD1471, SN65HVD1474 和 SN65HVD1477 器件无需外部使能引脚即可完全启用。

SN65HVD1470, SN65HVD1473 和 SN65HVD1476 器件具有高电平有效驱动器使能和低电平有效接收器使能。禁用驱动器和接收器可实现少于 $5\mu\text{A}$ 的低待机电流。

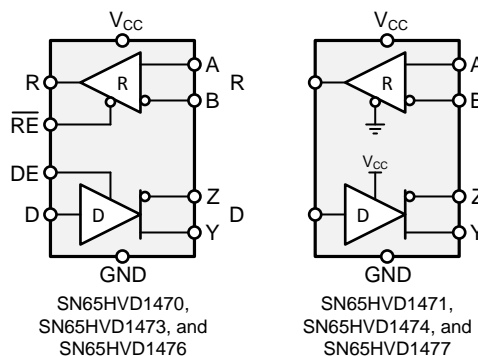
这些器件额定运行温度范围为 -40°C 至 125°C 。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|---|------------------------|------------------------------------|
| SN65HVD1471 SN65HVD1474 SN65HVD1477 | MSOP (8) SOIC (8) | 3.00mm x 3.00mm 4.90mm x 3.91mm |
| SN65HVD1470 SN65HVD1473 SN65HVD1476 | MSOP (10) SOIC (14) | 3.00mm x 3.00mm 8.65mm x 3.91mm |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Revision D (October 2014) to Revision E | Page |
|--|------|
| • Changed the <i>Pin Configuration</i> images | 3 |
| • Changed the Supply Voltage MAX value From: 5.5 V To 5 V in the <i>Absolute Maximum Ratings</i> | 6 |
| • Moved Storage Temperature From the ESD table to the <i>Absolute Maximum Ratings</i> | 6 |
| • Changed the Handling Ratings table to <i>ESD Ratings</i> | 6 |
| • Added Note: to Supply voltage in the <i>Recommended Operating Conditions</i> | 7 |

| Changes from Revision C (August 2014) to Revision D | Page |
|---|------|
| • Updated the MSOP–10 logic diagram | 4 |

| Changes from Revision B (July 2014) to Revision C | Page |
|--|------|
| • Updated the <i>Device Comparison Table</i> | 3 |

| Changes from Revision A (June 2014) to Revision B | Page |
|---|------|
| • Updated SN65HVD1470 and SN65HVD1471 specifications to production values | 3 |

| Changes from Original (May 2014) to Revision A | Page |
|--|------|
| • 已更改 器件状态从 产品预览 更改为 生产数据（混合状态） | 1 |

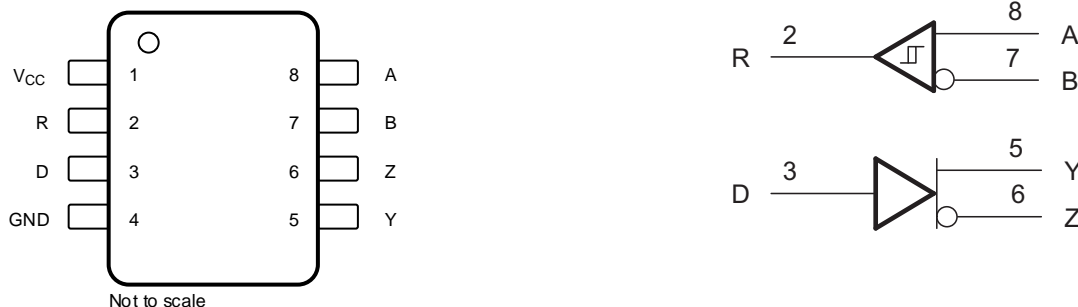
5 Device Comparison Table

| PART NUMBER ⁽¹⁾ | SIGNALING RATE | DUPLEX | ENABLES | PACKAGE | NODES |
|----------------------------|----------------|--------|---------------------|--------------------|-------|
| SN65HVD1470 | up to 400 kbps | Full | DE, \overline{RE} | SOIC-14 MSOP-10 | 256 |
| SN65HVD1471 | up to 400 kbps | Full | None | SOIC-8 MSOP-8 | 256 |
| SN65HVD1473 | up to 20 Mbps | Full | DE, \overline{RE} | SOIC-14 MSOP-10 | 256 |
| SN65HVD1474 | up to 20 Mbps | Full | None | SOIC-8 MSOP-8 | 256 |
| SN65HVD1476 | up to 50 Mbps | Full | DE, \overline{RE} | SOIC-14 MSOP-10 | 96 |
| SN65HVD1477 | up to 50 Mbps | Full | None | SOIC-8 MSOP-8 | 96 |

(1) For device status, see the [机械、封装和可订购信息](#) section.

6 Pin Configuration and Functions

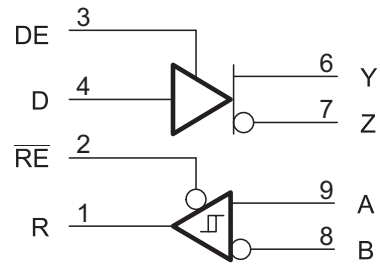
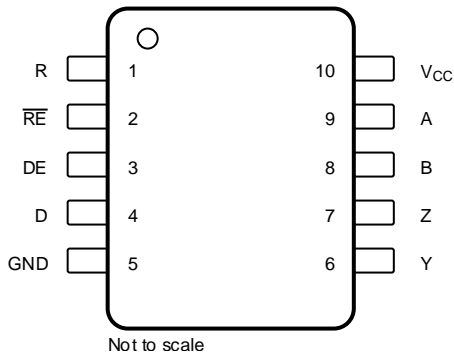
SN65HVD1471, SN65HVD1474, SN65HVD1477
8-Pin SOIC, D Package, and 8-Pin MSOP, DGK Package
(Top View)



Pin Functions — SOIC-8 and MSOP-8

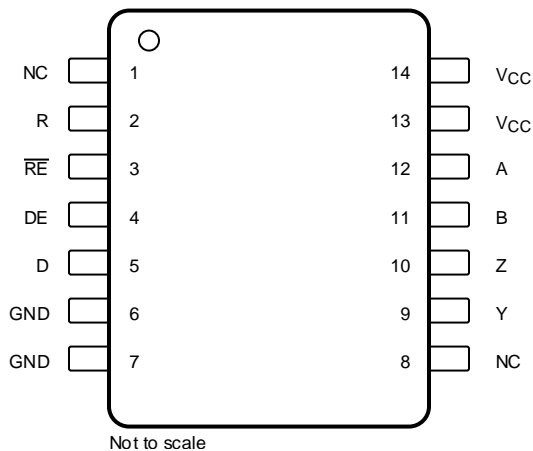
| PIN | | TYPE | DESCRIPTION |
|-----------------|-----|---------------------|--|
| NAME | NO. | | |
| V _{CC} | 1 | Supply | 3-V to 3.6-V supply |
| R | 2 | Digital output | Receive data output |
| D | 3 | Digital input | Driver data input |
| GND | 4 | Reference potential | Local device ground |
| Y | 5 | Bus output | Digital bus output, Y (Complementary to Z) |
| Z | 6 | Bus output | Digital bus output, Z (Complementary to Y) |
| B | 7 | Bus input | Digital bus input, B (Complementary to A) |
| A | 8 | Bus input | Digital bus input, A (Complementary to B) |

SN65HVD1470, SN65HVD1473, SN65HVD1476
 10-Pin MSOP, DGS Package
 (Top View)

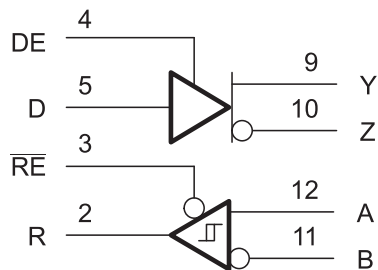


Pin Functions — MSOP-10

| PIN | | TYPE | DESCRIPTION |
|------------------------|-----|---------------------|--|
| NAME | NO. | | |
| R | 1 | Digital output | Receive data output |
| $\overline{\text{RE}}$ | 2 | Digital input | Receive enable <i>Low</i> |
| DE | 3 | Digital input | Driver enable <i>High</i> |
| D | 4 | Digital input | Driver data input |
| GND | 5 | Reference potential | Local device ground |
| Y | 6 | Bus output | Digital bus output, Y (Complementary to Z) |
| Z | 7 | Bus output | Digital bus output, Z (Complementary to Y) |
| B | 8 | Bus input | Digital bus input, B (Complementary to A) |
| A | 9 | Bus input | Digital bus input, A (Complementary to B) |
| V _{CC} | 10 | Supply | 3-V to 3.6-V supply |

**SN65HVD1470, SN65HVD1473, SN65HVD1476
14-Pin SOIC, D Package
(Top View)**


NC = no internal connection


Pin Functions — SOIC-14

| PIN | | TYPE | DESCRIPTION |
|-----------------|-------------------|---------------------|--|
| NAME | NO. | | |
| NC | 1 | No connect | Not connected |
| | 8 | | |
| R | 2 | Digital output | Receive data output |
| \overline{RE} | 3 | Digital input | Receive enable <i>Low</i> |
| DE | 4 | Digital input | Driver enable <i>High</i> |
| D | 5 | Digital input | Driver data input |
| GND | 6 ⁽¹⁾ | Reference potential | Local device ground |
| | 7 ⁽¹⁾ | | |
| Y | 9 | Bus output | Digital bus output, Y (Complementary to Z) |
| Z | 10 | Bus output | Digital bus output, Z (Complementary to Y) |
| B | 11 | Bus input | Digital bus input, B (Complementary to A) |
| A | 12 | Bus input | Digital bus input, A (Complementary to B) |
| V _{CC} | 13 ⁽²⁾ | Supply | 3-V to 3.6-V supply |
| | 14 ⁽²⁾ | | |

(1) Pin 6 and pin 7 are connected internally.

(2) Pin 13 and pin 14 are connected internally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------------------------|--|---|------|------|
| Supply voltage | V_{CC} | -0.5 | 5 | V |
| Voltage | Range at any bus pin (A, B, Y, or Z) | -13 | 16.5 | V |
| Input voltage | Range at any logic pin (D, DE, or \overline{RE}) | -0.3 | 5.7 | V |
| | Voltage input range, transient pulse, any bus pin (A, B, Y, or Z) through 100 Ω | -100 | 100 | V |
| Output current | Receiver output | -24 | 24 | mA |
| Junction temperature, T_J | | | 170 | °C |
| Storage temperature range, T_{stg} | | -65 | 150 | °C |
| Continuous total power dissipation | | See the Thermal Information table | | |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|---|--------|------|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND | ±16000 | V |
| | | IEC 61000-4-2 ESD (Air-Gap Discharge), bus pins and GND ⁽¹⁾⁽²⁾ | ±16000 | V |
| | | IEC 61000-4-4 EFT (Fast transient or burst), bus pins and GND | ±4000 | V |
| | | IEC 60749-26 ESD (Human Body Model), bus pins and GND ⁽²⁾ | ±30000 | V |
| | | Human body model (HBM), bus pins and GND ⁽³⁾ | ±40000 | V |
| | | Human body model (HBM), per JEDEC specification JESD22-A114, all pins | ±8000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins | ±1500 | V |
| | | Machine model (MM), all pins | ±30000 | V |

- (1) By inference from contact-discharge results, see the [Application and Implementation](#) section
 (2) Limited by tester capability.
 (3) Modeled performance only; based on measured IEC ESD (Contact) capability.

7.3 Recommended Operating Conditions

| IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND | | MIN | NOM | MAX | UNIT |
|---|---|------------------|-----|-----------------|------|
| V _{CC} | Supply voltage ⁽¹⁾ | 3 | 3.3 | 3.6 | V |
| V _I | Input voltage at any bus pin (separately or common mode) ⁽²⁾ | -7 | | 12 | V |
| V _{IH} | High-level input voltage (Driver, driver enable, and receiver enable inputs) | 2 | | V _{CC} | V |
| V _{IL} | Low-level input voltage (Driver, driver enable, and receiver enable inputs) | 0 | | 0.8 | V |
| V _{ID} | Differential input voltage | -12 | | 12 | V |
| I _O | Output current, Driver | -60 | | 60 | mA |
| I _O | Output current, Receiver | -8 | | 8 | mA |
| R _L | Differential load resistance | 54 | 60 | | Ω |
| C _L | Differential load capacitance | | 50 | | pF |
| 1/t _{UI} | Signaling rate | HVD1470, HVD1471 | | 400 | kbps |
| | | HVD1473, HVD1474 | | 20 | |
| | | HVD1476, HVD1477 | | 50 | |
| T _A ⁽³⁾ | Operating free-air temperature (See the Application and Implementation for thermal information) | -40 | | 125 | °C |
| T _J | Junction Temperature | -40 | | 150 | °C |

- (1) Exposure to conditions beyond the recommended operation maximum for extended periods may affect device reliability.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(3) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating because of internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

7.4 Thermal Information — D Packages

| THERMAL METRIC | | D (8 PINS) | D (14 PINS) | UNIT |
|-----------------------|--|---------------|----------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance | 110.7 | 83.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 54.7 | 42.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 51.3 | 37.8 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 9.2 | 9.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 50.7 | 37.5 | °C/W |
| T _{J(TSD)} | Thermal shut-down junction temperature | 170 | | °C |

7.5 Thermal Information — DGS and DGK Packages

| THERMAL METRIC | | DGS (10 PINS) | DGK (8 PINS) | UNIT |
|-----------------------|--|------------------|-----------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance | 165.5 | 168.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 37.7 | 62.2 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 86.4 | 89.5 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1.4 | 7.4 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 84.8 | 87.9 | °C/W |
| T _{J(TSD)} | Thermal shut-down junction temperature | 170 | | °C |

7.6 Power Dissipation

| PARAMETER | | TEST CONDITIONS | | VALUE | UNIT | |
|-----------|--|-----------------|--|---------------------|------|----|
| PD | Power Dissipation driver and receiver enabled, $V_{CC} = 3.6\text{ V}$, $T_J = 150^\circ\text{C}$ 50% duty cycle square-wave signal at signaling rate: <ul style="list-style-type: none"> HVD1470 and HVD1471 at 400 kbps HVD1473 and HVD1474 at 20 Mbps HVD1476 and HVD1477 at 50 Mbps | Unterminated | $R_L = 300\ \Omega$, $C_L = 50\text{ pF}$ (driver) | HVD1470, HVD1471 | 150 | mW |
| | | | | HVD1473, HVD1474 | 180 | |
| | | | | HVD1476, HVD1477 | 220 | |
| | | RS-422 load | $R_L = 100\ \Omega$, $C_L = 50\text{ pF}$ (driver) | HVD1470, HVD1471 | 190 | mW |
| | | | | HVD1473, HVD1474 | 220 | |
| | | | | HVD1476, HVD1477 | 250 | |
| | | RS-485 load | $R_L = 54\ \Omega$, $C_L = 50\text{ pF}$ (driver) | HVD1470, HVD1471 | 230 | mW |
| | | | | HVD1473, HVD1474 | 255 | |
| | | | | HVD1476, HVD1477 | 285 | |

7.7 Electrical Characteristics

over recommended operating range (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|---|---|--|---------------------|--------------|--------------------|---------------|
| $ V_{OD} $ | Driver differential output voltage magnitude | $R_L = 60\ \Omega$, 375 Ω on each output to -7 V to 12 V , See Figure 15 | | 1.5 | 2 | | V |
| | | $R_L = 54\ \Omega$ (RS-485), See Figure 16 | | 1.5 | 2 | | V |
| | | $R_L = 100\ \Omega$ (RS-422) $T_J \geq 0^\circ\text{C}$, $V_{CC} \geq 3.2\text{ V}$, See Figure 16 | | 2 | | | V |
| $\Delta V_{OD} $ | Change in magnitude of driver differential output voltage | $R_L = 54\ \Omega$, $C_L = 50\text{ pF}$, See Figure 16 | | -50 | 0 | 50 | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | Center of two 27- Ω load resistors, See Figure 16 | | 1 | $V_{CC}/2$ | 3 | V |
| ΔV_{OC} | Change in differential driver output common-mode voltage | | | -50 | 0 | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak driver common-mode output voltage | | | | 500 | | mV |
| C_{OD} | Differential output capacitance | | | | 15 | | pF |
| V_{IT+} | Positive-going receiver differential input voltage threshold | | | See ⁽¹⁾ | -70 | -20 | mV |
| V_{IT-} | Negative-going receiver differential input voltage threshold | | | -200 | -140 | See ⁽¹⁾ | mV |
| V_{hys} | Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$) | | | 40 | 70 | | mV |
| V_{OH} | Receiver high-level output voltage | $I_{OH} = -8\text{ mA}$ | | 2.4 | $V_{CC}-0.3$ | | V |
| V_{OL} | Receiver low-level output voltage | $I_{OL} = 8\text{ mA}$ | | | 0.2 | 0.4 | V |
| I_I | Driver input, driver enable, and receiver enable input current | | | -3 | | 3 | μA |
| I_{OZ} | Receiver output high-impedance current | HVD1470, HVD1473, HVD1476 | $V_O = 0\text{ V}$ or V_{CC} , $\overline{RE} = V_{CC}$ | -1 | | 1 | μA |
| I_{OS} | Driver short-circuit output current | | | -150 | | 150 | mA |
| I_I | Bus input current (disabled driver) | $V_{CC} = 0$ to ROC (max), $DE = GND$ | HVD1470, HVD1473 | $V_I = 12\text{ V}$ | 75 | 125 | μA |
| | | | | $V_I = -7\text{ V}$ | -100 | -40 | |
| | | | HVD1476 | $V_I = 12\text{ V}$ | 240 | 333 | |
| | | | | $V_I = -7\text{ V}$ | -267 | -180 | |
| I_{CC} | Supply current (quiescent) | Driver and Receiver enabled | $DE = V_{CC}$, $\overline{RE} = GND$, No load | | 750 | 1100 | μA |
| | | Driver enabled, receiver disabled | $DE = V_{CC}$, $\overline{RE} = V_{CC}$, No load | | 350 | 650 | μA |
| | | Driver disabled, receiver enabled | $DE = GND$, $\overline{RE} = GND$, No load | | 650 | 800 | μA |
| | | Driver and receiver disabled | $DE = GND$, $D = \text{open}$, $\overline{RE} = V_{CC}$, No load | | 0.1 | 5 | μA |

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{hys} higher than V_{IT-} .

Electrical Characteristics (continued)

over recommended operating range (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|---|-----|-----|-----|------|
| Supply current (dynamic) | | See the Typical Characteristics section | | | | |
| T_{sd} | Thermal Shut-down junction temperature | | | | 170 | °C |

7.8 Switching Characteristics — 400 kbps

400-kbps devices (SN65HVD1470, SN65HVD1471) bit time $\geq 2 \mu\text{s}$ (over recommended operating conditions)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|--|--|------------------|-----|------|---------------|
| DRIVER | | | | | | | |
| t_r, t_f | Driver differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ | See Figure 17 | 100 | 400 | 750 | ns |
| t_{PHL}, t_{PLH} | Driver propagation delay | | | 350 | 550 | | ns |
| $t_{SK(P)}$ | Driver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | 40 | | ns |
| t_{PHZ}, t_{PLZ} | Driver disable time | HVD1470 | See Figure 18 and Figure 19 | 50 | 200 | | ns |
| t_{PZH}, t_{PZL} | Driver enable time | | | Receiver enabled | 300 | 750 | |
| | | | | 3 | 8 | | μs |
| | | | | | | | |
| RECEIVER | | | | | | | |
| t_r, t_f | Receiver output rise/fall time | $C_L = 15 \text{ pF}$ | See Figure 20 | 13 | 25 | | ns |
| t_{PHL}, t_{PLH} | Receiver propagation delay time | | | 70 | 110 | | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | 7 | | ns |
| t_{PLZ}, t_{PHZ} | Receiver disable time | HVD1470 | See Figure 21 | 45 | 60 | | ns |
| $t_{PZL(1)}, t_{PZH(1)}, t_{PZL(2)}, t_{PZH(2)}$ | Receiver enable time | | | Driver enabled | 20 | 115 | |
| | | | | 3 | 8 | | μs |
| | | | | | | | |
| | | | | | | | |

7.9 Switching Characteristics — 20 Mbps

20-Mbps devices (SN65HVD1473, SN65HVD1474) bit time \geq 50 ns (over recommended operating conditions)

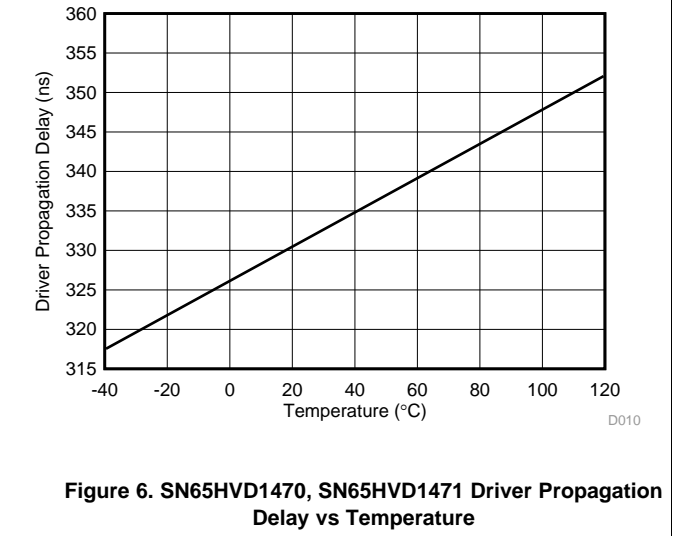
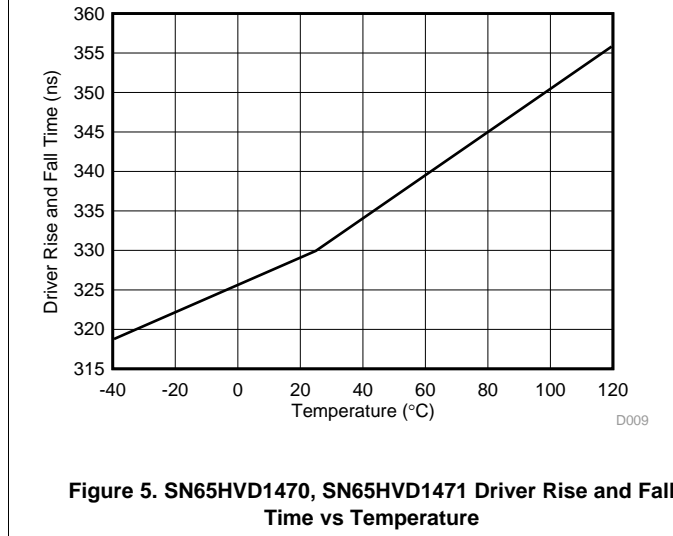
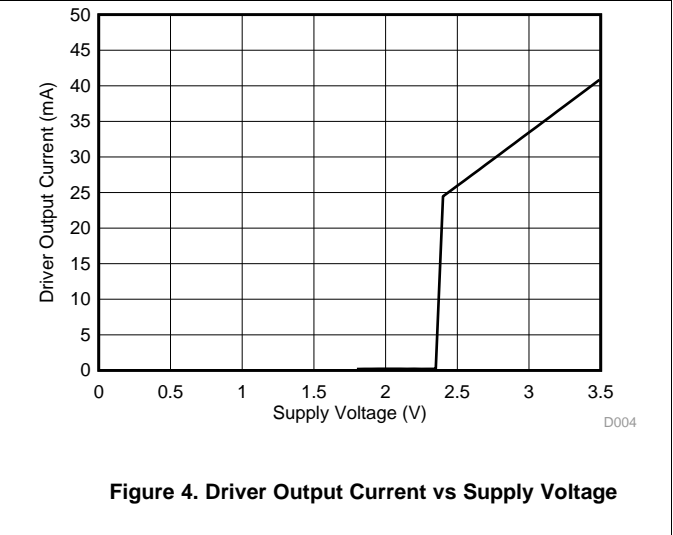
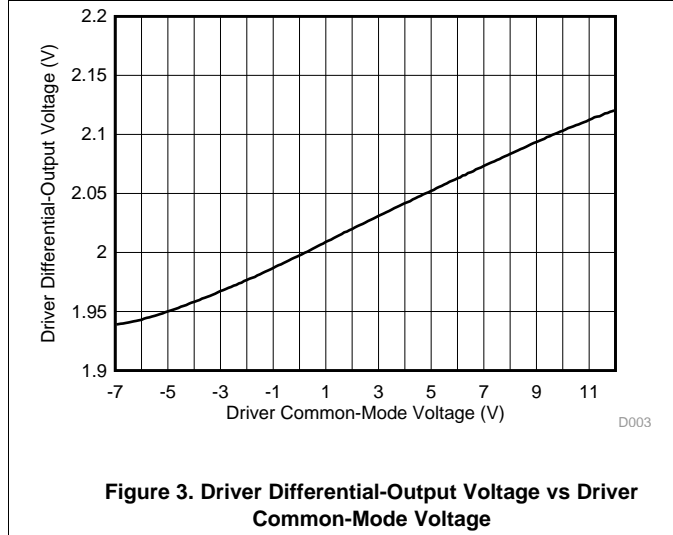
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|--|--|---|-------------------------------|-----|---------------|---------------|
| DRIVER | | | | | | | |
| t_r, t_f | Driver differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ | See Figure 17 | 4 | 7 | 14 | ns |
| t_{PHL}, t_{PLH} | Driver propagation delay | | | 4 | 10 | 20 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $ t_{PHL} - t_{PLH} $ | | | 0 | 4 | ns | |
| t_{PHZ}, t_{PLZ} | Driver disable time | HVD1473 | See Figure 18 and Figure 19 | 12 | 25 | ns | |
| t_{PZH}, t_{PZL} | Driver enable time | | | Receiver enabled | 10 | 20 | ns |
| | | | Receiver disabled | 3 | 8 | μs | |
| RECEIVER | | | | | | | |
| t_r, t_f | Receiver output rise/fall time | $C_L = 15 \text{ pF}$ | See Figure 20 | 5 | 10 | ns | |
| t_{PHL}, t_{PLH} | Receiver propagation delay time | | | 60 | 90 | ns | |
| $t_{SK(P)}$ | Receiver pulse skew, $ t_{PHL} - t_{PLH} $ | | | 0 | 5 | ns | |
| t_{PLZ}, t_{PHZ} | Receiver disable time | HVD1473 | See Figure 21 | 17 | 25 | ns | |
| $t_{pZL(1)}, t_{pZH(1)}$ $t_{pZL(2)}, t_{pZH(2)}$ | Receiver enable time | | | Driver enabled | 12 | 90 | ns |
| | | | Driver disabled | See Figure 22 | 3 | 8 | μs |

7.10 Switching Characteristics — 50 Mbps

50-Mbps devices (SN65HVD1476, SN65HVD1477) bit time \geq 20 ns (over recommended operating conditions)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|--|--|---|-------------------------------|-----|---------------|---------------|
| DRIVER | | | | | | | |
| t_r, t_f | Driver differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ | See Figure 17 | 2 | 3 | 6 | ns |
| t_{PHL}, t_{PLH} | Driver propagation delay | | | 3 | 10 | 16 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $ t_{PHL} - t_{PLH} $ | | | 0 | 3.5 | ns | |
| t_{PHZ}, t_{PLZ} | Driver disable time | HVD1476 | See Figure 18 and Figure 19 | 10 | 20 | ns | |
| t_{PZH}, t_{PZL} | Driver enable time | | | Receiver enabled | 10 | 20 | ns |
| | | | Receiver disabled | 3 | 8 | μs | |
| RECEIVER | | | | | | | |
| t_r, t_f | Receiver output rise/fall time | $C_L = 15 \text{ pF}$ | See Figure 20 | 1 | 3 | 6 | ns |
| t_{PHL}, t_{PLH} | Receiver propagation delay time | | | 25 | 40 | ns | |
| $t_{SK(P)}$ | Receiver pulse skew, $ t_{PHL} - t_{PLH} $ | | | 0 | 2 | ns | |
| t_{PLZ}, t_{PHZ} | Receiver disable time | HVD1476 | See Figure 21 | 8 | 15 | ns | |
| $t_{pZL(1)}, t_{pZH(1)}$ $t_{pZL(2)}, t_{pZH(2)}$ | Receiver enable time | | | Driver enabled | 8 | 90 | ns |
| | | | Driver disabled | See Figure 22 | 3 | 8 | μs |

7.11 Typical Characteristics



Typical Characteristics (continued)

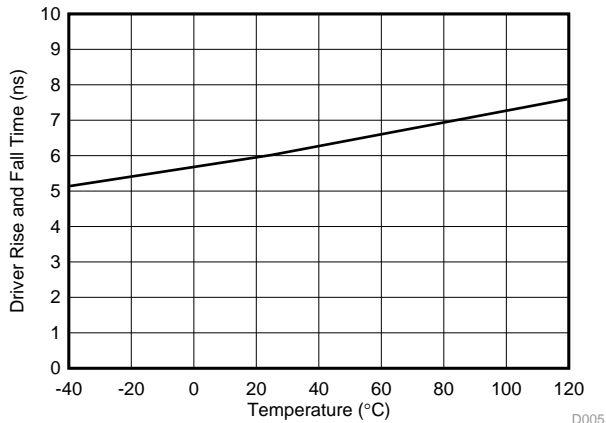


Figure 7. SN65HVD1473, SN65HVD1474 Driver Rise and Fall Time vs Temperature

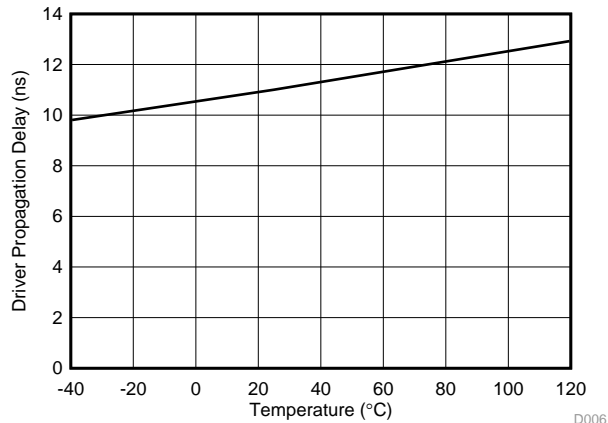


Figure 8. SN65HVD1473, SN65HVD1474 Driver Propagation Delay vs Temperature

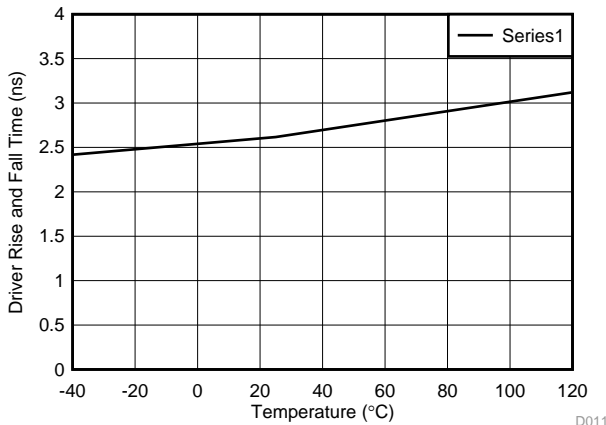


Figure 9. SN65HVD1476, SN65HVD1477 Driver Rise and Fall Time vs Temperature

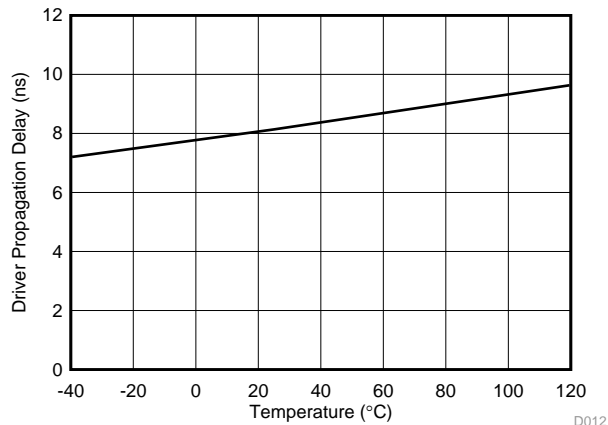


Figure 10. SN65HVD1476, SN65HVD1477 Driver Propagation Delay vs Temperature

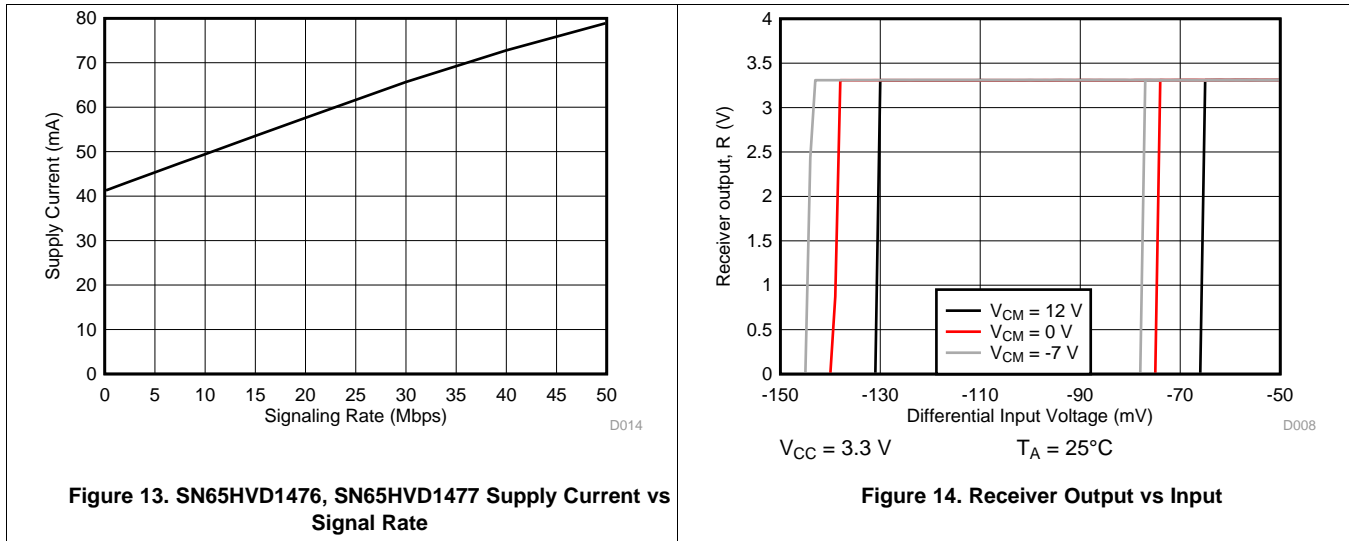


Figure 11. SN65HVD1470, SN65HVD1471 Supply Current vs Signal Rate



Figure 12. SN65HVD1473, SN65HVD1474 Supply Current vs Signal Rate

Typical Characteristics (continued)



8 Parameter Measurement Information

The input generator rate is 100 kbps with 50% duty cycle, than 6-ns rise and fall times, and 50-Ω output impedance.

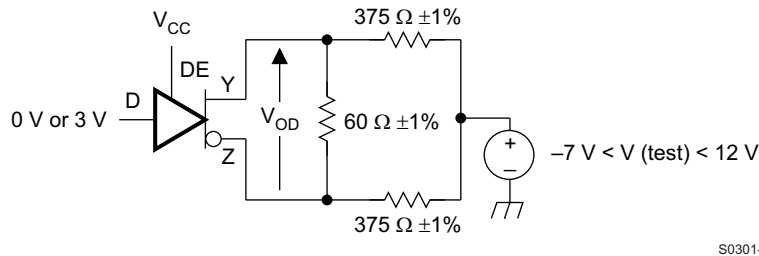


Figure 15. Measurement of Driver Differential Output Voltage With Common-Mode Load

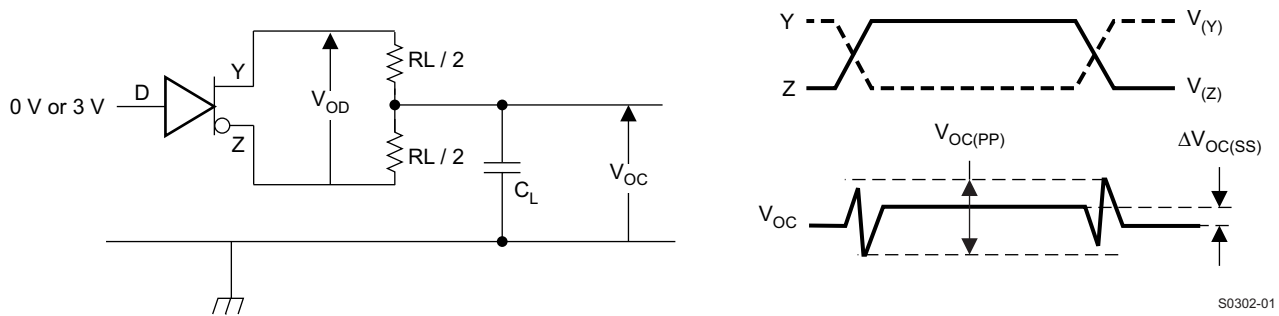


Figure 16. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

Parameter Measurement Information (continued)

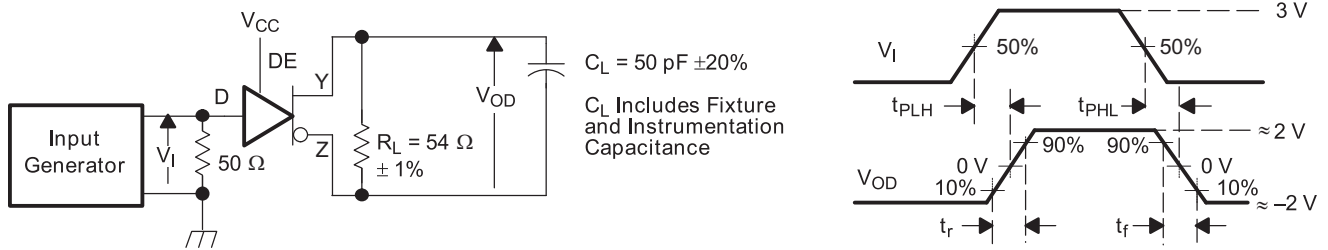


Figure 17. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 18. Measurement of Driver Enable and Disable Times with Active-High Output and Pulldown Load



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 19. Measurement of Driver Enable and Disable Times with Active-Low Output and Pullup Load

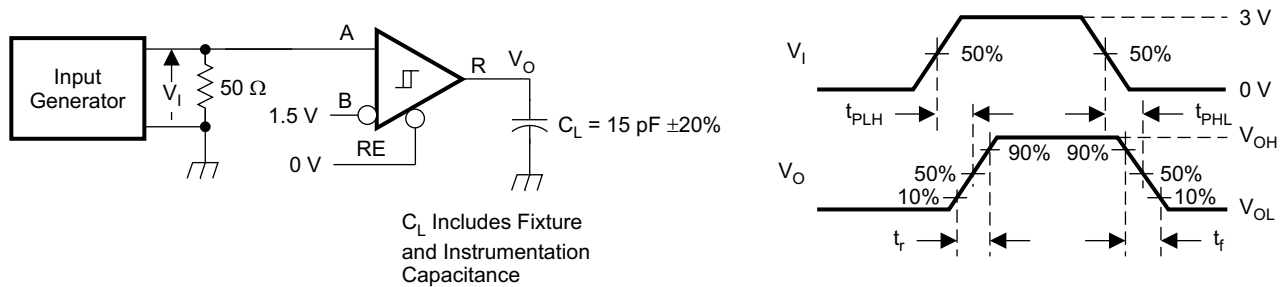
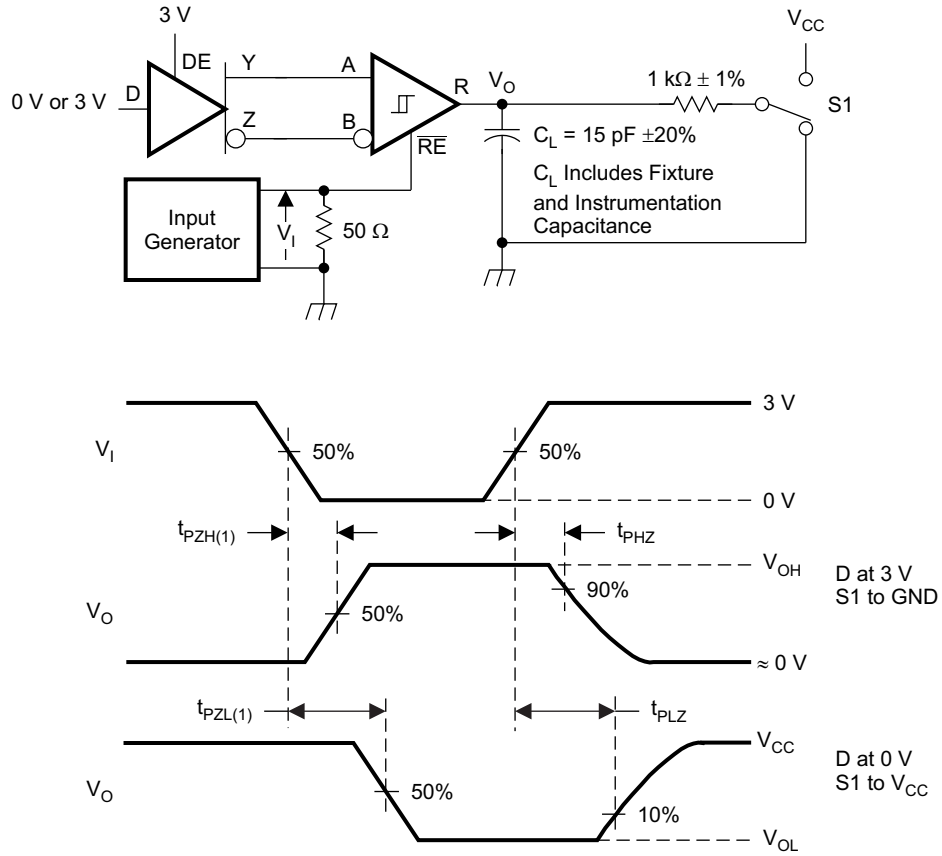


Figure 20. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)



S0307-01

Figure 21. Measurement of Receiver Enable and Disable Times With Driver Enabled

Parameter Measurement Information (continued)

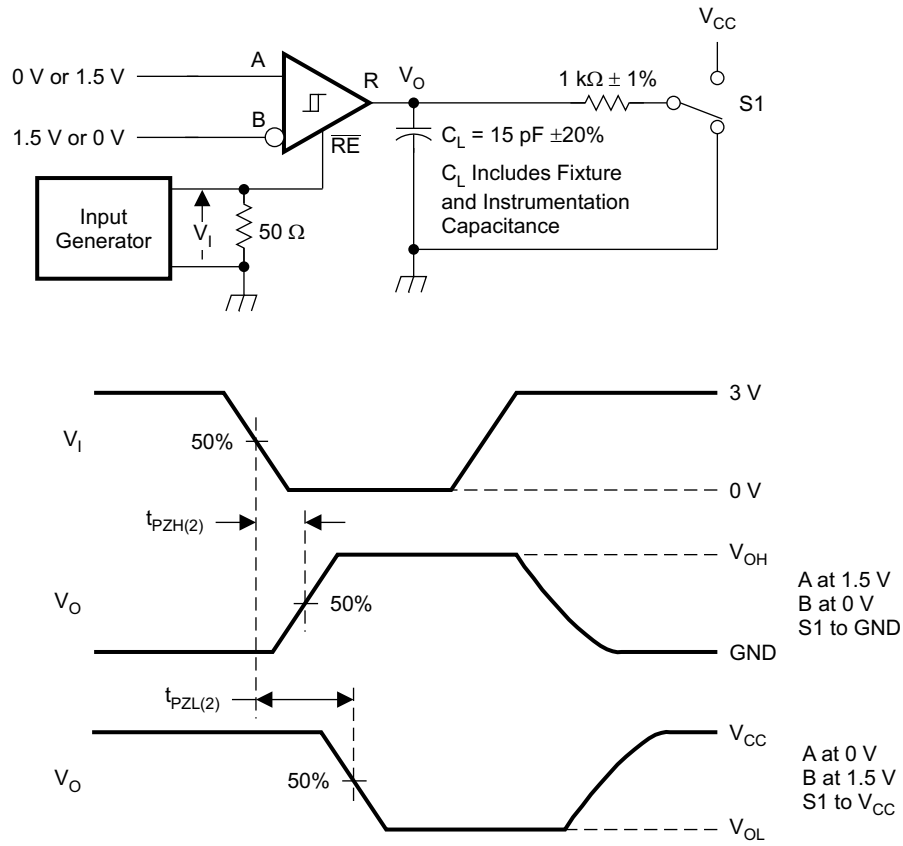


Figure 22. Measurement of Receiver Enable Times With Driver Disabled

9 Detailed Description

9.1 Overview

The SN65HVD1470, SN65HVD1471, SN65HVD1473, SN65HVD1474, SN65HVD1476, and SN65HVD1477 devices are low-power, full-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 400 kbps, 20 Mbps, and 50 Mbps.

The SN65HVD1471, SN65HVD1474, and SN65HVD1477 are fully enabled with no external enabling pins. The SN65HVD1470, SN65HVD1473, and SN65HVD1476 have active-high driver enables and active-low receiver enables. A standby current of less than 5 μ A can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram

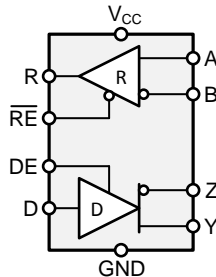


Figure 23. Block Diagram
SN65HVD1470, SN65HVD1473, and SN65HVD1476

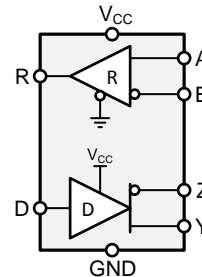


Figure 24. Block Diagram
SN65HVD1471, SN65HVD1474, and SN65HVD1477

9.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC61000-4-2 of up to ± 16 kV, and against electrical fast transients (EFT) according to IEC61000-4-4 of up to ± 4 kV.

The SN65HVD147x full-duplex family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of $V_{IT+} = -20$ mV and an input hysteresis of $V_{hys} = 40$ mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 120 mV_{PP} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide temperature range from -40°C to 125°C .

9.4 Device Functional Modes

For the SN65HVD1470, SN65HVD1473, and SN65HVD1476, when the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} - V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC} , thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 1. Driver Function Table SN65HVD1470, SN65HVD1473, SN65HVD1476

| INPUT | ENABLE | OUTPUTS | | FUNCTION |
|-------|--------|---------|---|---|
| | | Y | Z | |
| H | H | H | L | Actively drives the bus high |
| L | H | L | H | Actively drives the bus low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drives the bus high by default |

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} - V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, V_{IT-} , the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table SN65HVD1470, SN65HVD1473, SN65HVD1476

| DIFFERENTIAL INPUT | ENABLE | OUTPUT | FUNCTION |
|------------------------------|-----------------|--------|------------------------------|
| $V_{ID} = V_{(A)} - V_{(B)}$ | \overline{RE} | R | |
| $V_{IT+} < V_{ID}$ | L | H | Receives valid bus High |
| $V_{IT-} < V_{ID} < V_{IT+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{IT-}$ | L | L | Receives valid bus Low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

For the SN65HVD1471, HVD1474, and HVD1477, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} - V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. The D pin has an internal pullup resistor to V_{CC} , thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 3. Driver Function Table SN65HVD1471, SN65HVD1474, SN65HVD1477

| INPUT | OUTPUTS | | FUNCTION |
|-------|---------|---|---|
| D | Y | Z | |
| H | H | L | Actively drives the bus High |
| L | L | H | Actively drives the bus Low |
| OPEN | H | L | Actively drives the bus High by default |

When the differential input voltage defined as $V_{ID} = V_{(A)} - V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and less than the negative input threshold, V_{IT-} , the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 4. Receiver Function Table SN65HVD1471, SN65HVD1474, SN65HVD1477

| DIFFERENTIAL INPUT | OUTPUT | FUNCTION |
|------------------------------|--------|-------------------------|
| $V_{ID} = V_{(A)} - V_{(B)}$ | R | |
| $V_{IT+} < V_{ID}$ | H | Receives valid bus High |
| $V_{IT-} < V_{ID} < V_{IT+}$ | ? | Indeterminate bus state |
| $V_{ID} < V_{IT-}$ | L | Receives valid bus Low |
| Open-circuit bus | H | Fail-safe high output |
| Short-circuit bus | H | Fail-safe high output |
| Idle (terminated) bus | H | Fail-safe high output |

9.4.1 Equivalent Circuits



Figure 25. D and RE Inputs



Figure 26. DE Input



Figure 27. R Output



Figure 28. Receiver Inputs



Figure 29. Driver Outputs

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD147x family consists of full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

To eliminate line reflections, each cable end is terminated with a termination resistor, $R_{(T)}$, whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.



Figure 30. Typical RS-485 Network With SN65HVD147x Full-Duplex Transceivers

10.2 Typical Application

A full-duplex RS-485 network consists of multiple transceivers connecting in parallel to two bus cables. On one signal pair, a master driver transmits data to multiple slave receivers. The master driver and slave receivers may remain fully enabled at all times. On the other signal pair, multiple slave drivers transmit data to the master receiver. To avoid bus contention, the slave drivers must be intermittently enabled and disabled such that only one driver is enabled at any time, as in half-duplex communication. The master receiver may remain fully enabled at all times.

Because the driver may not be disabled, only one driver should be connected to the bus when using the SN65HVD1471, SN65HVD1474, or SN65HVD1477 device.



Figure 31. Full-Duplex Transceiver Configurations

Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying parameter requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

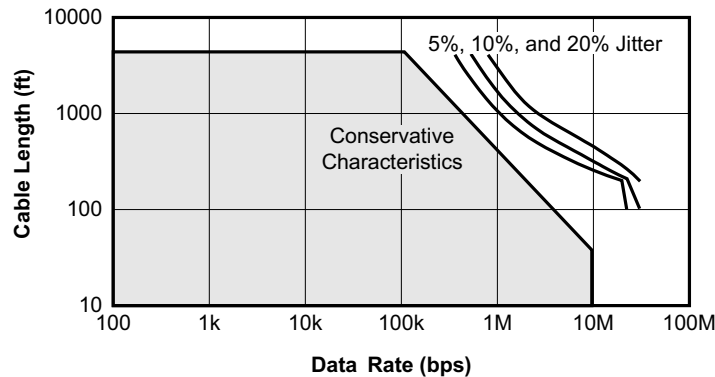


Figure 32. Cable Length vs Data Rate Characteristic

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(\text{STUB})} \leq 0.1 \times t_r \times v \times c$$

where

- t_r is the 10/90 rise time of the driver
- v is the signal velocity of the cable or trace as a factor of c
- c is the speed of light (3×10^8 m/s)

(1)

Per Equation 1, Table 5 lists the maximum cable-stub lengths for the minimum-driver output rise-times of the SN65HVD147x full-duplex family of transceivers for a signal velocity of 78%.

Table 5. Maximum Stub Length

| DEVICE | MINIMUM DRIVER OUTPUT RISE TIME (ns) | MAXIMUM STUB LENGTH | |
|-------------|---|---------------------|------|
| | | (m) | (ft) |
| SN65HVD1470 | 100 | 2.34 | 7.7 |
| SN65HVD1471 | 100 | 2.34 | 7.7 |
| SN65HVD1473 | 4 | 0.1 | 0.3 |
| SN65HVD1474 | 4 | 0.1 | 0.3 |
| SN65HVD1476 | 2 | 0.05 | 0.15 |
| SN65HVD1477 | 2 | 0.05 | 0.15 |

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD147x family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

10.2.1.4 Receiver Failsafe

The differential receivers of the SN65HVD147x family are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a Low when V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} , V_{IT-} , and V_{hys} (the separation between V_{IT+} and V_{IT-}). As shown in the [Electrical Characteristics](#) table, differential signals more negative than -200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more than V_{hys} below V_{IT+} will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{hys} , as well as the value of V_{IT+} .

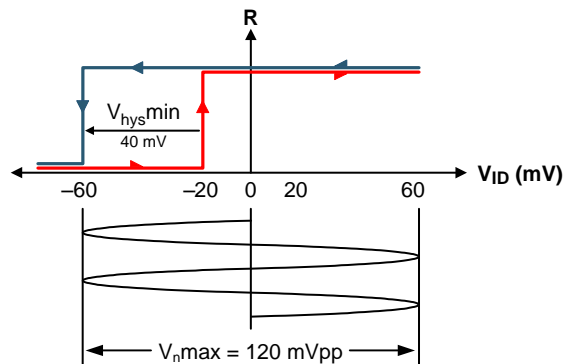


Figure 33. SN65HVD147x Noise Immunity Under Bus Fault Conditions

10.2.1.5 Transient Protection

The bus pins of the SN65HVD147x full-duplex transceiver family include on-chip ESD protection against ± 30 -kV HBM and ± 16 -kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from contact discharge test results.

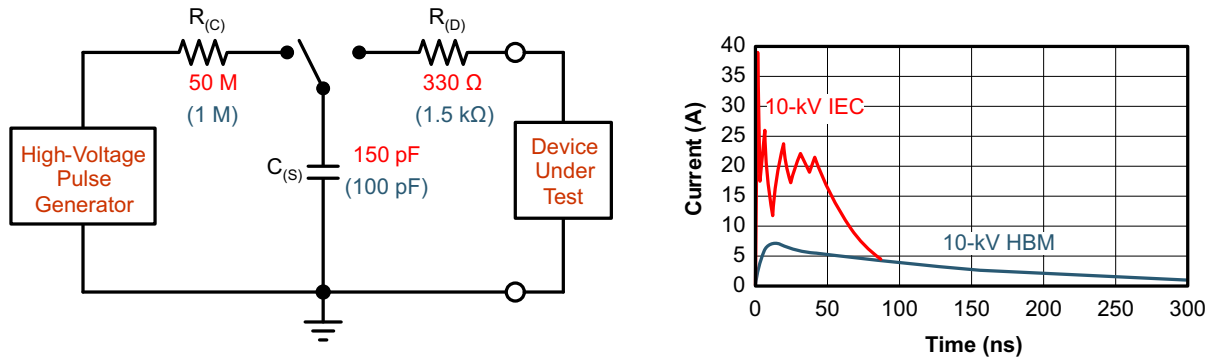


Figure 34. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 35 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automations.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

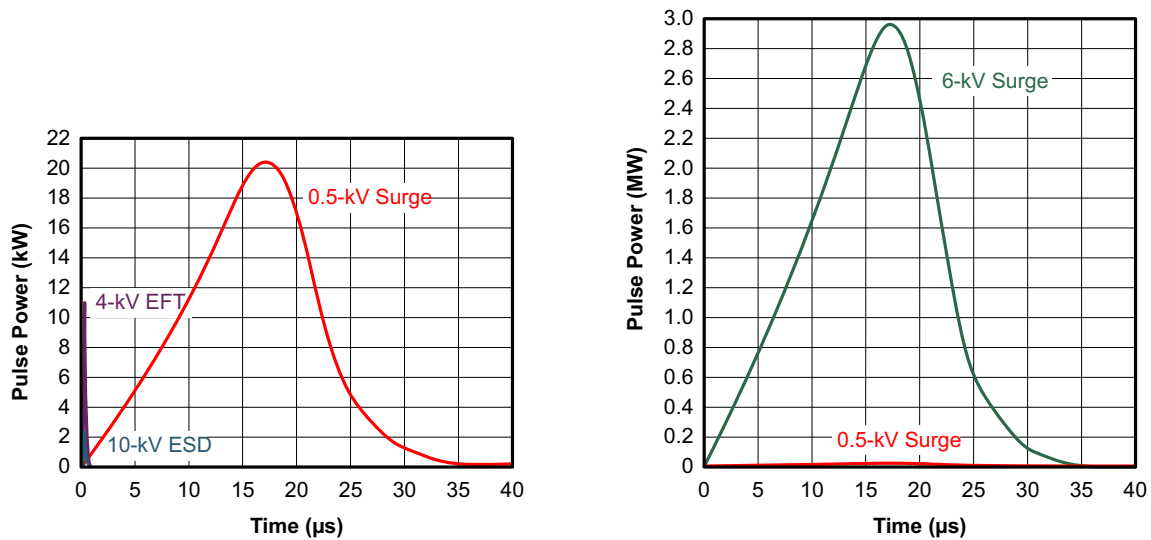


Figure 35. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver.

Figure 36 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

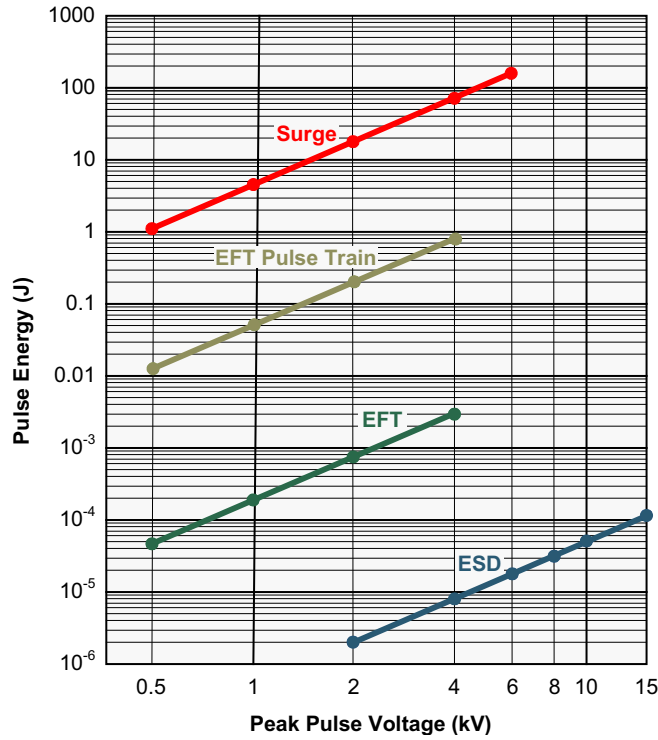


Figure 36. Comparison of Transient Energies

10.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. Figure 37 shows a protection circuit against 16-kV ESD, 4-kV EFT, and 1-kV surge transients.

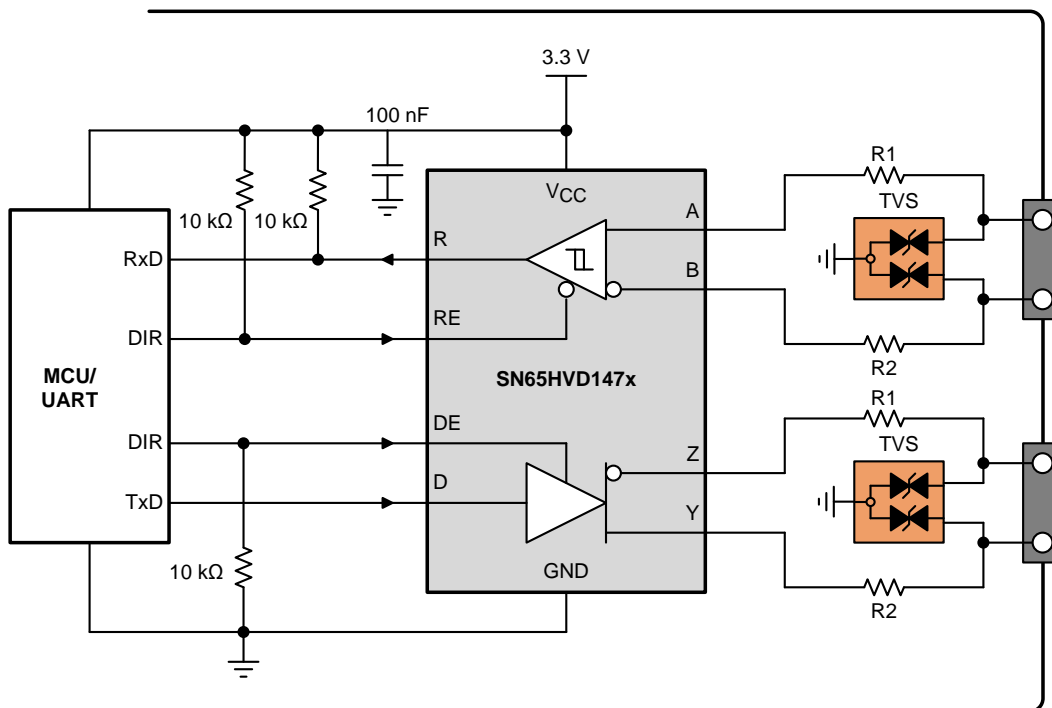
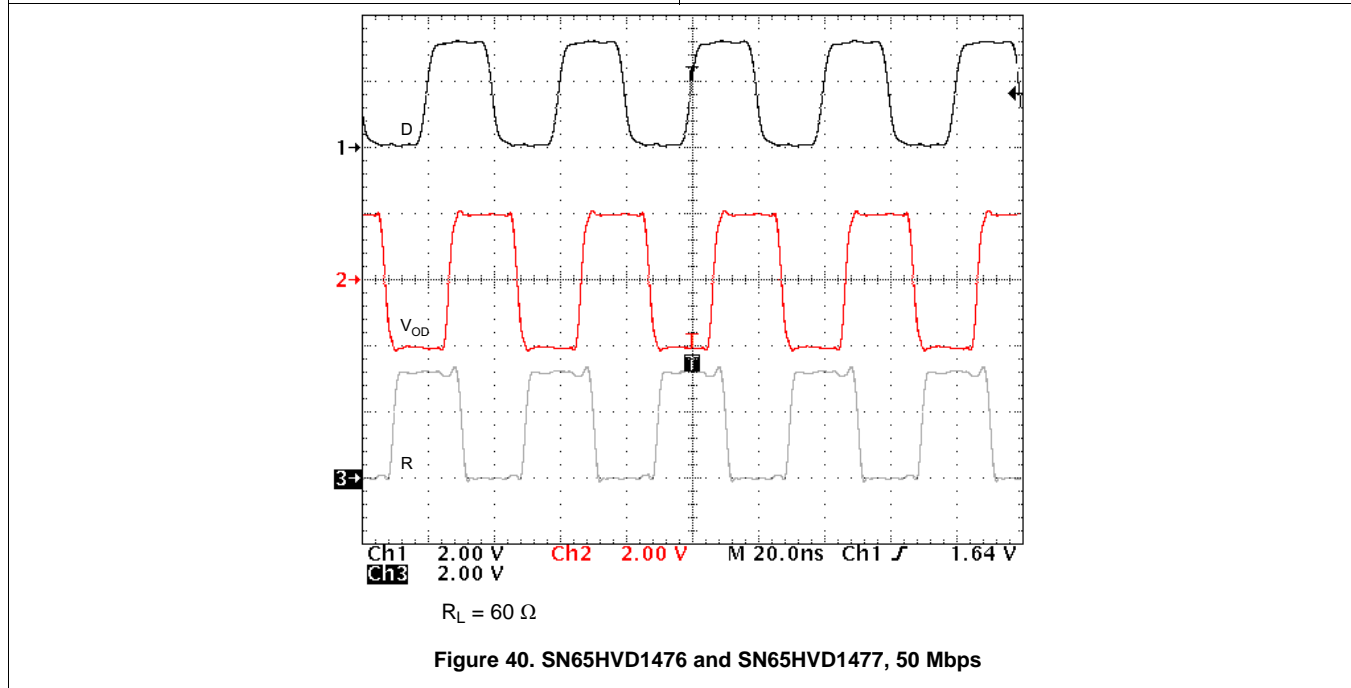
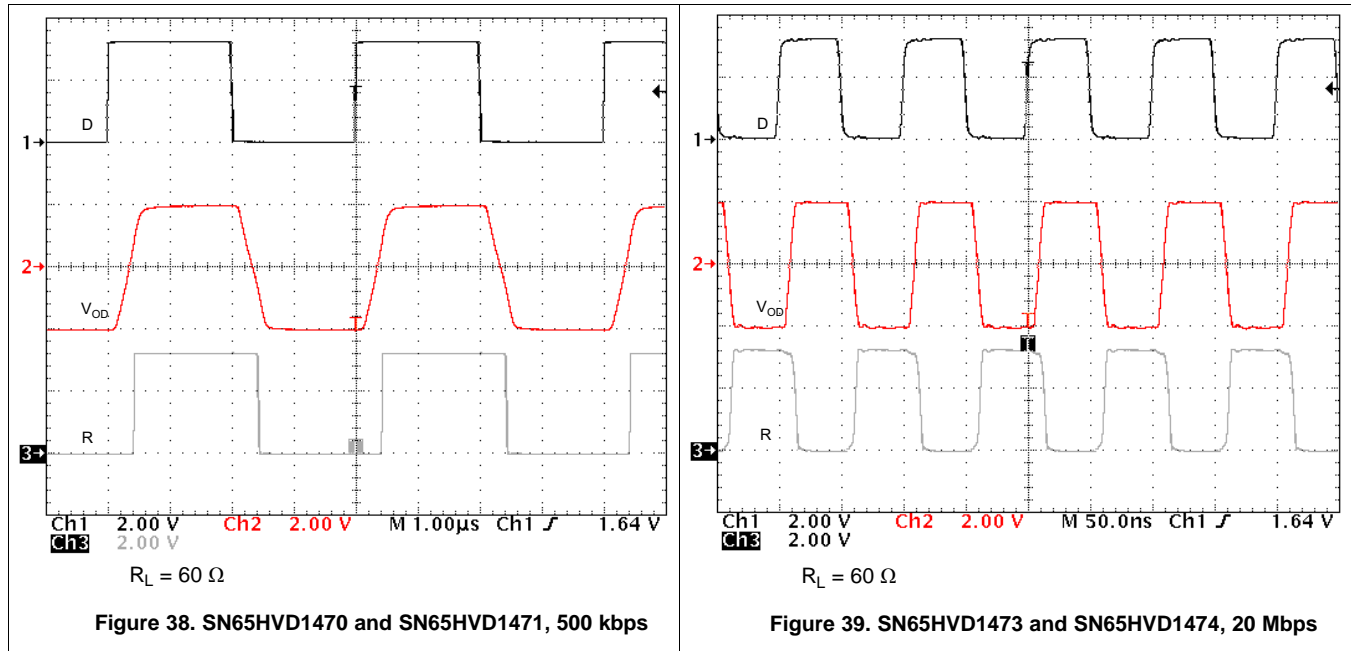


Figure 37. Transient Protection Against ESD, EFT, and Surge transients

Table 6. Bill of Materials

| DEVICE | FUNCTION | ORDER NUMBER | MANUFACTURER |
|----------|--|--------------------|--------------|
| XCVR | 3.3-V, full-duplex RS-485 transceiver | SN65HVD147xD | TI |
| R1 R2 | 10-Ω, pulse-proof thick-film resistor | CRCW0603010RJNEAHP | Vishay |
| TVS | Bidirectional 400-W transient suppressor | CDSOT23-SM712 | Bourns |

10.2.3 Application Curves



11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3-V supply.

12 Layout

12.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design.

For successful PCB design, begin with the design of the protection circuit (see [Figure 41](#)).

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} -pins of transceiver, UART, controller ICs on the board (see [Figure 41](#)).
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see [Figure 41](#)).
6. Use 1-k Ω to 10-k Ω pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events (see [Figure 41](#)).
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see [Figure 41](#)).
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

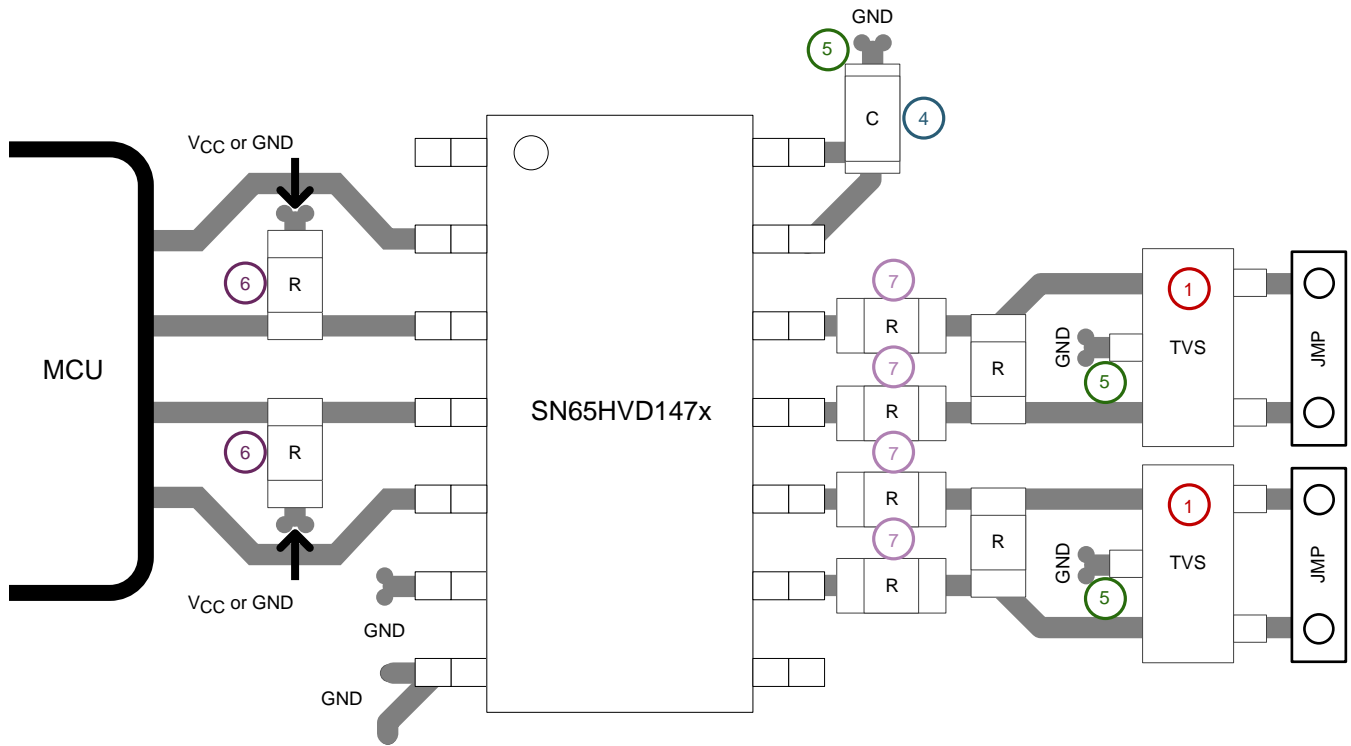


Figure 41. SN65HVD147x Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 7. 相关链接

| 器件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持和社区 |
|-------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| SN65HVD1470 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| SN65HVD1471 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| SN65HVD1473 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| SN65HVD1474 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| SN65HVD1476 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| SN65HVD1477 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN65HVD1470D | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1470 |
| SN65HVD1470D.B | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1470 |
| SN65HVD1470DGS | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1470 |
| SN65HVD1470DGS.B | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1470 |
| SN65HVD1470DGSR | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1470 |
| SN65HVD1470DGSR.B | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1470 |
| SN65HVD1470DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1470 |
| SN65HVD1470DR.B | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1470 |
| SN65HVD1471D | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 |
| SN65HVD1471D.B | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 |
| SN65HVD1471DGK | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1471 |
| SN65HVD1471DGK.B | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1471 |
| SN65HVD1471DGKR | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1471 |
| SN65HVD1471DGKR.B | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1471 |
| SN65HVD1471DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 |
| SN65HVD1471DR.B | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 |
| SN65HVD1471DRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 |
| SN65HVD1471DRG4.B | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1471 |
| SN65HVD1473D | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 |
| SN65HVD1473D.B | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 |
| SN65HVD1473DGS | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1473 |
| SN65HVD1473DGS.B | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1473 |
| SN65HVD1473DGSR | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1473 |
| SN65HVD1473DGSR.B | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1473 |
| SN65HVD1473DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 |
| SN65HVD1473DR.B | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 |
| SN65HVD1473DRG4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 |
| SN65HVD1473DRG4.B | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1473 |
| SN65HVD1474D | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1474 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN65HVD1474D.B | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1474 |
| SN65HVD1474DGK | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1474 |
| SN65HVD1474DGK.B | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1474 |
| SN65HVD1474DGKR | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU SN NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1474 |
| SN65HVD1474DGKR.B | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1474 |
| SN65HVD1474DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1474 |
| SN65HVD1474DR.B | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1474 |
| SN65HVD1476D | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476D.A | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476D.B | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476DGS | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 |
| SN65HVD1476DGS.A | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 |
| SN65HVD1476DGS.B | Active | Production | VSSOP (DGS) 10 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 |
| SN65HVD1476DGSR | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 |
| SN65HVD1476DGSR.A | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 |
| SN65HVD1476DGSR.B | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1476 |
| SN65HVD1476DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476DR.B | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476DRG4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476DRG4.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1476DRG4.B | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD1476 |
| SN65HVD1477D | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 |
| SN65HVD1477D.A | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 |
| SN65HVD1477D.B | Active | Production | SOIC (D) 8 | 75 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 |
| SN65HVD1477DGK | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1477 |
| SN65HVD1477DGK.A | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1477 |
| SN65HVD1477DGK.B | Active | Production | VSSOP (DGK) 8 | 80 TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1477 |
| SN65HVD1477DGKR | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1477 |
| SN65HVD1477DGKR.A | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1477 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN65HVD1477DGKR.B | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1477 |
| SN65HVD1477DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 |
| SN65HVD1477DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 |
| SN65HVD1477DR.B | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD1477 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

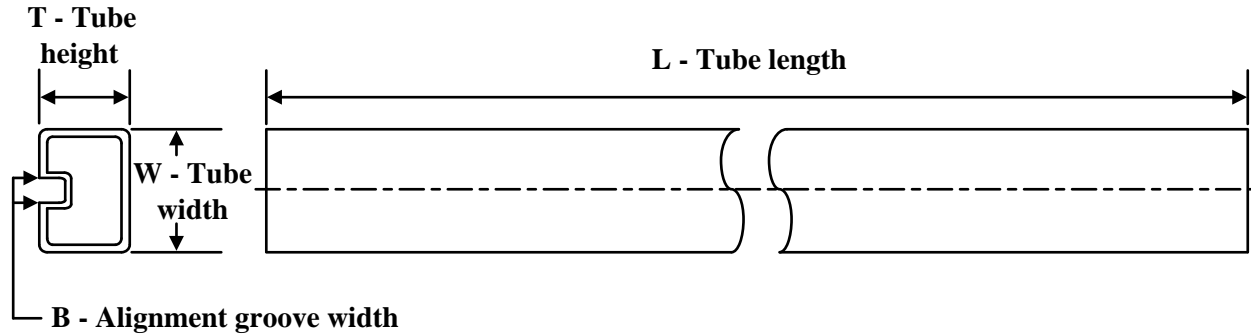

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD1470DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1470DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65HVD1471DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1471DR | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD1471DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD1473DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1474DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1474DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD1476DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1476DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65HVD1476DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65HVD1477DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD1477DR | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD1470DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1470DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1471DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1471DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1471DRG4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1473DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1474DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1474DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1476DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD1476DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1476DRG4 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1477DGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD1477DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65HVD1470D | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1470D.B | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1470DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1470DGS.B | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1471D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1471D.B | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1471DGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1471DGK.B | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1473D | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1473D.B | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1473DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1473DGS.B | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1474D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1474D.B | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1474DGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1474DGK.B | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1476D | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1476D.A | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1476D.B | D | SOIC | 14 | 50 | 507 | 7.85 | 3750 | 2.24 |
| SN65HVD1476DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1476DGS.A | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1476DGS.B | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1477D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1477D.A | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1477D.B | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN65HVD1477DGK | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1477DGK.A | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| SN65HVD1477DGK.B | DGK | VSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

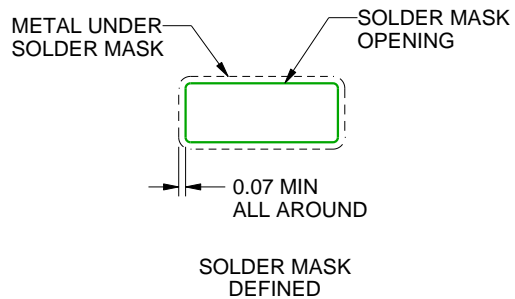
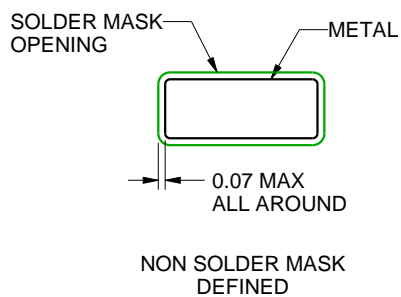
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月