SN65HVD0x、SN75HVD0x 高输出 RS-485 收发器

1 特性

- 向 54Ω 负载提供的最小差分输出电压为 2.5V
- 针对开路、短路和总线空闲情况的失效防护接收器
- 可提供 1/8 单位负载选项（总线上多达 256 个节点）
- 总线引脚 ESD 保护超过 16 kV HBM
- 驱动器输出压摆率控制选项
- 电气特性符合 ANSI TIA/EIA-485-A 标准
- 低电流待机模式：1μA（典型值）
- 用于热插拔应用的无干扰上电和断电保护
- 与业界通用的 SN75176 引脚兼容

2 应用

- 在长线路、有损耗的线路或有电噪声的环境中进行数据传输
- Profibus 线路接口
- 工业过程控制网络
- 销售点 (POS) 网络
- 电力计量
- 楼宇自动化
- 数字电机控制

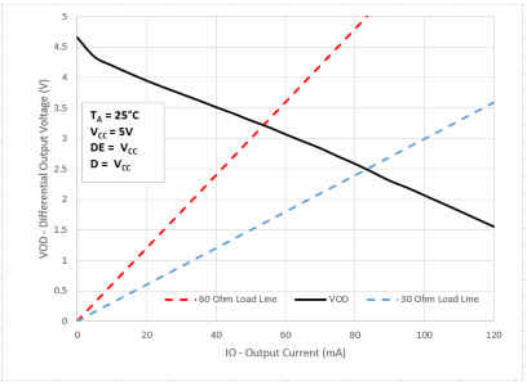


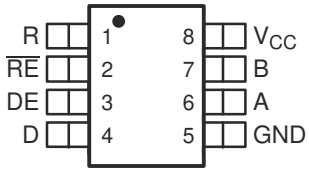
图 3-1. 差分输出电压与差分输出电流之间的关系

3 说明

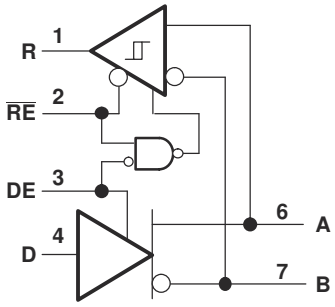
SN65HVD05 、 SN75HVD05 、 SN65HVD06 、 SN75HVD06、SN65HVD07 和 SN75HVD07 将一个三态差分线路驱动器和一个差分线路接收器组合在一起。它们专为实现平衡的数据传输而设计，可与符合 ANSI TIA/EIA-485-A 和 ISO 8482E 标准的器件进行互操作。该驱动器可提供大于这些标准所要求的差分输出电压，从而提高噪声容限。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起，用作方向控制。

驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，该端口用于在驱动器禁用或未通电时为总线提供最小负载。这些器件具有较宽的正负共模电压范围，因此适用于合用线应用。

D OR P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM
(POSITIVE LOGIC)



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (August 2009) to Revision F (March 2023)	Page
• 删除了 *订购信息* 表	1
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics*	9

Changes from Revision D (July 2006) to Revision E (August 2009)	Page
• Added IDLE Bus to the Receivers Function Table	16
• Added the Receiver Failsafe paragraph	16

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

			SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07
Supply voltage range, V_{CC}			– 0.3 V to 6 V
Voltage range at A or B			– 9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			– 0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see 图 6-11)			– 50 V to 50 V
Receiver output current, I_O			– 11 mA to 11mA
Electrostatic discharge	Human body model(3)	A, B, and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under" recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		– 7(1)		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see 图 6-7)		– 12		12	V
High-level output current, I_{OH}	Driver	– 100			mA
	Receiver	– 8			
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65HVD05	– 40		85	°C
	SN65HVD06				
	SN65HVD07				
	SN75HVD05	0		70	°C
	SN75HVD06				
	SN75HVD07				

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.3 Thermal Information

THERMAL METRIC[1]		D (SOIC) SN65 Variation	D (SOIC) SN75 Variation	P (PDIP)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	175.4	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	53.6	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	45.1	23.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	10.1	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	44.4	23.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.4 Package Dissipation Ratings

(See 图 5-1 and 图 5-2)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR[1] ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D[2]	710 mW	5.7 mW/°C	455 mW	369 mW
D[3]	1282 mW	10.3 mW/°C	821 mW	667 mW
P	1000 mW	8.0 m W/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

5.5 Driver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = – 18 mA		– 1.5			V
$\|V_{OD}\|$	Differential output voltage		No Load				V_{CC}	V
			R_L = 54 Ω, See 图 6-4		2.5			
			V_{test} = – 7 V to 12 V, See 图 6-2		2.2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See 图 6-4 and 图 6-2		– 0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		See 图 6-3		2.2		3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				– 0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD05	See 图 6-3			600		mV
		HVD06				500		
		HVD07				900		
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			– 100		0	μA
		DE			0		100	
I_{OS}	Short-circuit output current		– 7 V ≤ V_O ≤ 12 V		– 250		250	mA
$C_{(diff)}$	Differential output capacitance		V_{ID} = 0.4 sin (4E6 π t) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC} DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

5.6 Driver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD05	R_L = 54 Ω, C_L = 50 pF, See 图 6-4		6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD05			6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_r	Differential output signal rise time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
t_f	Differential output signal fall time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD05				2	ns
		HVD06				2.5	
		HVD07				10	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD05				3.5	ns
		HVD06				14	
		HVD07				100	
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See 图 6-5			25	ns
		HVD06				45	
		HVD07				250	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD05				25	ns
		HVD06				60	
		HVD07				250	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See 图 6-6			15	ns
		HVD06				45	
		HVD07				200	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD05				14	ns
		HVD06				90	
		HVD07				550	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110Ω , $\overline{RE}$ at 3 V, See 图 6-5			6	μs
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See 图 6-6			6	μs

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.7 Receiver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = – 8 mA					– 0.01	V
V_{IT-}	Negative-going input threshold voltage		I_O = 8 mA			– 0.2			
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})						35		mV
V_{IK}	Enable-input clamp voltage		I_I = – 18 mA			– 1.5			V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = – 8 mA,	See 图 6-7	4			V
V_{OL}	Low-level output voltage		V_{ID} = -200 mV,	I_{OL} = 8 mA,	See 图 6-7			0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	$\overline{RE}$ at V_{CC}		– 1		1	μA
I_I	Bus input current	HVD05	Other inputat 0 V	V_A or V_B = 12 V			0.23	0.5	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.3	0.5	
				V_A or V_B = – 7 V		– 0.4	0.13		
				V_A or V_B = – 7 V,	V_{CC} = 0 V	– 0.4	0.15		
		HVD06 HVD07	Other inputat 0 V	V_A or V_B = 12 V			0.06	0.1	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.08	0.13	
				V_A or V_B = – 7 V		– 0.1	0.05		
				V_A or V_B = – 7 V,	V_{CC} = 0 V	– 0.05	0.03		
I_{IH}	High-level input current, $\overline{RE}$		V_{IH} = 2 V			– 60	26.4		μA
I_{IL}	Low-level input current, $\overline{RE}$		V_{IL} = 0.8 V			– 60	27.4		μA
$C_{(diff)}$	Differential input capacitance		V_I = 0.4 sin (4E6 π t) + 0.5 V, DE at 0 V				16		pF
I_{CC}	Supply current		$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled and driver disabled			5	10	mA
			$\overline{RE}$ at V_{CC}, DE at 0 V, D at V_{CC}, No load	Receiver disabled and driver disabled (standby)			1	5	μA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled			9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

5.8 Receiver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output 1/2 UL	HVD05	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See 图 6-8		14.6	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output 1/2 UL	HVD05			14.6	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
t_{PHL}	Propagation delay time, high-to-low-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD05				2	ns
		HVD06				4.5	
		HVD07				4.5	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD05				6.5	ns
		HVD06				14	
		HVD07				14	
t_r	Output signal rise time		C_L = 15 pF, See 图 6-8		2	3	ns
t_f	Output signal fall time				2	3	
t_{PZH1}	Output enable time to high level		C_L = 15 pF, DE at 3 V, See 图 6-9			10	ns
t_{PZL1}	Output enable time to low level					10	
t_{PHZ}	Output disable time from high level					15	
t_{PLZ}	Output disable time from low level					15	
t_{PZH2}	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0, See 图 6-10			6	µs
t_{PZL2}	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.9 Typical Characteristics

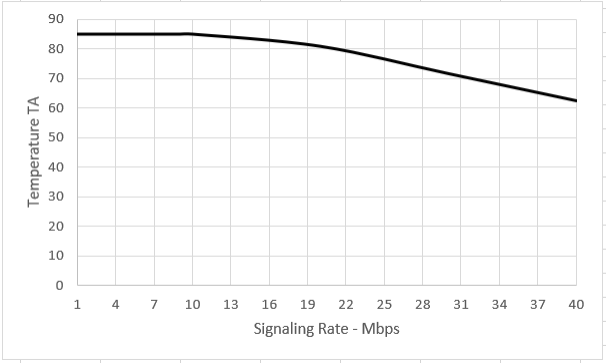


图 5-1. HVD05 Maximum Recommended Still-Air Operating Temperature vs Signaling Rate (D-Package)

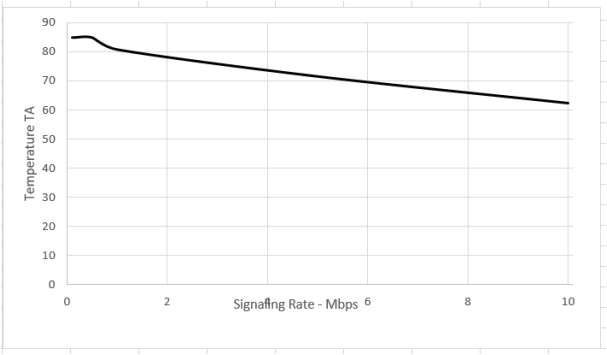


图 5-2. HVD06 Maximum Recommended Still-Air Operating Temperature vs Signaling Rate (D-Package)

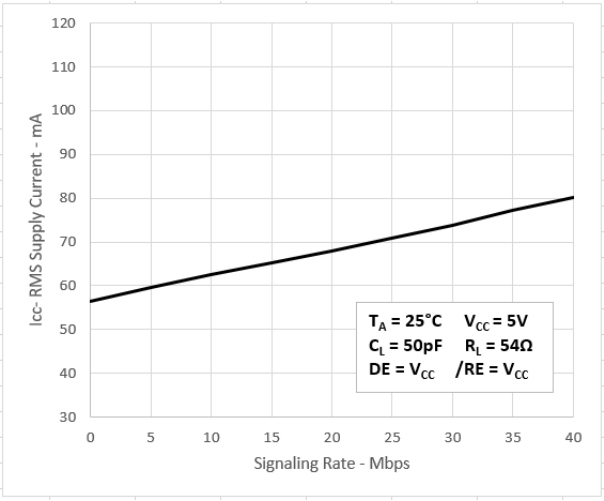


图 5-3. HVD05 RMS Supply Current vs Signaling Rate

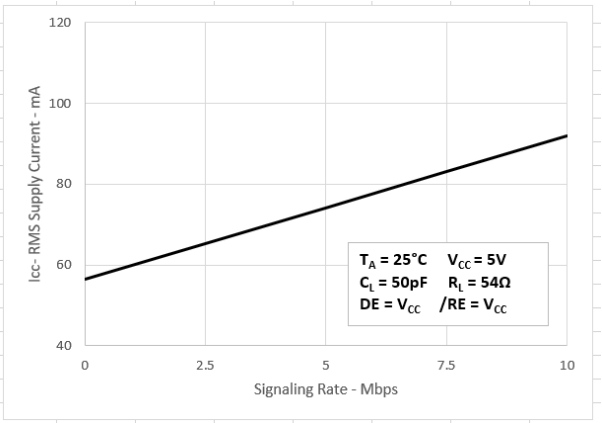


图 5-4. HVD06 RMS Supply Current vs Signaling Rate

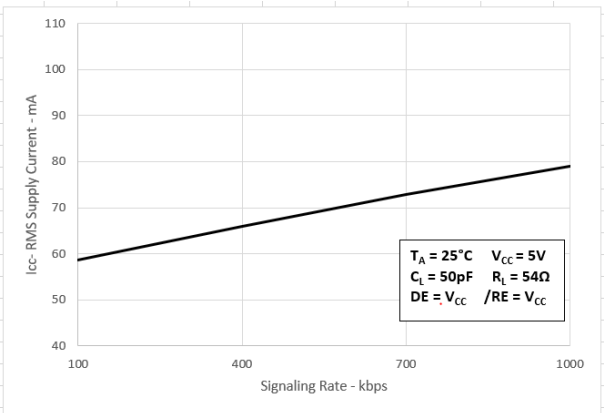


图 5-5. HVD07 RMS Supply Current vs Signaling Rate

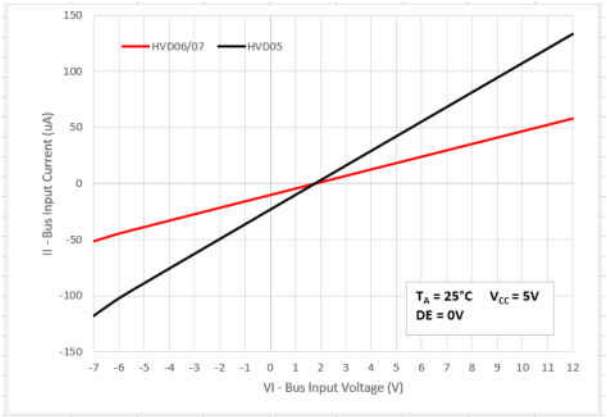


图 5-6. BUS Input Current vs BUS Input Voltage

5.9 Typical Characteristics (continued)

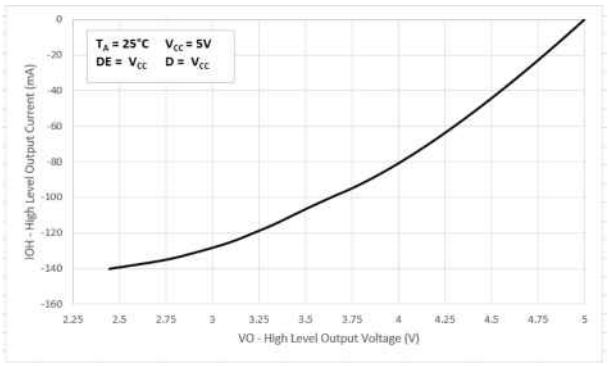


图 5-7. Driver High-Level Output Current vs High-Level Output Voltage

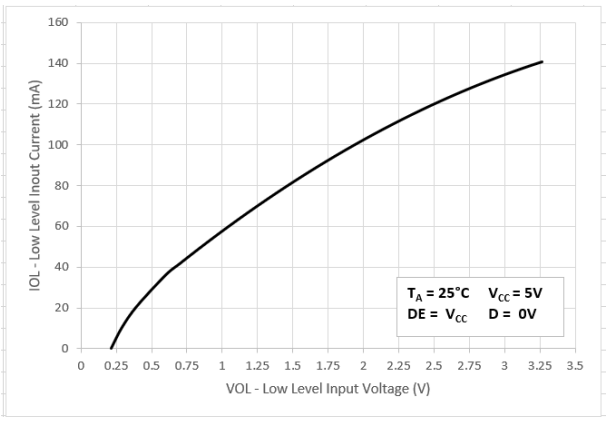


图 5-8. Driver Low-Level Output Current vs Low-Level Output Voltage

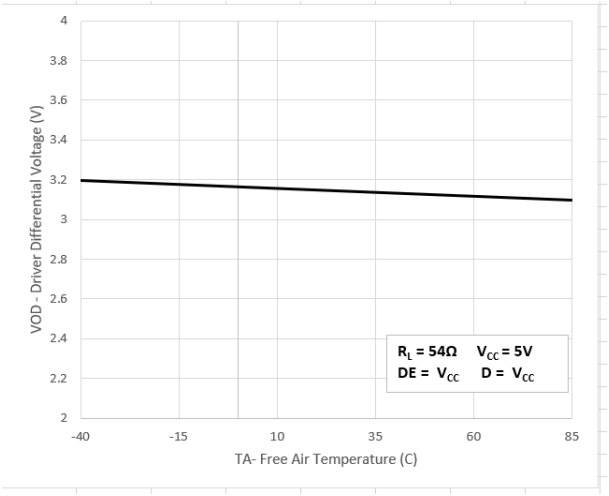


图 5-9. Differential Output Voltage vs Free-Air Temperature

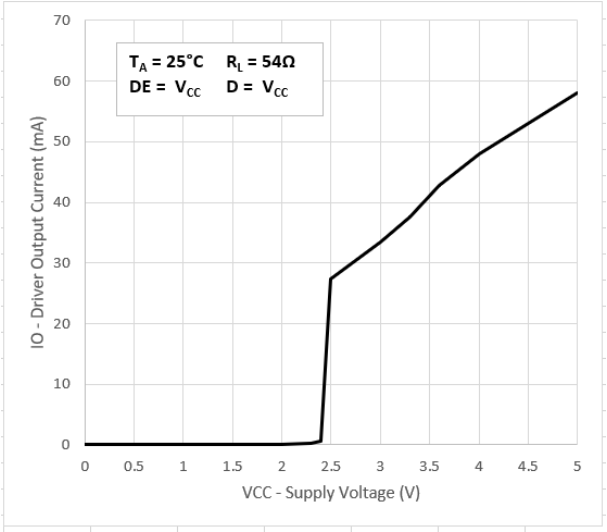


图 5-10. Driver Output Current vs Supply Voltage

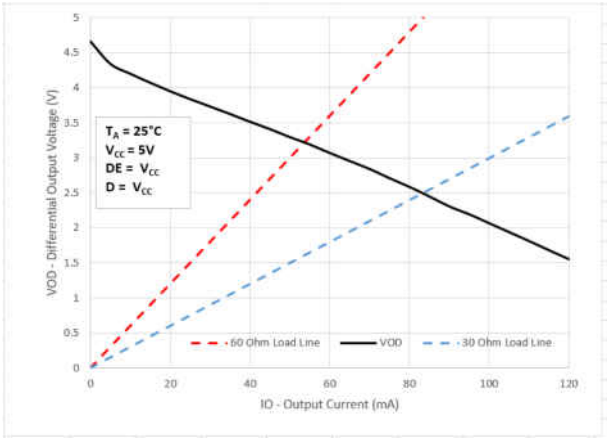


图 5-11. Differential Output Voltage vs Differential Output Current

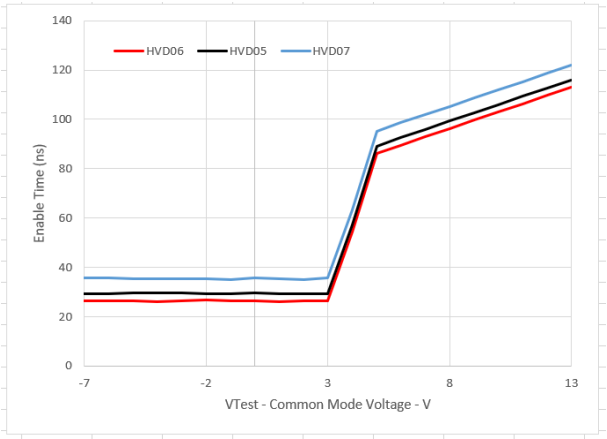


图 5-12. Enable Time vs Common-Mode Voltage (See 图 5-13)

5.9 Typical Characteristics (continued)

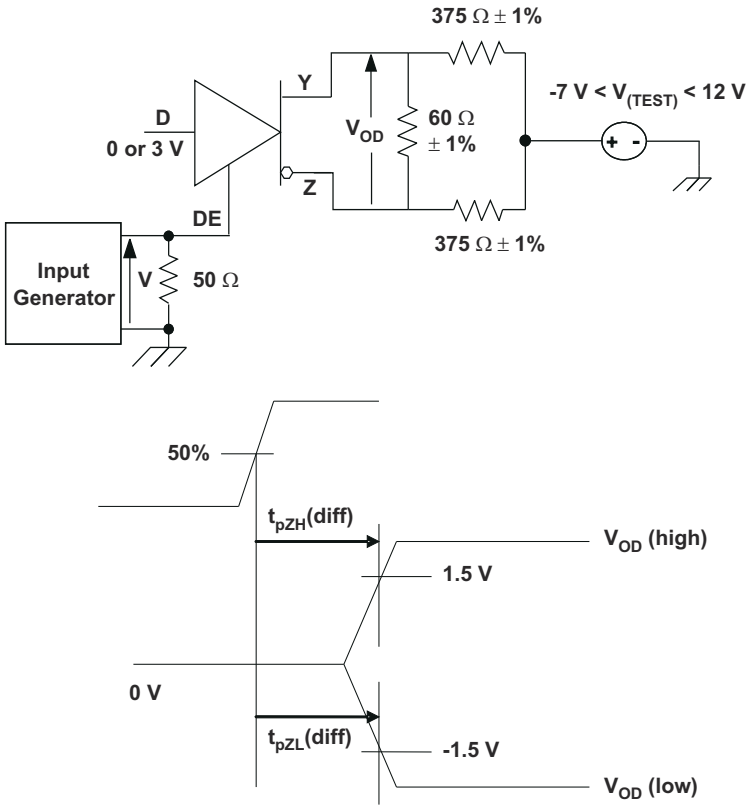


图 5-13. Driver Enable Time From DE to V_{OD}

Parameter Measurement Information

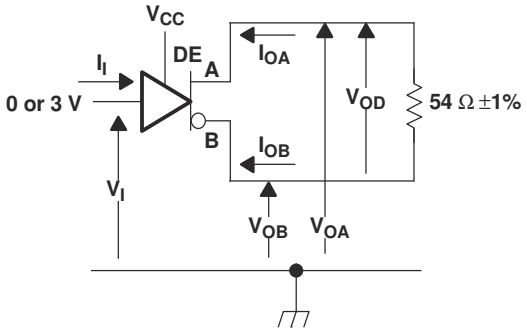


图 6-1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

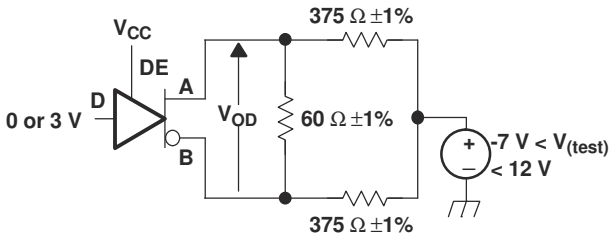
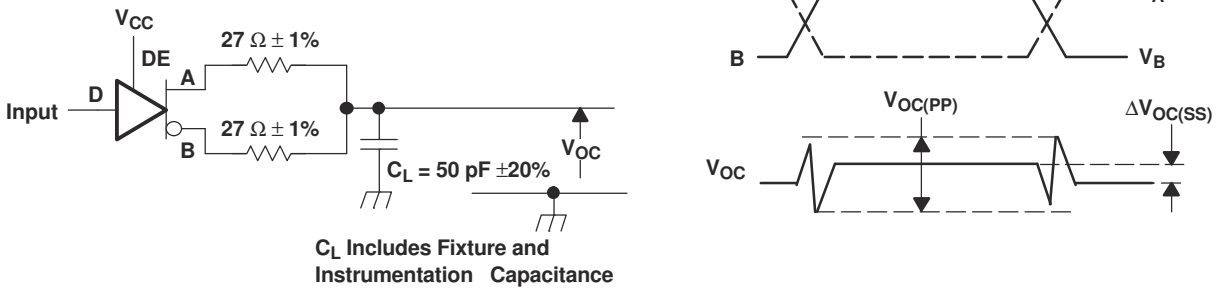
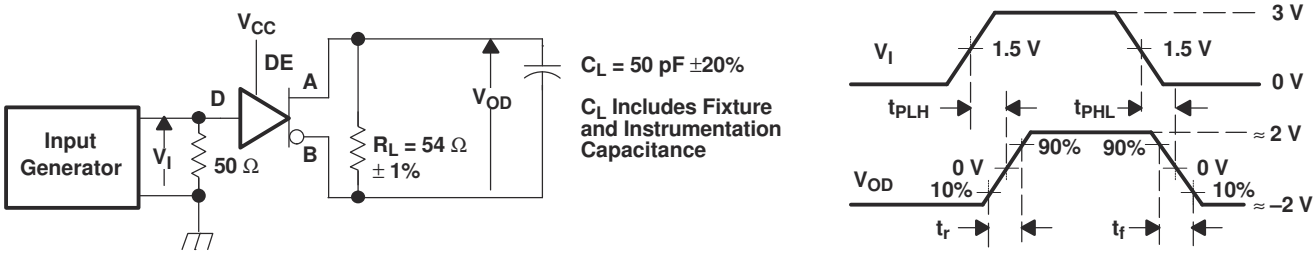


图 6-2. Driver V_{OD} With Common-Mode Loading Test Circuit



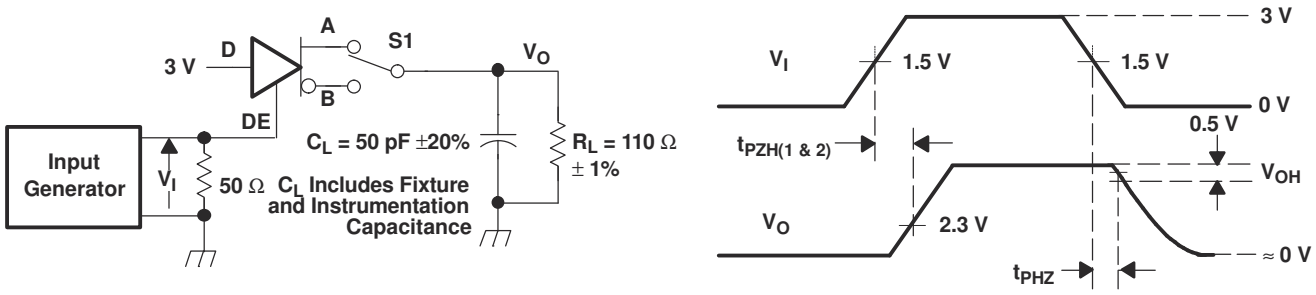
Input: PRR = 500 kHz, 50% Duty Cycle,t_r<6ns, t_f<6ns, Z_O = 50 Ω

图 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



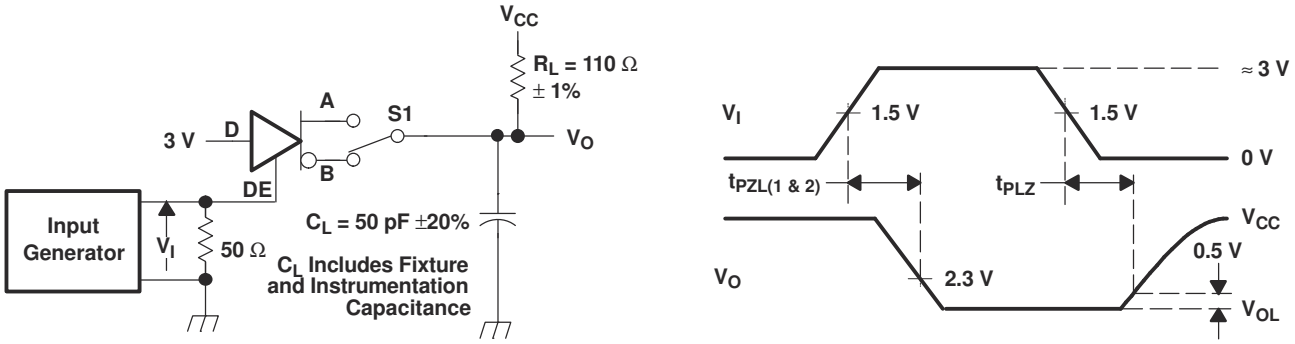
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

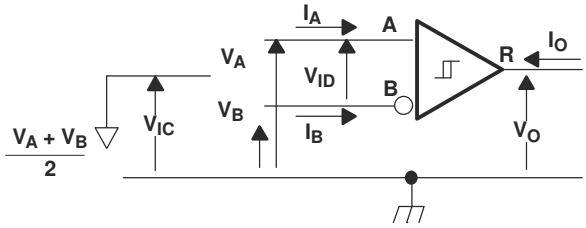
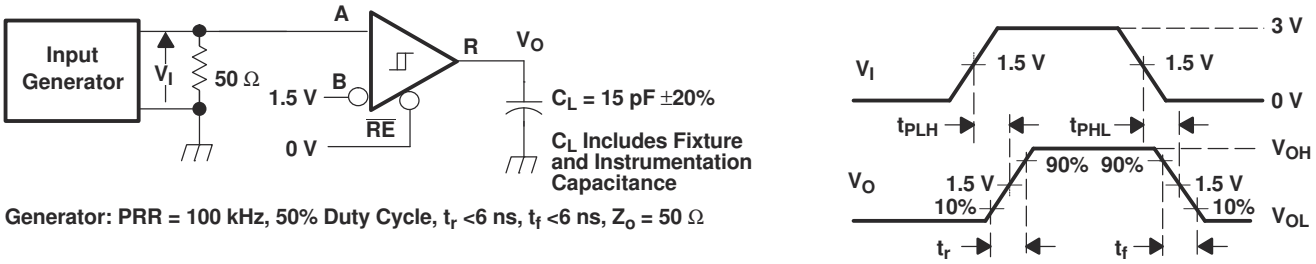


图 6-7. Receiver Voltage and Current Definitions



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-8. Receiver Switching Test Circuit and Voltage Waveforms

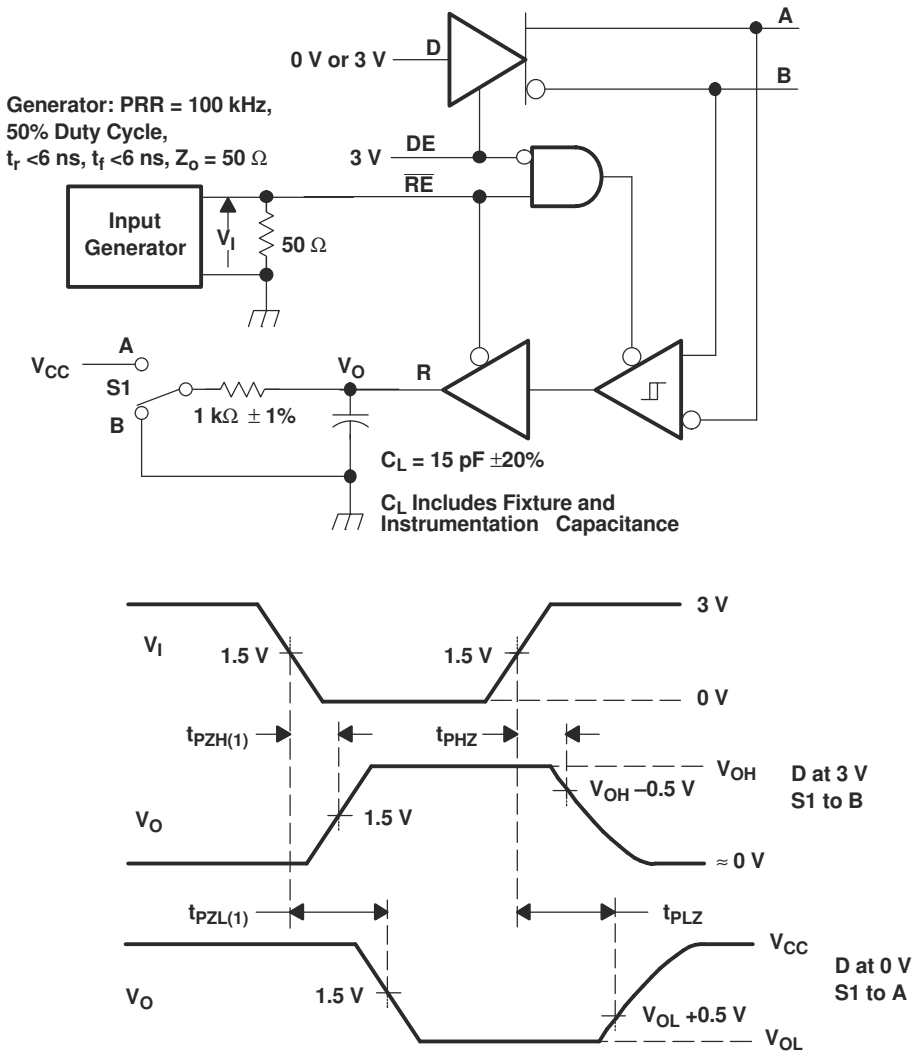


图 6-9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

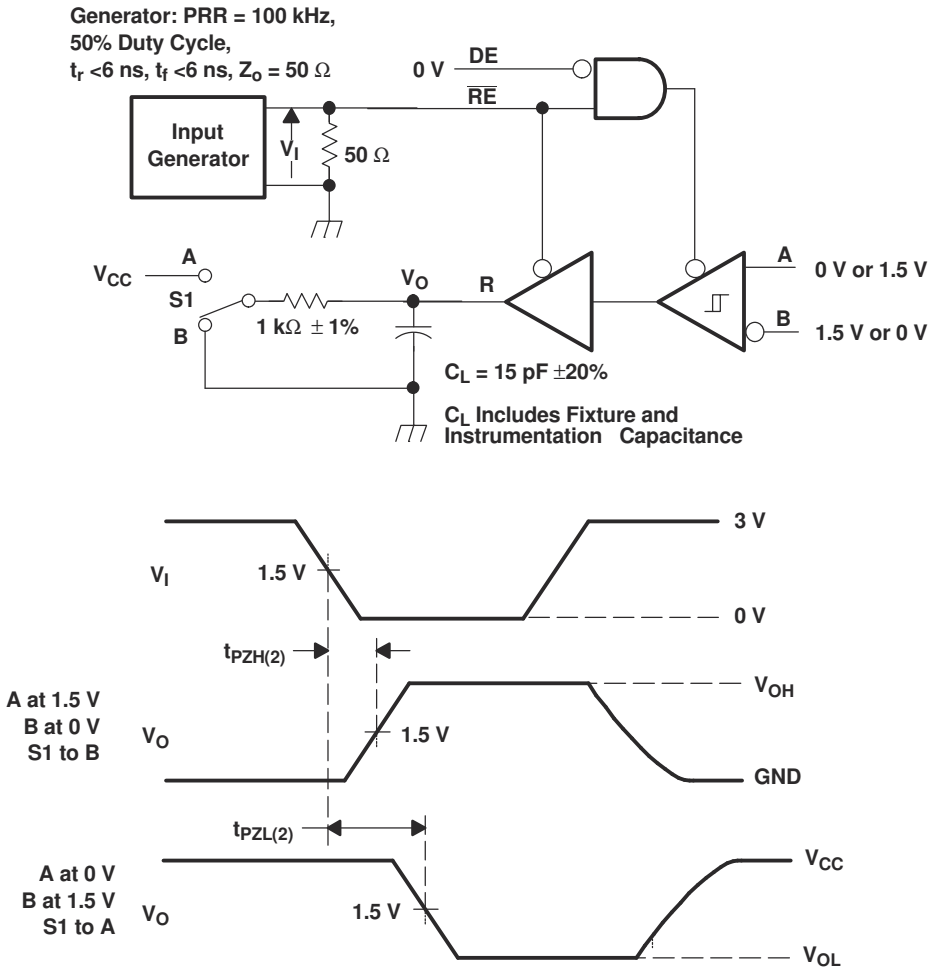
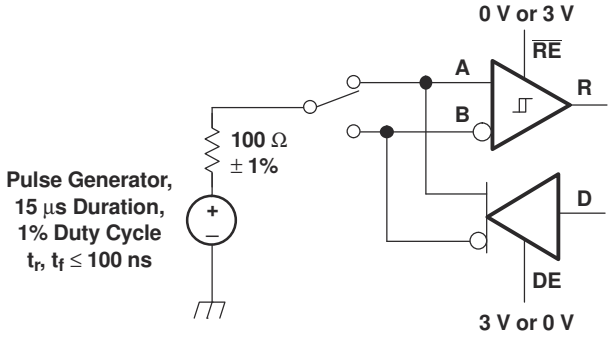


图 6-10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

图 6-11. Test Circuit, Transient Over Voltage Test

6 Function Tables

表 6-1. DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L
X	Open	Z	Z

表 6-2. RECEIVER

DIFFERENTIAL INPUTS(1)	ENABLE	OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \leqslant -0.2$ V	L	L
-0.2 V < V_{ID} < -0.01 V	L	?
-0.01 V $\leqslant V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H
IDLE Bus	L	H
X	Open	Z

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

6.1 Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

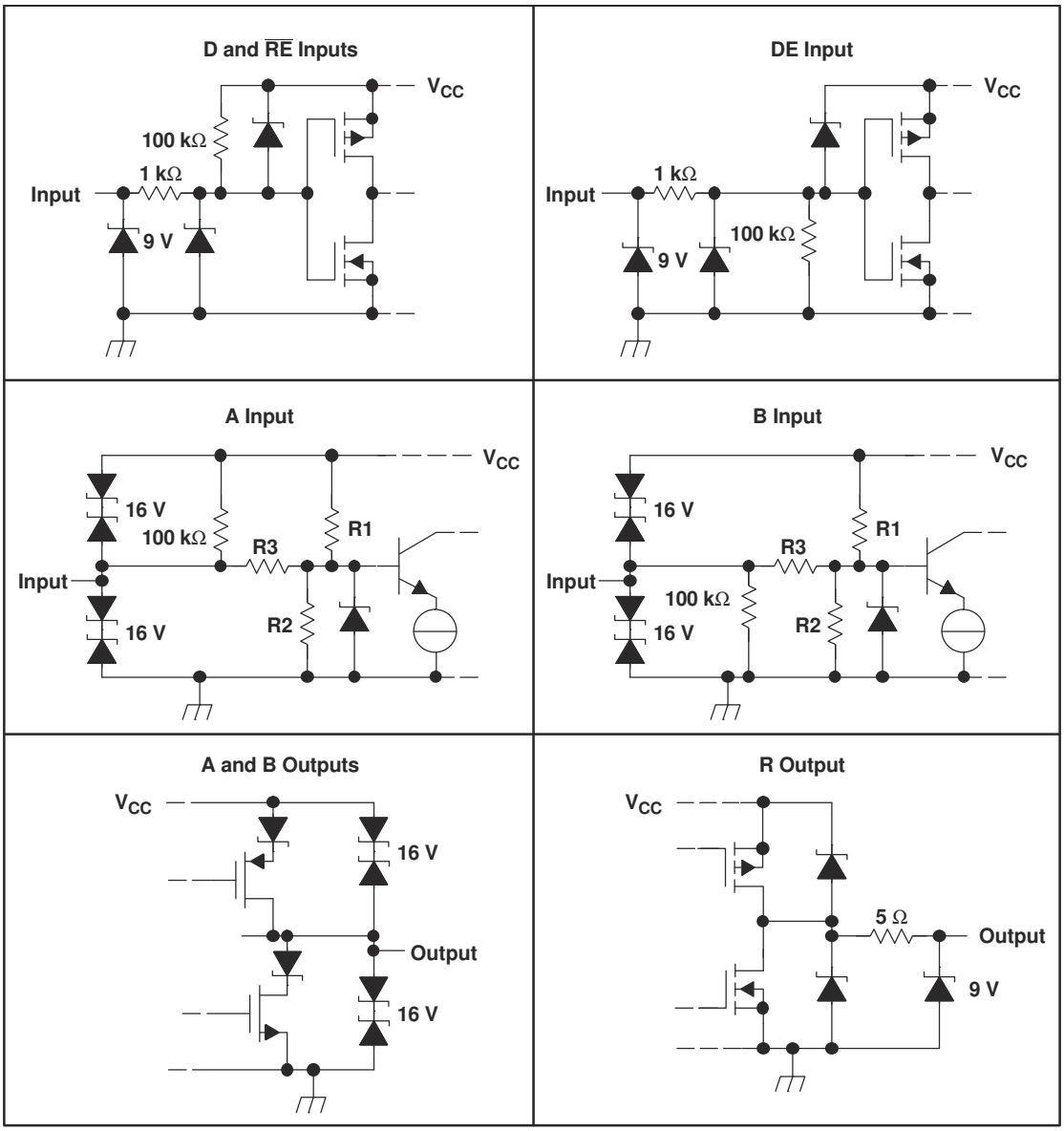
- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output *must* output a High when the differential input V_{ID} is more positive than +200 mV, and *must* output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. As seen in the Receiver Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will *always* cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

7 Equivalent Input and Output Schematic Diagrams



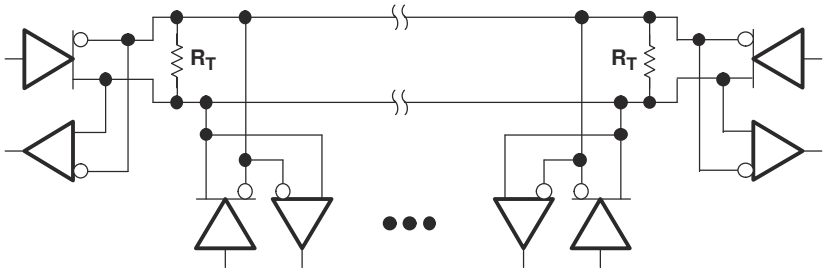
	R1/R2	R3
SN65HVD05	9 kΩ	45 kΩ
SN65HVD06	36 kΩ	180 kΩ
SN65HVD07	36 kΩ	180 kΩ

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

Typical Application



Device	Number of Devices on Bus
HVD05	64
HVD06	256
HVD07	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD05D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP05
SN65HVD05DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP05
SN65HVD05P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD05
SN65HVD05P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD05
SN65HVD06DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP06
SN65HVD06DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP06
SN65HVD06P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD06
SN65HVD06P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD06
SN65HVD07D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP07
SN65HVD07DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP07
SN65HVD07P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD07
SN65HVD07P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD07
SN75HVD05D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN05
SN75HVD05P	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	0 to 70	75HVD05
SN75HVD06D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD06D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD06DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD06DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN06
SN75HVD07D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN07
SN75HVD07P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD07

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75HVD07P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD07

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

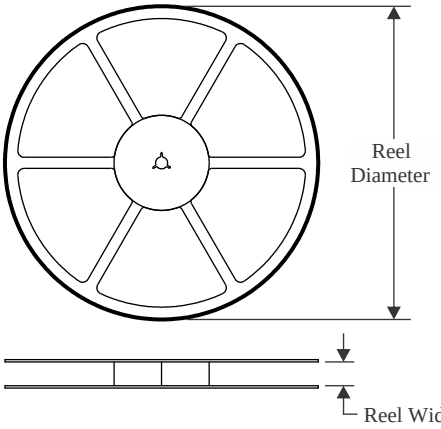
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

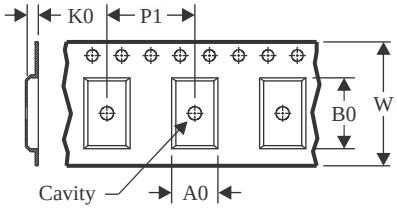
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

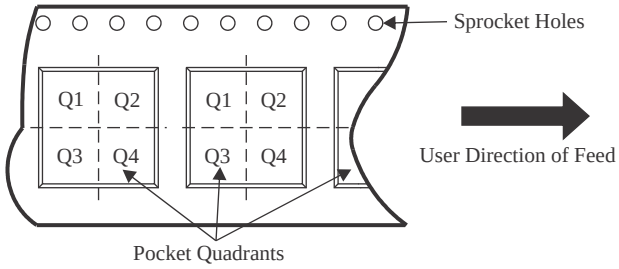


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

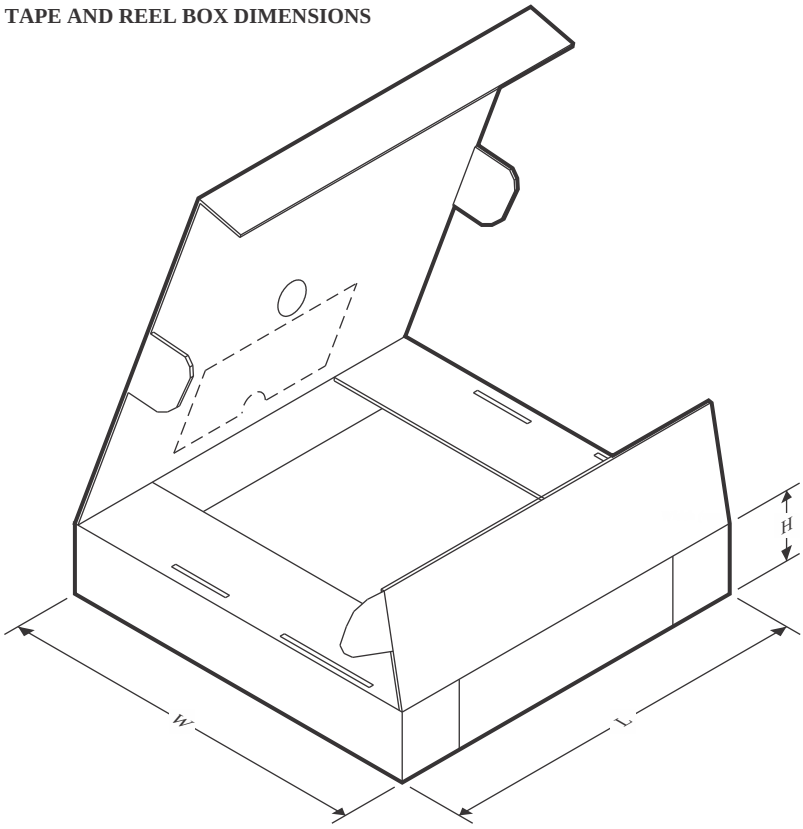
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD05DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD05DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD06DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD07DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD07DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD06DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD07DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

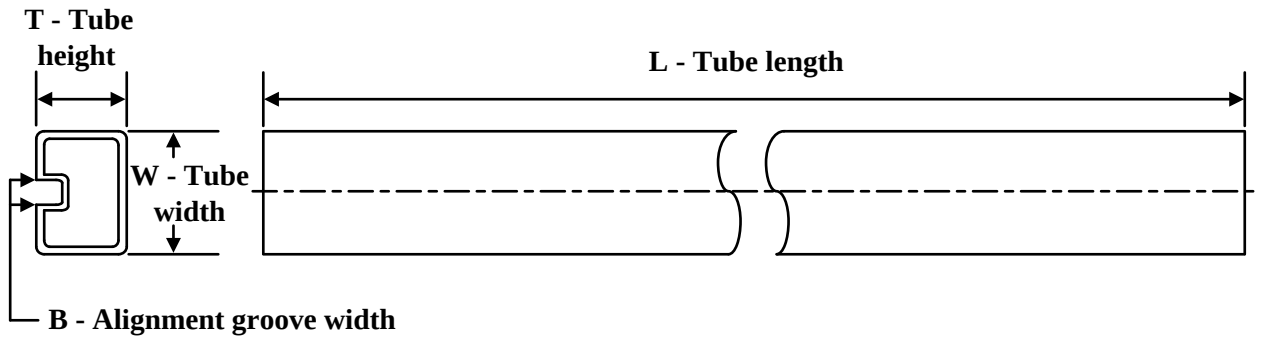
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

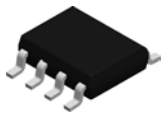
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD05DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD05DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD06DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD07DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD07DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN75HVD06DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75HVD07DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD05P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD05P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD06P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD06P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD07P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD07P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD06D	D	SOIC	8	75	507	8	3940	4.32
SN75HVD06D.A	D	SOIC	8	75	507	8	3940	4.32
SN75HVD07D	D	SOIC	8	75	507	8	3940	4.32
SN75HVD07D.A	D	SOIC	8	75	507	8	3940	4.32
SN75HVD07P	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD07P.A	P	PDIP	8	50	506	13.97	11230	4.32

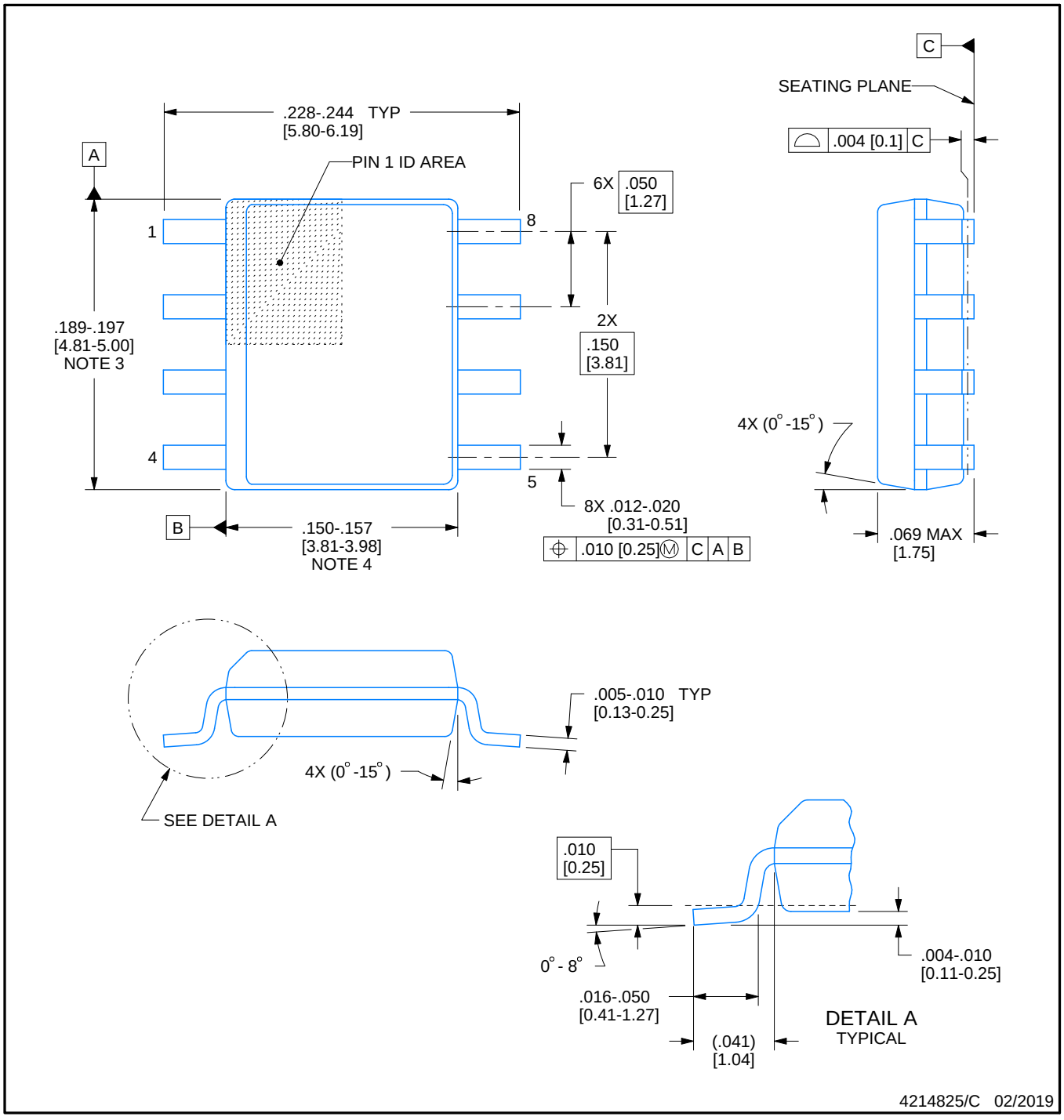


PACKAGE OUTLINE

D0008A

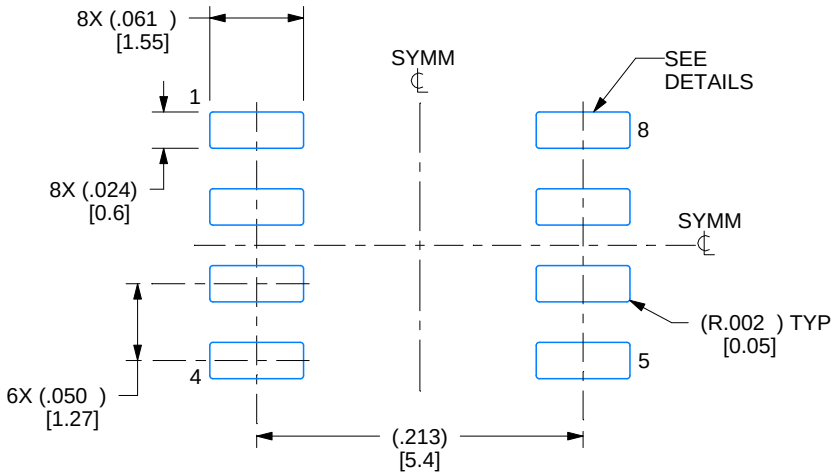
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

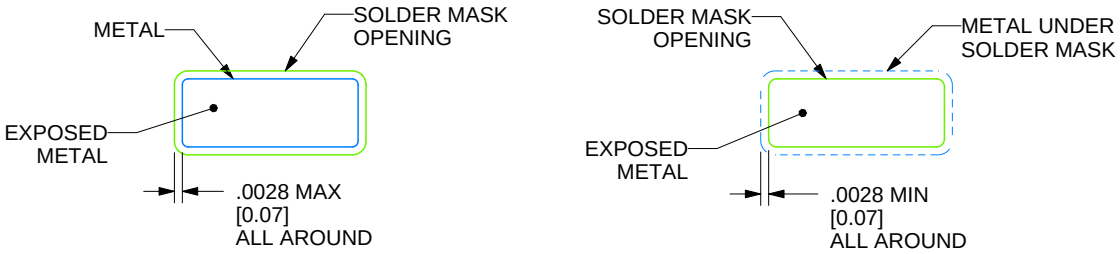


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

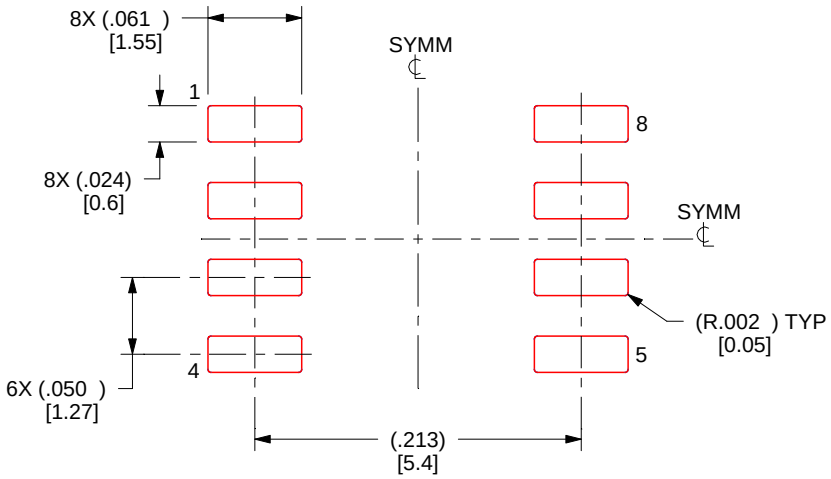
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



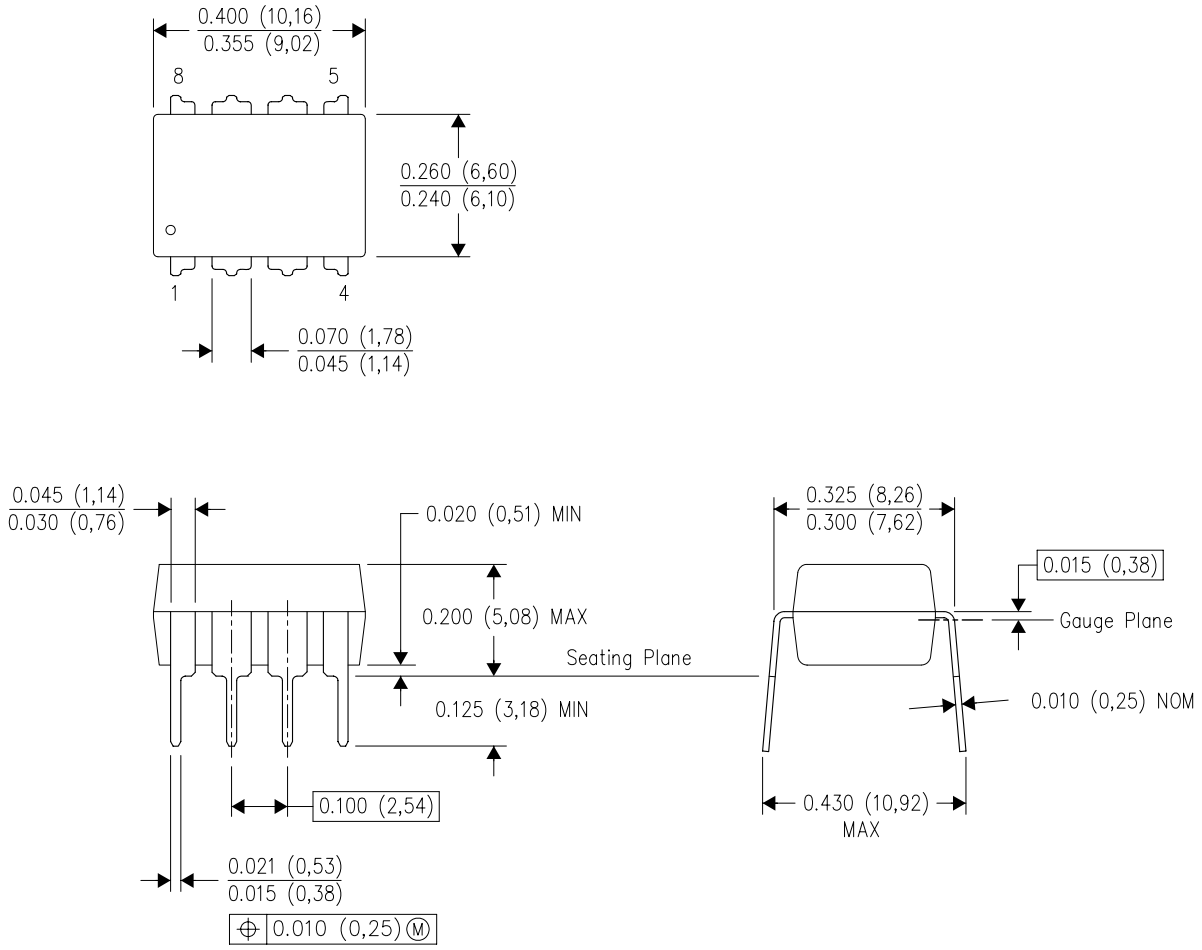
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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