

# SN64BCT245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS040A – JANUARY 1990 – REVISED JANUARY 1994

- BiCMOS Design Significantly Reduces  $I_{CCZ}$
- 3-State True Outputs Drive Bus Lines Directly
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)

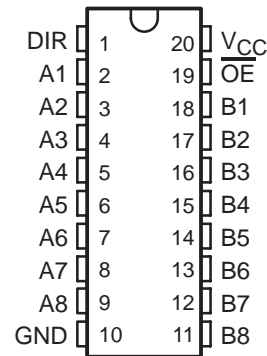
## description

This octal bus transceiver is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

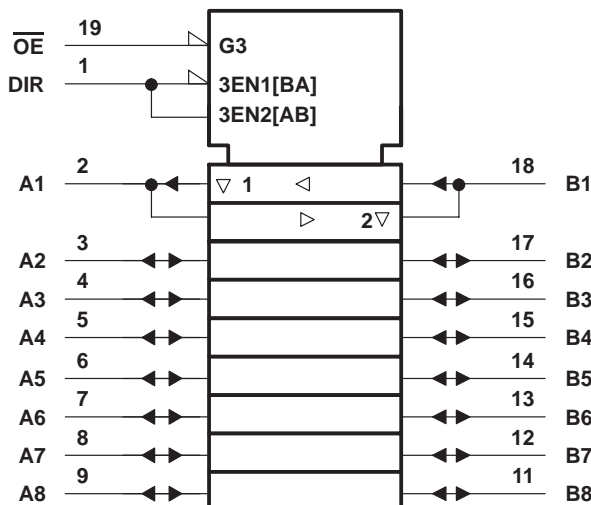
DW OR N PACKAGE  
(TOP VIEW)



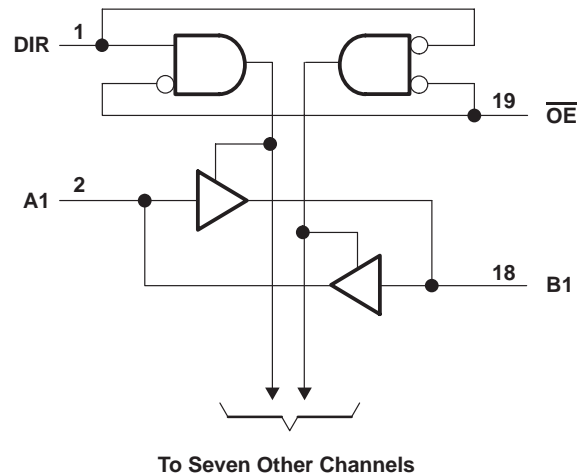
FUNCTION TABLE

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN64BCT245

## OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|   |                     |
|---|---------------------|
| Supply voltage range, $V_{CC}$  | – 0.5 V to 7 V      |
| Input voltage range, $V_I$ (see Note 1)                                       | – 0.5 V to 7 V      |
| Voltage range applied to any output in the disabled or power-off state, $V_O$ | – 0.5 V to 5.5 V    |
| Voltage range applied to any output in the high state, $V_O$                  | – 0.5 V to $V_{CC}$ |
| Current into any output in the low state                                      | 128 mA              |
| Operating free-air temperature range  | – 40°C to 85°C      |
| Storage temperature range   | – 65°C to 150°C     |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

#### recommended operating conditions

|          |                                | MIN     | NOM | MAX | UNIT |
|----------|--------------------------------|---------|-----|-----|------|
| $V_{CC}$ | Supply voltage                 | 4.5     | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2       |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |         |     | 0.8 | V    |
| $I_{IK}$ | Input clamp current            |         |     | –18 | mA   |
| $I_{OH}$ | High-level output current      | A1 – A8 |     | –3  | mA   |
|          |                                | B1 – B8 |     | –15 |      |
| $I_{OL}$ | Low-level output current       | A1 – A8 |     | 24  | mA   |
|          |                                | B1 – B8 |     | 64  |      |
| $T_A$    | Operating free-air temperature | –40     |     | 85  | °C   |



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## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                                | TEST CONDITIONS                     |                                      | MIN  | TYP† | MAX   | UNIT          |
|-------------------|--------------------------------|-------------------------------------|--------------------------------------|------|------|-------|---------------|
| $V_{IK}$          |                                | $V_{CC} = 4.5\text{ V}$ ,           | $I_I = -18\text{ mA}$                |      |      | -1.2  | V             |
| $V_{OH}$          | Any A                          | $V_{CC} = 4.5\text{ V}$             | $I_{OH} = -1\text{ mA}$              | 2.5  | 3.4  |       | V             |
|                   | Any A or B                     |                                     | $I_{OH} = -3\text{ mA}$              | 2.4  | 3.3  |       |               |
|                   | Any B                          |                                     | $I_{OH} = -15\text{ mA}$             | 2    | 3.1  |       |               |
| $V_{OL}$          | Any A                          | $V_{CC} = 4.5\text{ V}$             | $I_{OL} = 24\text{ mA}$              |      | 0.35 | 0.5   | V             |
|                   | Any B                          |                                     | $I_{OL} = 64\text{ mA}$              |      | 0.42 | 0.55  |               |
| $I_{OZ}$          | Power up                       | $V_{CC} = 0\text{ to }2.3\text{ V}$ | $V_O = 2.7\text{ V}$                 |      |      | 70    | $\mu\text{A}$ |
|                   |                                |                                     | $V_O = 0.5\text{ V}$                 |      |      | -0.65 | $\text{mA}$   |
|                   | Power down                     | $V_{CC} = 1.8\text{ V to }0$        | $V_O = 2.7\text{ V}$                 |      |      | 70    | $\mu\text{A}$ |
|                   |                                |                                     | $V_O = 0.5\text{ V}$                 |      |      | -0.65 | $\text{mA}$   |
| $I_I^\ddagger$    | A and B                        | $V_{CC} = 5.5\text{ V}$ ,           | $V_I = 5.5\text{ V}$                 |      |      | 1     | $\text{mA}$   |
|                   | DIR and $\overline{\text{OE}}$ |                                     |                                      |      |      | 0.1   |               |
| $I_{IH}^\ddagger$ | A and B                        | $V_{CC} = 5.5\text{ V}$ ,           | $V_I = 2.7\text{ V}$                 |      |      | 70    | $\mu\text{A}$ |
|                   | DIR and $\overline{\text{OE}}$ |                                     |                                      |      |      | 20    |               |
| $I_{IL}$          | A and B                        | $V_{CC} = 5.5\text{ V}$ ,           | $V_I = 0.5\text{ V}$                 |      |      | -0.65 | $\text{mA}$   |
|                   | DIR and $\overline{\text{OE}}$ |                                     |                                      |      |      | -1.2  |               |
| $I_{OS}^\S$       | Any A                          | $V_{CC} = 5.5\text{ V}$ ,           | $V_O = 0$                            | -60  |      | -150  | $\text{mA}$   |
|                   | Any B                          |                                     |                                      | -100 |      | -225  |               |
| $I_{CCH}$         | A-to-B                         | $V_{CC} = 5.5\text{ V}$             |                                      |      | 36   | 57    | $\text{mA}$   |
| $I_{CCL}$         | A-to-B                         | $V_{CC} = 5.5\text{ V}$             |                                      |      | 57   | 90    |               |
| $I_{CCZ}$         |                                | $V_{CC} = 5.5\text{ V}$             |                                      |      | 10   | 15    |               |
| $C_i$             | $\overline{\text{OE}}$ and DIR | $V_{CC} = 5\text{ V}$ ,             | $V_I = 2.5\text{ V or }0.5\text{ V}$ |      | 7    |       | $\text{pF}$   |
| $C_{io}$          | A to B                         | $V_{CC} = 5\text{ V}$ ,             | $V_I = 2.5\text{ V or }0.5\text{ V}$ |      | 9    |       | $\text{pF}$   |
|                   | B to A                         |                                     |                                      |      | 12   |       |               |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

### switching characteristics (see Note 2)

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = 25°C |      | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω |      |                                 |      | UNIT |
|------------------|------------------------|----------------|--|------|---|------|---------------------------------|------|------|
|                  |                        |                |  |      | T <sub>A</sub> = −40°C<br>to 85°C   |      | T <sub>A</sub> = 0°C<br>to 70°C |      |      |
|                  |                        |                | MIN  | MAX  | MIN   | MAX  | MIN                             | MAX  |      |
| t <sub>PLH</sub> | A or B                 | B or A         | 1  | 6    | 1   | 7.2  | 1                               | 7    | ns   |
| t <sub>PHL</sub> |                        |                | 1.5  | 6.6  | 1.5   | 7.6  | 1.5                             | 7    |      |
| t <sub>PZH</sub> | $\overline{\text{OE}}$ | A or B         | 1.5  | 9.4  | 1.5   | 11.2 | 1.5                             | 10.9 | ns   |
| t <sub>PZL</sub> |                        |                | 1.5  | 10.2 | 1.5   | 11.8 | 1.5                             | 11.6 |      |
| t <sub>PHZ</sub> | $\overline{\text{OE}}$ | A or B         | 1.5  | 8.3  | 1.5   | 9.7  | 1.5                             | 9.3  | ns   |
| t <sub>PLZ</sub> |                        |                | 1.5  | 7.8  | 1.5   | 9.6  | 1.5                             | 9.1  |      |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.





## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN64BCT245DW</a> | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6BCT245             |
| SN64BCT245DW.A               | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6BCT245             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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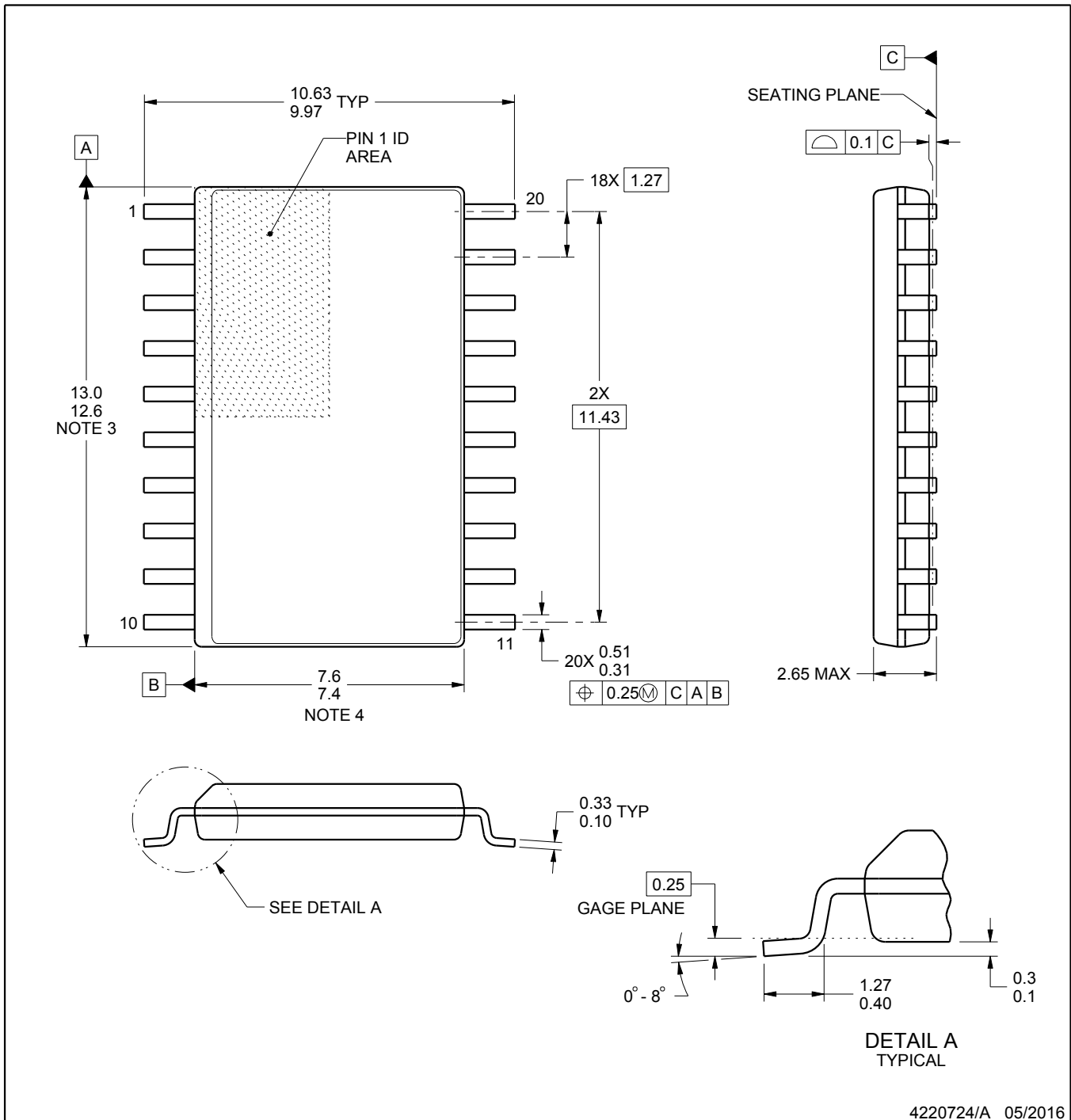
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## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN64BCT245DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN64BCT245DW.A | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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