

SN5426, SN54LS26, SN7426, SN74LS26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

DECEMBER 1983—REVISED MARCH 1988

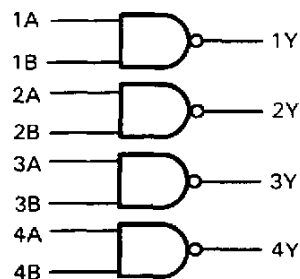
- For Driving Low-Threshold-Voltage MOS Inputs

description

These 2-input open-collector NAND gates feature high-output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source.

The SN5426 and SN54LS26 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7426 and SN74LS26 are characterized for operation from 0°C to 70°C .

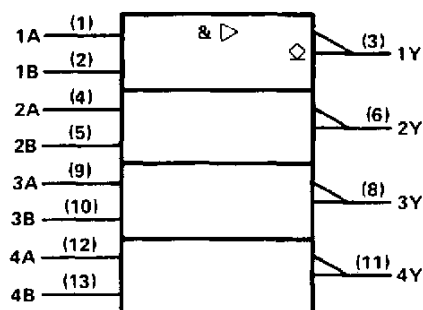
logic diagram



positive logic

$$Y = \overline{AB}$$

logic symbol†

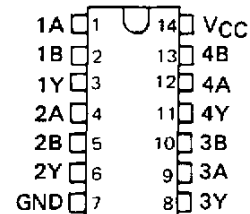


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

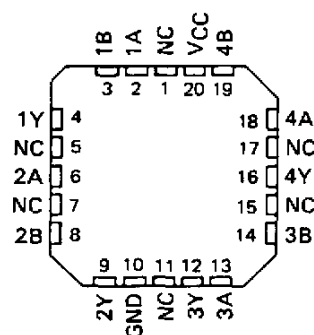
SN5426 . . . J PACKAGE
SN54LS26 . . . J OR W PACKAGE
SN7426 . . . N PACKAGE
SN74LS26 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS26 . . . FK PACKAGE

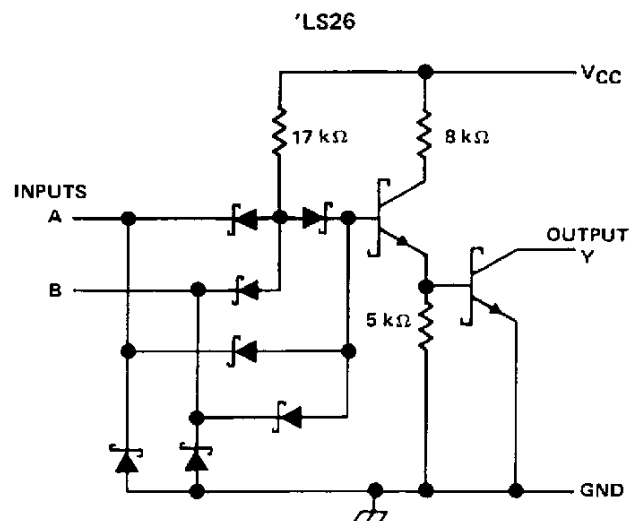
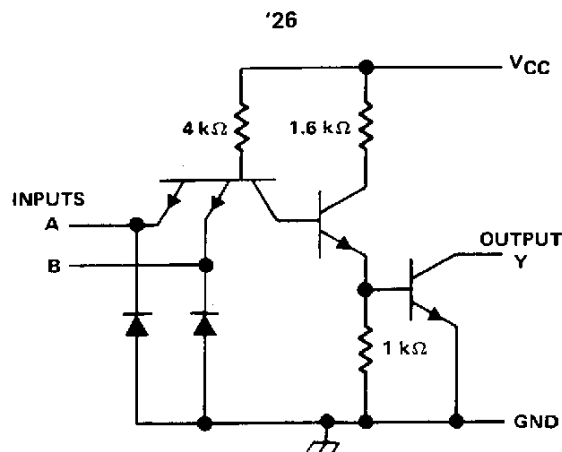
(TOP VIEW)



NC - No internal connection

SN5426, SN54LS26, SNSN7426, SN74LS26 **QUADRUPLE 2-INPUT** **HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES**

schematics



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---------------------------------------|--|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '26 | 5.5 V |
| 'LS26 | 7 V |
| Operating free-air temperature: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS26, SN74LS26
QUADRUPL 2-INPUT
HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

recommended operating conditions

| | SN54LS26 | | | SN74LS26 | | | UNIT |
|---|----------|-----|-----|----------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.7 | | | 0.8 | V |
| V _{OH} High-level output voltage | | | 15 | | | 15 | V |
| I _{OL} Low-level output current | | | 4 | | | 8 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS26 | | | SN74LS26 | | | UNIT |
|------------------|--|----------|------|-----|----------|------|-----|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | -1.5 | | | -1.5 | | V |
| I _{OH} | V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 12 V | | | 50 | | | 50 | μA |
| | V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 15 V | | | 1 | | | 1 | mA |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA | 0.25 | 0.4 | | 0.25 | 0.4 | | V |
| | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA | | | | 0.35 | 0.5 | | |
| I _I | V _{CC} = MAX, V _I = 7 V | | 0.1 | | | 0.1 | | mA |
| I _{IH} | V _{CC} = MAX, V _{IH} = 2.7 V | | 20 | | | 20 | | μA |
| I _{IL} | V _{CC} = MAX, V _{IL} = 0.4 V | | -0.4 | | | -0.4 | | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 | 0.8 | 1.6 | | 0.8 | 1.6 | | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | 2.4 | 4.4 | | 2.4 | 4.4 | | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|---|-----|-----|-----|------|
| t _{PLH} | A or B | Y | R _L = 2 kΩ, C _L = 15 pF | | 17 | 32 | ns |
| t _{PHL} | | | | | 15 | 28 | ns |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN5426, SN7426
QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

recommended operating conditions

| | SN5426 | | | SN7426 | | | UNIT |
|---|--------|-----|-----|--------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| V _{OH} High-level output voltage | | | 15 | | | 15 | V |
| I _{OL} Low-level output current | | | 16 | | | 16 | mA |
| T _A Operating free-air temperature | - 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN5426 | | | SN7426 | | | UNIT |
|-------------------|--|--------|------|------|--------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -12 mA | | | -1.5 | | | -1.5 | V |
| I _{OH} | V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 12 V | | | | | | 50 | μA |
| | V _{CC} = MIN, V _{IL} = 0.7 V, V _{OH} = 12 V | | | 50 | | | | |
| | V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 15 V | | | | | | 1 | mA |
| | V _{CC} = MIN, V _{IL} = 0.7 V, V _{OH} = 15 V | | | 1 | | | | |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA | | | 0.4 | | | 0.4 | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.4 V | | | 40 | | | 40 | μA |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | -1.6 | | | -1.6 | mA |
| I _{CCCH} | V _{CC} = MAX, V _I = 0 | | | 4 | | | 4 | mA |
| I _{CCCL} | V _{CC} = MAX, V _I = 4.5 V | | | 12 | | | 12 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|---|-----|-----|-----|------|
| t _{PLH} | A or B | Y | R _L = 1 kΩ, C _L = 15 pF | | 16 | 24 | ns |
| t _{PHL} | | | | | 11 | 17 | ns |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS26DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS26DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-7602001VDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-7602001VDA.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 7602001DA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32102BDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32102BDA.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/32102BDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LS26N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS26N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS26N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS26N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS26W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS26W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

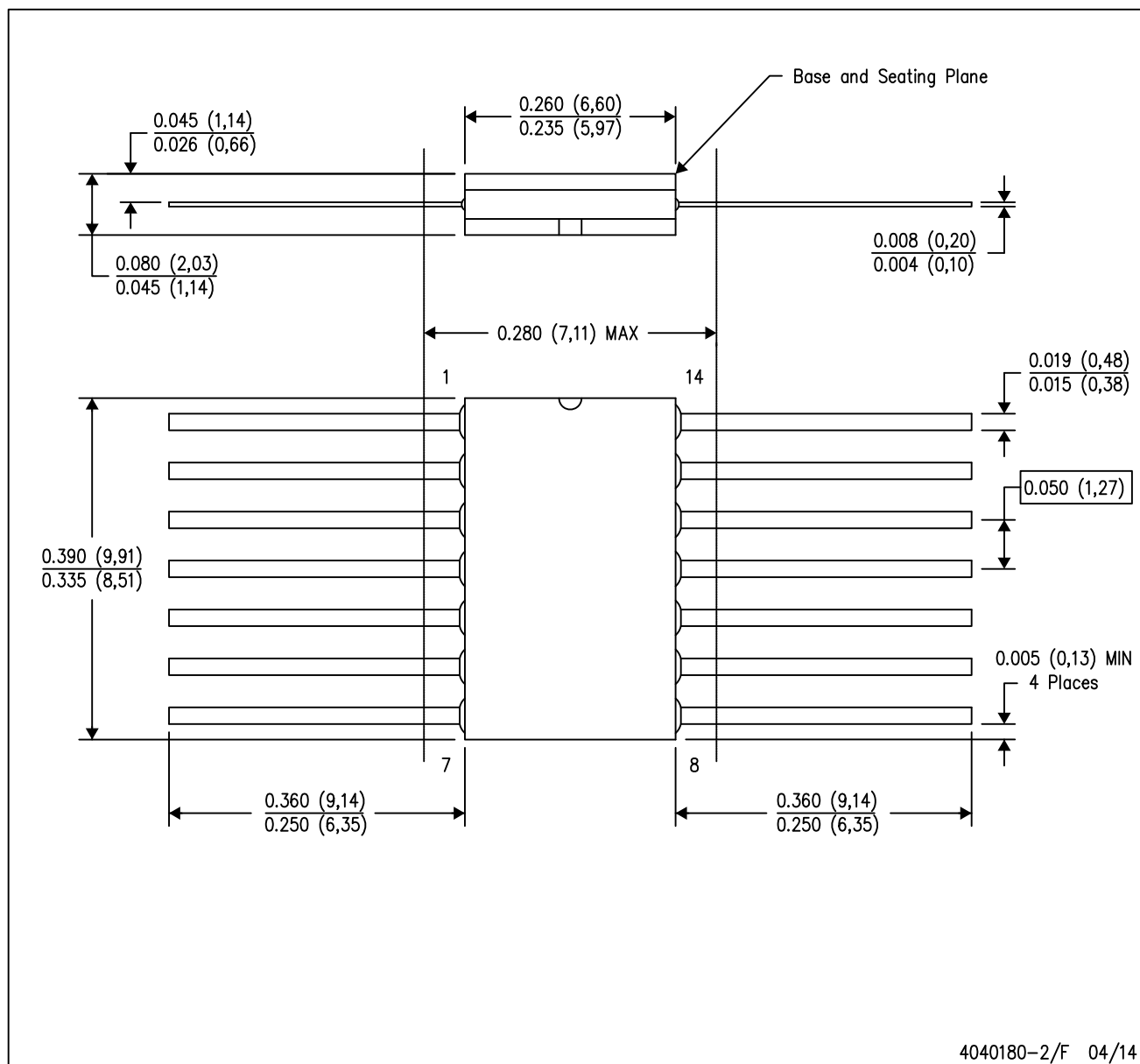
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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