- **Functionally Equivalent to AMD's AM29823 and AM29824**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Outputs Have Undershoot-Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce dc Loading Effects**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

## description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing, and working registers.

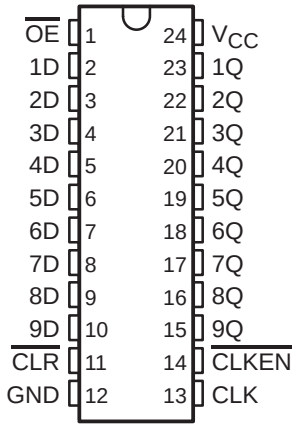
With the clock-enable ($\overline{CLKEN}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking $\overline{CLKEN}$ high disables the clock buffer, latching the outputs. The SN54AS823A and SN74AS823A have noninverting data (D) inputs and the SN74AS824A has inverting ($\overline{D}$) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

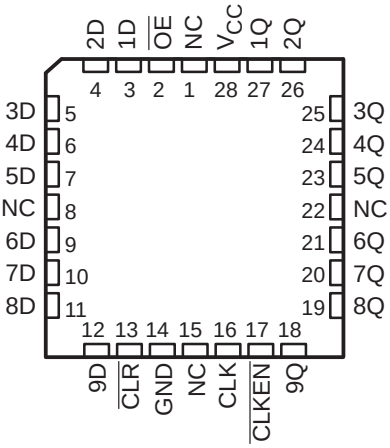
$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS823A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS823A and SN74AS824A are characterized for operation from 0°C to 70°C.

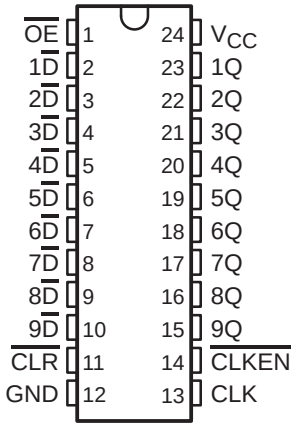
**SN54AS823A . . . JT PACKAGE**
**SN74AS823A . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN54AS823A . . . FK PACKAGE**
**(TOP VIEW)**




**SN74AS824A . . . DW OR NT PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## Function Tables

**SN54AS823A, SN74AS823A**
**(each flip-flop)**

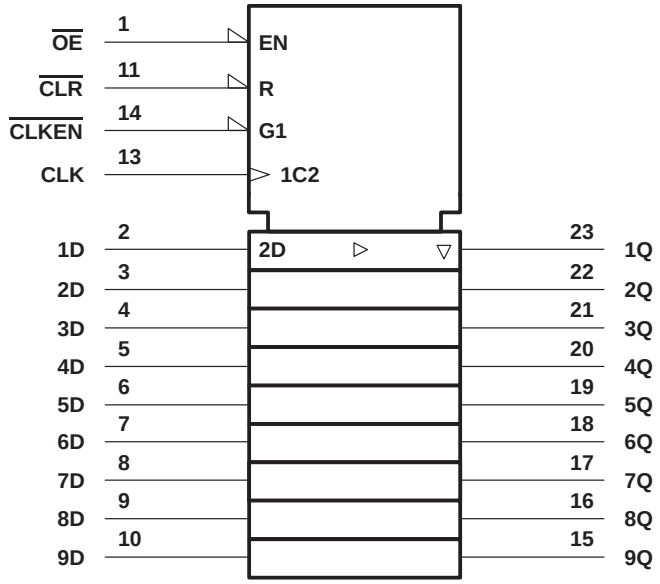
| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{CLKEN}$ | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | $Q_0$ |
| H | X | X | X | X | Z |

**SN74AS824A**
**(each flip-flop)**

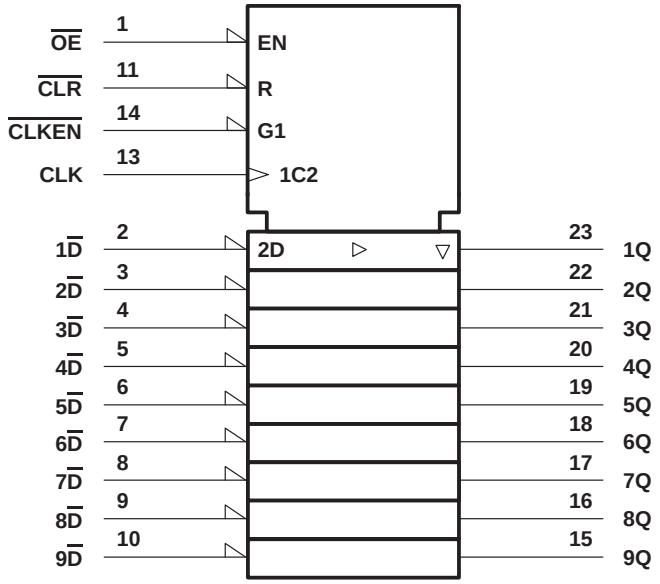
| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{CLKEN}$ | CLK | $\overline{D}$ | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | L |
| L | H | L | ↑ | L | H |
| L | H | H | X | X | $Q_0$ |
| H | X | X | X | X | Z |

## logic symbols†

**SN54AS823A, SN74AS823A**



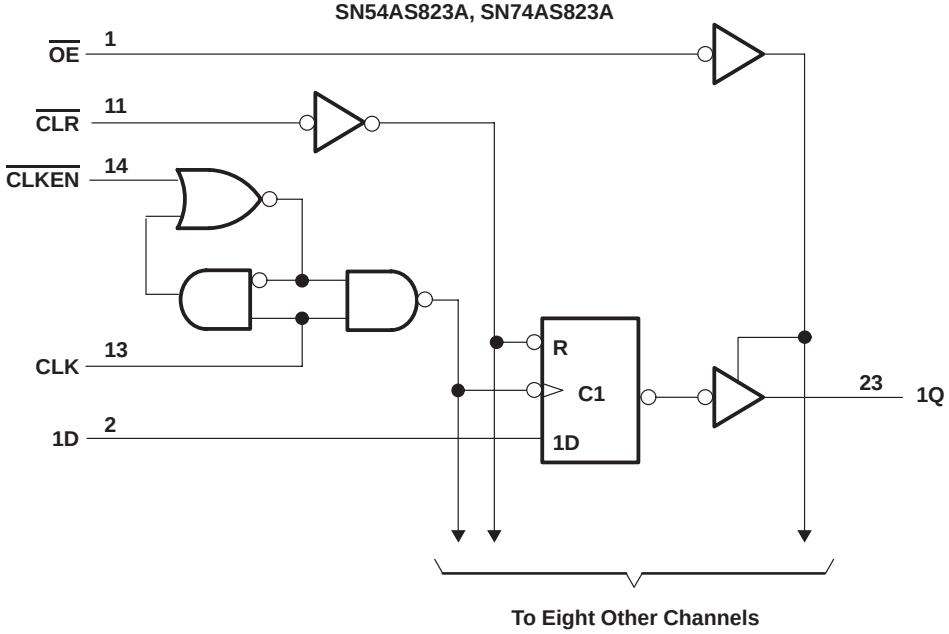

**SN74AS824A**



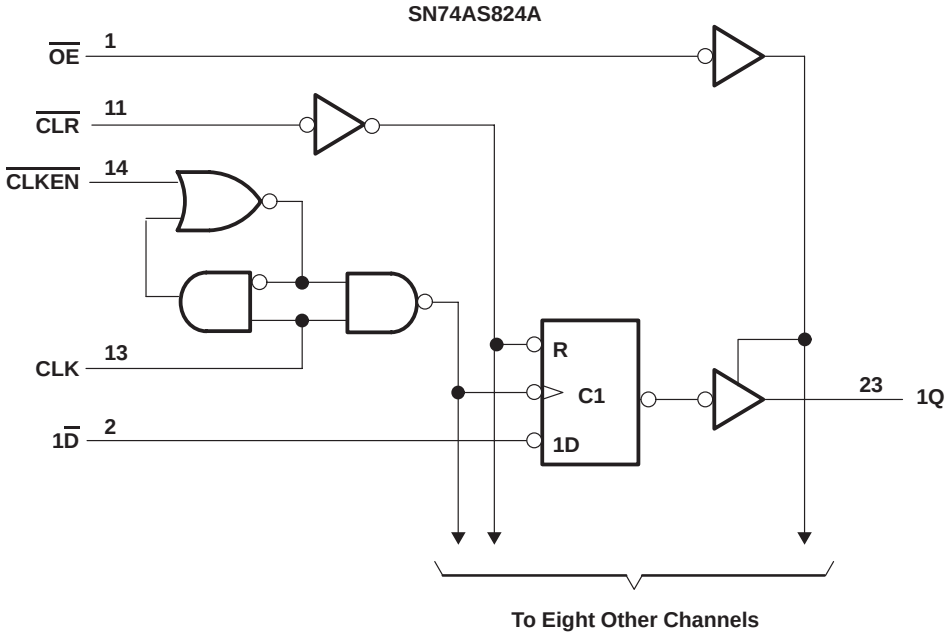

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagrams (positive logic)

**SN54AS823A, SN74AS823A**




**SN74AS824A**




Pin numbers shown are for the DW, JT, and NT packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN54AS823A . . . . . –55°C to 125°C
SN74AS823A, SN74AS824A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN54AS823A | | | SN74AS823A SN74AS824A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –24 | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | | 32 | | | 48 | mA |
| $t_w$* | Pulse duration | $\overline{CLR}$ low | 7.5 | | | 6.5 | | | ns |
| | | CLK high or low | 9.5 | | | 8 | | | |
| $t_{su}$* | Setup time before CLK↑ | $\overline{CLR}$ high | 8 | | | 8 | | | ns |
| | | Data | 7 | | | 6 | | | |
| | | $\overline{CLKEN}$ high or low | 8.5 | | | 7.5 | | | |
| $t_h$* | Hold time after CLK↑ | $\overline{CLKEN}$ low | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS823A | | | SN74AS823A SN74AS824A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –2 mA | $V_{CC}$ –2 | | | $V_{CC}$ –2 | | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –15 mA | 2.4 | 3.2 | | 2.4 | 3.2 | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 32 mA | | 0.3 | 0.5 | | | | V |
| | | | $I_{OL}$ = 48 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –50 | | | –50 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.5 | | | –0.5 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | SN54AS823A, SN74AS823A | $V_{CC}$ = 5.5 V | Outputs high | | 49 | 80 | | 49 | 80 | mA |
| | | | Outputs low | | 61 | 100 | | 61 | 100 | |
| | | | Outputs disabled | | 64 | 103 | | 64 | 103 | |
| | SN74AS824A | $V_{CC}$ = 5.5 V | Outputs high | | 49 | 80 | | 49 | 80 | |
| | | | Outputs low | | 61 | 100 | | 61 | 100 | |
| | | | Outputs disabled | | 64 | 103 | | 64 | 103 | |

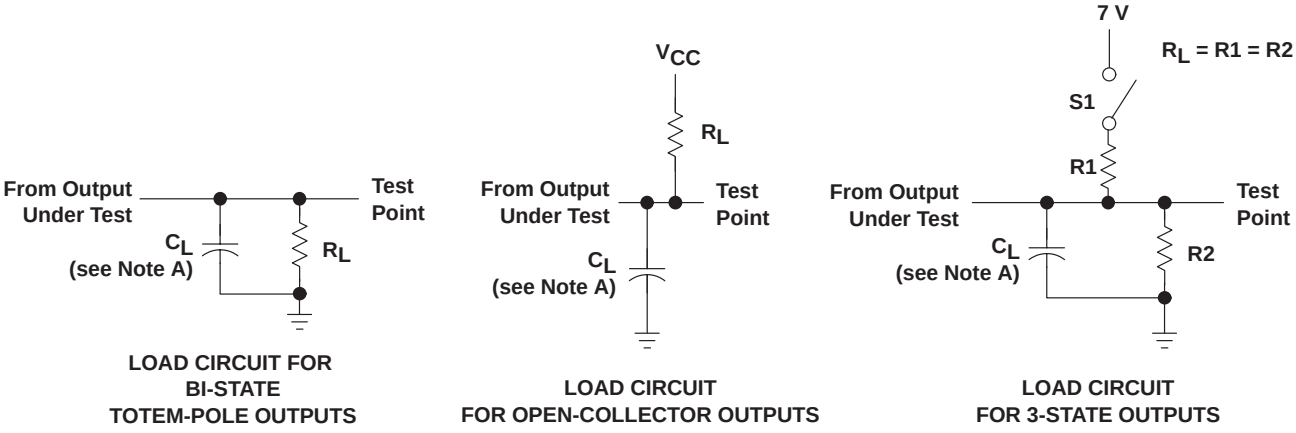
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS823A | | SN74AS823A SN74AS824A | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | CLK | Any Q | 3.5 | 9 | 3.5 | 7.5 | ns |
| $t_{PHL}$ | | | 3.5 | 14 | 3.5 | 13 | |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 3.5 | 16.5 | 3.5 | 15.5 | ns |
| $t_{PZH}$ | $\overline{OE}$ | Any Q | 4 | 12 | 4 | 11 | ns |
| $t_{PZL}$ | | | 4 | 13 | 4 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Q | 1 | 10 | 1 | 8 | ns |
| $t_{PLZ}$ | | | 1 | 10 | 1.5 | 8 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

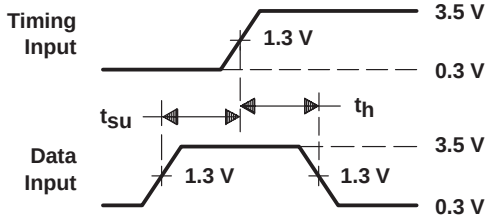
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



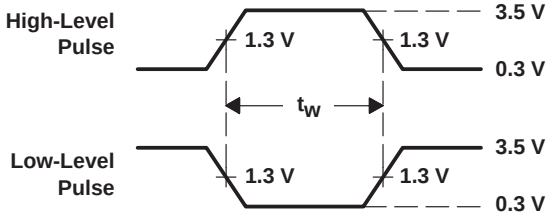

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

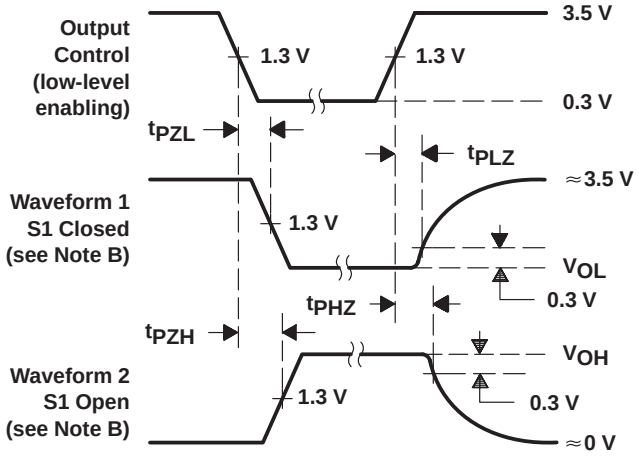
LOAD CIRCUIT FOR 3-STATE OUTPUTS



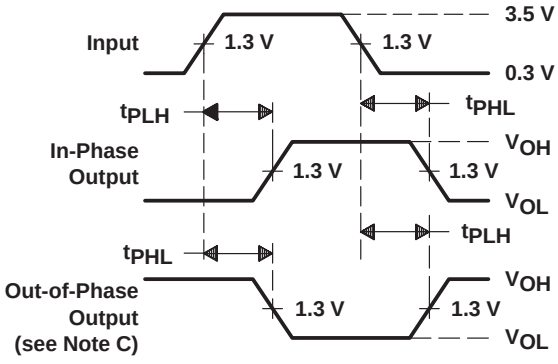

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS PULSE DURATIONS




VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8952501LA | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8952501LA<br>SNJ54AS823AJT |
| SNJ54AS823AJT | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8952501LA<br>SNJ54AS823AJT |
| SNJ54AS823AJT.A | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8952501LA<br>SNJ54AS823AJT |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

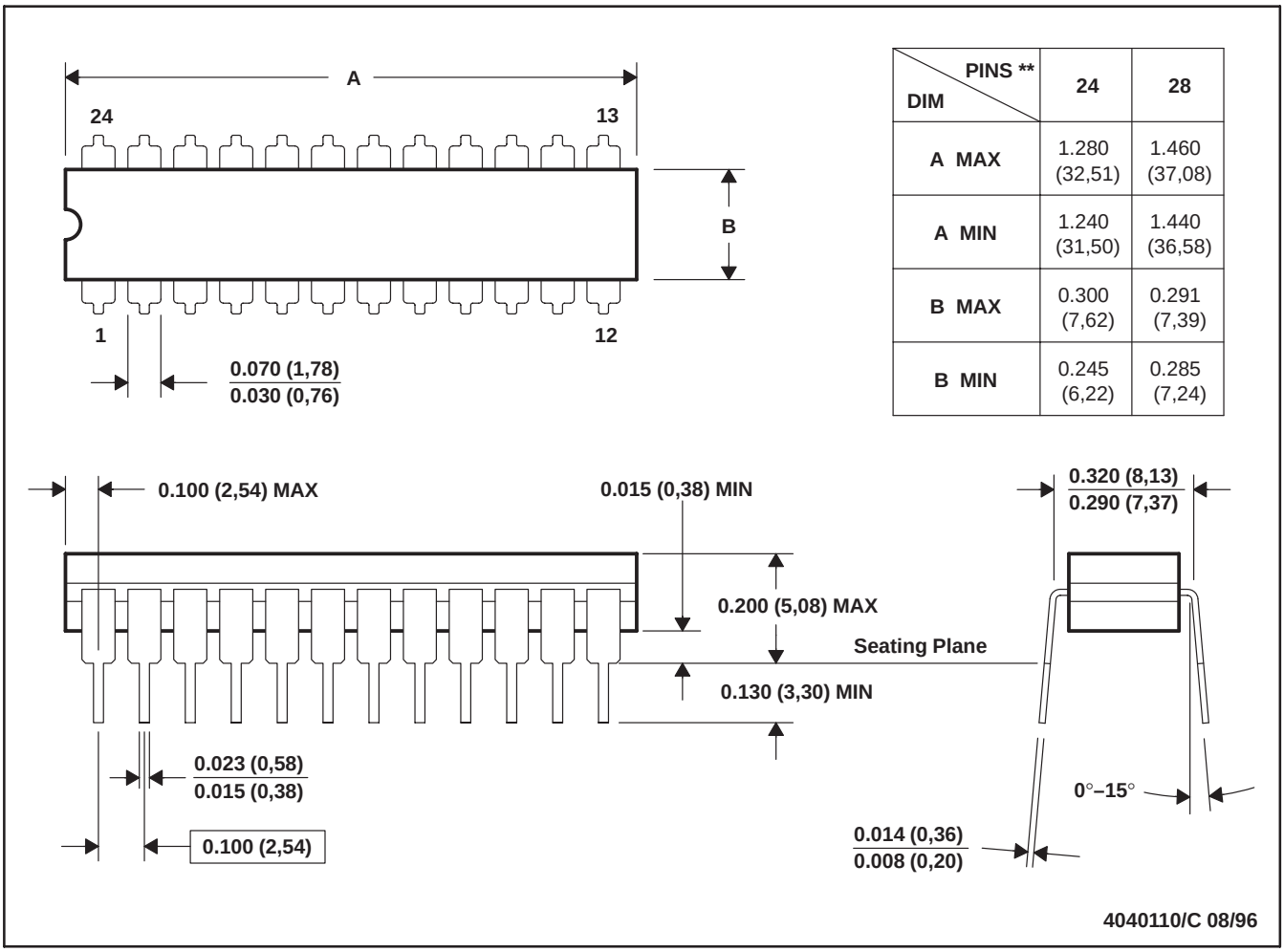
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

**JT (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE**

**24 LEADS SHOWN**




| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.280 (32,51) | 1.460 (37,08) |
| A MIN | 1.240 (31,50) | 1.440 (36,58) |
| B MAX | 0.300 (7,62) | 0.291 (7,39) |
| B MIN | 0.245 (6,22) | 0.285 (7,24) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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