

SN54ALS563B, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS163B – DECEMBER 1982 – REVISED NOVEMBER 2004

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

description/ordering information

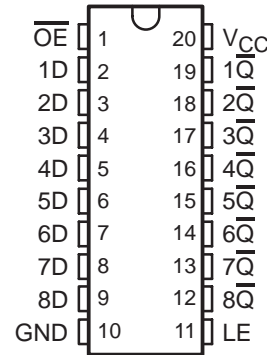
These 8-bit D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the complements of data (D) inputs. When LE is taken low, the outputs are latched at the inverse of the levels set up at the D inputs.

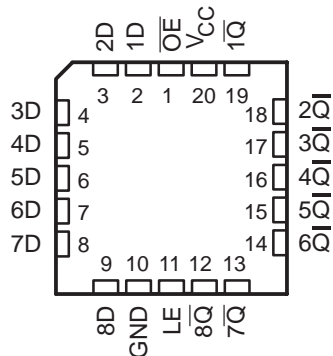
A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54ALS563B . . . J OR W PACKAGE
SN74ALS563B . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS563B . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN74ALS563BN	SN74ALS563BN
	SOIC – DW	Tube of 25	SN74ALS563BDW	ALS563B
		Reel of 2000	SN74ALS563BDWR	
	SOP – NS	Reel of 2000	SN74ALS563BNSR	ALS563B
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54ALS563BJ	SNJ54ALS563BJ
	CFP – W	Tube of 85	SNJ54ALS563BW	SNJ54ALS563BW
	LCCC – FK	Tube of 55	SNJ54ALS563BFK	SNJ54ALS563BFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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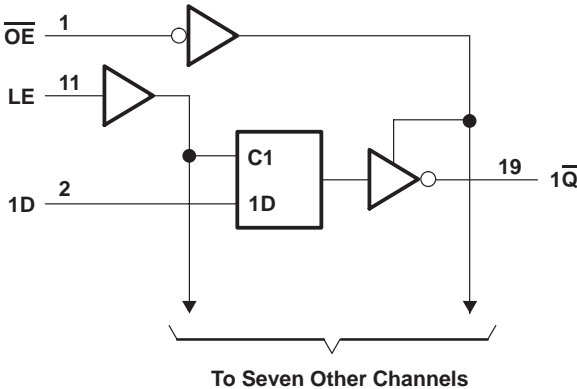
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FUNCTION TABLE
(each latch)

INPUTS			OUTPUT \overline{Q}
\overline{OE}	LE	D	
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Package thermal impedance, θ _{JA} (see Notes 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54ALS563B			SN74ALS563B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			–1			–2.6	mA
I _{OL}	Low-level output current			12			24	mA
t _w	Pulse duration, LE high	15			15			ns
t _{su}	Setup time, data before LE↓	20			10			ns
t _h	Hold time, data after LE↓	12			10			ns
T _A	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS563B			SN74ALS563B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA				–1.2			–1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = –0.4 mA		V _{CC} – 2			V _{CC} – 2			V
	V _{CC} = 4.5 V, I _{OH} = –1 mA		2.4	3.3					
	V _{CC} = 4.5 V, I _{OH} = –2.6 mA					2.4	3.2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25	0.4		0.25	0.4		V
	V _{CC} = 4.5 V, I _{OL} = 24 mA					0.35	0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V				20			20	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V				–20			–20	μA
I _I	V _{CC} = 5.5 V, V _I = 7 V				0.1			0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V				20			20	μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V				–0.1			–0.1	mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		–20		–112	–30		–112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		16	26		16	26	
		Outputs disabled		17	29		17	29	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS563B, SN74ALS563B

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

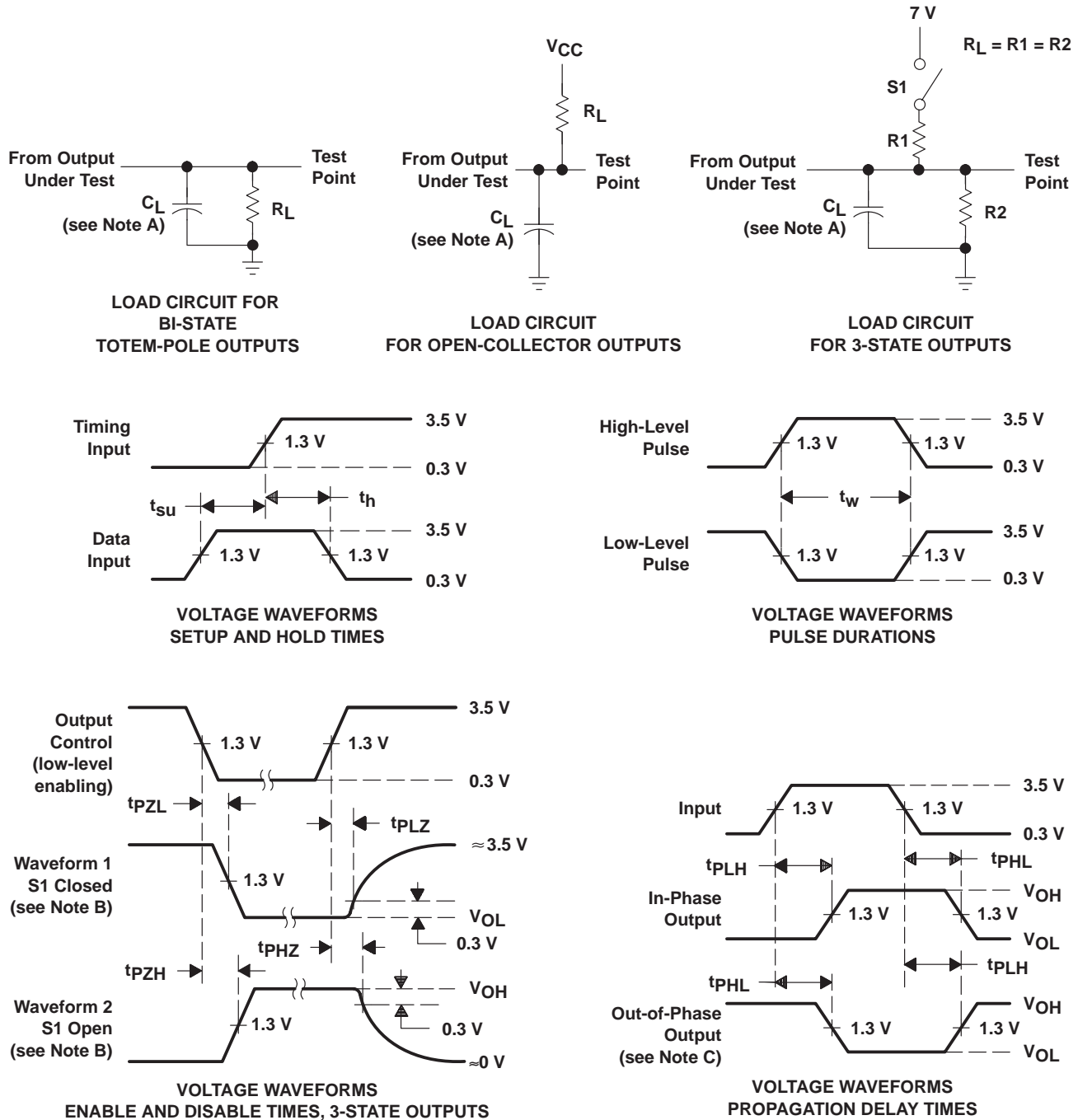
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V C _L = 50 pF R1 = 500 Ω R2 = 500 Ω T _A = MIN to MAX†				UNIT
			SN54ALS563B		SN74ALS563B		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	\overline{Q}	3	26	3	18	ns
t _{PHL}			3	15	3	14	
t _{PLH}	LE	\overline{Q}	8	29	6	22	ns
t _{PHL}			4	22	6	21	
t _{PZH}	\overline{OE}	\overline{Q}	4	25	3	18	ns
t _{PZL}			4	21	4	18	
t _{PHZ}	\overline{OE}	\overline{Q}	2	12	1	10	ns
t _{PLZ}			3	22	1	15	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS563B, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8870001RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870001RA SNJ54ALS563BJ
SN74ALS563BDW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B
SN74ALS563BDW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B
SN74ALS563BN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS563BN
SN74ALS563BN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS563BN
SN74ALS563BNSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B
SN74ALS563BNSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B
SN74ALS563BNSRG4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B
SNJ54ALS563BJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870001RA SNJ54ALS563BJ
SNJ54ALS563BJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8870001RA SNJ54ALS563BJ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS563B, SN74ALS563B :

- Catalog : [SN74ALS563B](#)
- Military : [SN54ALS563B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS563BNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS563BNSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS563BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS563BDW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS563BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS563BN.A	N	PDIP	20	20	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

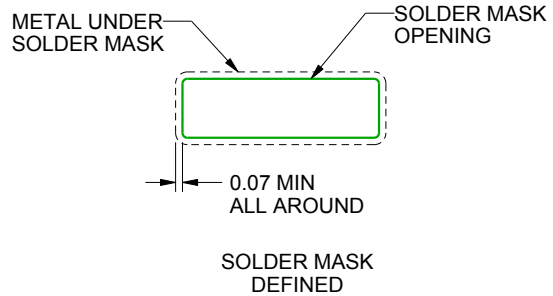
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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