SNx4ACT86 四路双输入异或门

1 特性

- 4.5V 至 5.5V V_{CC} 运行
- 输入电压高达 5.5V
- t_{pd} 最大值为 10ns（5V 时）
- 输入兼容 TTL 电压

2 说明

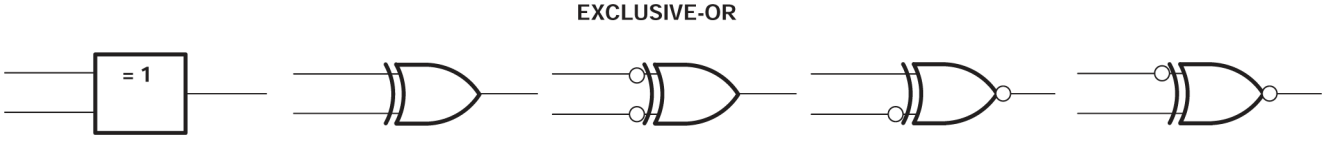
’ACT86 器件是四路双输入异或门。该器件采用正逻辑执行布尔函数 $Y = A \oplus B$ 或 $Y = \overline{A}B + A\overline{B}$。

常用作真/补元件。如果一个输入为低电平，则可在输出时重新生成真实形态的其他输入。如果一个输入为高电平，另一个输入的信号则可在输出时重新生成反向信号。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4ACT86	DB（SSOP，14）	6.2mm × 7.8mm	6.2mm × 5.3mm
	D（SOIC，14）	8.65mm × 6mm	8.65mm × 3.9mm
	N（PDIP，14）	19.3mm × 9.4mm	19.3mm × 6.35mm
	NS（SO，14）	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW（TSSOP，14）	5mm × 6.4mm	5mm × 4.4mm
	BQA (WQFN)	3mm × 2.5mm	3mm × 2.5mm

(1) 有关更多信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



异或逻辑

内容

3 引脚配置和功能

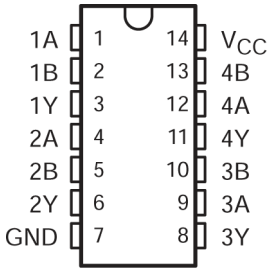


图 3-1. SN54ACT86 J 或 W 封装；SN74ACT86 D、DB、N、NS 或 PW 封装（顶视图）

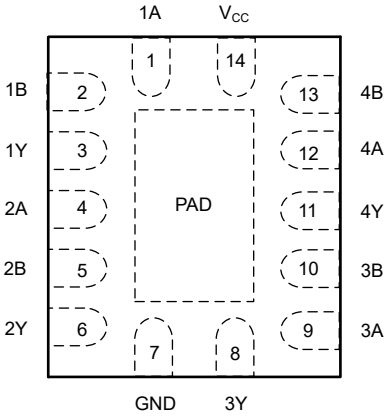
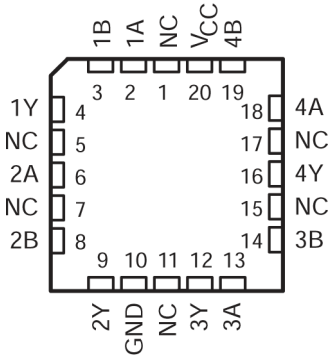


图 3-2. SN74ACT86 BQA 封装（透明顶视图）



NC – No internal connection

图 3-3. SN54ACT86 FK 封装（顶视图）

表 3-1. 引脚功能

引脚			类型[1]	说明
名称	BQA、D、DB、N、NS、PW、J 或 W	FK		
1A	1	2	I	通道 1，输入 A
1B	2	3	I	通道 1，输入 B
1Y	3	4	O	通道 1，输出 Y
2A	4	6	I	通道 2，输入 A
2B	5	8	I	通道 2，输入 B
2Y	6	9	O	通道 2，输出 Y
GND	7	10	G	接地
3Y	8	12	O	通道 3，输出 Y
3A	9	13	I	通道 3，输入 A
3B	10	14	I	通道 3，输入 B
4Y	11	16	O	通道 4，输出 Y
4A	12	18	I	通道 4，输入 A
4B	13	19	I	通道 4，输入 B

表 3-1. 引脚功能（续）

引脚			类型[1]	说明
名称	BQA、D、DB、N、NS、PW、J 或 W	FK		
V_{CC}	14	20	P	正电源
NC	—	1、5、7、11、15、17	—	无内部连接
散热焊盘[2]			—	散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源

(1) 信号类型：I = 输入，O = 输出，G = 接地，P = 电源。
(2) 仅限 BQA 封装。

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得 (除非另有说明) (1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I (2)	输入电压范围		-0.5	V_{CC} + 0.5	V
V_O (2)	输出电压范围		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	(V_I < 0 或 V_I > V_{CC})		±20	mA
I_{OK}	输出钳位电流	(V_O < 0 或 V_O > V_{CC})		±20	mA
I_O	持续输出电流	(V_O = 0 至 V_{CC})		±50	mA
	通过 V_{CC} 或 GND 的持续电流			±200	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 应力超出“绝对最大额定值”下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，这并不表示器件在这些条件下以及在“建议运行条件”以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

4.2 建议运行条件

在自然通风条件下的工作温度范围内测得 (除非另有说明) (1)

		SN54ACT86		SN74ACT86		单位
		最小值	最大值	最小值	最大值	
V_{CC}	电源电压	4.5	5.5	4.5	5.5	V
V_{IH}	高电平输入电压	2		2		V
V_{IL}	低电平输入电压		0.8		0.8	V
V_I	输入电压	0	V_{CC}	0	V_{CC}	V
V_O	输出电压	0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流		-24		-24	mA
I_{OL}	低电平输出电流		24		24	mA
$\Delta t/\Delta v$	输入转换上升或下降速率		8		8	ns/V
T_A	自然通风条件下的工作温度范围	-55	125	-40	85	°C

(1) 器件的所有未使用输入必须保持在 V_{CC} 或 GND 以验证器件是否正常运行。请参阅*慢速或浮点 CMOS 输入的影响*应用手册。

4.3 热性能信息

热指标(1)		SN74ACT86						
		BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	单位
		14 引脚						
$R_{\theta JA}$	结温至环境温度热阻	91.3	119.9	96	80	76	145.7	°C/W
$R_{\theta JC(top)}$	结至外壳 (顶部) 热阻	99.4	—	—	—	—	—	°C/W
$R_{\theta JB}$	结至电路板热阻	60.0	—	—	—	—	—	°C/W
ψ_{JT}	结至顶部特征参数	14.5	—	—	—	—	—	°C/W
ψ_{JB}	结至电路板特征参数	60.8	—	—	—	—	—	°C/W
$R_{\theta JC(bot)}$	结至外壳 (底部) 热阻	37.0	—	—	—	—	—	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用手册。

4.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			SN54ACT86		SN74ACT86		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA	4.5V	4.4	4.49		4.4		4.4		V
		5.5V	5.4	5.49		5.4		5.4		
	I_{OH} = -24mA	4.5V	3.86			3.7		3.76		
		5.5V	4.86			4.7		4.76		
	I_{OH} = -50mA (1)	5.5V				3.85				
	I_{OH} = -75mA (1)	5.5V						3.85		
V_{OL}	I_{OL} = 50μA	4.5V		0.001	0.1		0.1		0.1	V
		5.5V		0.001	0.1		0.1		0.1	
	I_{OL} = 24mA	4.5V			0.36		0.5		0.44	
		5.5V			0.36		0.5		0.44	
	I_{OL} = 50mA (1)	5.5V					1.65			
	I_{OL} = 75mA (1)	5.5V							1.65	
I_I	V_I = V_{CC} 或 GND	5.5V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0	5.5V			4		80		40	μA
ΔI_{CC} (2)	一个输入电压为 3.4V，其他输入电压为 GND 或 V_{cc}	5.5V		0.6			1.6		1.5	mA
C_i	V_I = V_{CC} 或 GND	5V		2.6						pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 10ms。
(2) 这是每个输入在指定 TTL 电压电平之一而不是 0V 或 V_{CC} 时电源电流的增加情况。

4.5 开关特性

在自然通风条件下的建议工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（参阅负载电路与电压波形）

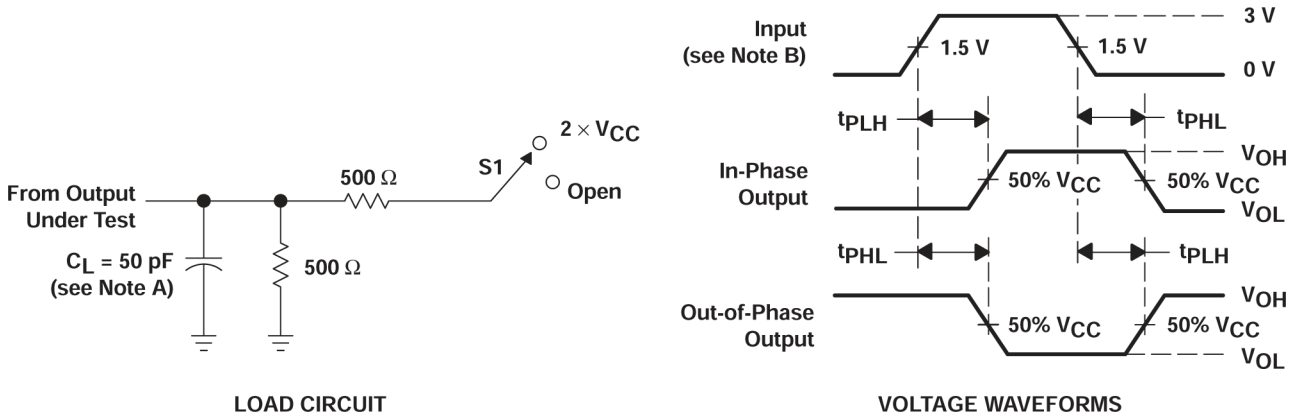
参数	从（输入）	至（输出）	T_A = 25°C			SN54ACT86		SN74ACT86		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A 或 B	Y	1.5	8.5	9.5	1	10	1	10	ns
t_{PHL}			1.5	7	9.5	1	10.5	1	10.5	

4.6 工作特性

V_{CC} = 5V，T_A = 25°C

参数		测试条件		典型值	单位
C_{pd}	功率耗散电容	C_L = 50pF	f = 1MHz	25	pF

5 参数测量信息



A. C_L 包括探头和夹具电容。
B. 所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50Ω，t_r v 2.5ns，t_f v 2.5ns。
C. 一次测量一个输出，每次测量一个输入转换。

图 5-1. 负载电路和电压波形

测试	S1
t_{PLH}/t_{PHL}	开路

6 详细说明

6.1 功能方框图

异或门具有许多应用，可用其他逻辑符号更好地表示其中部分应用。

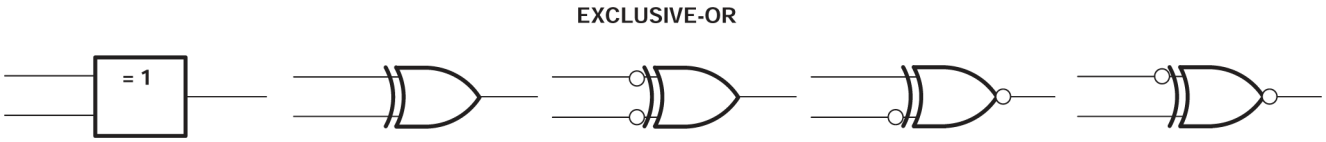
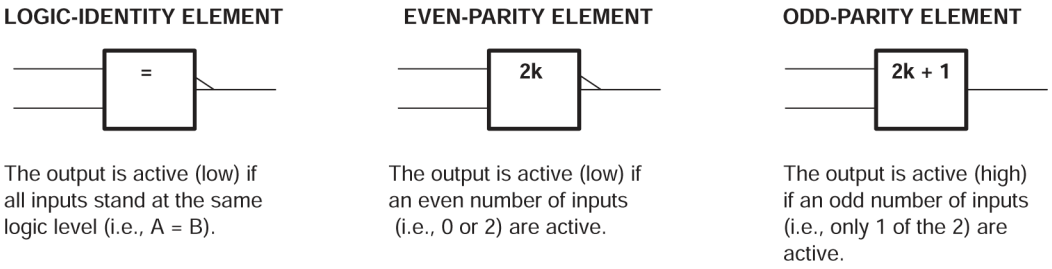


图 6-1. 异或逻辑

这五个等效的异或门符号对于采用正逻辑的 'ACT86 门有效；任意两个端口可能显示否定逻辑。



6.2 器件功能模式

表 6-1. 功能表（每个逻辑门）

输入		输出 Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 电源相关建议

电源可以是*建议运行条件* 中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个旁路电容器，以防止功率干扰。建议为该器件使用 0.1 µF 电容。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。旁路电容器应安装在尽可能靠近电源端子的位置，以获得更佳效果，如图 7-1 所示。

7.2 布局

7.2.1 布局指南

使用多输入和多通道逻辑器件时，输入不得悬空。在许多情况下，未使用数字逻辑器件的功能或部分功能；例如，当仅使用三输入与门的两个输入时。此类未使用的输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的操作状态。数字逻辑器件的所有未使用输入必须连接到由输入电压规范定义的逻辑高电平电压或逻辑低电平电压，以防止其悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，输入连接到 GND 或 V_{CC}，以对逻辑功能更有意义或更方便者为准。

7.2.2 布局示例

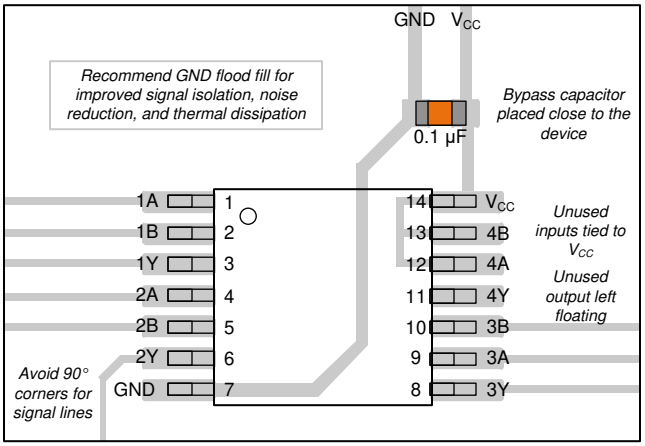


图 7-1. SN74ACT86 的示例布局

8 器件和文档支持

8.1 文档支持

8.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
SN54ACT86	点击此处	点击此处	点击此处	点击此处	点击此处
SN74ACT86	点击此处	点击此处	点击此处	点击此处	点击此处

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (July 2024) to Revision E (April 2025)	Page
• 添加了 BQA 封装	3
• 添加了 BQA 热性能信息	5

Changes from Revision C (October 2003) to Revision D (July 2024)	Page
• 添加了*器件信息* 表、*引脚功能* 表、*热性能信息* 表、*器件功能模式*、”应用和实施“部分、*器件和文档支持* 部分以及*机械、封装和订购信息* 部分	1
• 更新了 $R_{\theta JA}$ 值：D = 86 至 119.9，PW = 113 至 145.7，所有值均以 °C/W 为单位	5

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9068701Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701Q2A SNJ54ACT 86FK
5962-9068701QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QCA SNJ54ACT86J
5962-9068701QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QDA SNJ54ACT86W
SN74ACT86BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	ACT86
SN74ACT86DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT86N
SN74ACT86N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT86N
SN74ACT86NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	AD86
SN74ACT86PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SNJ54ACT86FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701Q2A SNJ54ACT 86FK

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ACT86FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701Q2A SNJ54ACT 86FK
SNJ54ACT86J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QCA SNJ54ACT86J
SNJ54ACT86J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QCA SNJ54ACT86J
SNJ54ACT86W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QDA SNJ54ACT86W
SNJ54ACT86W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QDA SNJ54ACT86W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54ACT86, SN74ACT86 :

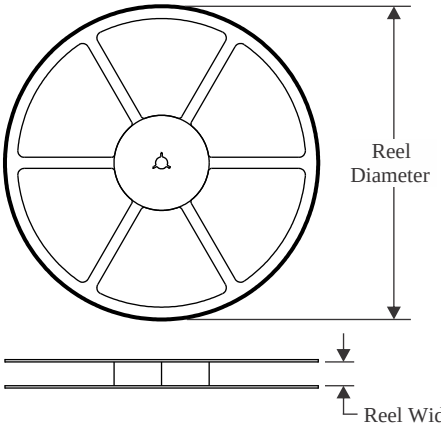
- Catalog : SN74ACT86
- Automotive : SN74ACT86-Q1, SN74ACT86-Q1
- Military : SN54ACT86

NOTE: Qualified Version Definitions:

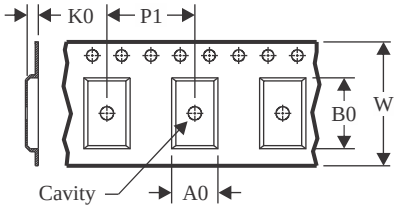
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

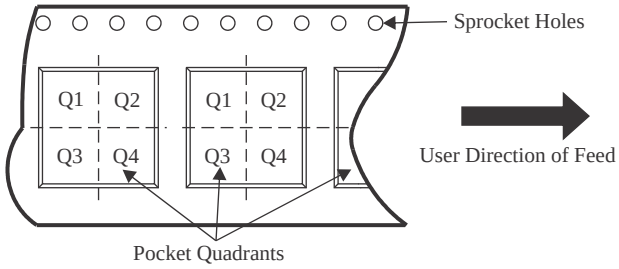


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

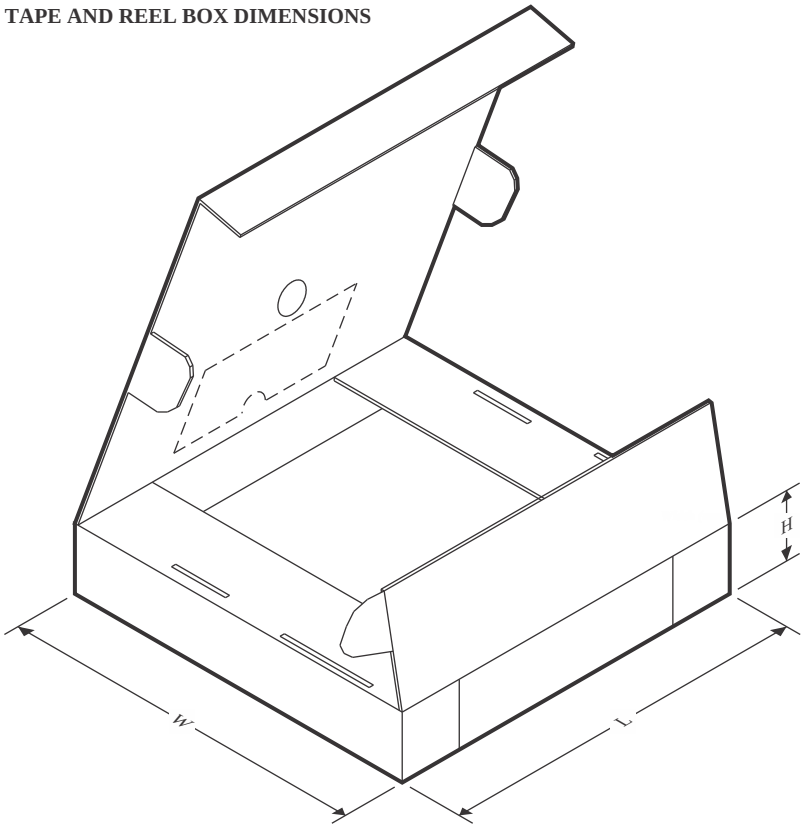
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74ACT86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT86NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74ACT86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT86PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

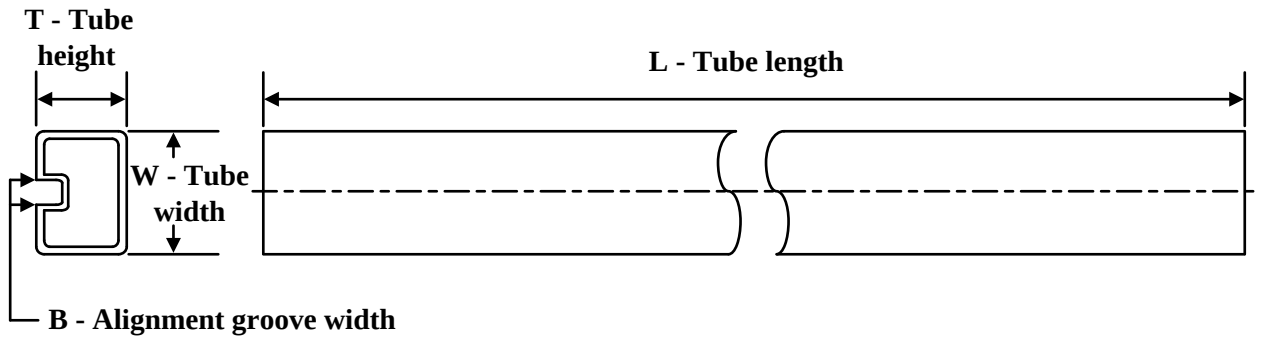
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

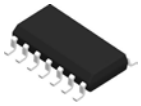
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74ACT86DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74ACT86NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74ACT86PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT86PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9068701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9068701QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT86FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT86FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT86W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54ACT86W.A	W	CFP	14	25	506.98	26.16	6220	NA

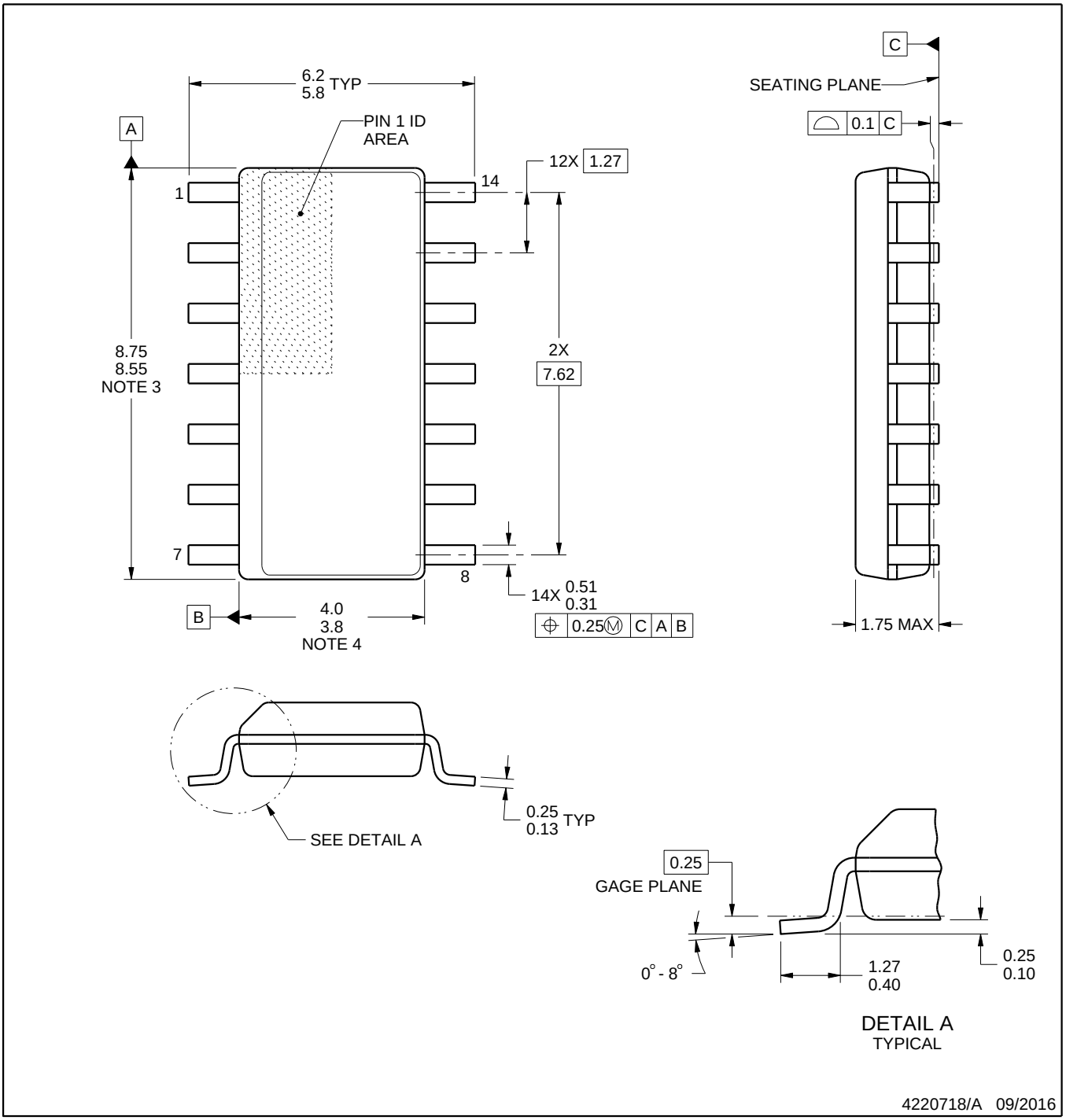


PACKAGE OUTLINE

D0014A

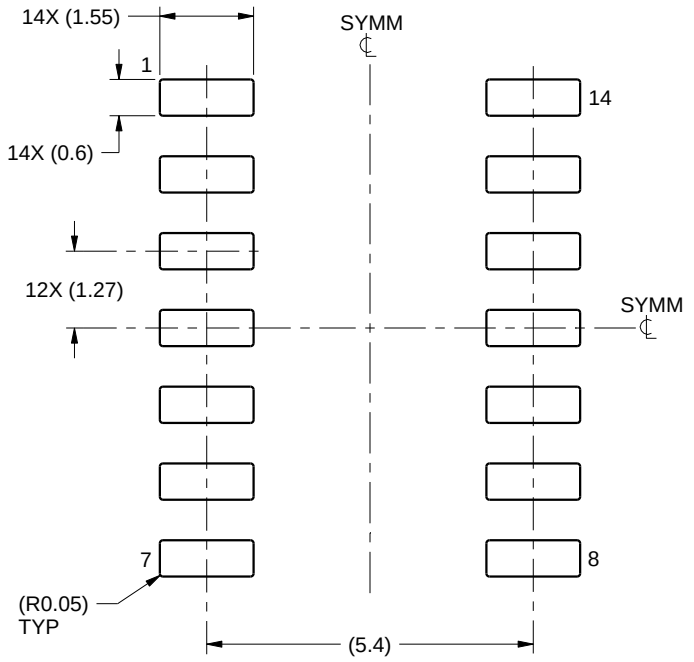
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

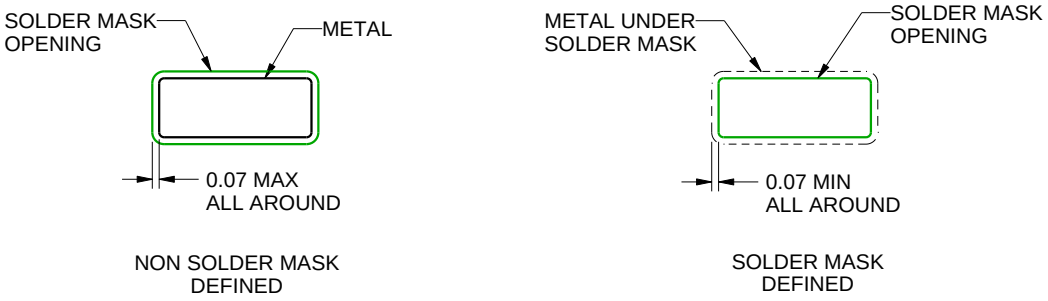


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

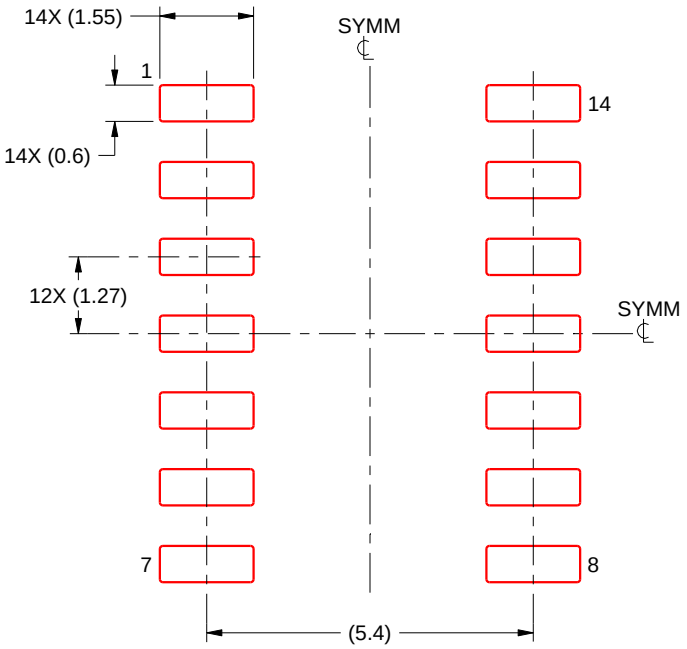
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

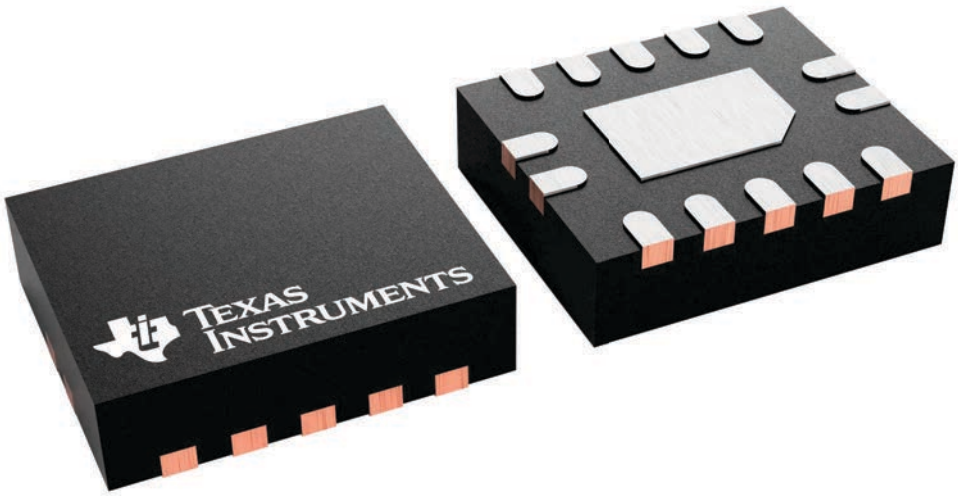
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

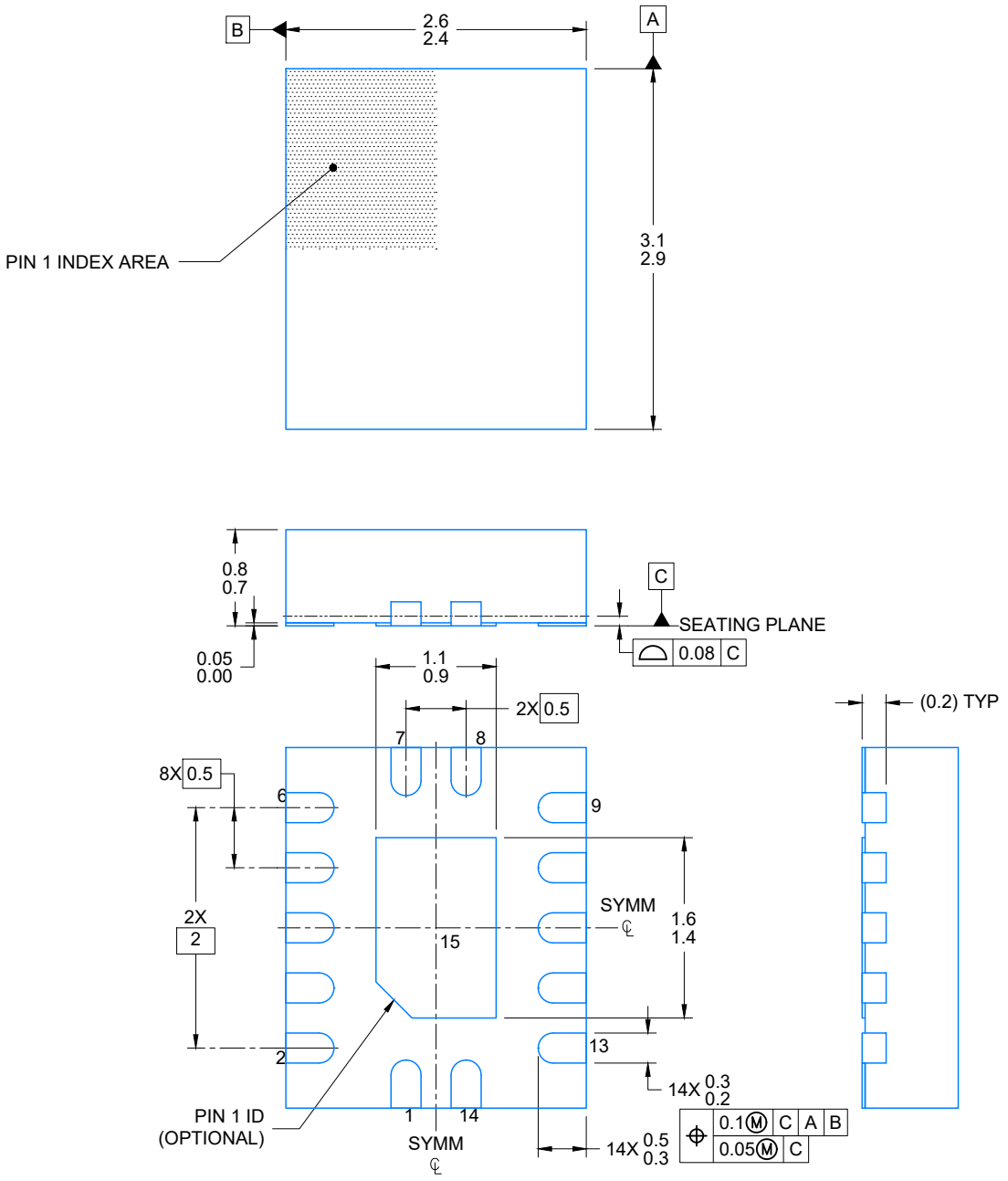


PACKAGE OUTLINE

BQA0014A

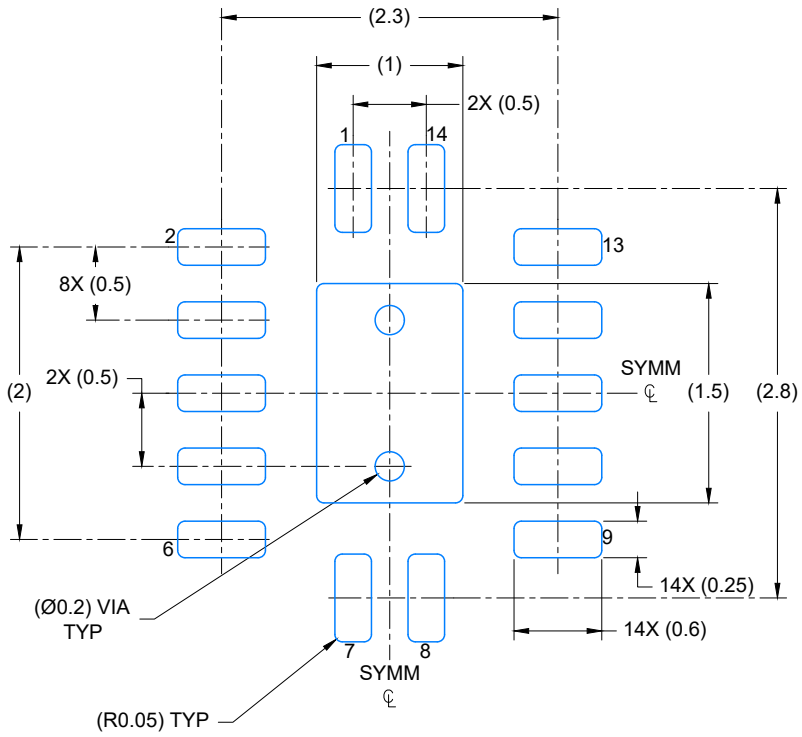
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

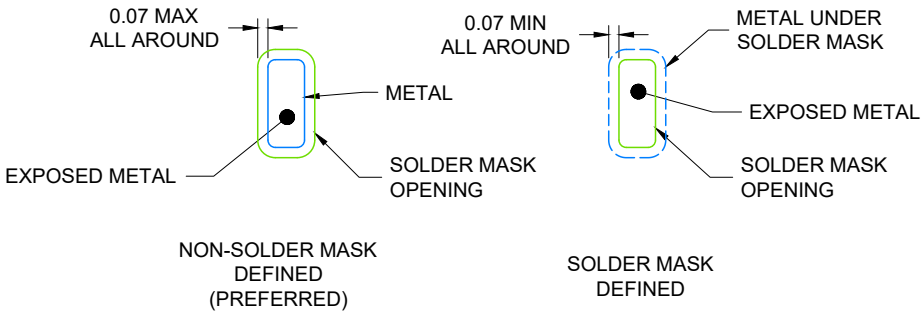


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



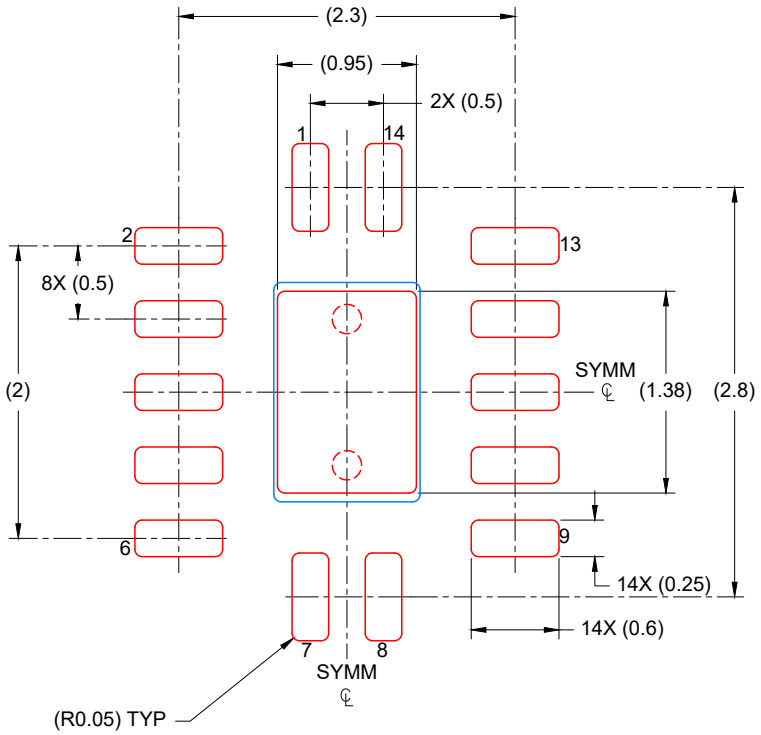
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

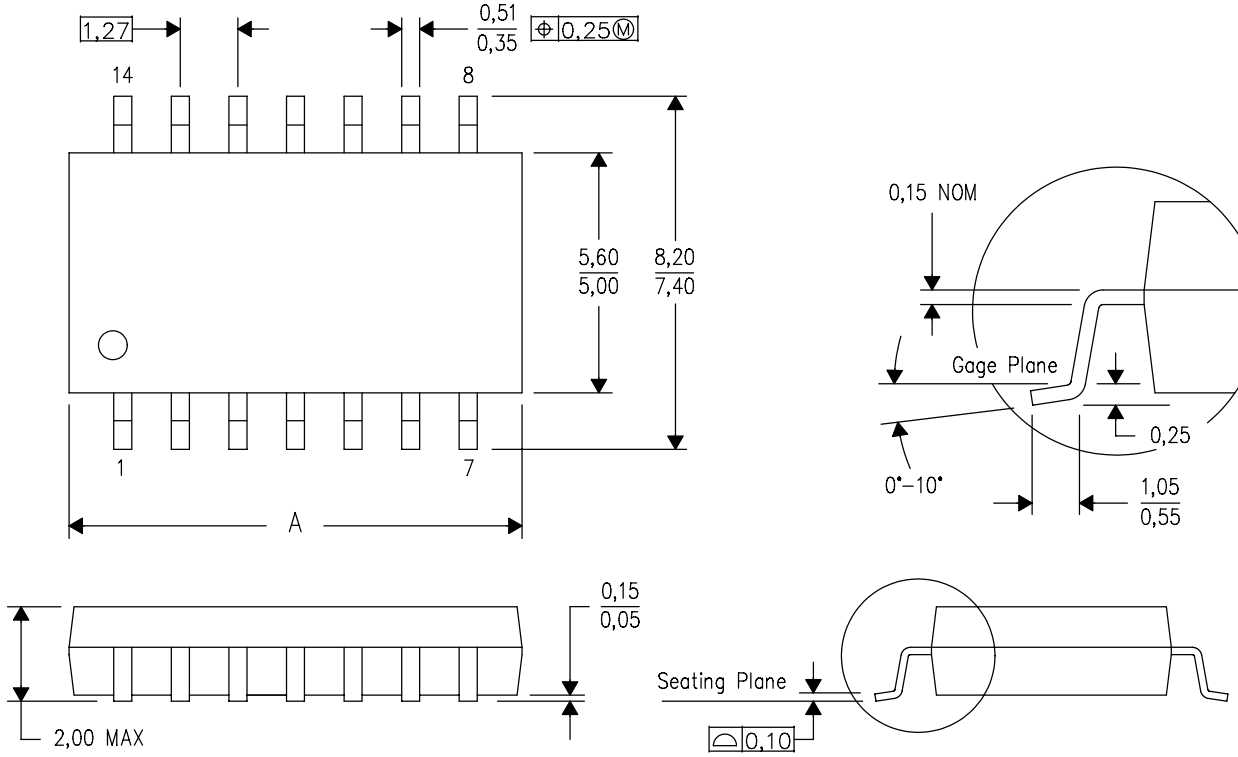
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

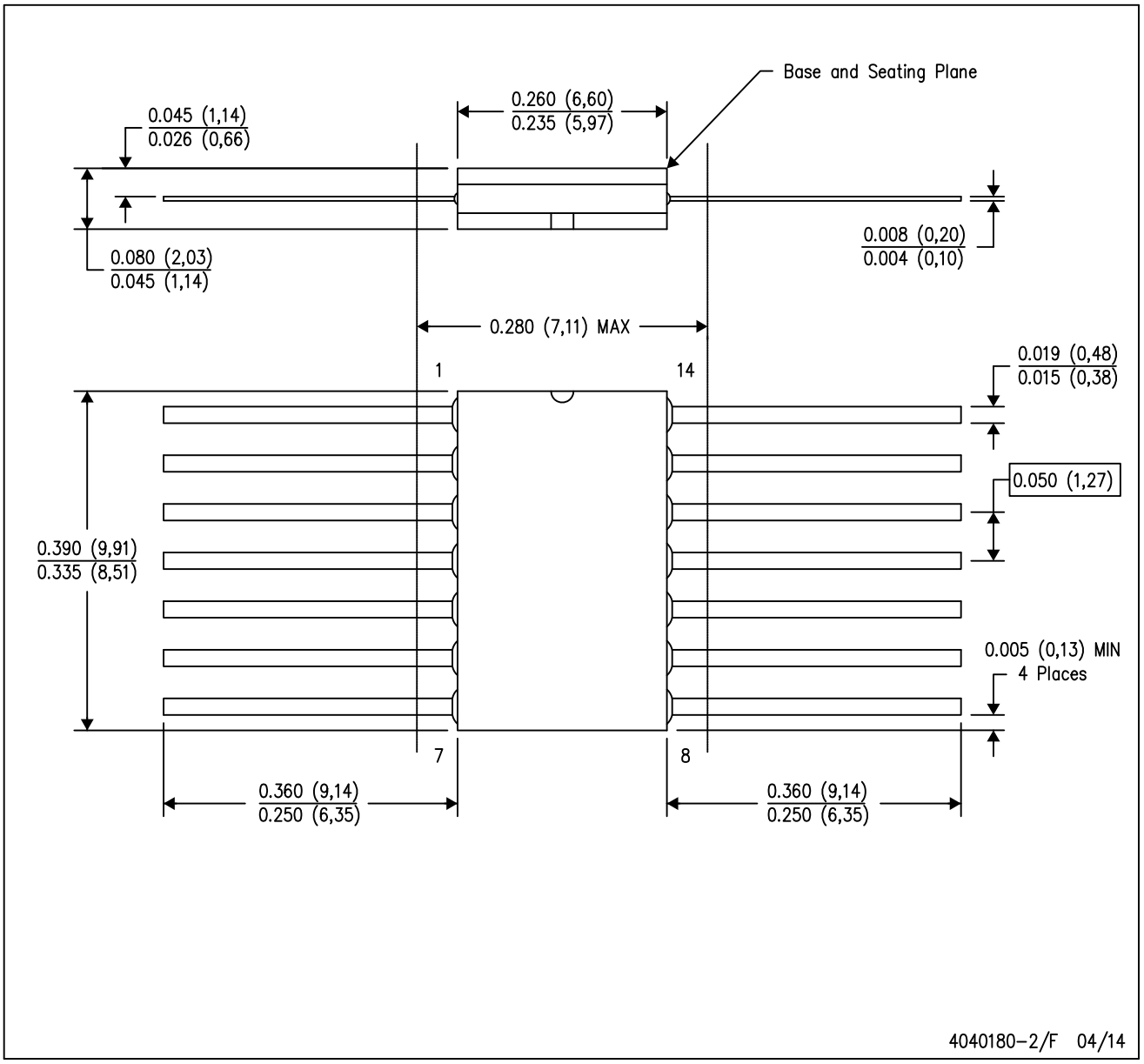


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



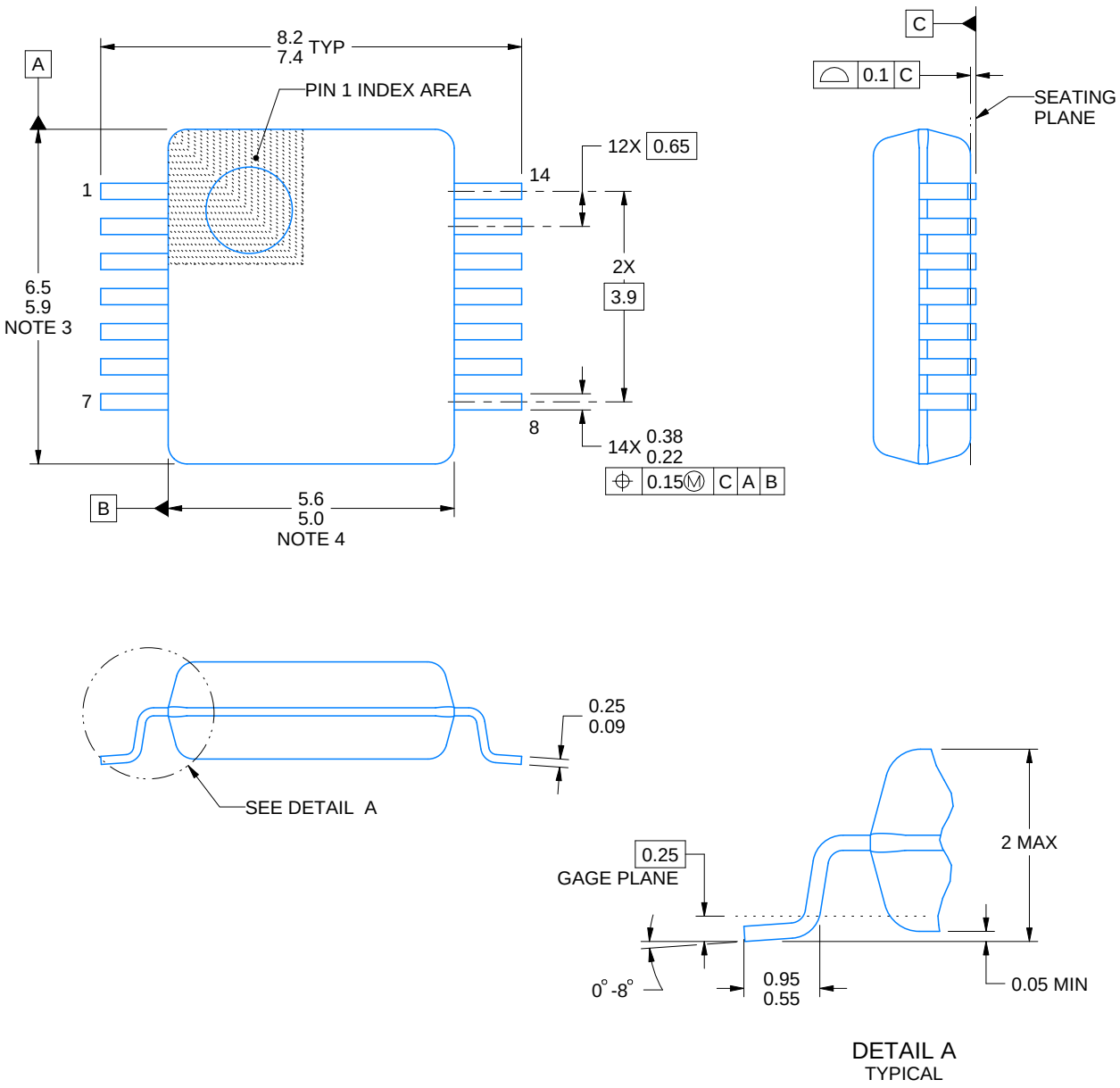
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

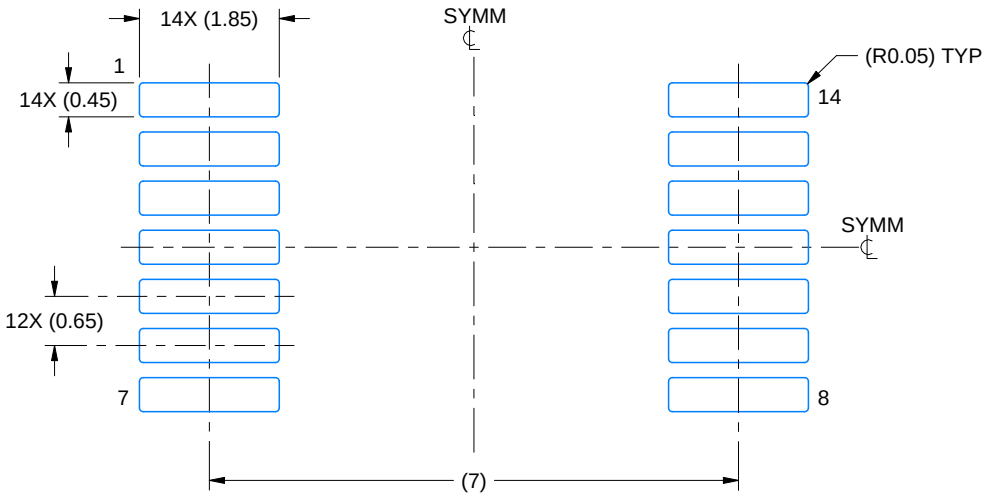
SMALL OUTLINE PACKAGE



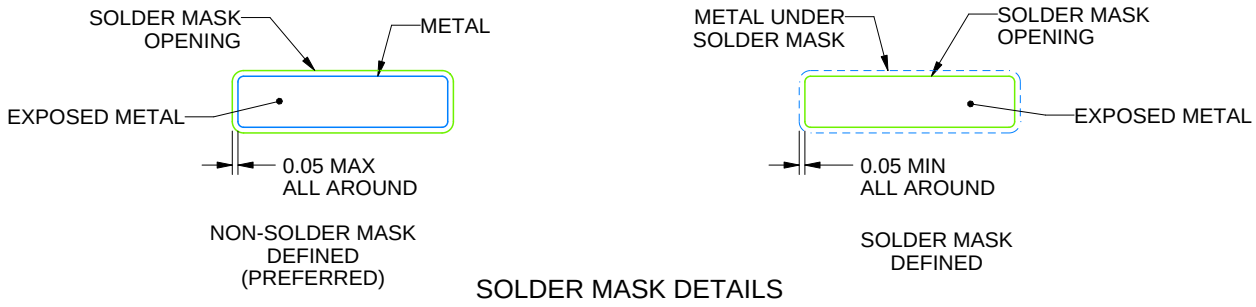
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

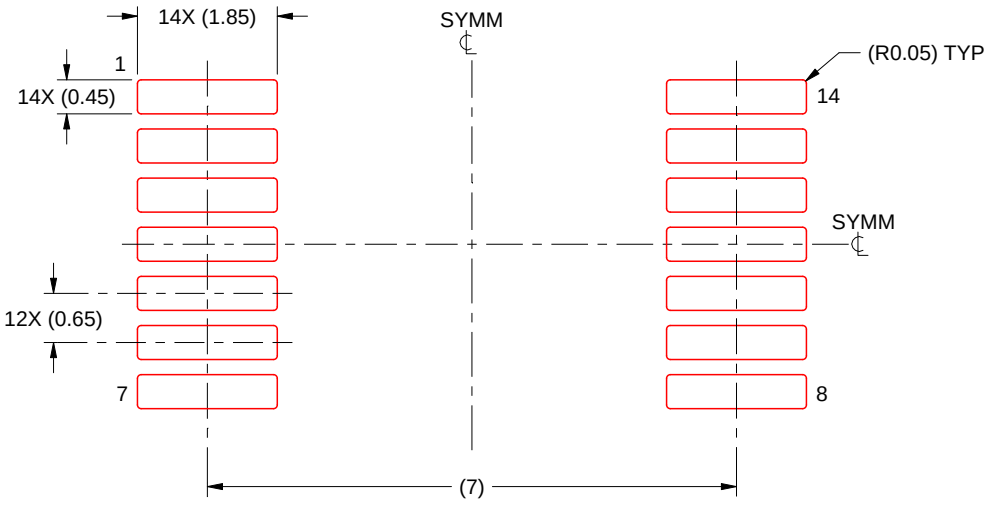


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

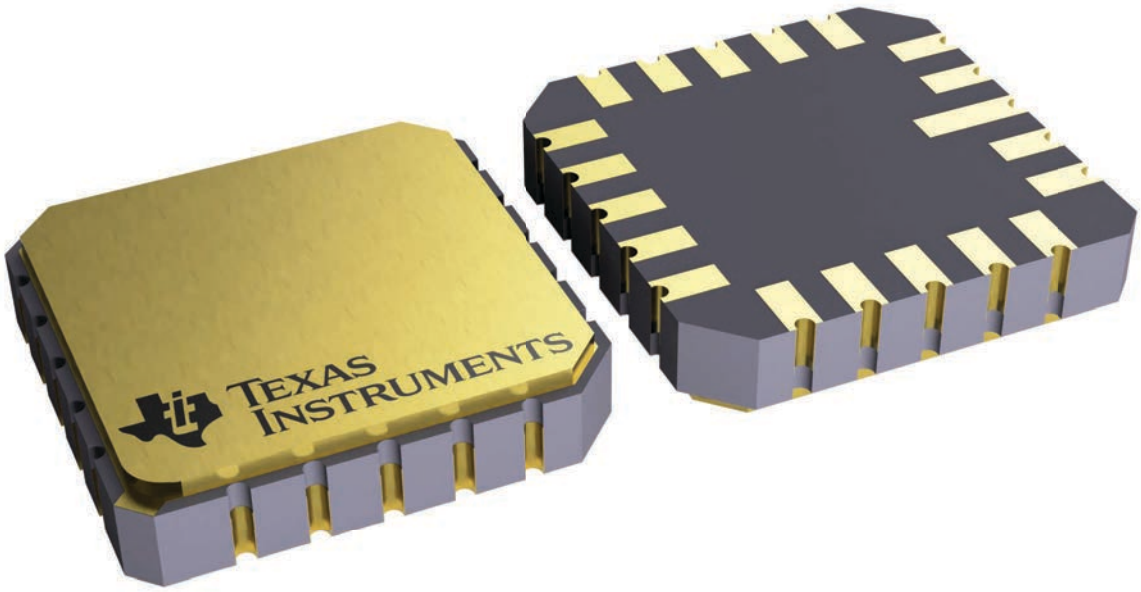
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

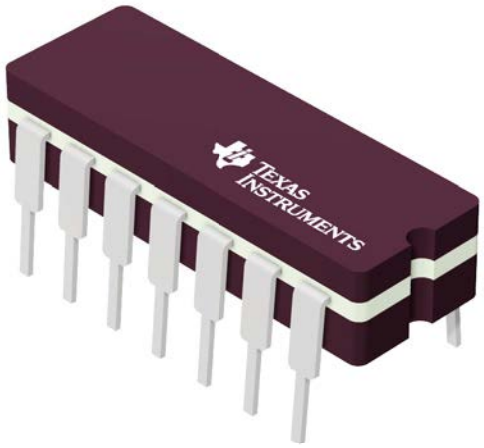


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

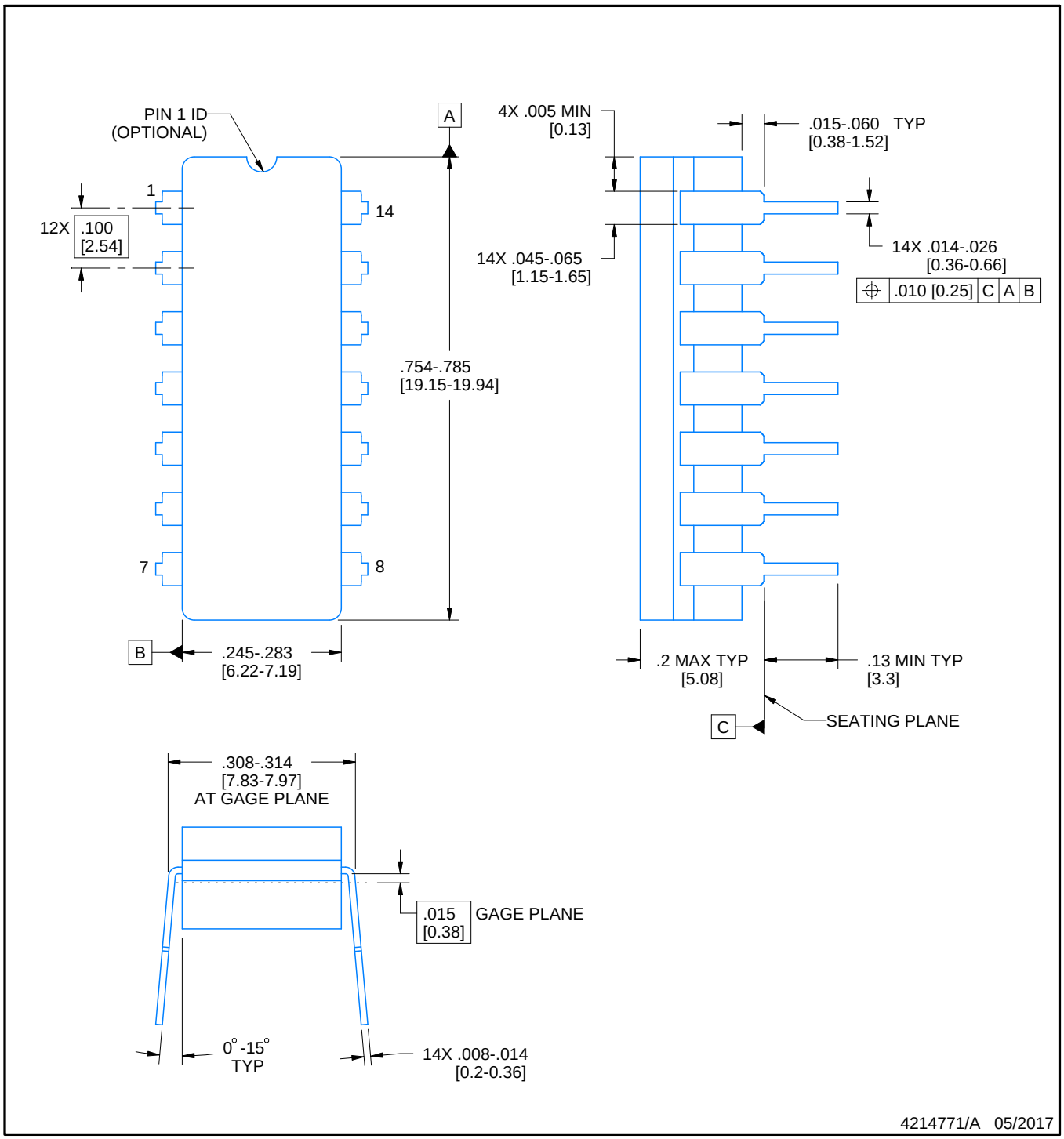
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

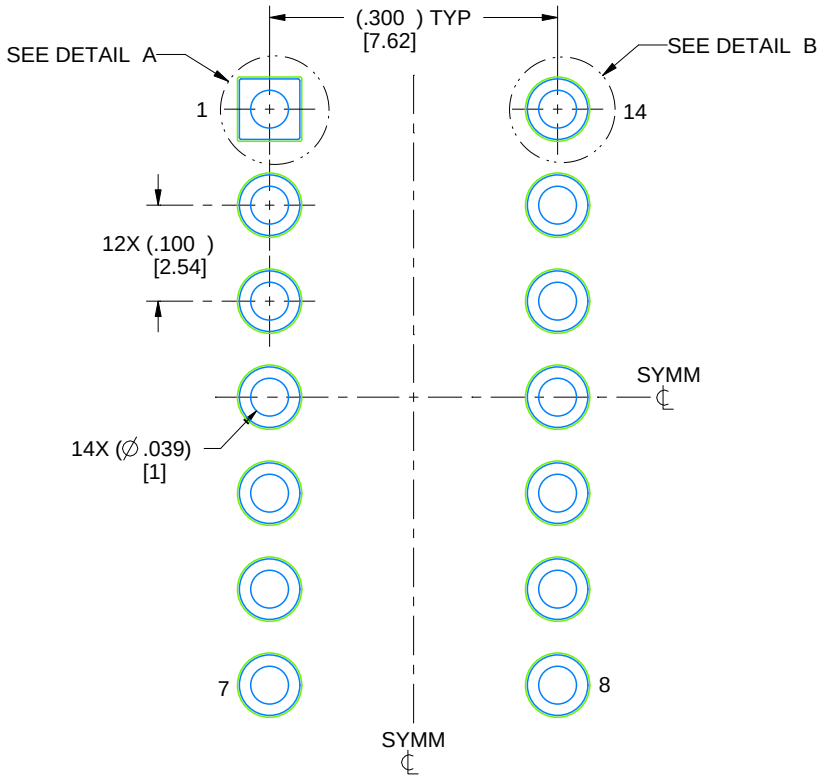
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

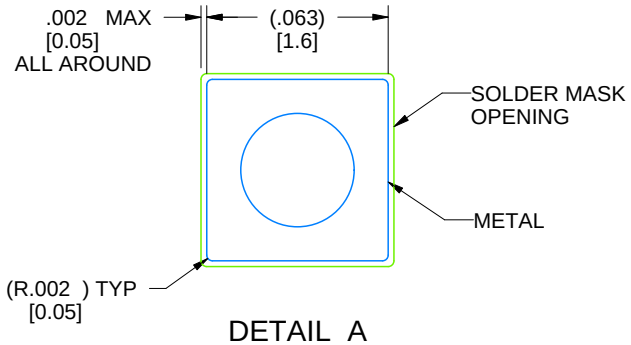
J0014A

CDIP - 5.08 mm max height

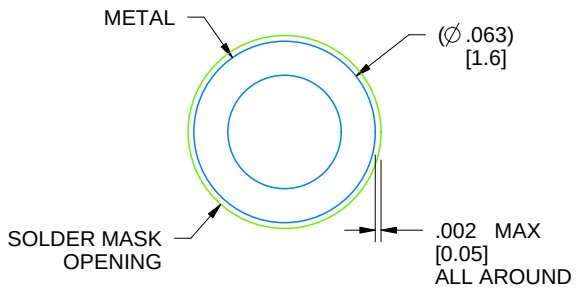
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



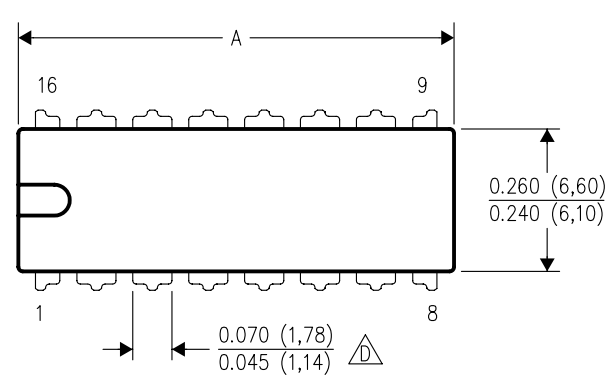
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

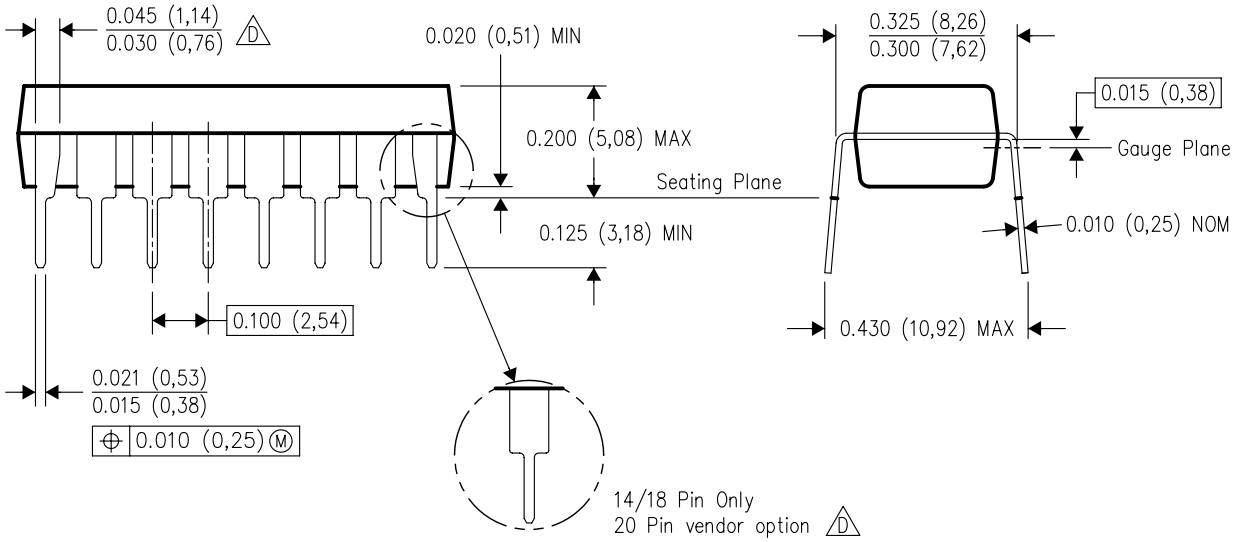
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

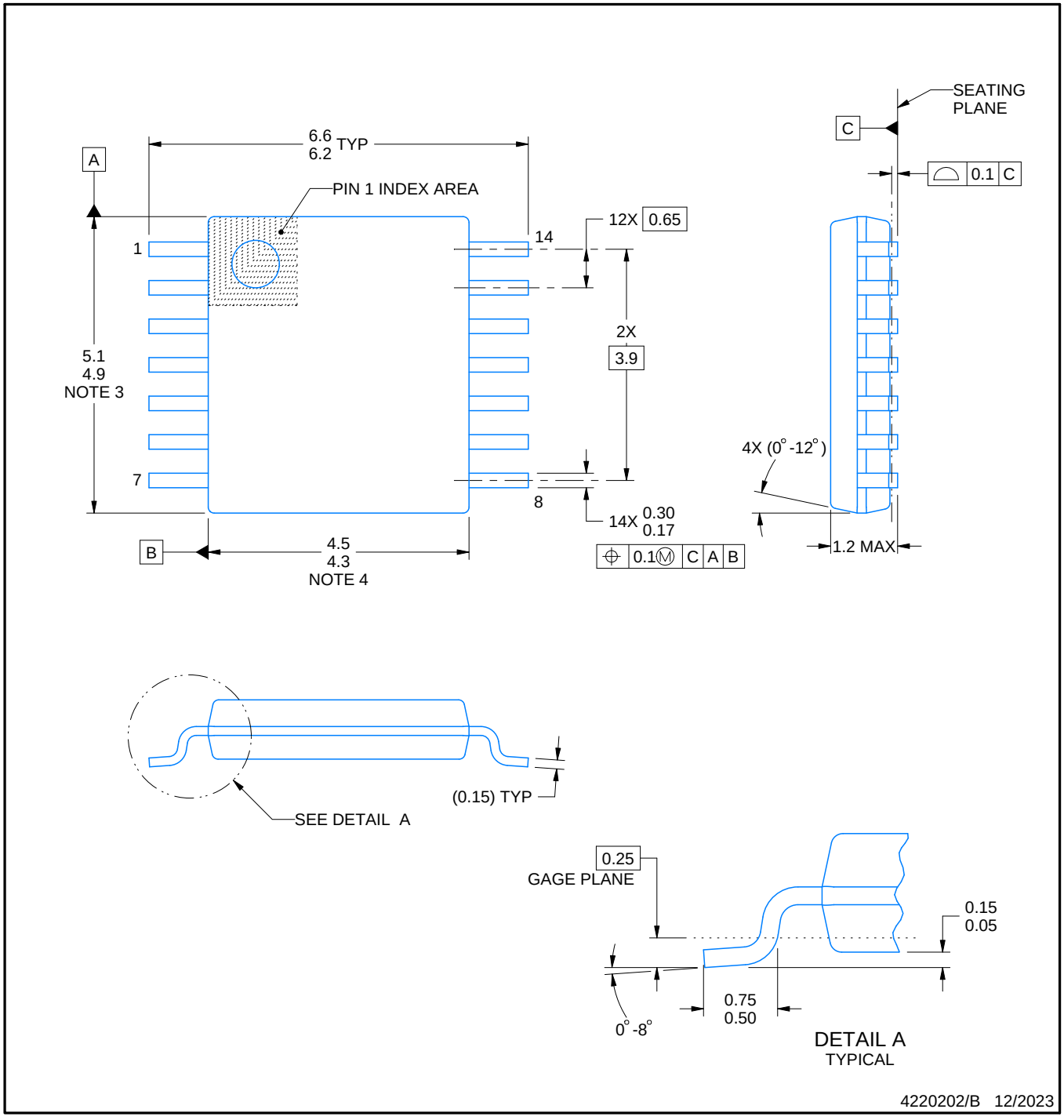
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

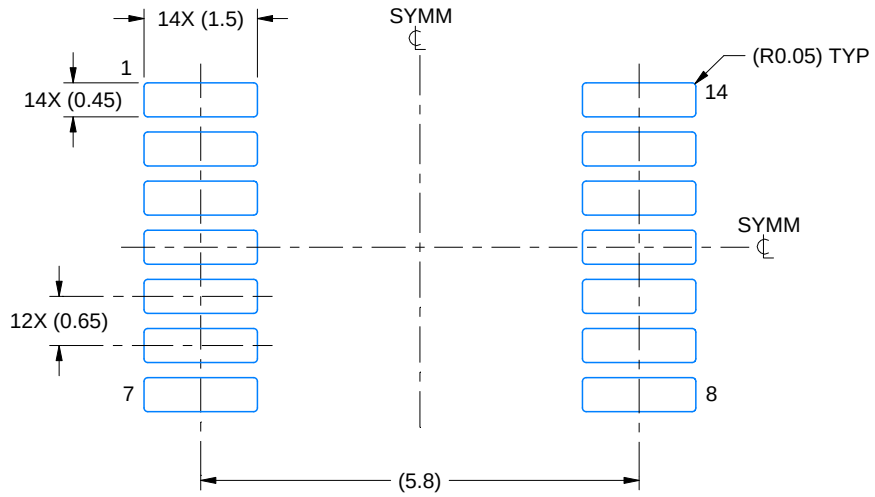
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

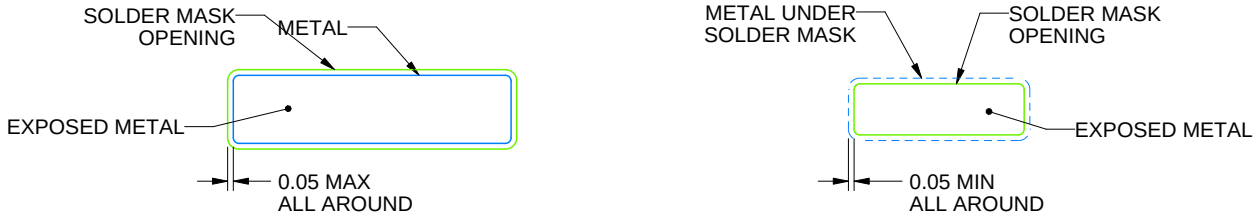


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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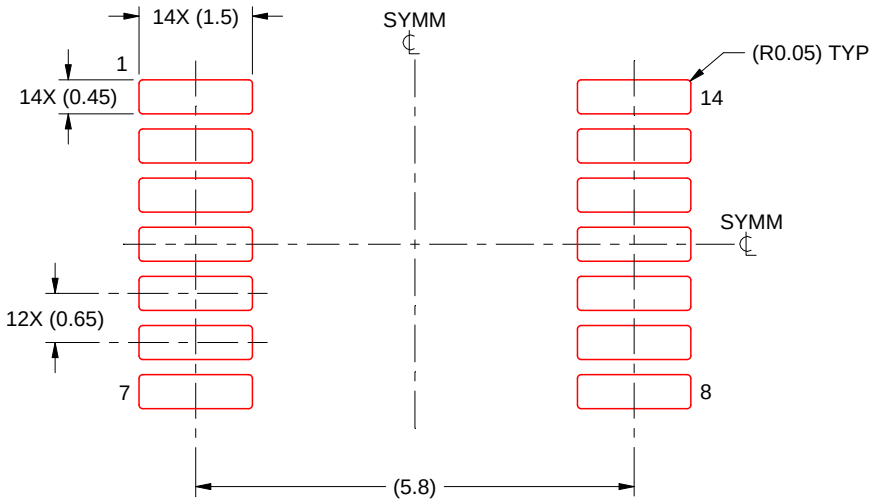
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月