SM74611 智能旁路二极管

1 特性

- 最低反向电压 (V_R)：30V
- 正向工作电流 (I_F)：高达 15A
- 低平均正向电压：8A 时为 26mV
- 功耗比肖特基二极管低
- 泄漏电流比肖特基二极管低
- 与传统的 D2PAK 肖特基二极管封装和引脚兼容
- 工作温度范围 (Tj)：-40°C 至 125°C

2 应用

- 用于光伏板的旁路二极管
- 用于微型逆变器和电源优化器的旁路二极管

3 说明

SM74611 是一款面向光伏应用的智能旁路二极管。 该二极管可为正常工作期间被遮蔽的部分光伏板提供另外一条线串电流路径。 如果没有旁路二极管，被遮蔽单元会因反向偏置单元功耗过大而呈现为过热点。

目前采用传统的 P-N 结二极管或肖特基二极管来缓解这一问题。 遗憾的是，此类二极管的正向电压仍偏高（普通二极管约为 0.6V，而肖特基二极管为 0.4V）。 当流过二极管的电流为 10A 时，功耗会高达 6W。这会导致二极管所在接线盒的内部温度升高并降低模块可靠性。

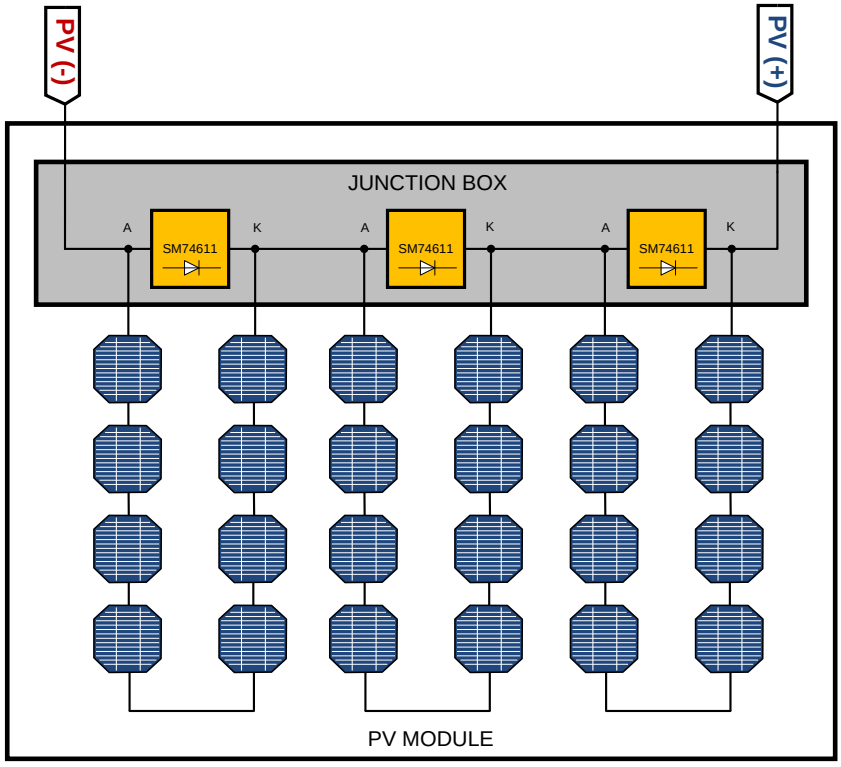
SM74611 的优势在于，正向压降比 P-N 结二极管和肖特基二极管低。 该二极管在 8A 电流下的平均正向压降典型值为 26mV。 此时的功耗典型值为 208mW，明显低于传统肖特基二极管的功耗典型值 3.2W。 此外，SM74611 还与传统的 D2PAK 肖特基二极管封装和引脚兼容，可以直接替换许多应用中的二极管。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SM74611	DDPAK/TO-263 (KTT) (3)	10.16mm x 9.02mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

在接线盒中的典型应用



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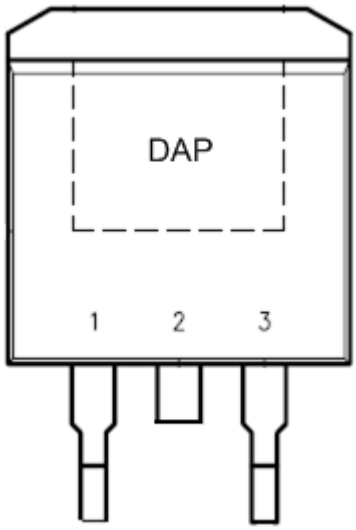
4 修订历史记录

Changes from Original (December 2012) to Revision A **Page**

- Added new junction temperature for t ≤ 1 hour 4
- Added Thermal Table 4
- Changed typical characteristic curves 5

5 Pin Configuration and Functions

DDPAK
3 Pin (KTT)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ANODE	1,3(1)	I	Connect both of these pins to the negative side of the PV cells
CATHODE	2,DAP(2)	O	Pin 2 and the DAP are shorted internally. Connect the DAP to the positive side of the PV cells

(1) Pin 1 and Pin 3 should be connected together for proper operation
(2) Package drawing at the end of datasheet is shown without Pin 2 being trimmed

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

	MIN	MAX	UNIT
Ambient Storage temperature, T_{stg}	-65	125	°C
DC Reverse Voltage		30	V
Forward Current		24	A
Junction Temperature, t ≤ 1 hour		135	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) System must be thermally managed so as not to exceed maximum junction temperature

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±YYY V may actually have higher performance.

6.3 Recommended Operating Conditions (1)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DC Reverse Voltage				28	V
Junction Temperature Range (T_J)		-40		125	°C
Forward Current		0		15	A

(1) System must be thermally managed so as not to exceed maximum junction temperature

6.4 Thermal Information

THERMAL METRIC (1)		SM74611 DDPAK (KTT) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.0	
ψ_{JT}	Junction-to-top characterization parameter	9.8	
ψ_{JB}	Junction-to-board characterization parameter	22.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{F(AVG)}$	Forward Current				8	15	A
$V_{F(AVG)}$	Forward Voltage	I_F = 8A	T_J = 25°C		26		mV

Electrical Characteristics (continued)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_D	Power Dissipation	I_F = 8A	T_J = 25°C		208		mW
			T_J = 125°C		450		
			-40°C to 125°C (1)			575	
		I_F = 15A	T_J = 25°C		695		
			T_J = 125°C		1389		
D	Duty Cycle	I_F = 8A	T_J = 25°C		99.5%		
			T_J = 125°C		96.0%		
I_R	Reverse Leakage Current	$V_{REVERSE}$ = 28V	T_J = 25°C		0.3		µA
			T_J = 125°C		3.3		

(1) Limits -40°C to 125°C apply over the entire junction temperature range for operation. Limits appearing in normal type apply for $T_A = T_J$ = 25°C.

6.6 Typical Characteristics

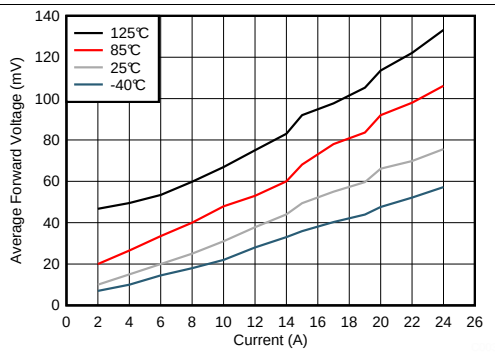


Figure 1. Average Forward Voltage (Anode to Cathode) Over Temperature

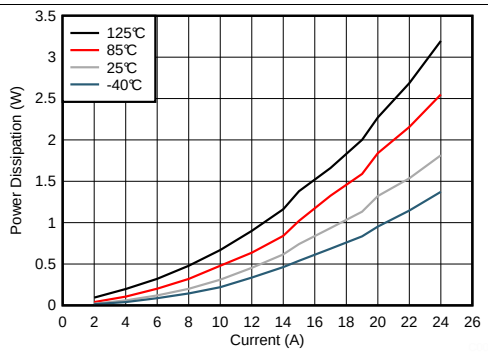


Figure 2. Power Dissipation Over Temperature

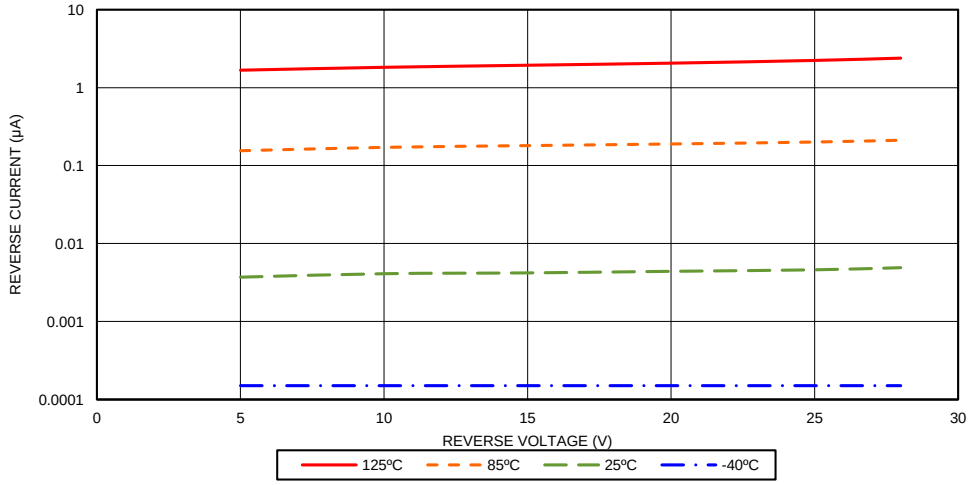


Figure 3. Reverse Current Over Temperature (Cathode to Anode)

7 Detailed Description

7.1 Overview

The SM74611 is designed for use as a bypass diode in photovoltaic modules. The SM74611 utilizes a charge pump to drive an N-channel FET to provide a resistive path for the bypass current to flow.

7.2 Functional Block Diagram

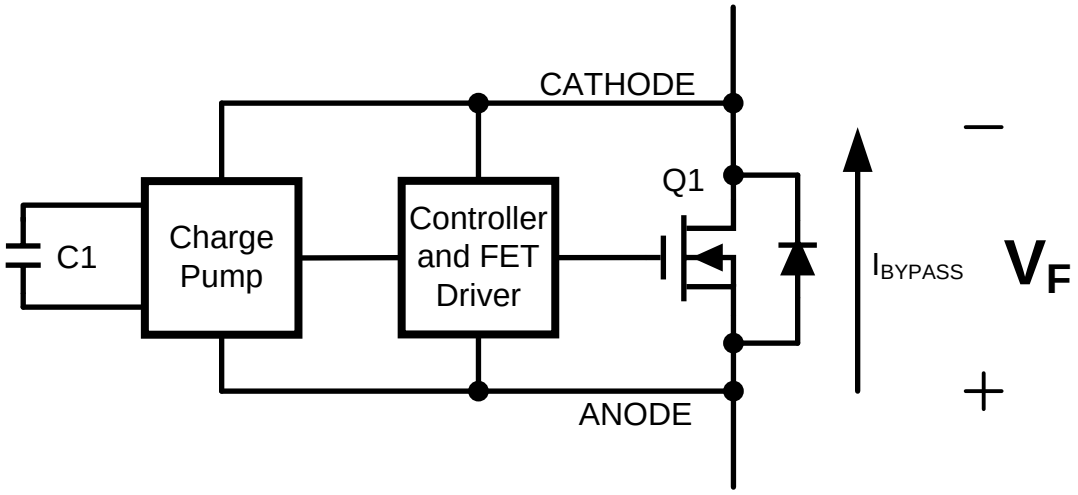


Figure 4. SM74611 Block Diagram

7.3 Feature Description

The operational description is described below. Please refer to Figure 4 and Figure 5.

From t_0 to t_1:

When cells in the solar panels are shaded, the FET Q1 is off and the bypass current will flow through the body diode of the FET as shown on Figure 4. This current will produce a voltage drop (V_F) across ANODE and CATHODE terminal of the bypass diode. During this time, the charge pump circuitry is active and charging capacitor C1 to a higher voltage.

At t_1:

Once the voltage on the capacitor reaches its predetermined voltage level, the charge pump is disabled and the capacitor voltage is used to drive the FET through the FET driver stage.

From t_1 to t_2 :

When the FET is active, it provides a low resistive path for the bypass current to flow thus minimizing the power dissipation across ANODE and CATHODE. Since the FET is active, the voltage across the ANODE and CATHODE is too low to operate the charge pump. During this time, the stored charge on C1 is used to supply the controller as well as drive the FET.

At t_2:

When the voltage on the capacitor C1 reaches its predetermined lower level, the FET driver shuts off the FET. The bypass current will then begin to flow through the body diode of the FET, causing the FET body diode voltage drop of approximately 0.6V to appear across ANODE and CATHODE. The charge pump circuitry is re-activated and begins charging the capacitor C1. This cycle repeats until the shade on the panel is removed and the string current begins to flow through the PV cells instead of the body diode of the FET.

The key factor to minimizing the power dissipation on the device is to keep the FET on at a high duty cycle. The average forward voltage drop will then be reduced to a much lower voltage than for a Schottky or regular P-N junction diode.

Feature Description (continued)

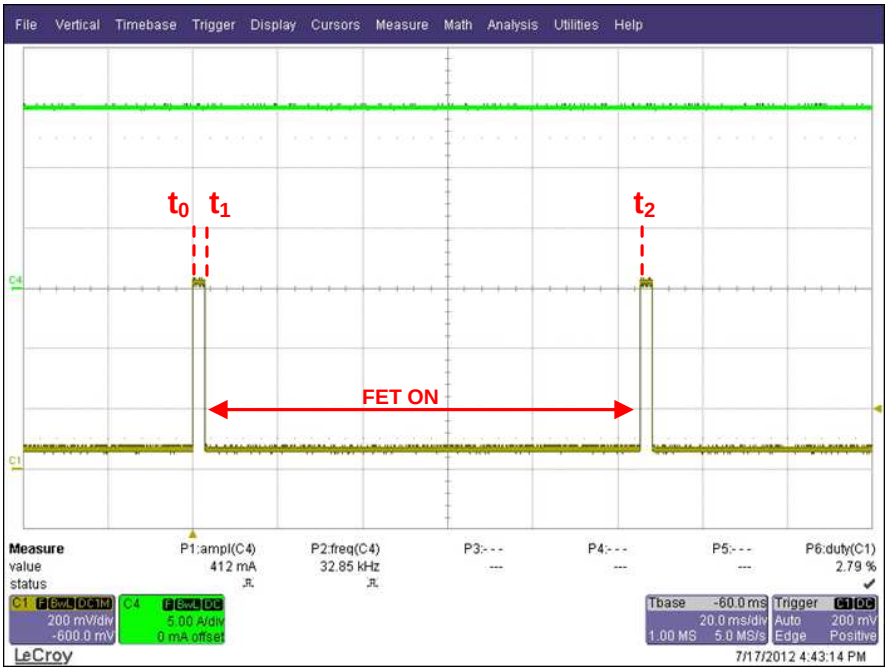


Figure 5. ANODE to CATHODE Voltage (Ch1) with I_{BYPASS} = 15A (Ch4) for SM74611 in Junction Box at 85˚C Ambient

8 器件和文档支持

8.1 商标

All trademarks are the property of their respective owners.

8.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

9 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SM74611KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	SM74611KTT
SM74611KTTR.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

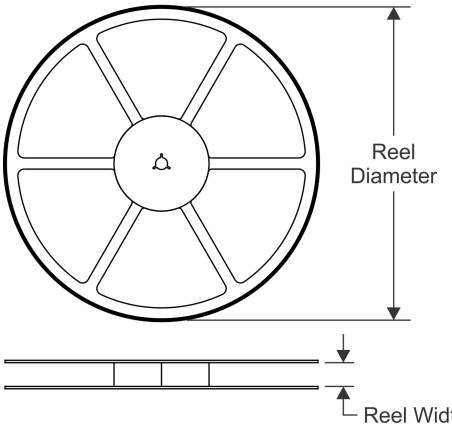
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

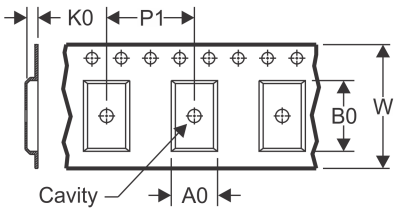
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

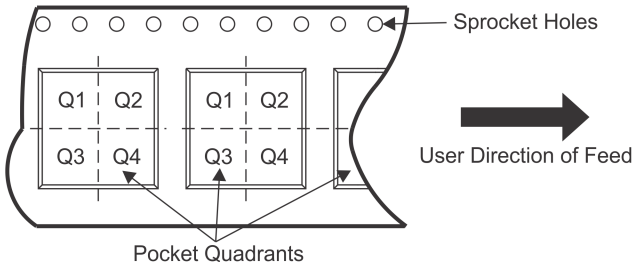


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

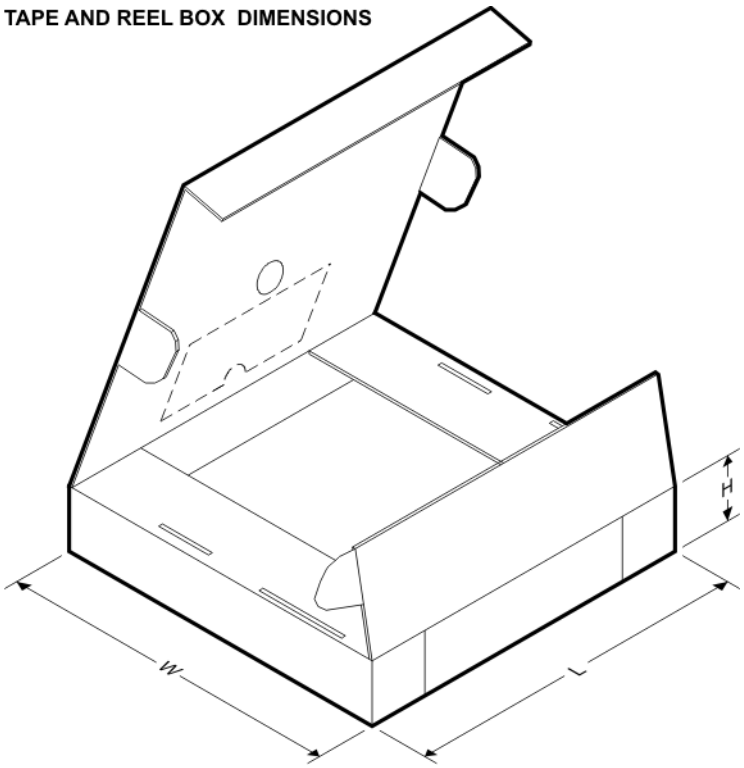
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM74611KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

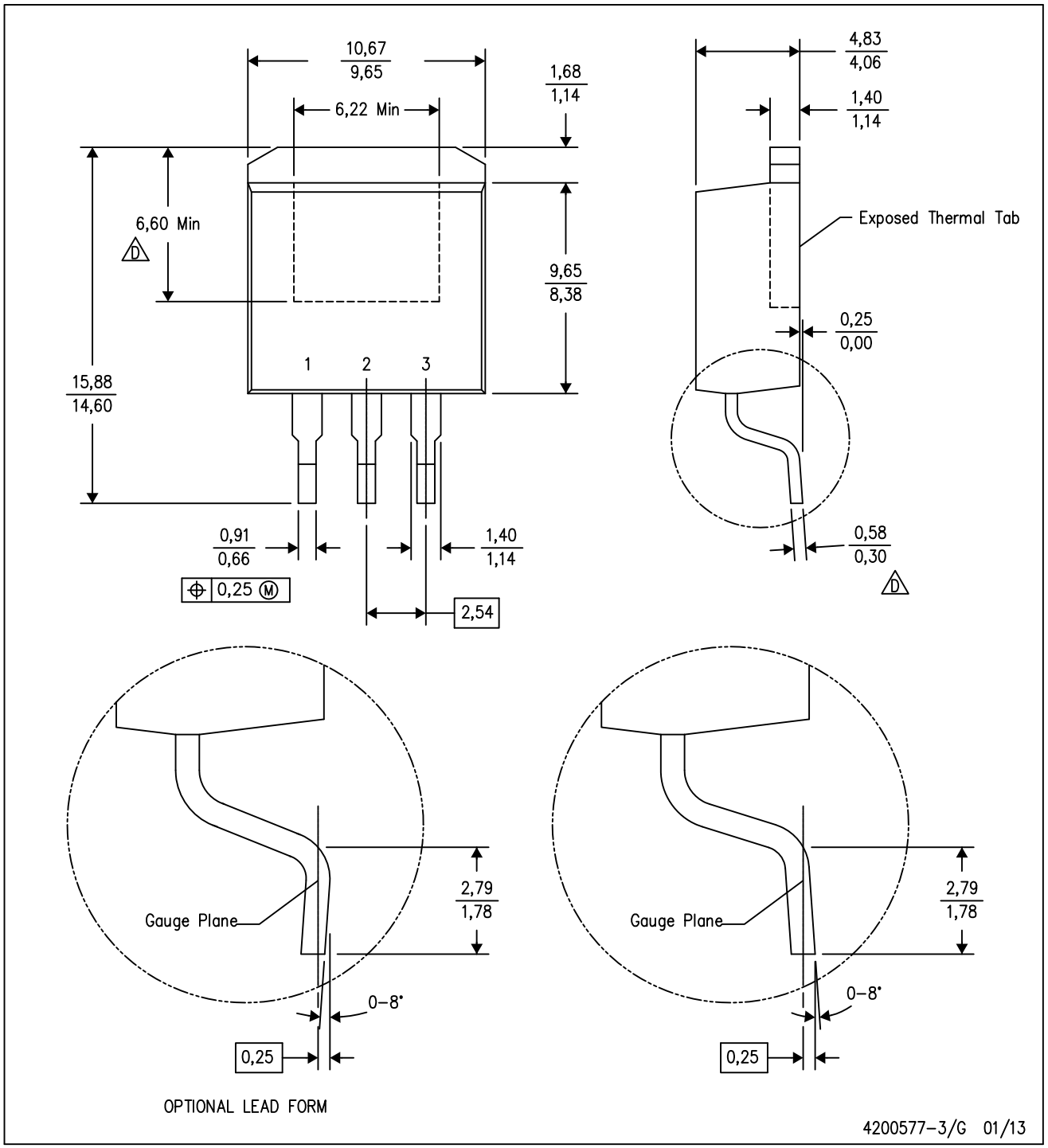
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM74611KTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

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