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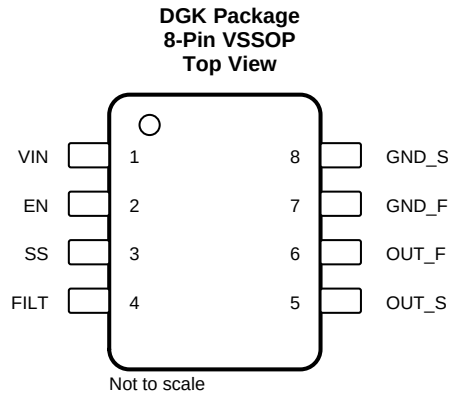
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日期	修订版本	注释
2016 年 9 月	*	最初发布。

4 Device Comparison Table

DEVICE FAMILY	TEMPERATURE DRIFT
REF60xx	5 ppm/°C from –40 to 125°C
REF61xx	8 ppm/°C from –40 to 125°C
REF62xx	3 ppm/°C from 0 to 70°C

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Input	Enable pin
FILT	4	—	Filter capacitor pin. A capacitor ($C_{FILT} \geq 1 \mu F$) must be connected between the FILT pin and ground for stability.
GND_F	7	Ground	Ground force pin
GND_S	8	Ground	Ground sense pin
OUT_F	6	Output	Output voltage force pin
OUT_S	5	Input	Output voltage sense pin
SS	3	—	Short circuit current limit pin. Connect a resistor to this pin to set the output short-circuit current limit. Connect to VIN pin for highest current limit
VIN	1	Power	Input supply voltage pin

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	$V_{IN} + 0.3$	V
Operating temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN} Supply input voltage ($I_{OUT} = 0$ mA)	REF6225	3		5.5	V
	REF6230, REF6233, REF6241, REF6245	$V_{OUT} + 0.25$		5.5	
	REF6250	5.3		5.5	
V_{EN} Enable voltage		0		V_{IN}	V
I_L Output current	REF6225, REF6230, REF6233, REF6241	–4		4	mA
	REF6245	–3.5		3.5	
	REF6250	–3		3	
T_A Operating temperature		0	25	70	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF62xx	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$ for all devices except REF6250, $V_{IN} = 5.4\text{ V}$ for REF6250, $I_L = 0\text{ mA}$, $C_L = 22\text{ }\mu\text{F}$, $C_{FILT} = 1\text{ }\mu\text{F}$, and $V_{EN} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
Output voltage accuracy					-0.05%	0.05%		
Output voltage temperature coefficient ⁽¹⁾						3	ppm/°C	
LINE AND LOAD REGULATION								
$\Delta V_{O(\Delta V)}$ Line regulation	REF6225	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	4	20	ppm/V		
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	30				
	REF6230, REF6233, REF6241, REF6245	$V_{OUT} + 0.25\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	4	20			
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	30				
	REF6250	$V_{OUT} + 0.3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$	7	60			
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	120				
$\Delta V_{O(\Delta I)}$ Load regulation, sourcing and sinking	REF6225, REF6230, REF6233, REF6241	$I_L = 0\text{ mA to } 4\text{ mA}, V_{IN} = V_{OUT} + 600\text{ mV}$	$T_A = 25^\circ\text{C}$	2	20	ppm/mA		
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	30				
	REF6245	$I_L = 0\text{ mA to } 3.5\text{ mA}, V_{IN} = V_{OUT} + 600\text{ mV}$	$T_A = 25^\circ\text{C}$	2	20			
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	30				
	REF6250	$I_L = 0\text{ mA to } 3\text{ mA}, V_{IN} = V_{OUT} + 400\text{ mV}$	$T_A = 25^\circ\text{C}$	2	20			
			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	50				
I_{SC} Short-circuit current	SS = open			10.5		mA		
NOISE								
Total integrated noise	$C_L = 22\text{ }\mu\text{F}$			5		μV_{RMS}		
	$C_L = 47\text{ }\mu\text{F}$			5				
Low frequency noise	$0.1\text{ Hz} \leq f \leq 10\text{ Hz}$			3		$\mu\text{V}_{PP}/\text{V}$		
OUTPUT IMPEDANCE								
Output impedance	$f = \text{DC to } 200\text{ kHz}, C_L = 47\text{ }\mu\text{F}$			50		$\text{m}\Omega$		
TURN-ON TIME								
t_{on} Turn-on time	0.1% settling, $C_L = 47\text{ }\mu\text{F}$, SS = open, REF6225			100		ms		
HYSTERESIS AND LONG TERM DRIFT								
Long term stability	0 to 1000h at 25°C			80		ppm		
	1000h to 2000h at 25°C			20				
Output voltage hysteresis ⁽²⁾	$25^\circ\text{C}, 0^\circ\text{C}, 70^\circ\text{C}, 25^\circ\text{C}$ (cycle 1)			33		ppm		
	$25^\circ\text{C}, 0^\circ\text{C}, 70^\circ\text{C}, 25^\circ\text{C}$ (cycle 2)			8				
CAPACITIVE LOAD								
C_L Stable output capacitor value				10		47	μF	

(1) Temperature drift is specified according to the box method. See the [Feature Description](#) section for more details.

(2) See the [Thermal Hysteresis](#) section.

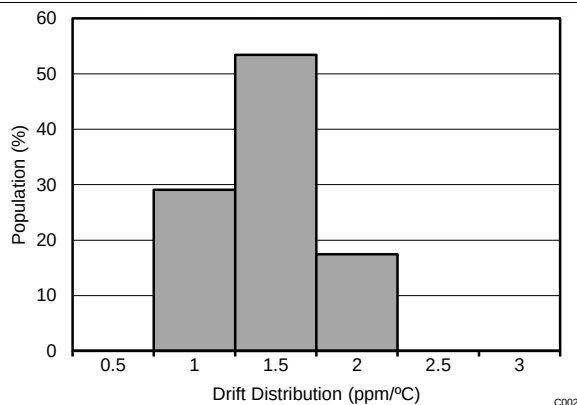
Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$ for all devices except REF6250, $V_{IN} = 5.4\text{ V}$ for REF6250, $I_L = 0\text{ mA}$, $C_L = 22\text{ }\mu\text{F}$, $C_{FILT} = 1\text{ }\mu\text{F}$, and $V_{EN} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE								
V _{OUT}	Output voltage	REF6225			2.5		V	
		REF6230			3			
		REF6233			3.3			
		REF6241			4.096			
		REF6245			4.5			
		REF6250			5			
POWER SUPPLY								
I _{CC}	Supply current	REF6225, REF6230, REF6233, REF6241	Active mode, V _{EN} = 5 V	T _A = 25°C	0.82	0.90	mA	
				T _A = −40°C to +125°C		1.1		
		REF6245, REF6250	Active mode, V _{EN} = 5 V	T _A = 25°C	0.83	0.95		
				T _A = −40°C to +125°C		1.15		
		Shutdown mode, V _{EN} = 0 V			T _A = 25°C	1	3	μA
					T _A = −40°C to +125°C		15	
Enable pin voltage		Voltage reference in active mode (EN = 1)			1.6		V	
		Voltage reference in shutdown mode (EN = 0)			0.6			
Enable pin current		V _{EN} = 5 V			100	150	nA	
Dropout voltage		REF6225		I _L = 0 mA	500	500	mV	
				I _L = 4 mA		600		
		REF6230, REF6233, REF6241		I _L = 0 mA	50	250		
				I _L = 4 mA		600		
		REF6245		I _L = 0 mA	50	250		
				I _L = 3.5 mA		600		
		REF6250		I _L = 0 mA	100	300		
				I _L = 3 mA		400		

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)



$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Figure 1. Drift Distribution

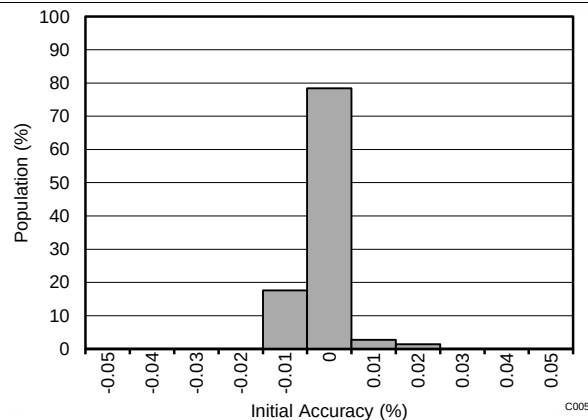


Figure 2. Initial Accuracy Distribution

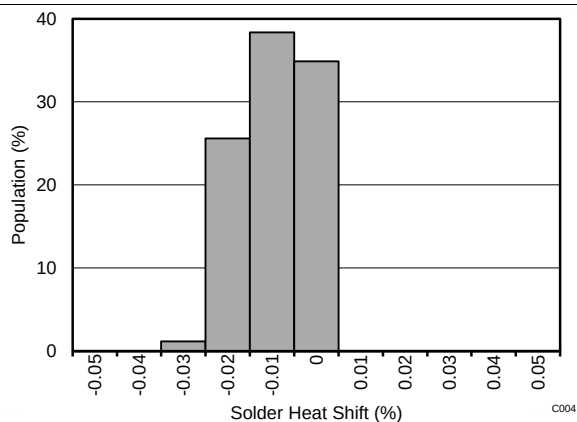


Figure 3. Solder-Heat Shift Distribution

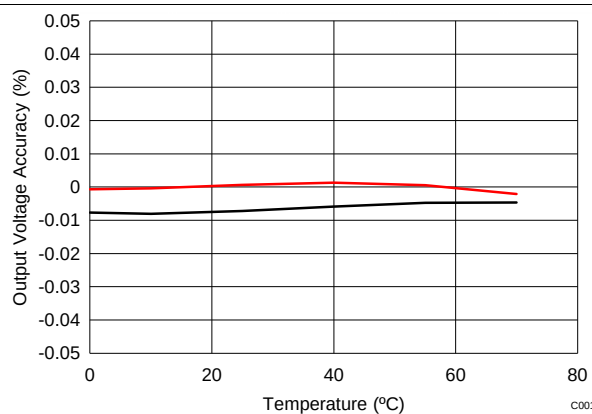


Figure 4. Output Voltage Accuracy vs Temperature

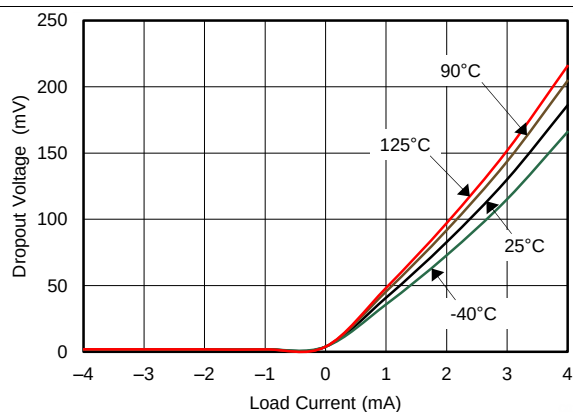
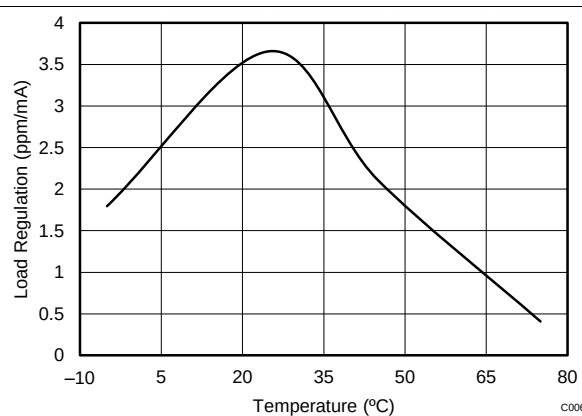


Figure 5. Dropout Voltage vs Load Current

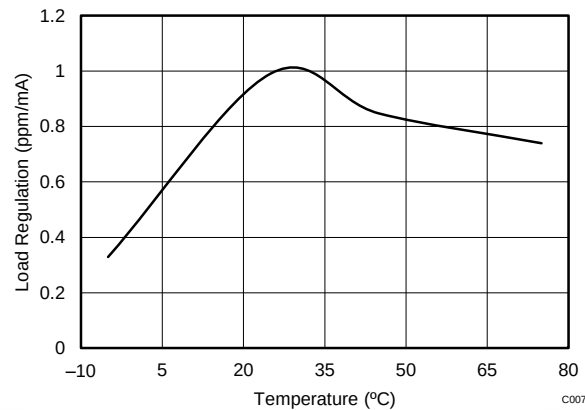


$V_{IN} = V_{OUT} + 600\text{ mV}$,
 $I_L = 0\text{ mA}$ to 4 mA

Figure 6. Load Regulation Sourcing vs Temperature

Typical Characteristics (continued)

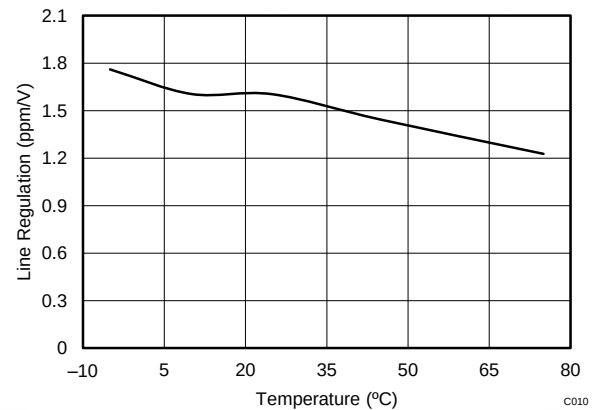
at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)



$$V_{IN} = V_{OUT} + 600\text{ mV},$$

$$I_L = 0\text{ mA to } 4\text{ mA}$$

Figure 7. Load Regulation Sinking vs Temperature



$$V_{OUT} + 0.25\text{ V} \leq V_{IN} \leq 5.5\text{ V}$$

Figure 8. Line Regulation vs Temperature

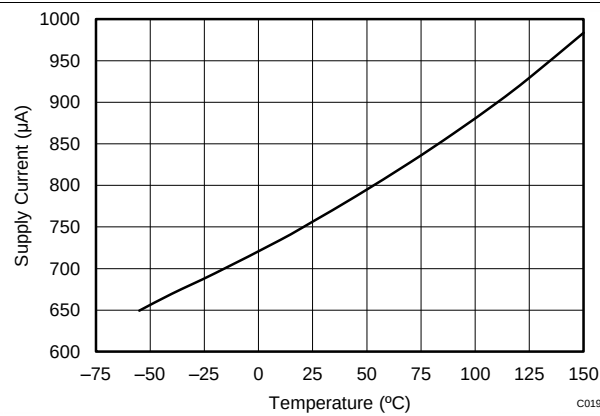


Figure 9. Supply Current vs Temperature

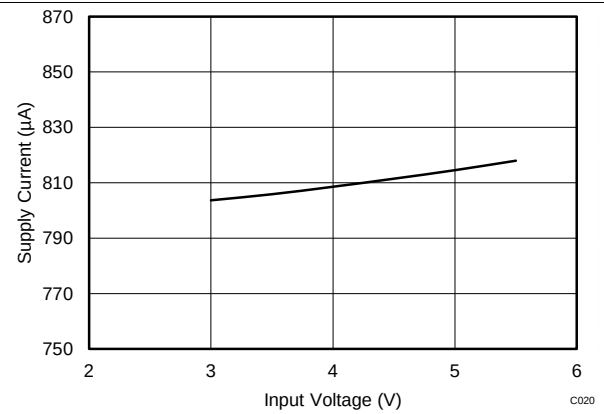


Figure 10. Supply Current vs Input Voltage

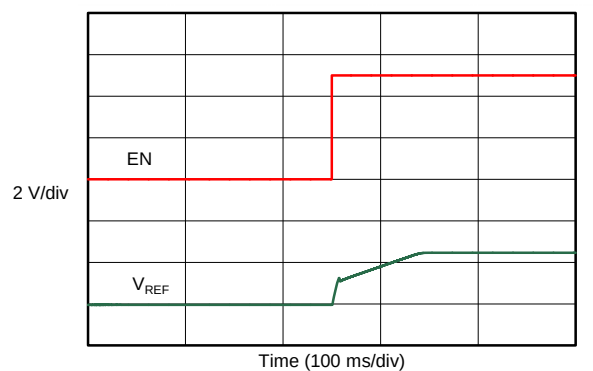


Figure 11. Turn-On Settling Time

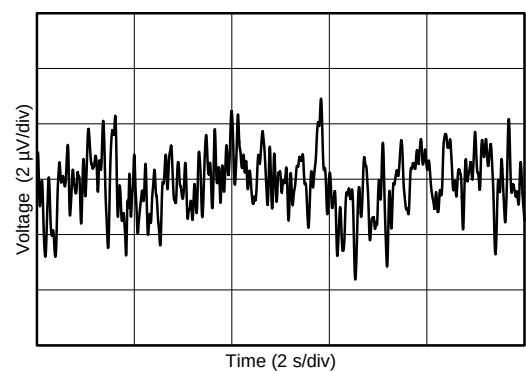


Figure 12. 0.1-Hz to 10-Hz Noise

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)

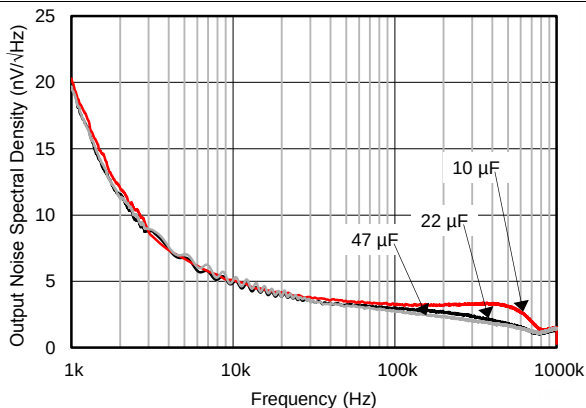


Figure 13. Output-Voltage Noise Spectrum

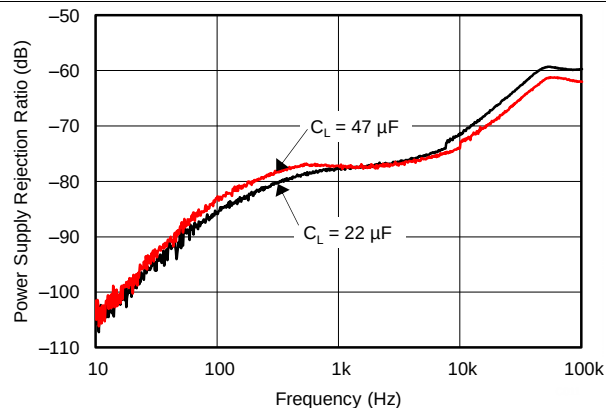
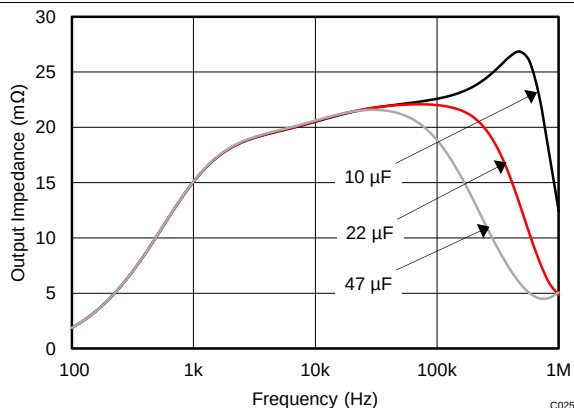
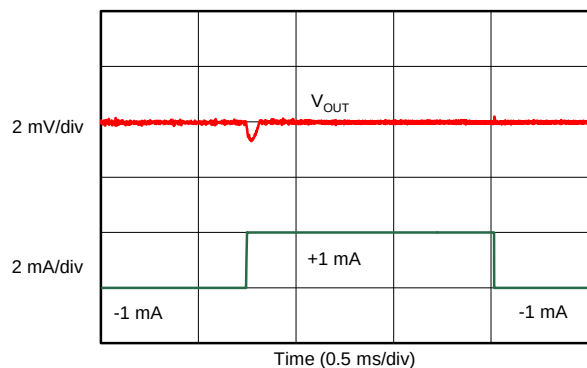


Figure 14. PSRR vs Frequency



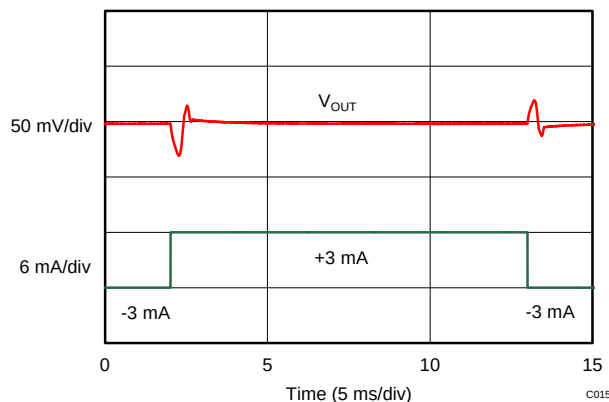
Graph obtained by design simulation

Figure 15. Output Impedance vs Frequency



Load current = $\pm 1\text{ mA}$

Figure 16. Load Transient Response



Load current = $\pm 3\text{ mA}$

Figure 17. Load Transient Response

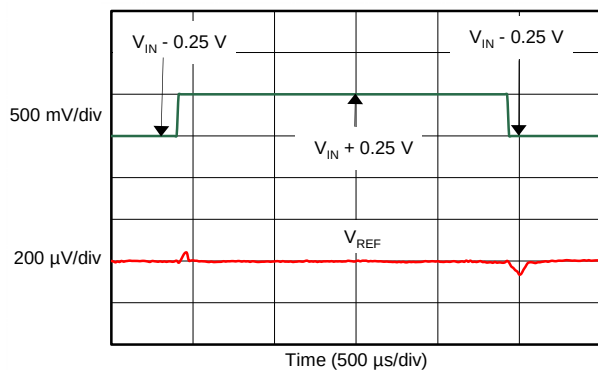
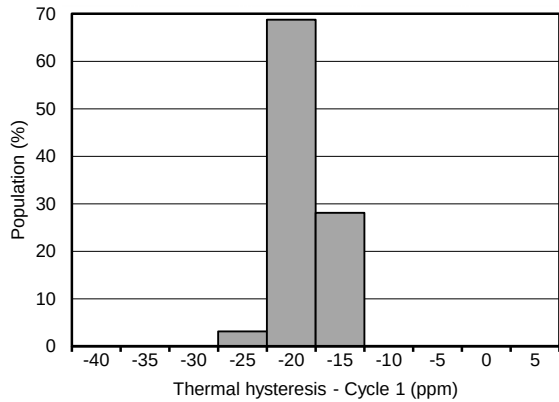


Figure 18. Line Transient Response

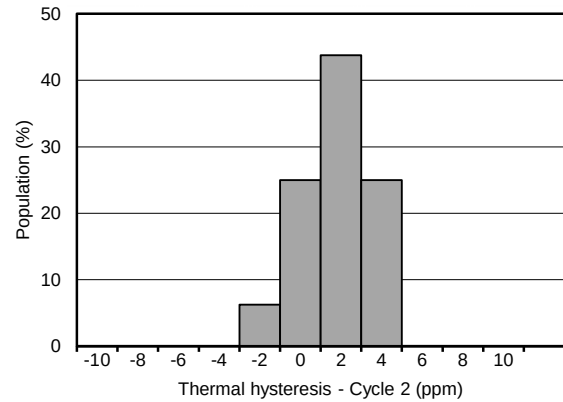
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)



C028

Figure 19. Thermal Hysteresis Distribution (Cycle 1)



C027

Figure 20. Thermal Hysteresis Distribution (Cycle 2)

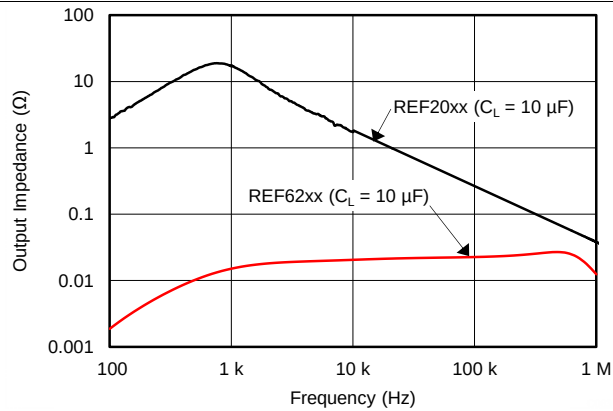
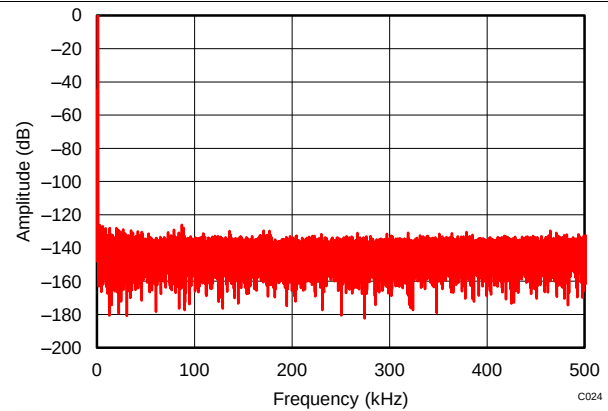
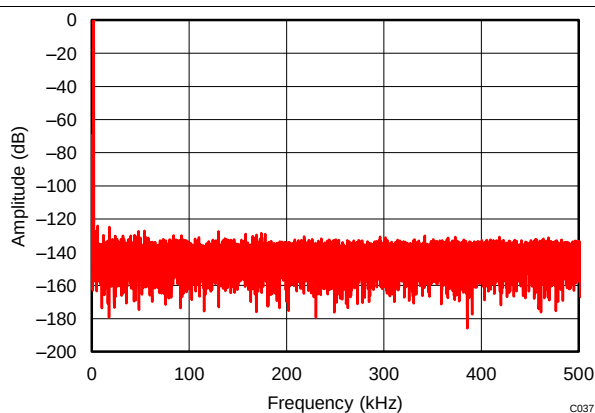


Figure 21. Output Impedance Comparison



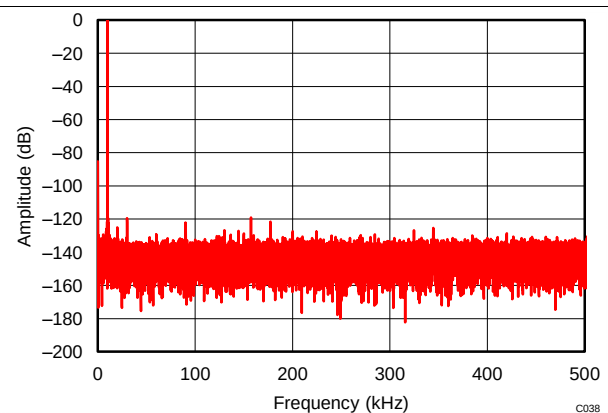
REF6250 driving REF pin of ADS8881,
 $f_{IN} = 1\text{ kHz}$, SNR = 100.5 dB, THD = -125.9 dB

Figure 22. Typical FFT Plot



REF6250 driving REF pin of ADS8881,
 $f_{IN} = 2\text{ kHz}$, SNR = 100.4 dB, THD = -123.9 dB

Figure 23. Typical FFT Plot



REF6250 driving REF pin of ADS8881,
 $f_{IN} = 10\text{ kHz}$, SNR = 99.2 dB, THD = -119.4 dB

Figure 24. Typical FFT Plot

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)

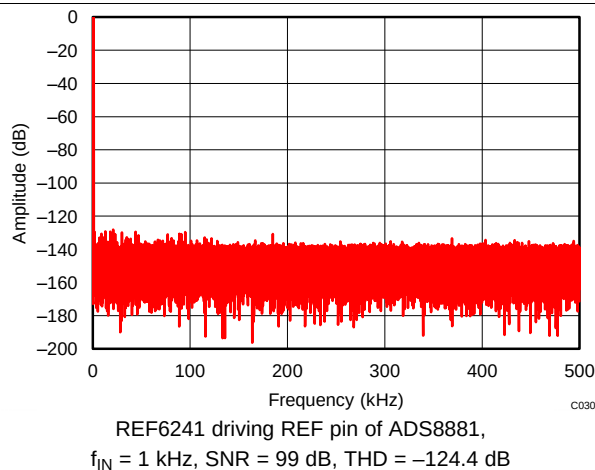


Figure 25. Typical FFT Plot

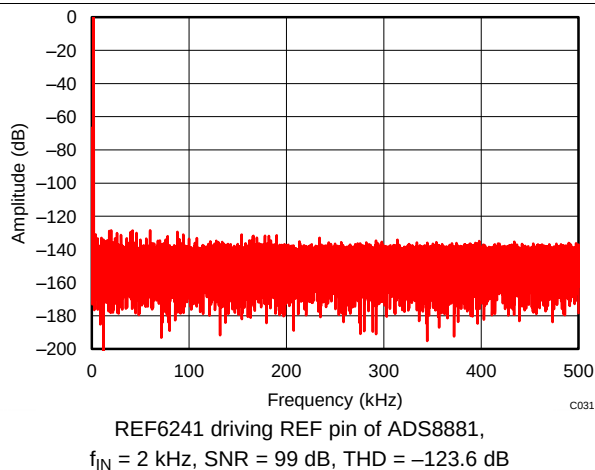


Figure 26. Typical FFT Plot

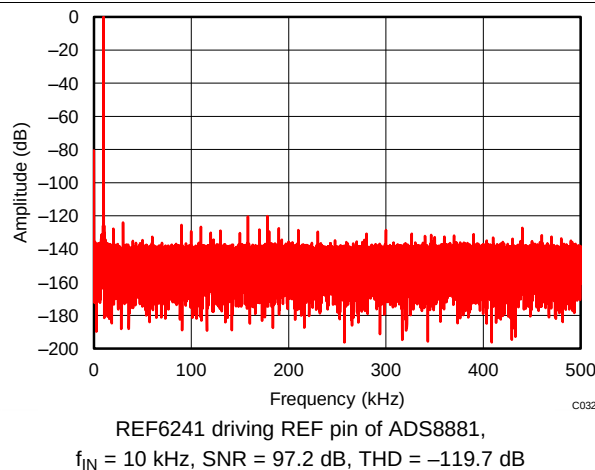


Figure 27. Typical FFT Plot

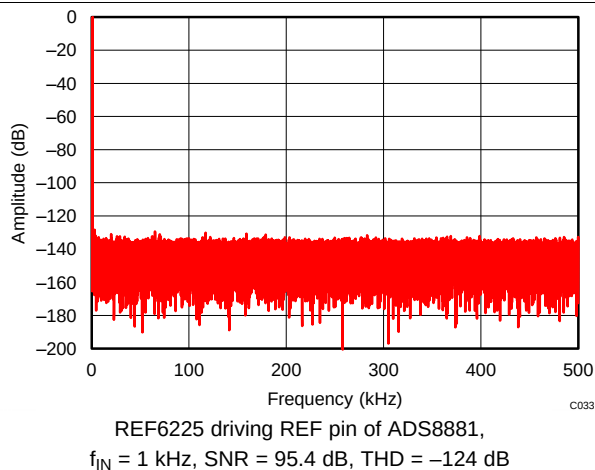


Figure 28. Typical FFT Plot

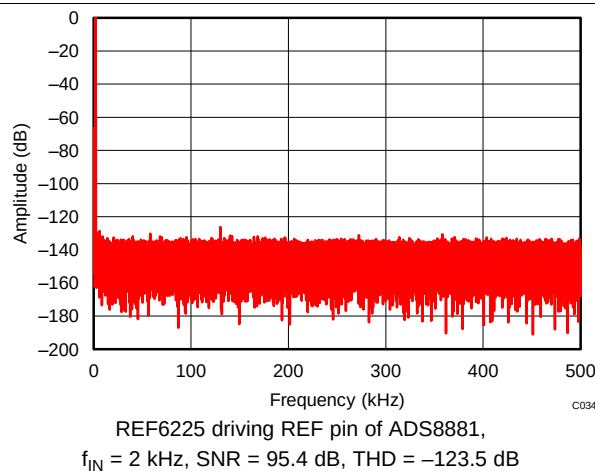


Figure 29. Typical FFT Plot

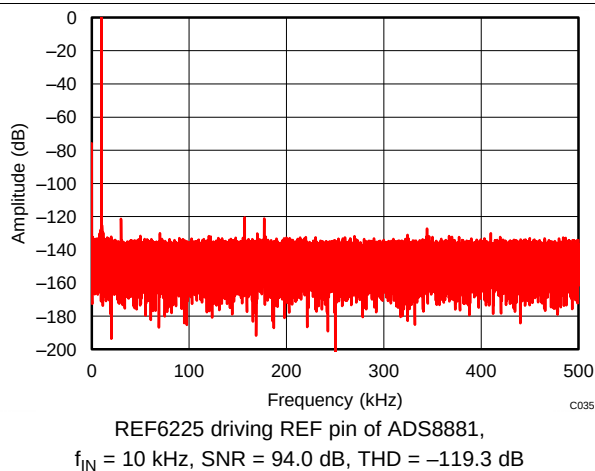
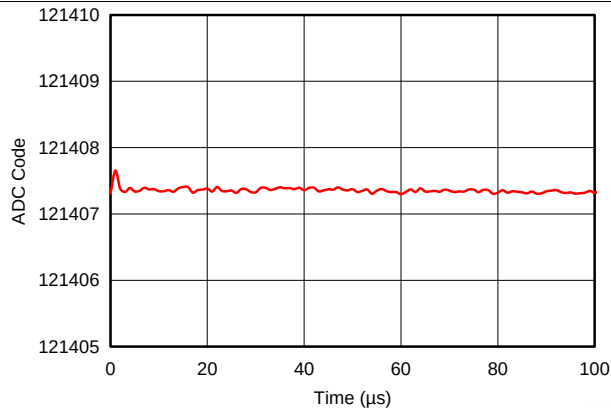


Figure 30. Typical FFT Plot

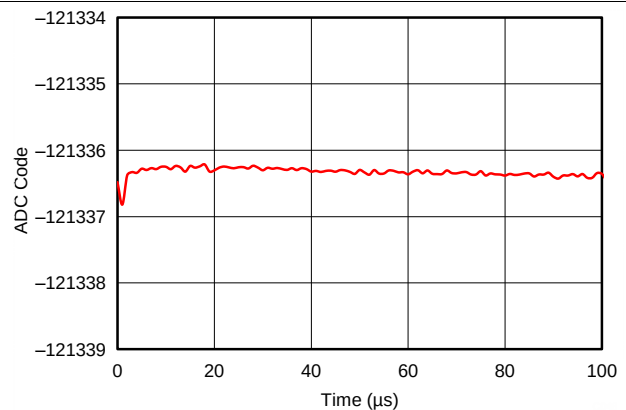
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)



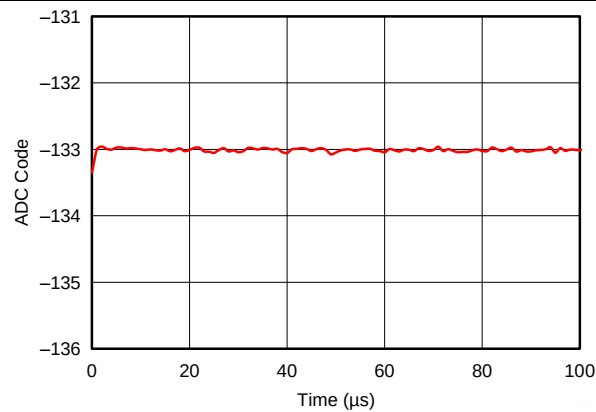
REF6250 driving REF pin of ADS8881 operating at 1 MSPS,
positive full-scale input to ADS8881

Figure 31. Reference Droop



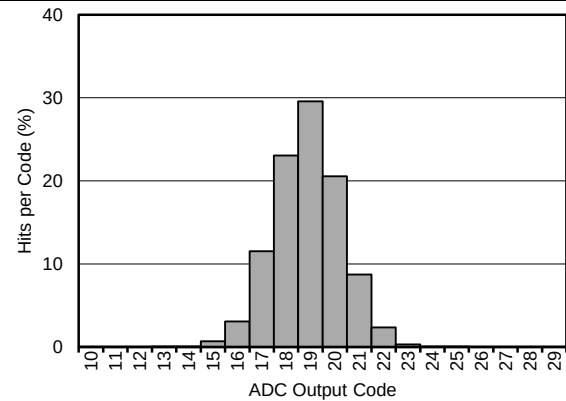
REF6250 driving REF pin of ADS8881 operating at 1 MSPS,
negative full-scale input to ADS8881

Figure 32. Reference Droop



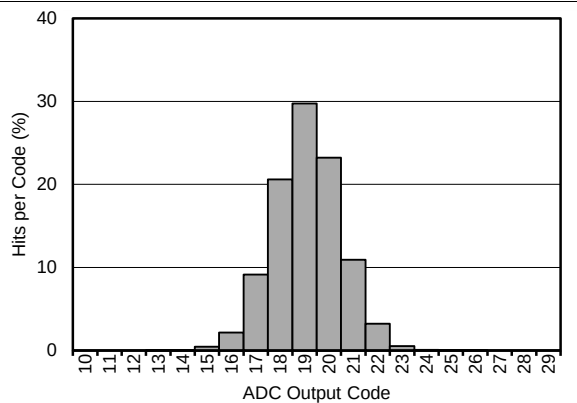
REF6250 driving REF pin of ADS8881 operating at 1 MSPS,
 $\text{AINP} = \text{AINN} = V_{\text{REF}} / 2$ for ADS8881

Figure 33. Reference Droop



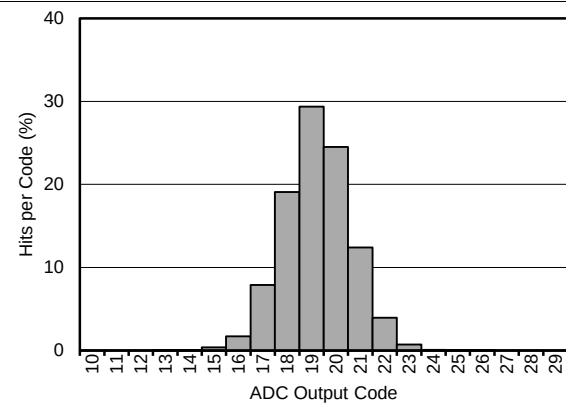
$\text{AINP} = \text{AINN} = V_{\text{REF}} / 2$ for ADS8881,
sampling rate = 1 MSPS

Figure 34. DC Input Histogram



$\text{AINP} = \text{AINN} = V_{\text{REF}} / 2$ for ADS8881,
sampling rate = 500 kSPS

Figure 35. DC Input Histogram

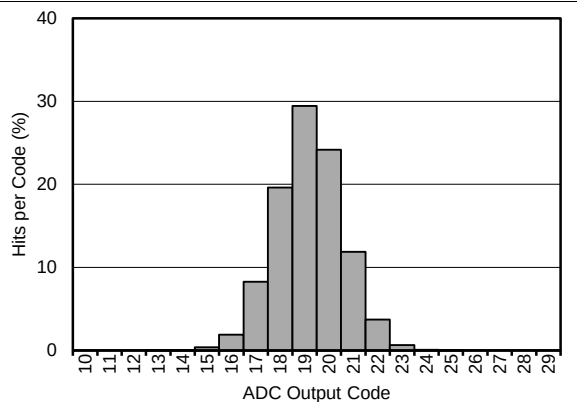


$\text{AINP} = \text{AINN} = V_{\text{REF}} / 2$ for ADS8881,
sampling rate = 100 kSPS

Figure 36. DC Input Histogram

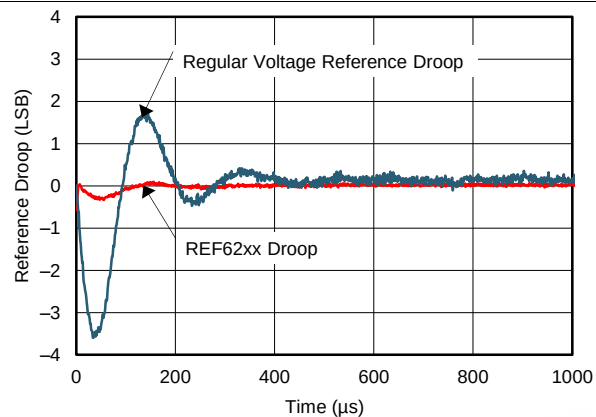
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, and $V_{IN} = 5\text{ V}$, using REF6225 (unless otherwise noted)



$A_{INP} = A_{INN} = V_{REF} / 2$ for ADS8881,
sampling rate = 20 kSPS

Figure 37. DC Input Histogram



1 LSB = 19.07 μV , with ADS8881 at 1 MSPS

Figure 38. Reference Droop Comparison

7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF62xx have differing coefficients of thermal expansion, and result in stress on the device die when the part is heated. Mechanical and thermal stress on the device die sometimes causes the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 128 devices were soldered on eight printed circuit boards (PCBs), with 16 devices on each PCB, using lead-free solder paste, and the manufacturer-suggested reflow profile. The reflow profile is as shown in [Figure 39](#). The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 101.6 mm × 127 mm.

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in [Figure 40](#). Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the PCB.

The histogram displays the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the final pass to minimize exposure to thermal stress.

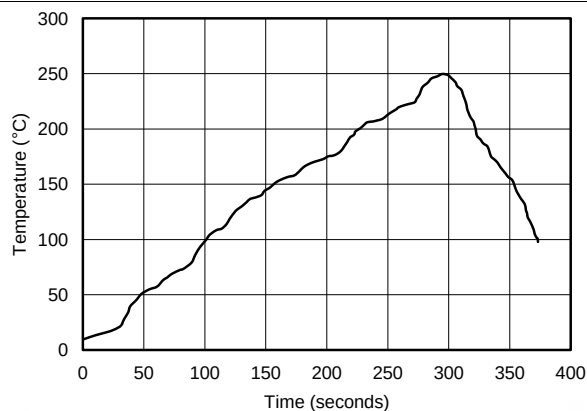


Figure 39. Reflow Profile

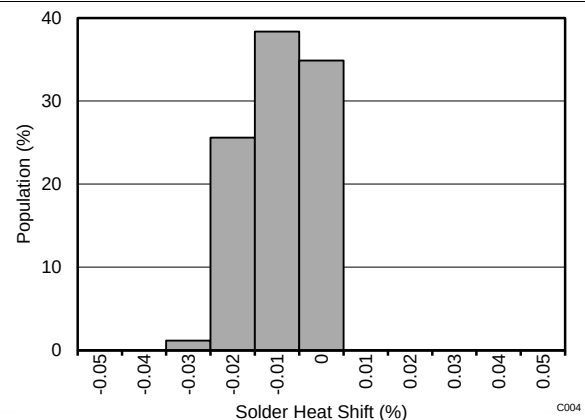


Figure 40. Solder Heat Shift Distribution

7.2 Thermal Hysteresis

Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Thermal hysteresis was measured with the REF62xx soldered to a PCB, similar to a real-world application. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Thermal hysteresis is expressed as:

$$V_{\text{HYST}} = \left(\frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \text{ (ppm)}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm).
 - V_{NOM} = the specified output voltage.
 - V_{PRE} = output voltage measured at 25°C pretemperature cycling.
 - V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of 0°C to 70°C and returns to 25°C.
- (1)

Typical thermal hysteresis distribution is shown in [Figure 41](#) and [Figure 42](#).

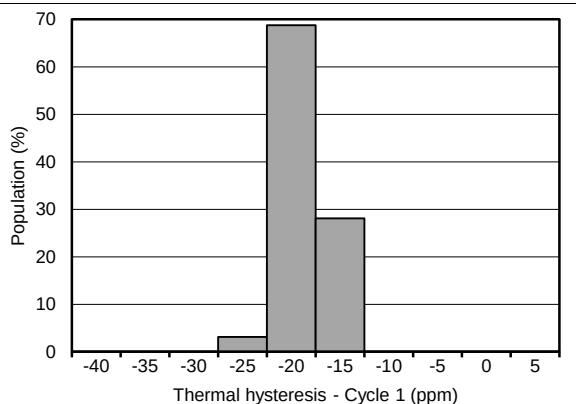


Figure 41. Thermal Hysteresis Distribution (Cycle 1)

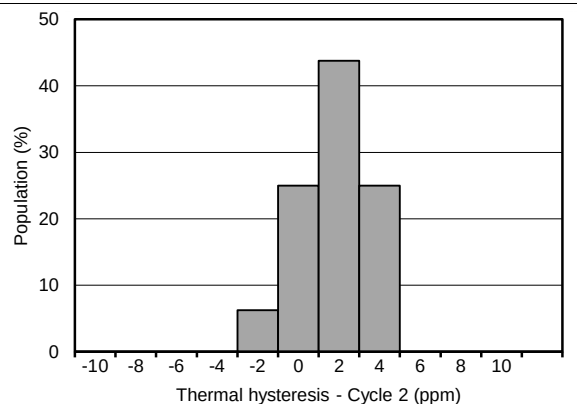


Figure 42. Thermal Hysteresis Distribution (Cycle 2)

7.3 Reference Droop Measurements

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data-acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is a very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. The REF62xx have an integrated ADC drive buffer that makes sure the reference droop is less than 1 LSB at 18-bit precision when used with the ADS8881, even at full throughput. [Figure 43](#) and [Figure 44](#) show the REF62xx output voltage droop when driving the REF pin of the ADS8881 at positive and negative full-scale inputs, respectively.

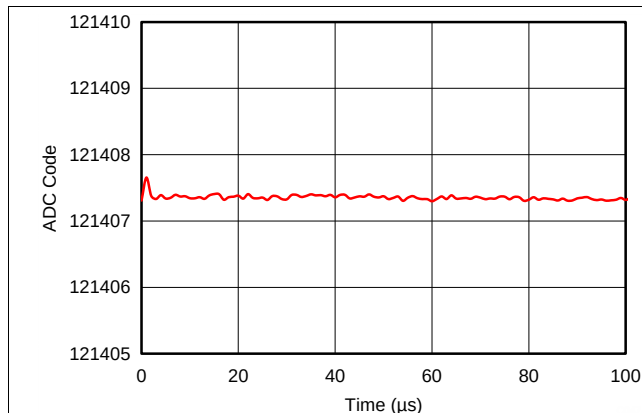


Figure 43. Output Voltage Droop

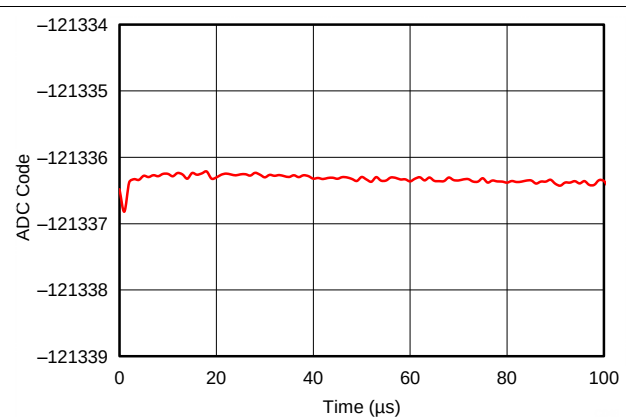


Figure 44. Output Voltage Droop

Direct measurement of the reference droop to 18-bit accuracy can be a challenging process. Therefore, the plots in [Figure 43](#) and [Figure 44](#) were obtained by processing the output code of the ADC. The ADC output code is given by:

$$C = (\text{Input Voltage} / V_{\text{REF}}) \times 2^N \quad (2)$$

If the input voltage is kept constant, V_{REF} is computed by monitoring the ADC output code C . The ADC code usually has six to seven LSBs of code spread due to the inherent noise of the ADC. In order to measure reference droop, this noise must be reduced drastically. Noise reduction is done by averaging the output code multiple times, as described in the next paragraph.

Reference Droop Measurements (continued)

Figure 45 shows the setup that was used to measure the reference droop. The output ADC code was captured using a field-programmable gate array (FPGA), and post-processing was done on a personal computer. The input to the THS4521, and hence in turn to the ADS8881, is a constant dc voltage (close to positive or negative full-scale because this condition is the worst-case for charge drawn from the REF pin). The dc source must have extremely low noise. After the REF62xx device is powered up and stable, the FPGA sends commands to the ADS8881 to capture data in bursts. The ADS8881 is initially in idle mode for 100 ms. The FPGA then sends a command to the ADS8881 to perform 100 conversions at 1 MSPS. The ADC code corresponding to these 100 conversions (one burst of data) is stored as the first row in a 1000×100 dimensional array. This operation is repeated 1000 times, and the data corresponding to each burst is stored in a new row of the 1000×100 dimensional array. Finally, each column in this array is averaged to get a final data-set of 100 elements. This final data-set now has code spread that is much less than 1 LSB because most of the noise has now been removed through averaging. This data-set was plotted on a graph with X axis = column number (each column number corresponds to $1 \mu\text{s}$ of time because the sampling rate is 1 MSPS), and Y axis = ADC output code to obtain reference-droop measurements.

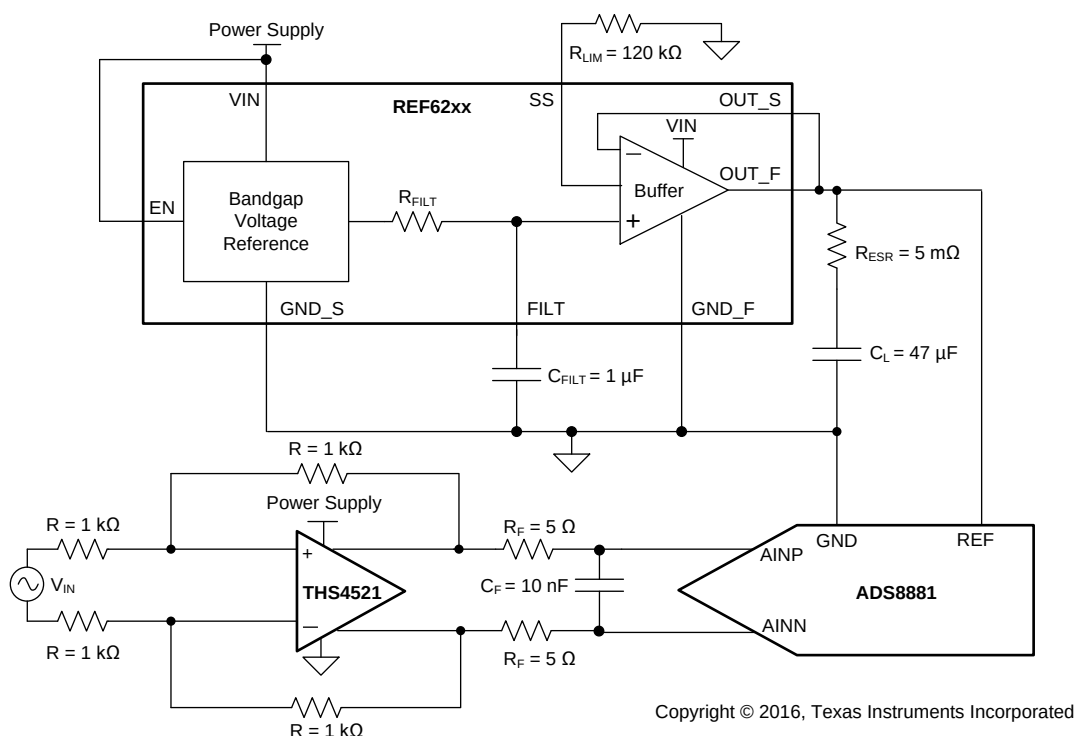
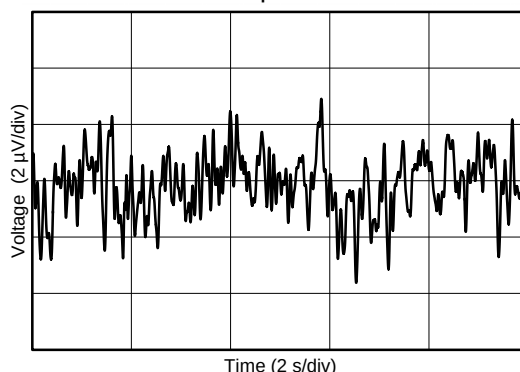


Figure 45. Burst-Mode Measurement Setup

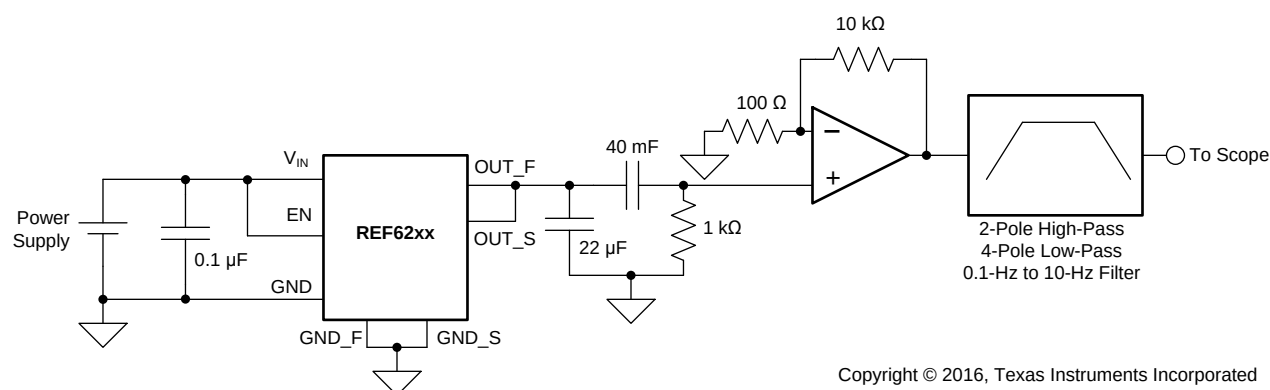
7.4 1/f Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for the REF6225 is shown in Figure 46. The 1/f noise scales with output voltage, but remains $3 \mu\text{V}_{\text{PP}}/\text{V}$ for all the variants. Peak-to-peak noise measurement setup is shown in Figure 47.



C021

Figure 46. 0.1-Hz to 10-Hz Noise



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Figure 47. 0.1-Hz to 10-Hz Noise Measurement Setup

8 Detailed Description

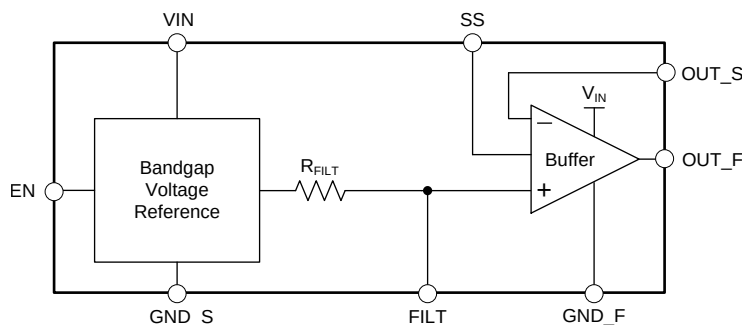
8.1 Overview

Most SAR ADCs, and a few delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. If a voltage reference is directly connected to the REF pin of these ADCs, the reference voltage droops because of the dynamic input signal dependent load of the binary-weighted capacitors. Because the reference voltage droop now has input signal dependence, significant degradation in THD and linearity for the system occurs.

In order to support this dynamic load and preserve the ADC linearity, distortion and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF62xx family of voltage references have an integrated low output impedance buffer that enables the user to directly drive the REF pin of a SAR ADC, while preserving ADC linearity and distortion. In addition, the total noise in the full bandwidth of the REF62xx is extremely low, thus preserving the noise performance of the ADC. [Voltage-Reference Impact on Total Harmonic Distortion](#) (SLYY097) correlates the effect of reference settling to ADC distortion, and how the REF62xx achieves lowest distortion with minimal components and lowest power consumption.

The output voltage of the REF62xx does not droop below 1 LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8881. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. [Functional Block Diagram](#) shows a simplified schematic of the REF62xx.

8.2 Functional Block Diagram

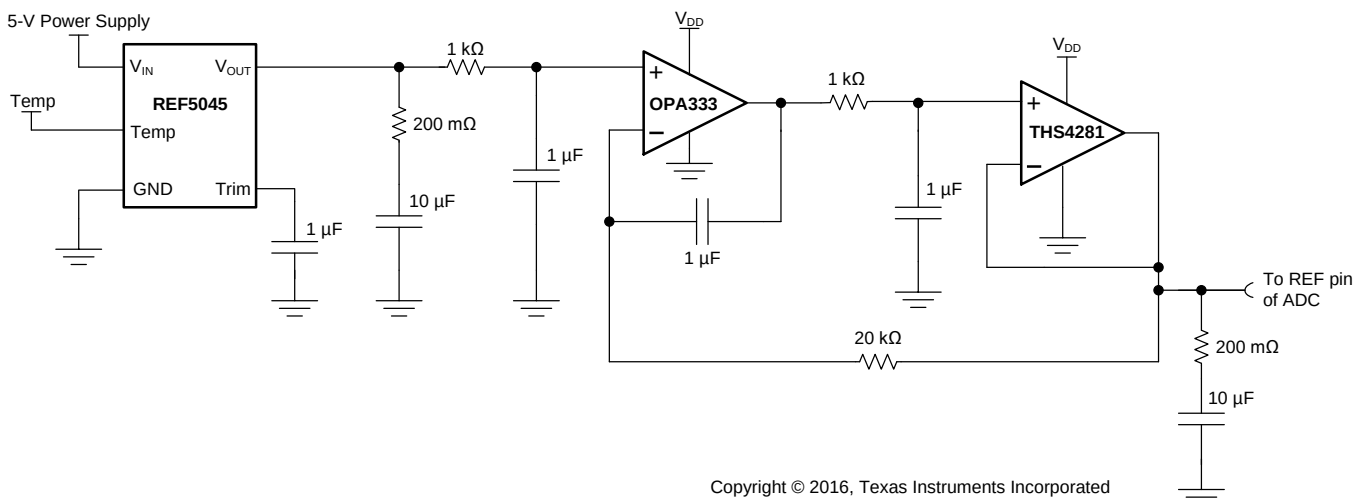


8.3 Feature Description

8.3.1 Integrated ADC Drive Buffer

Many ADC data sheets specify a few microamps of average current draw from the REF pin. Almost all voltage references provide these few microamps of average current; but not all voltage references are practical for driving a high-resolution, high-throughput SAR ADC because the peak current drawn can be very high when the capacitors are switched on the REF pin. The worst-case demand for the voltage reference is during a burst-mode conversion, when the ADC is idle for a very long time, before a conversion is initiated, and the first sample converted is expected to be precise. Usually, a large capacitor is connected between the REF pin and ground pin (or sometimes between the REFP and REFM pins) of the ADC to smoothen the current load and reduce the burden on the voltage reference. The voltage reference must then be capable of providing the average current required to completely charge the reference capacitor, but without causing the reference voltage to droop significantly. Most voltage references lack the ability to completely charge the reference capacitor, and settle when the binary-weighted capacitors are being switched onto the REF pin because of the large output impedance. Usually, voltage references have output impedances in the range of 10's of ohms at frequencies higher than 100 Hz. The output voltage of the voltage reference must be buffered with a low output impedance (usually high bandwidth) amplifier to achieve excellent linearity and distortion performance.

The key amplifier specifications to be considered when designing a reference buffer for a high-precision ADC are: low offset, low drift, wide bandwidth, and low output impedance. While it is possible to select an amplifier that sufficiently meets all these requirements, the amplifier comes at a cost of excessive power consumption. For example, the [OPA350](#) is a 38-MHz bandwidth amplifier with a maximum offset of 0.5 mV, and low offset drift of 4 $\mu\text{V}/^\circ\text{C}$, but consumes a quiescent current of 5.2mA. This is because (from an amplifier design perspective) offset and drift are dc specifications, whereas bandwidth, low output impedance, and high capacitive drive capability are high-frequency specifications. Therefore, achieving all the performance in one amplifier requires power. However, a more efficient design to meet the low power budget is to use a composite reference buffer, which uses an amplifier with superior high-frequency specifications in the feedback loop of a dc precision amplifier to get the overall performance at much lower power consumption. [Figure 48](#) shows such a composite amplifier design with the [OPA333](#) (dc precision amplifier) and [THS4281](#) (high-bandwidth amplifier). This reference buffer design requires three devices, and a large number of external components. This solution still consumes close to 2 mA of quiescent current.



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Figure 48. Composite Amplifier Reference Buffer

The REF62xx family of voltage references have an integrated low output impedance buffer (ADC drive buffer); therefore, there is no need for an external buffer while driving the REF pin of high-precision, high-throughput SAR ADCs, as shown in [Figure 49](#). The ADC drive buffer of the REF62xx is capable of replenishing a charge of 70 pC on a 47- μF capacitor in 1 μs , without allowing the voltage on the capacitor to droop more than 1 LSB at 18-bit precision. The REF62xx are trimmed at multiple temperatures in production, achieving a max drift of just 3

Feature Description (continued)

ppm/°C between 0°C and 70 °C for both the voltage reference and the buffer combined, while operating at a typical quiescent current of 820 μ A. The reference drift is guaranteed from 0°C and 70 °C. The REF62xx can operate from -55°C to 125°C without getting damaged. Figure 50 compares the output impedance of a regular voltage reference (REF20xx) and a voltage reference with integrated ADC drive buffer (REF62xx). Figure 51 compares the burst-mode, reference-settling performance of a regular voltage reference and the REF62xx.

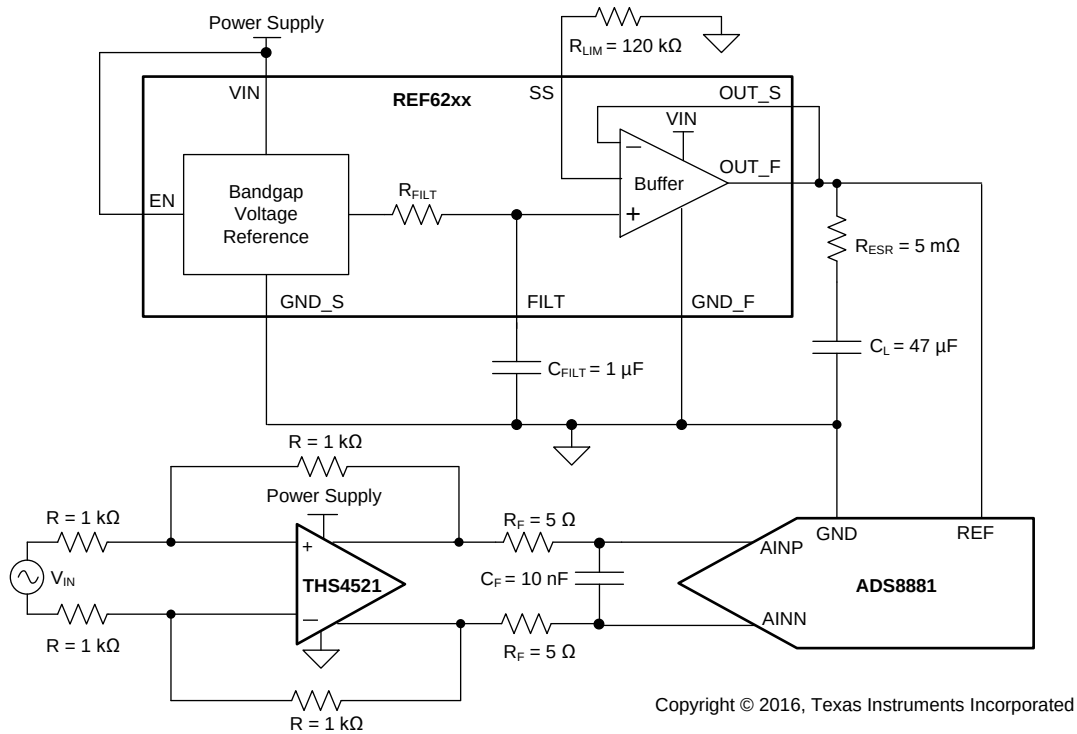


Figure 49. REF62xx Driving REF Pin of ADS8881 SAR ADC

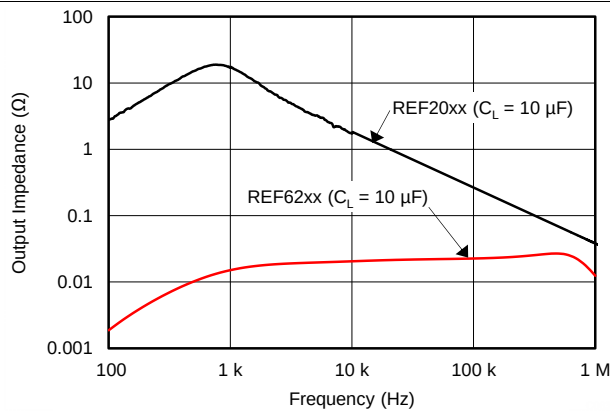
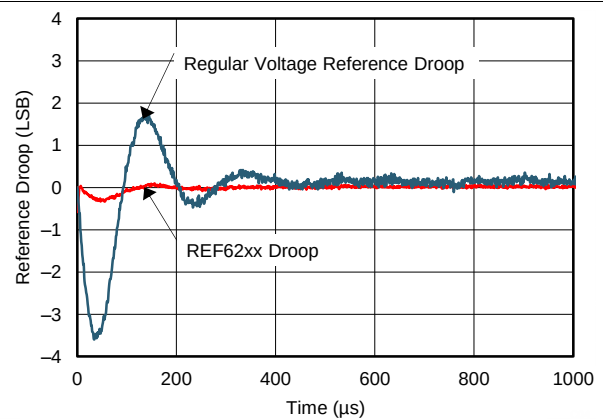


Figure 50. Output Impedance Comparison



1 LSB = 19.07 μ V, with ADS8881 at 1 MSPS

Figure 51. Reference Droop Comparison

Feature Description (continued)

8.3.2 Temperature Drift

The REF62xx family is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

8.3.3 Load Current

The REF6225, REF6230, REF6233 and REF6241 are specified to deliver current load of ± 4 mA. The REF6245 is specified to deliver ± 3.5 mA, and the REF6250 is specified to deliver ± 3 mA. The REF62xx are protected from short circuits at the output by limiting the output short-circuit current.

The short-circuit current limit (I_{SC}) of the REF62xx family of devices is adjusted by connecting a resistor (R_{SS}) on the SS pin. The short-circuit current limit when the REF62xx device is sourcing current can be calculated as shown in [Equation 4](#):

$$I_{\text{SC}} = (80 \cdot 10^{-9}) \cdot R_{\text{SS}} + (3 \cdot 10^{-3}) \quad (4)$$

The short circuit current limit when the REF62xx device is sinking is calculated as shown in [Equation 5](#):

$$I_{\text{SC}} = (115 \cdot 10^{-9}) \cdot R_{\text{SS}} + (4.6 \cdot 10^{-3}) \quad (5)$$

The recommended output current of the REF62xx also depends on the resistor connected to the SS pin. The recommended output current (sourcing and sinking) for the REF6225, REF6230, REF6233 and REF6241 is given by [Equation 6](#):

$$I_{\text{L}} = (31.25 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (6)$$

The recommended output current (sourcing and sinking) for the REF6245 is given by [Equation 7](#):

$$I_{\text{L}} = (27.08 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (7)$$

The recommended output current (sourcing and sinking) for the REF6250 is given by [Equation 8](#):

$$I_{\text{L}} = (23.75 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.15 \cdot 10^{-3}) \quad (8)$$

The temperature of the device increases according to [Equation 9](#):

$$T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \cdot R_{\theta\text{JA}}$$

where:

- T_{J} = junction temperature ($^{\circ}\text{C}$).
 - T_{A} = ambient temperature ($^{\circ}\text{C}$).
 - P_{D} = power dissipated (W).
 - $R_{\theta\text{JA}}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$).
- (9)

The REF62xx maximum junction temperature must not exceed the absolute maximum rating of 150°C .

Feature Description (continued)

8.3.4 Stability

The REF62xx family of voltage references are stable with output capacitor values ranging from 10 μF to 47 μF . At a low output-capacitor value of 10 μF , an effective series resistance (ESR) of 20 m Ω to 100 m Ω is required for stability; whereas, at a higher value of 47 μF , an ESR of 5 m Ω to 100 m Ω is required. The shaded region in [Figure 52](#) shows the stable region of operation for the REF62xx devices.

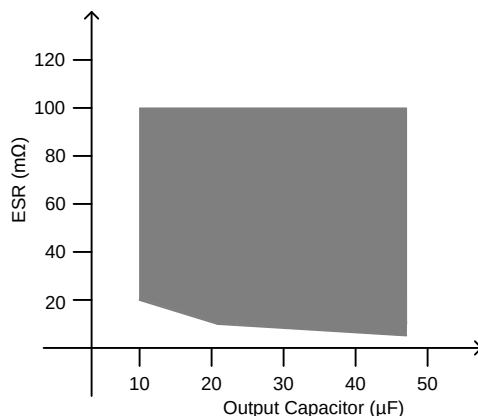


Figure 52. Stable Output Capacitor Range

A capacitor of value 1 μF is required at the FILT pin for stability and noise performance. A low ESR (5 m Ω to 20 m Ω) is easily achieved by increasing the PCB trace length, thus eliminating the need for a discrete resistor. Higher values of ESR (greater than 20 m Ω , but lesser than 100 m Ω) can be intentionally added to increase the output bandwidth of the REF62xx. This higher ESR improves the transient performance of the REF62xx, but worsens noise performance because of increased bandwidth.

8.4 Device Functional Modes

When the EN pin of the REF62xx is pulled high, the device is in active mode. The device must be in active mode for normal operation.

To place the REF62xx into a shutdown mode, pull the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 1 μA (typ). See the enable pin voltage parameter in the [Electrical Characteristics](#) table for logic high and logic low voltage levels.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. Furthermore, variable-sampling-rate systems require that the gain error of the system does not vary with sampling rate. The primary objective of this design example is to demonstrate the lowest distortion and noise, burst-mode data-acquisition block with low power consumption, using an 18-bit SAR ADC operating at a throughput of 1 MSPS, for a 1-kHz, full-scale, pure sine-wave input.

9.2 Typical Application

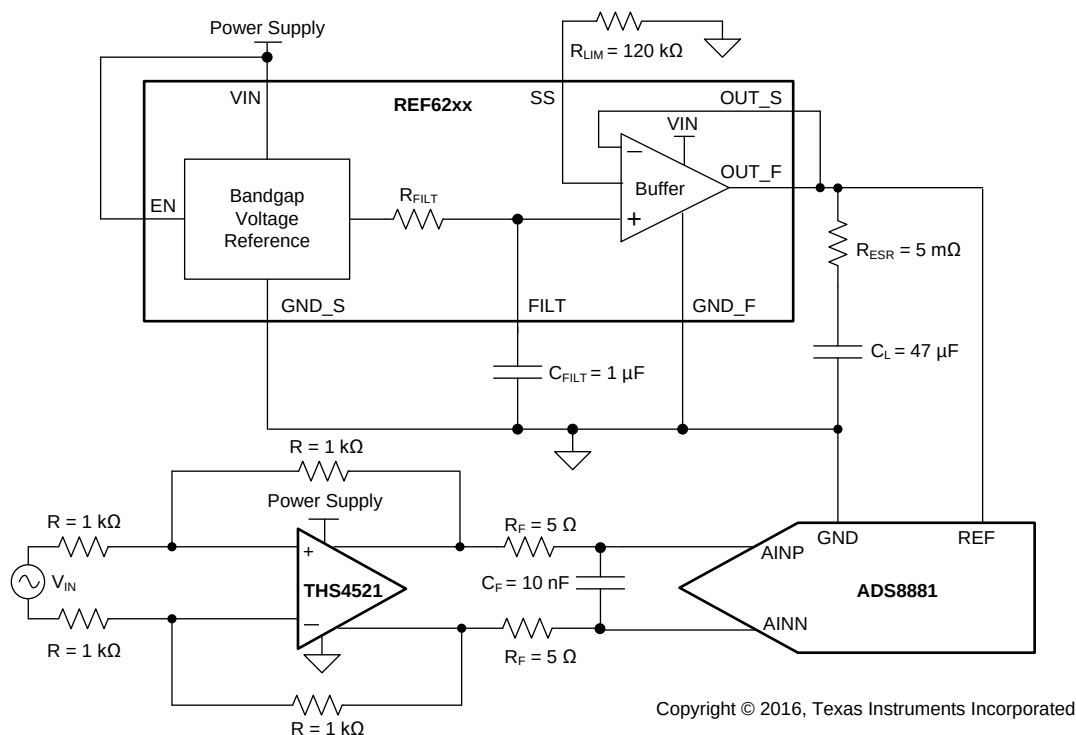


Figure 53. 18-bit, 1-MSPS, Burst-Mode Data Acquisition system

9.2.1 Design Requirements

1. Burst-mode support (see [Reference Droop Measurements](#) section for more details)
2. ENOB > 16 bits
3. THD < -120 dB
4. Power consumption < 50 mW
5. Throughput = 1 MSPS

Typical Application (continued)

9.2.2 Detailed Design Procedure

The data acquisition system shown in [Figure 53](#) has three major contributors to the noise and accuracy in the system: the input driver, the reference with driver, and the data converter. Each analog block is carefully designed so that the data converter specifications limit the system specifications. The [THS4551](#), a fully differential operational amplifier is used to drive the 18-bit ADC ([ADS8881](#)). The charge-kickback RC filter at the output of the THS4551 is used to reduce the charge kickback created by the opening and closing of the sampling switch inside the ADC. Design the RC filter so that the voltage at the sampling capacitor settles to 18-bit accuracy within the acquisition time of the ADC.

Data-acquisition systems require stable and accurate voltage references in order to perform the most accurate data conversion. The REF62xx family of voltage references have integrated an ADC drive buffer, and can therefore drive the REF pin of the ADS8881 directly, without the need for an external reference buffer. See the [Integrated ADC Drive Buffer](#) section for more details about reference-buffer requirements. Correct output capacitor selection for the REF62xx is very important in this design. The [Stability](#) section describes the ESR requirements of the output capacitor for stability and burst-mode requirements. A capacitance of 1 μ F is connected to the FILT pin to reduce broadband noise of the REF62xx.

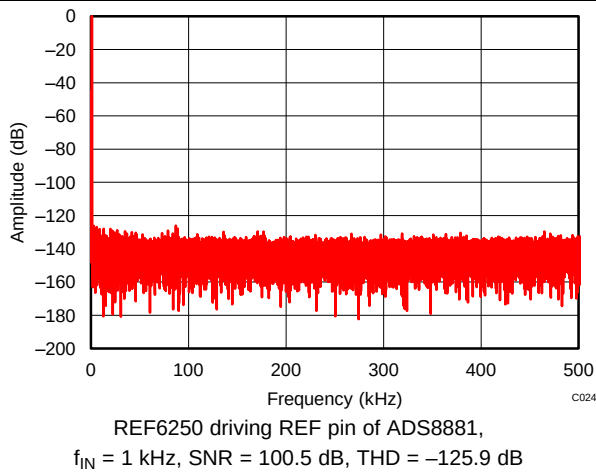
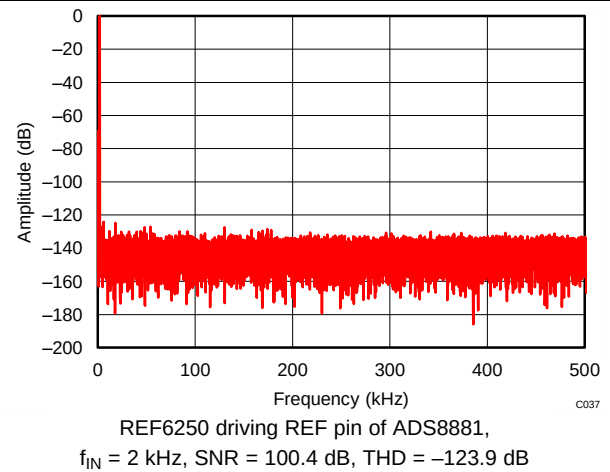
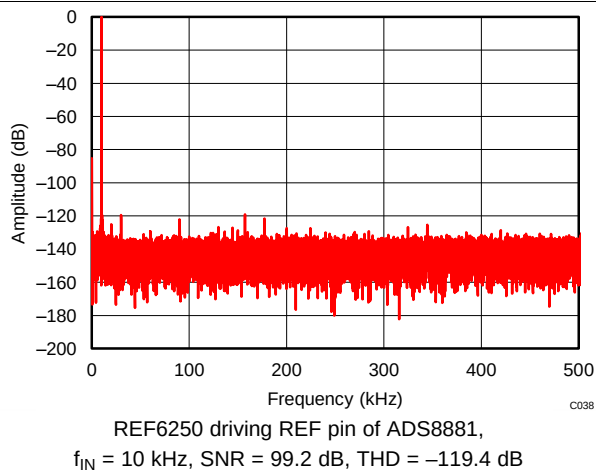
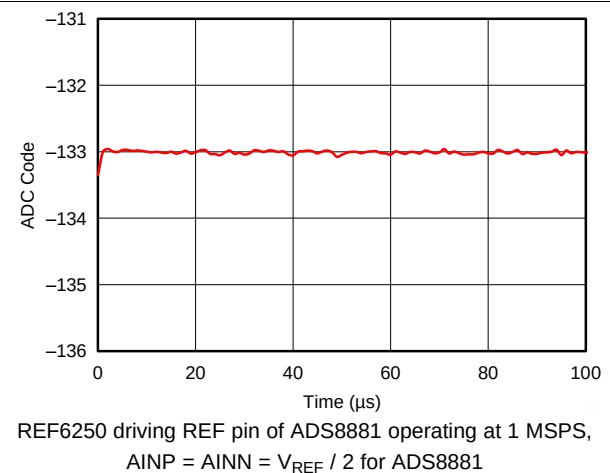
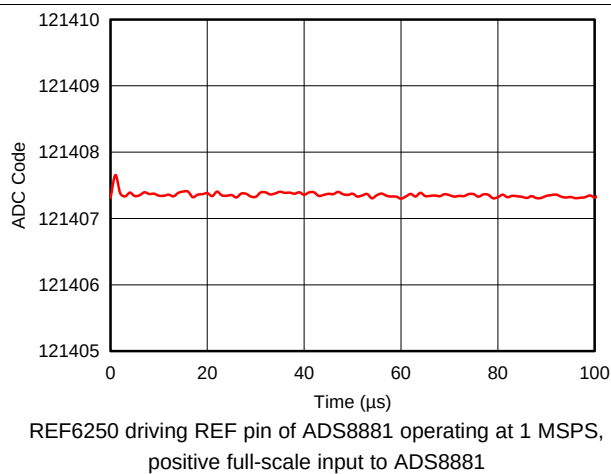
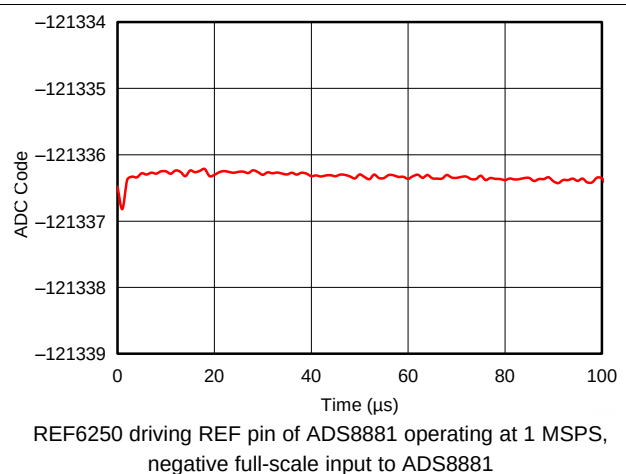
9.2.2.1 Results

[Table 2](#) summarizes the measured results.

Table 2. Measured Results

SPECIFICATION	MEASURED RESULT
SNR	100.5 dB
ENOB	16.4
THD	–125.9 dB
Throughput	1 MSPS
Burst mode	First sample > 18-bit precision
Power consumption	40 mW

9.2.3 Application Curves


Figure 54. Typical FFT Plot

Figure 55. Typical FFT Plot

Figure 56. Typical FFT Plot

Figure 57. Reference Droop

Figure 58. Reference Droop

Figure 59. Reference Droop

10 Power Supply Recommendations

The REF62xx family of references have extremely low dropout voltage. The dropout specifications can be found in the [Electrical Characteristics](#) section. A minimum 0.1 μF decoupling capacitor must be connected between the VIN and GND_F pins of the REF62xx. A typical dropout voltage versus load is shown in [Figure 60](#).

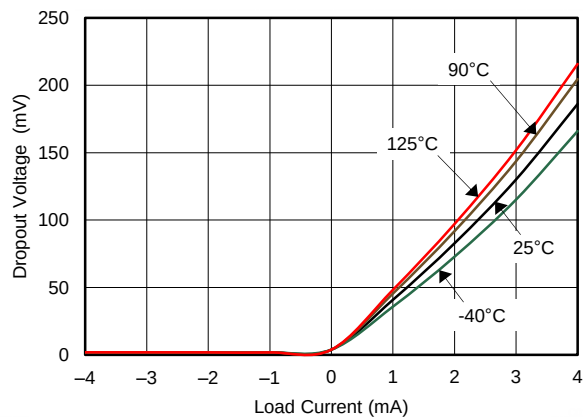


Figure 60. Dropout Voltage vs Load Current

11 Layout

11.1 Layout Guidelines

Figure 61 illustrates an example of a PCB layout for a data-acquisition system using the REF62xx. Some key considerations are:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between the VIN pin and ground.
- Place the REF62xx output capacitor (C_L) and the ADC as close to each other as possible.
- Run two separate traces between VOUT_F, VOUT_S and the output capacitor, as shown in Figure 61.
- Short the GND_F and GND_S pins with a solid plane, and extend this plane to connect to the output capacitor C_L , as shown in Figure 61.
- Use a solid ground plane to help distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

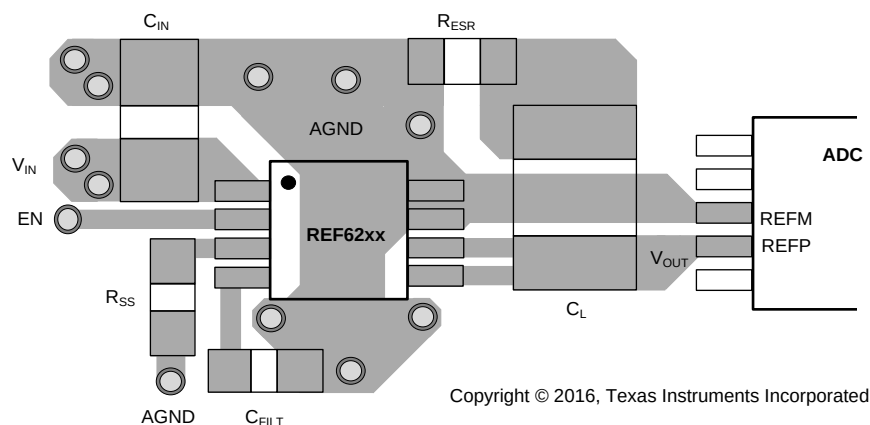


Figure 61. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- [《ADS8881x 18 位、1MSPS、串行接口、低功耗、微型、真正的差分输入、SAR 模数转换器数据表》](#)（文献编号：SBAS547）
- [《ADS127L01 24 位、高速、高带宽模数转换器数据表》](#)（文献编号：SBAS607）
- [《REF6025EVM-PDK 用户指南》](#)（文献编号：SBAU258）
- [《电压基准对总谐波失真的影响》](#)（文献编号：SLYY097）

12.2 相关链接

下面的表格中列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
REF6225	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6230	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6233	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6241	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6245	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6250	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的**提醒我 (Alert me)** 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF6225IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16ZV
REF6225IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16ZV
REF6225IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16ZV
REF6225IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16ZV
REF6230IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17CV
REF6230IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17CV
REF6230IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17CV
REF6230IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17CV
REF6233IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17DV
REF6233IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17DV
REF6233IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17DV
REF6233IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17DV
REF6241IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17EV
REF6241IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17EV
REF6241IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17EV
REF6241IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17EV
REF6245IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17FV
REF6245IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17FV
REF6245IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17FV
REF6245IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17FV
REF6250IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17GV
REF6250IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17GV
REF6250IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17GV
REF6250IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17GV

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

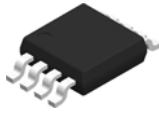
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

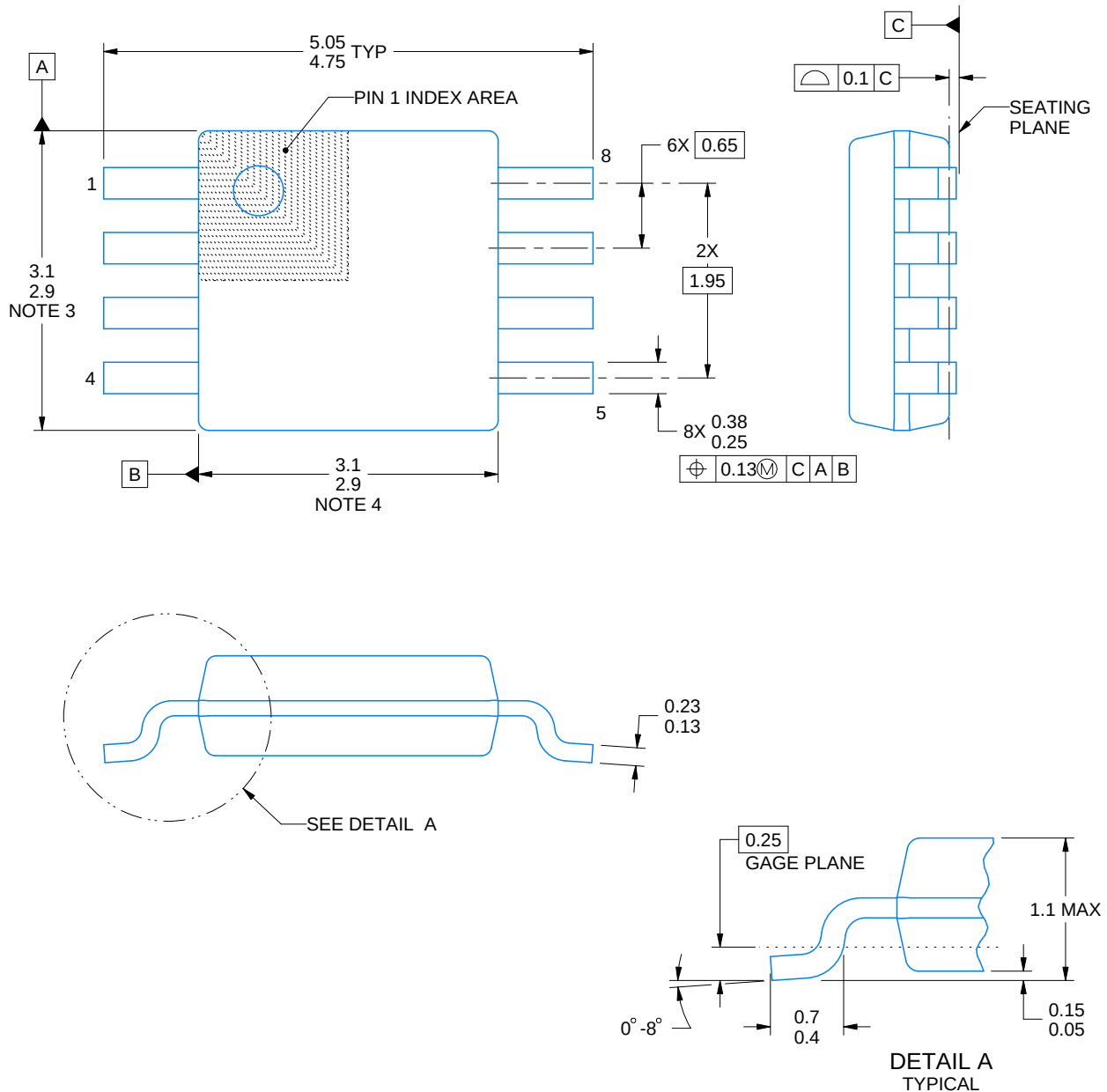
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

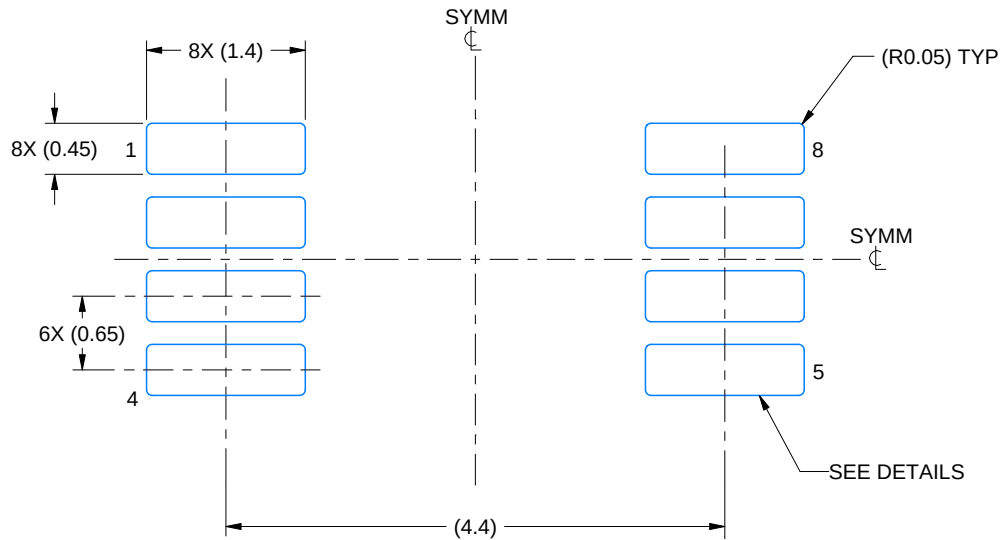
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

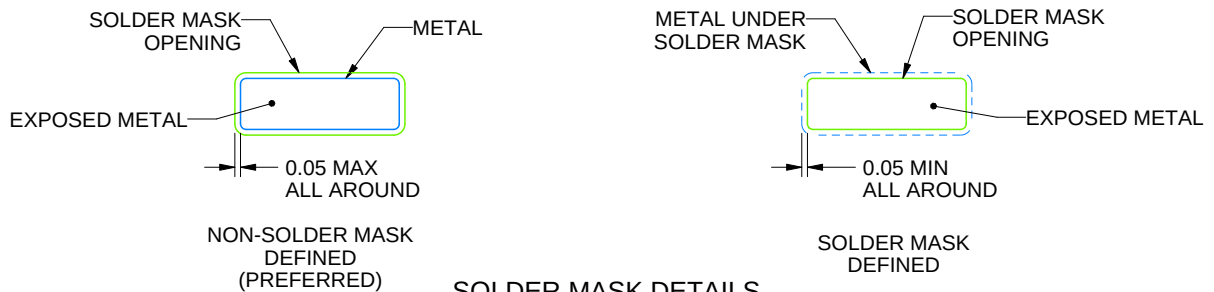
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

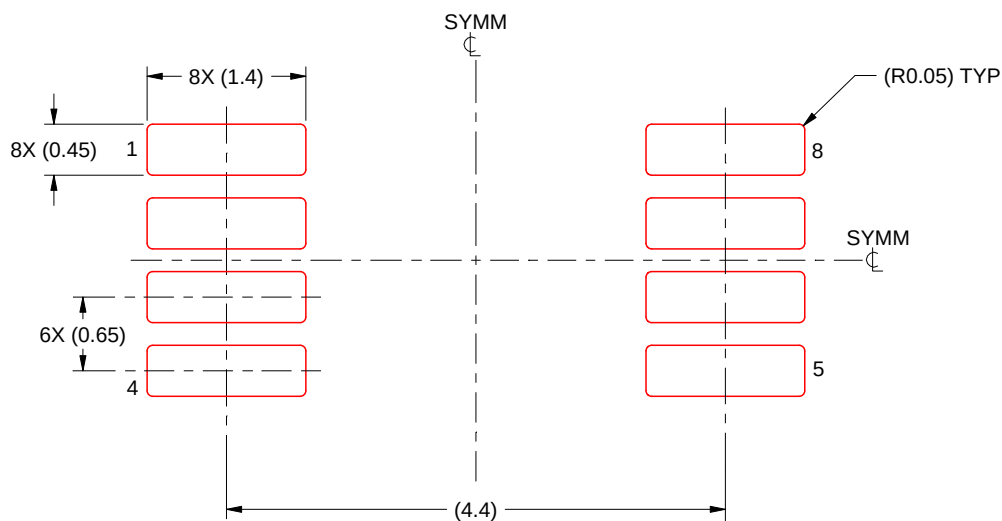
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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