TEXAS INSTRUMENTS

REF5020A-Q1, REF5025A-Q1, REF5030A-Q1
REF5040A-Q1, REF5045A-Q1, REF5050A-Q1

SBOS456H – SEPTEMBER 2008 – REVISED FEBRUARY 2015

# REF50xxA-Q1 Low-Noise, Very Low Drift, Precision Voltage Reference

## 1 Features

- Qualified for Automotive Applications
- Low Temperature Drift
  - Standard Grade: 8 ppm/°C (max)
- High Accuracy
  - Standard Grade: 0.1% (max)
- Low Noise: 3 $\mu V_{PP}$/V
- Excellent Long-Term Stability:
  - 5 ppm/1000 hr (typ) after 1000 hours
- High Output Current: ±10 mA
- Temperature Range: –40°C to 125°C

## 2 Applications

- 16-Bit Data Acquisition Systems
- ATE Equipment
- Industrial Process Control
- Medical Instrumentation
- Optical Control Systems
- Precision Instrumentation

## 3 Description

The REF50xxA-Q1 family of devices is low-noise, low-drift, very-high precision-voltage reference. These reference devices are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features combined with very low noise make the REF50xxA-Q1 family of devices ideal for use in high-precision data acquisition systems.

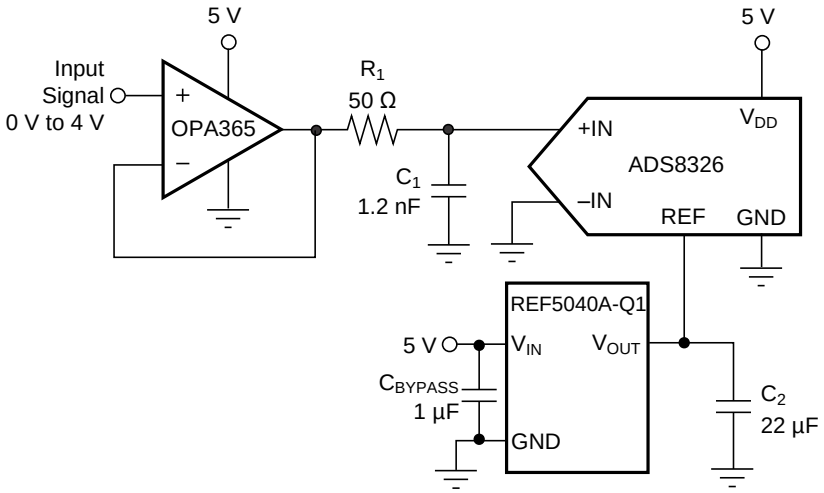
Each reference voltage is available in a standard-grade versions. The devices are offered in SO-8 packages and are specified from –40°C to 125°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | OUTPUT VOLTAGE |
|---|---|---|
| REF5020A-Q1 | SOIC (8) | 2.048 V |
| REF5025A-Q1 | | 2.5 V |
| REF5030A-Q1 | | 3 V |
| REF5040A-Q1 | | 4.096 V |
| REF5045A-Q1 | | 4.5 V |
| REF5050A-Q1 | | 5 V |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (October 2013) to Revision H** — **Page**

- Added the *Pin Configuration and Functions* section, *Recommended Operating Conditions* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *A-Q1* to the end of the device numbers ... 1
- Changed the MIN and MAX values for the REF5040 initial accuracy parameter in the *Electrical Characteristics* table ... 5

**Changes from Revision F (September 2011) to Revision G** — **Page**

- Deleted reference to *high grade* throughout the document ... 1
- Deleted *Package/Ordering Information* table from datasheet ... 4
- Deleted references to the MSOP-8 package and *High-Grade* from the *THERMAL HYSTERESIS* section of the *ELECTRICAL CHARACTERISTICS: ALL DEVICES* table ... 6
- Deleted references to the MSOP-8 package from the *LONG-TERM STABILITY* section of the *ELECTRICAL CHARACTERISTICS: ALL DEVICES* table ... 6
- Deleted graphs for MSOP-8 package from *TYPICAL CHARACTERISTICS* section ... 9

**Changes from Revision E (August 2011) to Revision F** — **Page**

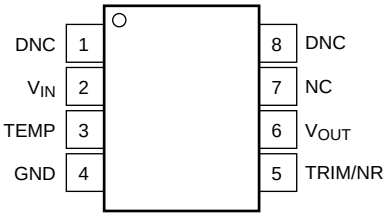
- Added REF5045AQDRQ1 HBM ESD rating of 1000 V ... 4

**Changes from Revision D (October, 2010) to Revision E** **Page**


- Added *Thermal Hysteresis* parameters and specifications ..... 6
- Added *Long-Term Stability* parameters and specifications ..... 6
- Added Figure 22 through Figure 24 ..... 9
- Added *Thermal Hysteresis* section ..... 13
- Revised *Noise Performance* section; added paragraph with links to applications articles ..... 14

# 6 Pin Configuration and Functions

**D Package**
**8-Pin SOIC**
**Top View**




DNC = Do not connect

NC = No internal connection

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DNC | 1 | — | Do not connect. Do not use. |
| | 8 | | |
| GND | 4 | — | Ground |
| NC | 7 | — | No internal connection. Do not use. |
| TEMP | 3 | O | Temperature-dependent voltage output |
| TRIM/NR | 5 | I | Trim and noise reduction for ±15-mV output adjustment |
| $V_{IN}$ | 2 | I | Input supply voltage |
| $V_{OUT}$ | 6 | O | Reference voltage output |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage | | 18 | V |
| Output short-circuit | | 30 | mA |
| Operating temperature | –40 | 125 | °C |
| Junction temperature ($T_J$ max) | | 150 | °C |
| Storage temperature ($T_{stg}$) | –65 | 150 | °C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| **REF5020A-Q1, REF5040A-Q1, AND REF5050A-Q1** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±500 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |
| | | Machine Model (MM) | 200 | |
| **REF5030A-Q1 AND REF5045A-Q1** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±1000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |
| | | Machine Model (MM) | 200 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage | $V_{OUT}$ + 0.2 (1) | 18 | V |

(1) For $V_{OUT}$ ≤ 2.5 V, the minimum supply voltage is 2.7 V.

## 7.4 Thermal Information

| THERMAL METRIC (1) | | D (SOIC) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 107.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.8 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 47.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics: Per Device

$T_A$ = 25°C, $I_{LOAD}$ = 0, $C_L$ = 1 µF, $V_{IN}$ = ($V_{OUT}$ + 0.2 V) to 18 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **REF5020 ($V_{OUT}$ = 2.048 V) (1)** | | | | | | |
| $V_{OUT}$ | Output voltage | 2.7 V < $V_{IN}$ < 18 V | | 2.048 | | V |
| | Initial accuracy, standard grade | | –0.1% | | 0.1% | |
| | Output voltage noise | f = 0.1 Hz to 10 Hz | | 6 | | $\mu V_{PP}$ |
| **REF5025 ($V_{OUT}$ = 2.5 V)** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 2.5 | | V |
| | Initial accuracy, standard grade | | –0.1% | | 0.1% | |
| | Output Voltage Noise | f = 0.1 Hz to 10 Hz | | 7.5 | | $\mu V_{PP}$ |
| **REF5030 ($V_{OUT}$ = 3 V)** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 3 | | V |
| | Initial accuracy, standard grade | | –0.1% | | 0.1% | |
| | Output voltage noise | f = 0.1 Hz to 10 Hz | | 9 | | $\mu V_{PP}$ |
| **REF5040 ($V_{OUT}$ = 4.096 V)** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 4.096 | | V |
| | Initial accuracy, standard grade | | –0.1% | | 0.1% | |
| | Output voltage noise | f = 0.1 Hz to 10 Hz | | 12 | | $\mu V_{PP}$ |
| **REF5045 ($V_{OUT}$ = 4.5 V)** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 4.5 | | V |
| | Initial accuracy, standard grade | | –0.1% | | 0.1% | |
| | Output voltage noise | f = 0.1 Hz to 10 Hz | | 13.5 | | $\mu V_{PP}$ |
| **REF5050 ($V_{OUT}$ = 5 V)** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 5 | | V |
| | Initial accuracy, standard grade | | –0.1% | | 0.1% | |
| | Output voltage noise | f = 0.1 Hz to 10 Hz | | 15 | | $\mu V_{PP}$ |

(1) For $V_{OUT}$ ≤ 2.5 V, the minimum supply voltage is 2.7 V.

## 7.6 Electrical Characteristics: All Devices

**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to 125°C.**
$T_A$ = 25°C, $I_{LOAD}$ = 0, $C_L$ = 1 µF, $V_{IN}$ = ($V_{OUT}$ + 0.2 V) to 18 V (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $dV_{OUT}/dT$ | Output voltage temperature drift, standard grade | | Over temperature | | 3 | 8 | ppm/°C |
| $dV_{OUT}/dV_{IN}$ | Line regulation | REF5020 only(1) | $V_{IN}$ = 2.7 V to 18 V | | 0.1 | 1 | ppm/V |
| | | All other devices | $V_{IN}$ = $V_{OUT}$ + 0.2 V | | 0.1 | 1 | ppm/V |
| | | All devices | Over temperature | | 0.2 | 1 | ppm/V |
| $dV_{OUT}/dI_{LOAD}$ | Load regulation | REF5020 only | –10 mA < $I_{LOAD}$ < +10 mA, $V_{IN}$ = 3 V | | 20 | 30 | ppm/mA |
| | | All other devices | –10 mA < $I_{LOAD}$ < +10 mA, $V_{IN}$ = $V_{OUT}$ + 0.75 V | | 20 | 30 | ppm/mA |
| | | All devices | Over temperature, –10 mA < $I_{LOAD}$ < +10 mA | | | 50 | ppm/mA |
| $I_{SC}$ | Short-circuit current | | $V_{OUT}$ = 0 V | | 25 | | mA |
| | Thermal hysteresis, (2) standard grade | | Cycle 1 | | 10 | | ppm |
| | | | Cycle 2 | | 5 | | ppm |
| | Long-Term Stability | | 0 to 1000 hours | | 90 | | ppm/1000 hr |
| | | | 1000 to 2000 hours | | 10 | | ppm/1000 hr |
| | Voltage output, TEMP pin | | At $T_A$ = 25°C | | 575 | | mV |
| | Temperature sensitivity , TEMP pin | | Over temperature | | 2.64 | | mV/°C |
| | Turn-on settling time | | To 0.1% with $C_L$ = 1 µF | | 200 | | µs |
| $V_S$ | Power supply voltage | | See Note (1) | $V_{OUT}$ + 0.2(1) | | 18 | V |
| | Power supply, quiescent current | | | | 0.8 | 1 | mA |
| | | | Over temperature | | | 1.2 | mA |
| **TEMPERATURE RANGE** | | | | | | | |
| | Specified range | | | –40 | | 125 | °C |
| | Operating range | | | –55 | | 125 | °C |
| | Thermal resistance | | | | 150 | | °C/W |

(1) For $V_{OUT}$ ≤ 2.5 V, the minimal supply voltage is 2.7 V.
(2) The *Thermal Hysteresis* section explains the thermal hysteresis procedure in detail.

## 7.7 Typical Characteristics

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = $V_{OUT}$ + 0.2 V (unless otherwise noted). For $V_{OUT}$ ≤ 2.5 V, the minimum supply voltage is 2.7 V.

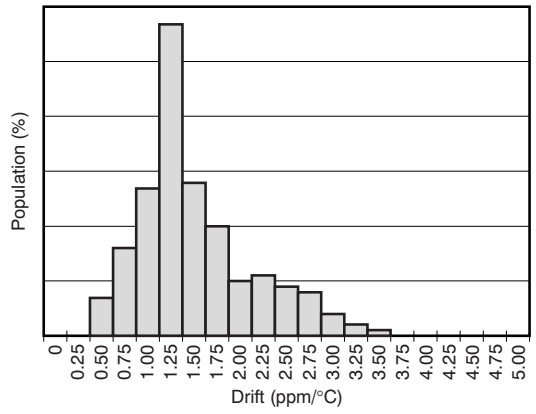



**Figure 1. Temperature Drift (0°C to 85°C)**

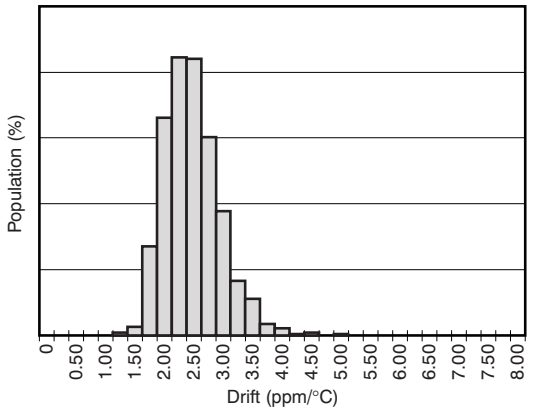



**Figure 2. Temperature Drift (–40°C to 125°C)**

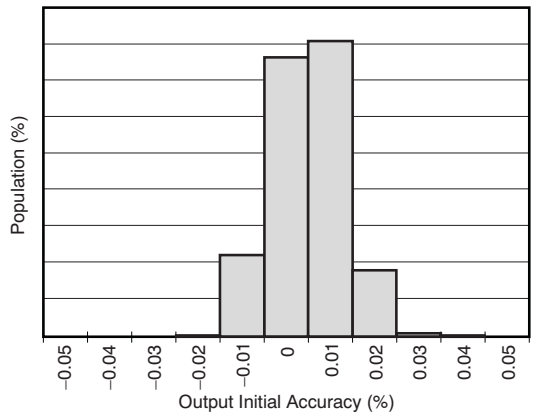



**Figure 3. Output Voltage Initial Accuracy**

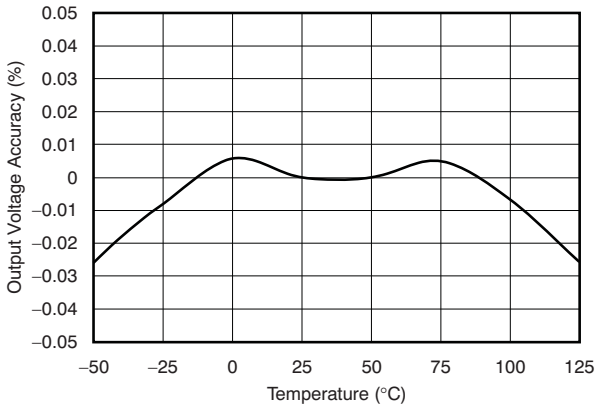



**Figure 4. Output Voltage Accuracy vs Temperature**

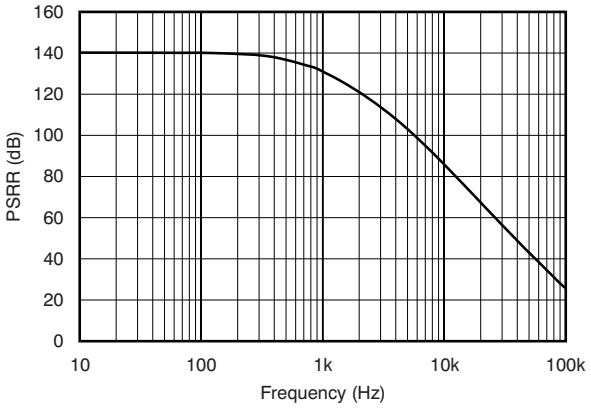



**Figure 5. Power-Supply Rejection Ratio vs Frequency**

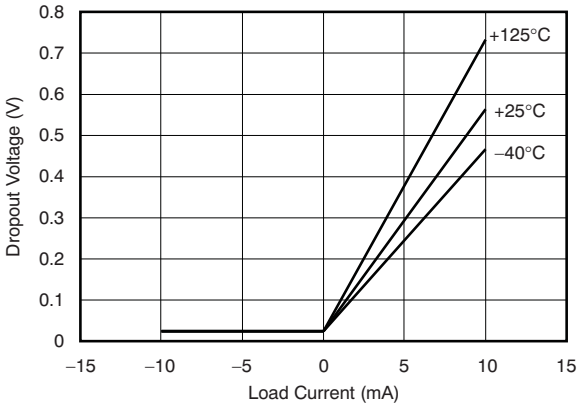



**Figure 6. Dropout Voltage vs Load Current**

## Typical Characteristics (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = $V_{OUT}$ + 0.2 V (unless otherwise noted). For $V_{OUT}$ ≤ 2.5 V, the minimum supply voltage is 2.7 V.

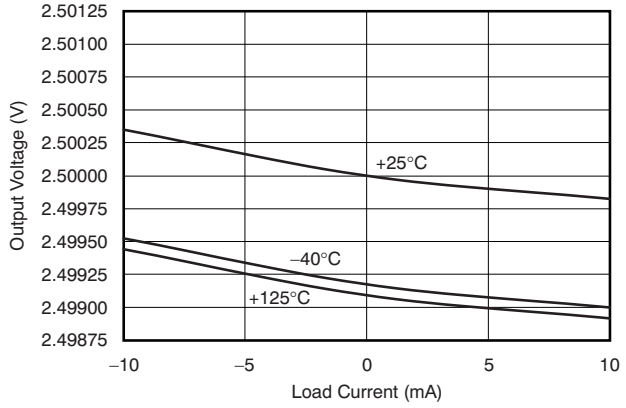



**Figure 7. REF5025A-Q1 Output Voltage vs Load Current**

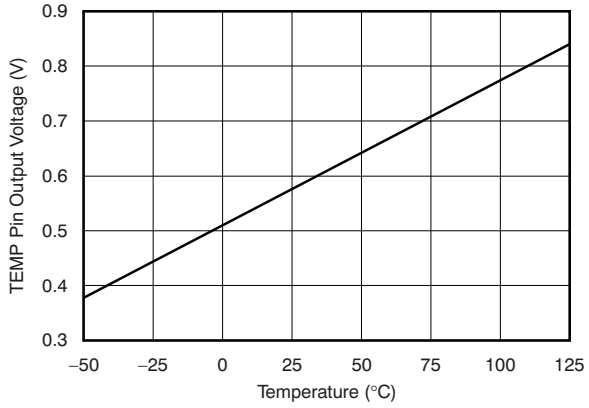



**Figure 8. TEMP Pin Output Voltage vs Temperature**

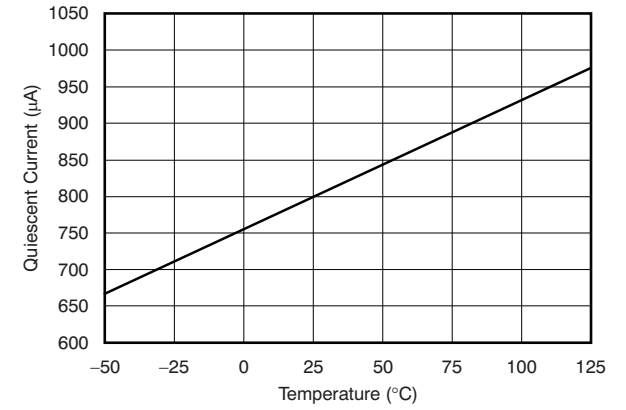



**Figure 9. Quiescent Current vs Temperature**

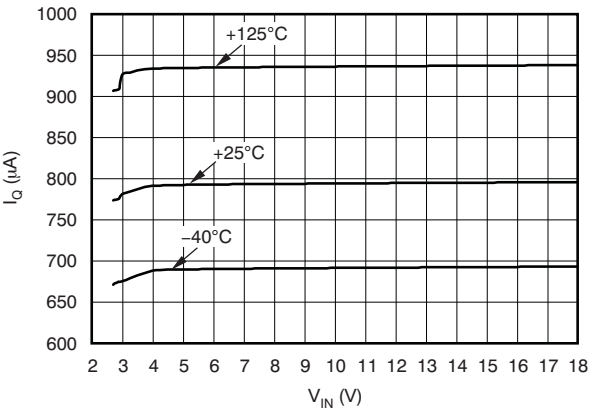



**Figure 10. Quiescent Current vs Input Voltage**

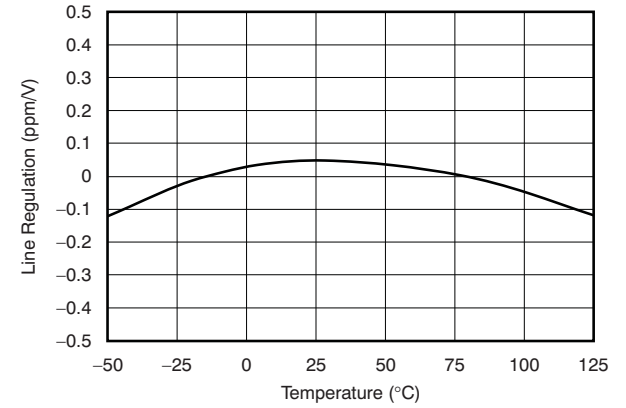



**Figure 11. Line Regulation vs Temperature**

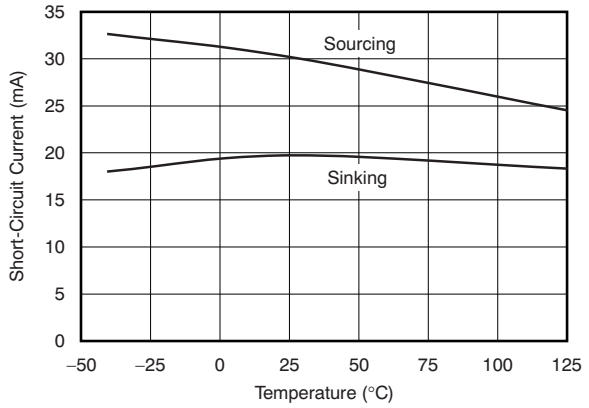



**Figure 12. Short-Circuit Current vs Temperature**

## Typical Characteristics (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = $V_{OUT}$ + 0.2 V (unless otherwise noted). For $V_{OUT}$ ≤ 2.5 V, the minimum supply voltage is 2.7 V.

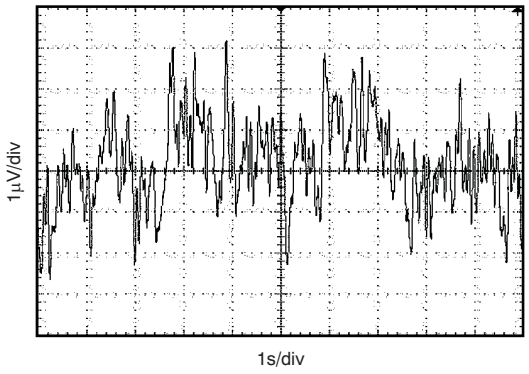



**Figure 13. Noise**

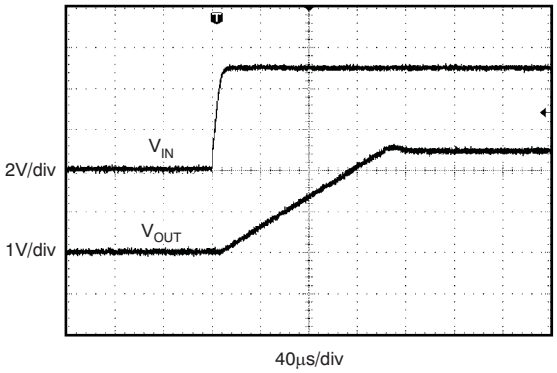



**Figure 14. Startup (REF5025A-Q1, $C_L$ = 1 µF)**

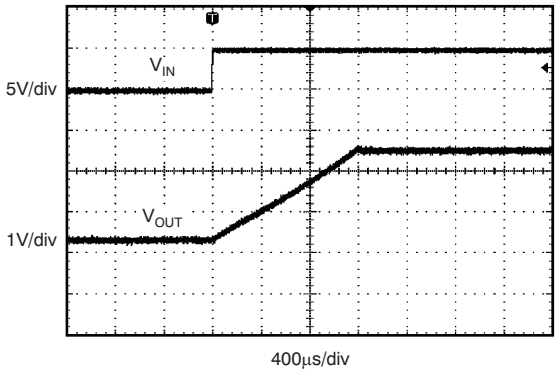



**Figure 15. Startup (REF5025A-Q1, $C_L$ = 10 µF)**

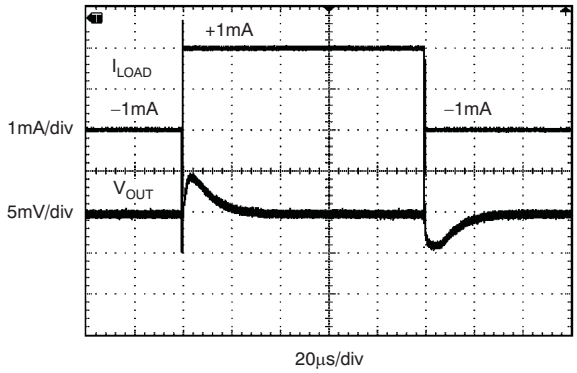



**Figure 16. Load Transient ($C_L$ = 1 µF, $I_{OUT}$ = 1 mA)**

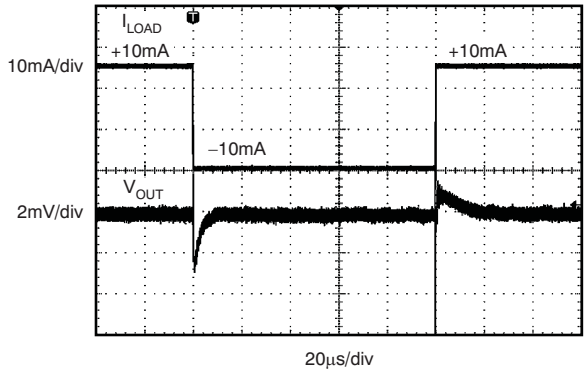



**Figure 17. Load Transient ($C_L$ = 1 µF, $I_{OUT}$ = 10 mA)**

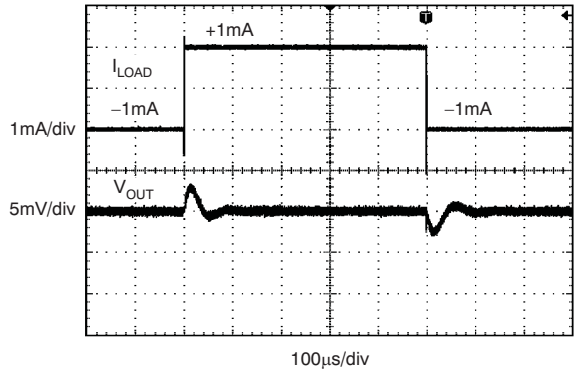



**Figure 18. Load Transient ($C_L$ = 10 µF, $I_{OUT}$ = 1 mA)**

## Typical Characteristics (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = $V_{OUT}$ + 0.2 V (unless otherwise noted). For $V_{OUT}$ ≤ 2.5 V, the minimum supply voltage is 2.7 V.

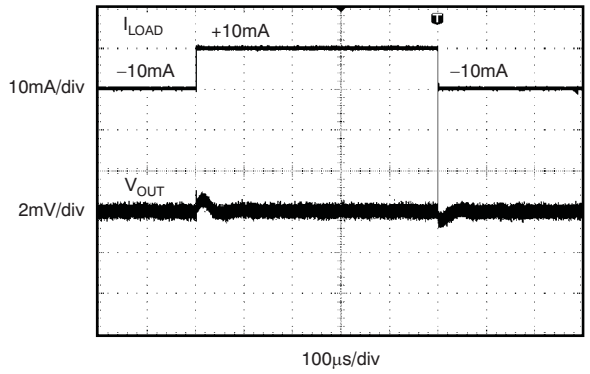



**Figure 19. Load Transient ($C_L$ = 10 µF, $I_{OUT}$ = 10 mA)**

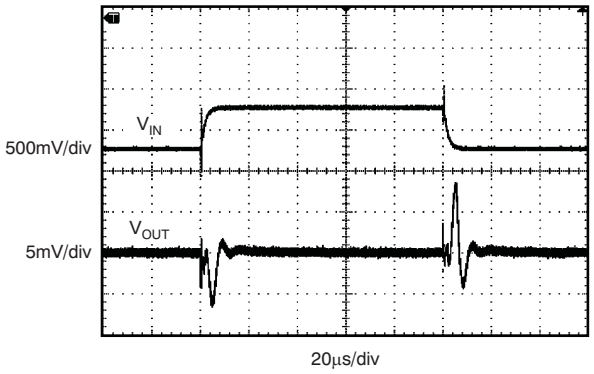



**Figure 20. Line Transient ($C_L$ = 1 µF)**

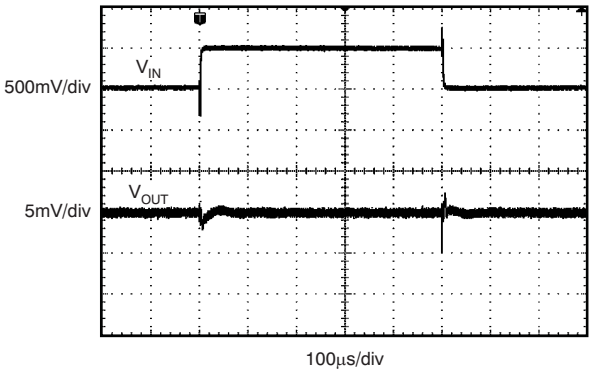



**Figure 21. Line Transient ($C_L$ = 10 µF)**

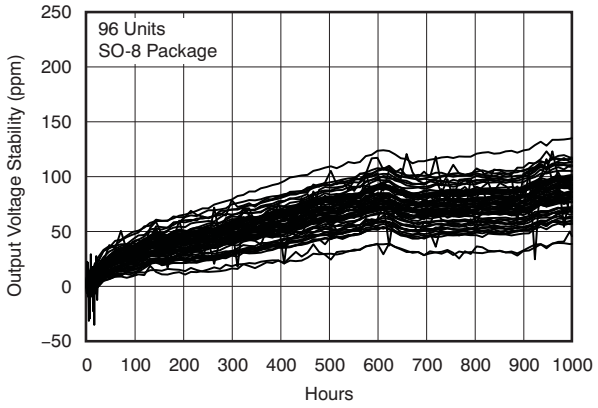



**Figure 22. REF50xxA-Q1 Long-Term Stability (First 1000 Hours)**

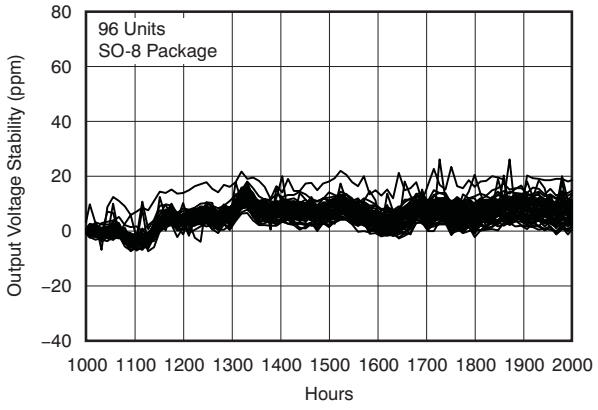



**Figure 23. REF50xxA-Q1 Long-Term Stability (Second 1000 Hours)**

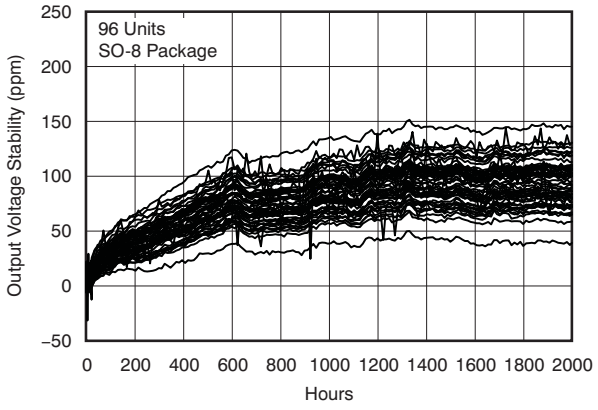


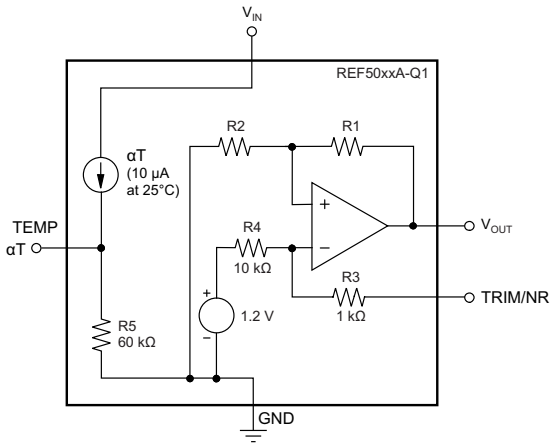

**Figure 24. REF50xxA-Q1 Long-Term Stability (2000 Hours)**

# 8 Detailed Description

## 8.1 Overview

The REF50xxA-Q1 family of devices is a low-noise, precision-bandgap voltage reference that is specifically designed for excellent initial voltage accuracy and drift. See the *Functional Block Diagram* section for a simplified block diagram of the REF50xxA-Q1 family of devices.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Supply Voltage

The REF50xxA-Q1 family of voltage references features extremely low dropout voltage. With the exception of the REF5020A-Q1 device, which has a minimum supply requirement of 2.7 V, these references can operate with a supply of 200 mV above the output voltage in an unloaded condition. For loaded conditions, Figure 6 in the *Typical Characteristics* section shows a typical dropout voltage versus load plot.

### 8.3.2 Using the TRIM/NR Pin

The REF50xxA-Q1 family of devices provides a very accurate voltage output. However, $V_{OUT}$ can be adjusted to reduce noise and shift the output voltage from the nominal value by configuring the trim and noise reduction pin (TRIM/NR, pin 5). The TRIM/NR pin provides a ±15-mV adjustment of the device bandgap, which produces a ±15-mV change on the $V_{OUT}$ pin. Figure 25 shows a typical circuit using the TRIM/NR pin to adjust $V_{OUT}$. When using this technique, the temperature coefficients of the resistors can degrade the temperature drift at the output.

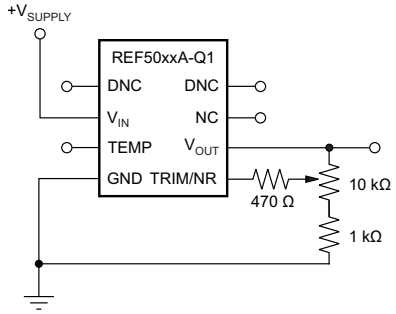



**Figure 25. $V_{OUT}$ Adjustment Using TRIM/NR Pin**

## Feature Description (continued)

The REF50xxA-Q1 family of devices allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (as shown in Figure 26) in combination with the internal 1-kΩ resistor creates a low-pass filter that lowers the overall noise measured on the $V_{OUT}$ pin. A capacitance of 1 µF is suggested for a low-pass filter with a corner frequency of 14.5 Hz. Higher capacitance results in a lower cutoff frequency.

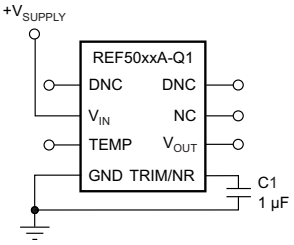



**Figure 26. Noise Reduction Using TRIM/NR Pin**

### 8.3.3 Temperature Drift

The REF50xxA-Q1 family of devices is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method. Use Equation 1 to calculate the drift.

$$\text{Drift} = \left( \frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

The REF50xxA-Q1 family of devices features a maximum drift coefficient of 8 ppm/°C for the standard-grade.

### 8.3.4 Temperature Monitoring

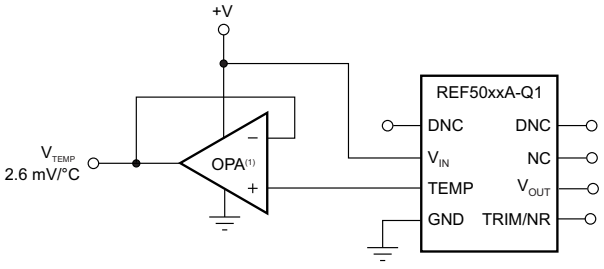
The temperature output pin (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-kΩ source impedance. As shown in Figure 8, the output voltage follows the nominal relationship:

$$V_{TEMP\ PIN} = 509\ \text{mV} + 2.64 \times T(°C) \quad (2)$$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although this pin is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79-mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see the *Functional Block Diagram* section). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on $V_{OUT}$ accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 27.




(1) Low drift op amp, such as the OPA333, OPA335, or OPA376 device.

**Figure 27. Buffering the TEMP Pin Output**

## 8.4 Device Functional Modes

The REF50xxA-Q1 family of devices can only operate in an on or off mode. As long as a sufficient input supply voltage is made available to device, the device performs in standard operation. The device cannot be placed in a low power or shutdown mode.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Thermal Hysteresis

Thermal hysteresis for the REF50xxA-Q1 family of devices is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Use Equation 3 to calculate the thermal hysteresis.

$$V_{HYST} = \left( \frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \cdot 10^6 \text{ (ppm)} \quad (3)$$

where

- $V_{HYST}$ = thermal hysteresis (in units of ppm)
- $V_{NOM}$ = the specified output voltage
- $V_{PRE}$ = output voltage measured at 25°C pretemperature cycling
- $V_{POST}$ = output voltage measured after the device has been cycled from 25°C through the specified temperature range of –40°C to +125°C and returned to 25°C

## 9.2 Typical Applications

### 9.2.1 Standalone Applications

Figure 28 shows the typical connections for the REF50xxA-Q1 family of devices.

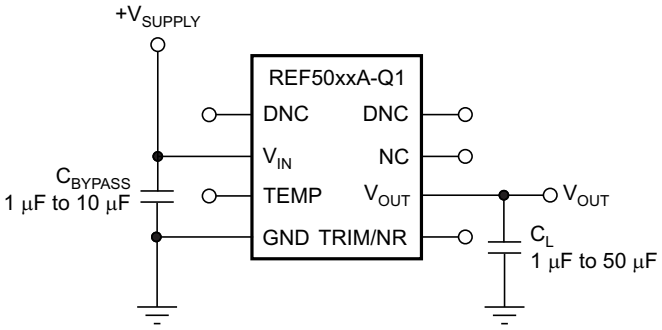



**Figure 28. Basic Connections**

## Typical Applications (continued)

### 9.2.1.1 Design Requirements

A supply bypass capacitor with a value between 1 µF to 10 µF is recommended. A 1-µF to 50-µF, low-ESR output capacitor ($C_L$) must be connected from $V_{OUT}$ to GND. The ESR value should be less than or equal to 1.5 Ω. The ESR minimizes gain peaking of the internal 1.2-V reference and thus reduces noise at the $V_{OUT}$ pin.

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Power Dissipation

The REF50xxA-Q1 family of devices is specified to deliver current loads of ±10 mA over the specified input voltage range. The temperature of the device increases according Equation 4.

$$T_J = T_A + P_D \times R_{\theta JA}$$

where

- $T_J$ = Junction temperature (°C)
- $T_A$ = Ambient temperature (°C)
- $P_D$ = Power dissipated (W)
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W) (4)

The junction temperature of the REF50xxA-Q1 family of devices must not exceed the absolute maximum rating of 150°C.

#### 9.2.1.2.2 Noise Performance

The *Electrical Characteristics: Per Device* section specifies the typical voltage noise at 0.1 Hz to 10 Hz for each member of the REF50xxA-Q1 family of devices. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications, such as data converters, refer to the series of *Analog Applications Journal* articles entitled, *How a Voltage Reference Affects ADC Performance*. See the *Related Documentation* section for a list of these articles.

### 9.2.1.3 Application Curves

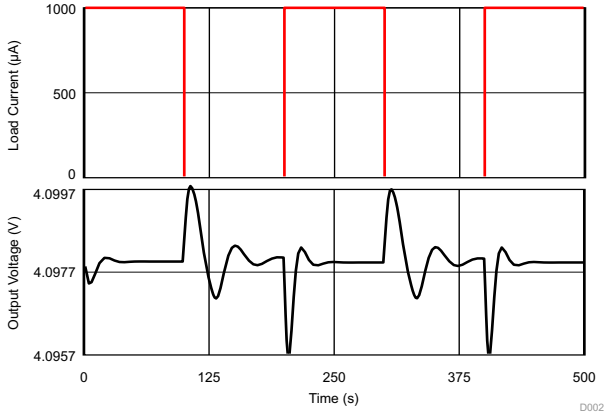



**Figure 29. Transient Behavior of $V_{OUT}$**

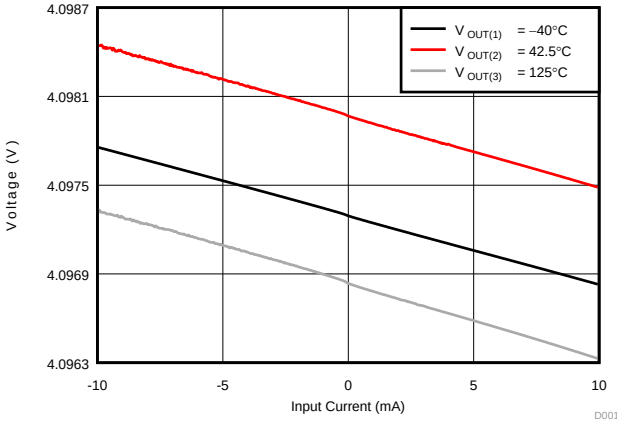
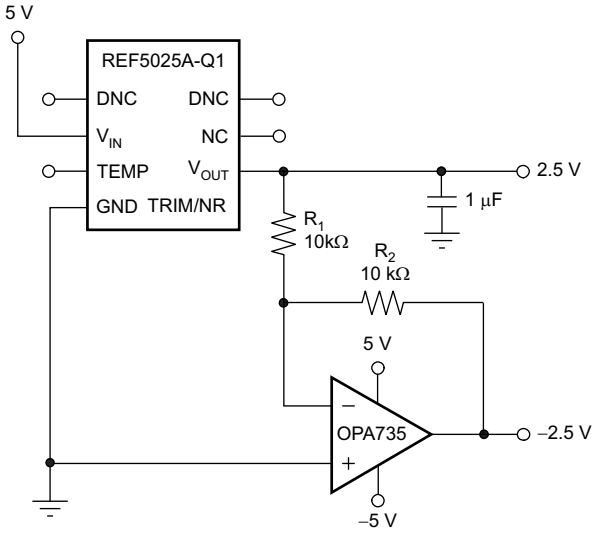



**Figure 30. DC Analysis of $V_{OUT}$ Across Various Temperatures and the Full Output-Current Range**

## Typical Applications (continued)

### 9.2.2 Negative-Reference Voltage Applications

For applications requiring a negative and positive reference voltage, the REF50xxA-Q1 family of devices and the OPA735 device can be used to provide a dual-supply reference from a 5-V supply. Figure 31 shows the REF5025A-Q1 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF50xxA-Q1 family of devices complements the low offset voltage and zero drift of the OPA735 device to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of $R_1$ and $R_2$.




NOTE: Bypass capacitors not shown.

**Figure 31. The REF5025A-Q1 and OPA735 Create Positive and Negative Reference Voltages**

### 9.2.3 Data-Acquisition Applications

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xxA-Q1 family of devices features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 32 shows the REF5040A-Q1 in a basic data acquisition system.

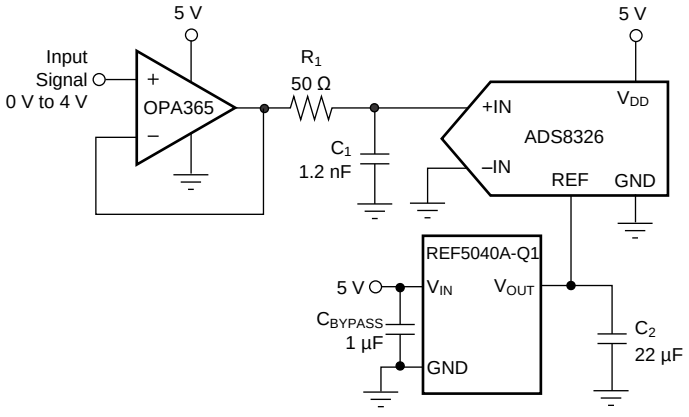



**Figure 32. Basic Data Acquisition System**

# 10 Power Supply Recommendations

The REF50xxA-Q1 family of voltage references features extremely low dropout voltage. With the exception of the REF5020A-Q1 device, which has a minimum supply requirement of 2.7 V, these references can operate with a supply of 200 mV above the output voltage in an unloaded condition. A supply bypass capacitor with a value ranging between 0.1 µF and 10 µF is recommended.

# 11 Layout

## 11.1 Layout Guidelines

Refer to Figure 33 and use the following guidelines for proper layout design:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at the $V_{IN}$ and $V_{OUT}$ pins.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane to help distribute heat and reduce electromagnetic-interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the end device to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when absolutely necessary.

## 11.2 Layout Example

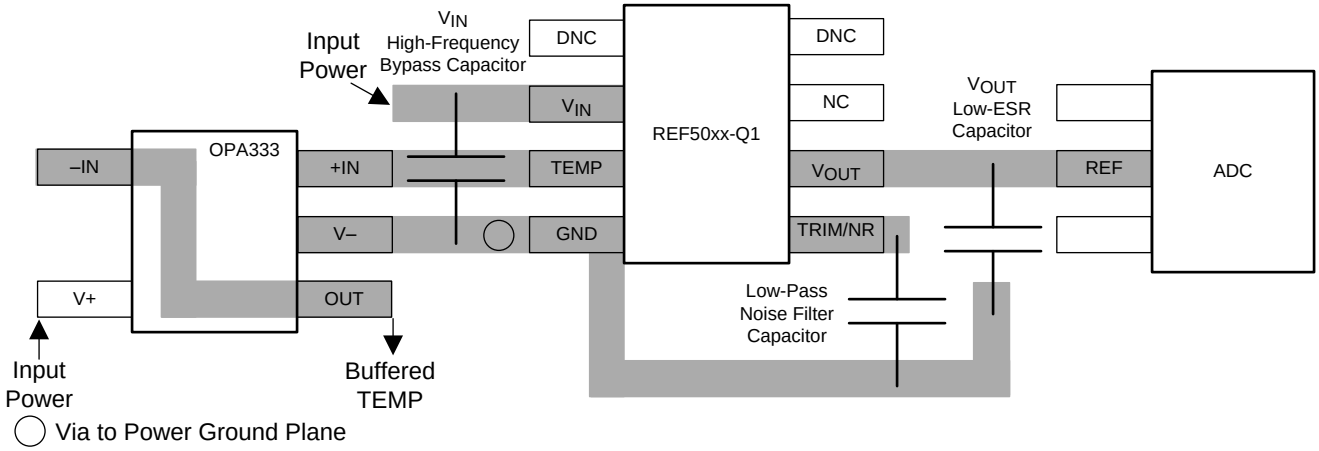



**Figure 33. REF50xxA-Q1 Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- ADS8326 *16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling ANALOG-TO-DIGITAL CONVERTER*, SBAS343
- *Analog Applications Journal—How a Voltage Reference Affects ADC Performance*:
  - Part 1, SLYT331
  - Part 2, SLYT339
  - Part 3, SLYT355
- OPA333 *1.8-V, microPower, CMOS Operational Amplifiers, Zero-Drift Series*, SBOS351
- OPA333-Q1 *1.8-V MICROPOWER CMOS OPERATIONAL AMPLIFIER ZERO-DRIFT SERIES*, SBOS522
- OPA335 *0.05μV/°C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zerø-Drift Series*, SBOS245
- OPA365 *50MHz, Low-Distortion, High CMRR, RRI/O, Single-Supply OPERATIONAL AMPLIFIER*, SBOS365
- OPA365-Q1 *50-MHz Low-Distortion High-CMRR Rail-to-Rail I/O, Single-Supply Operational Amplifier*, SBOS512
- OPA376 *Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim™ Series*, SBOS406
- OPA376-Q1 *Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim™ Series*, SBOS549
- OPA735 *0.05μV/°C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zerø-Drift Series*, SBOS282

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| REF5020A-Q1 | Click here | Click here | Click here | Click here | Click here |
| REF5025A-Q1 | Click here | Click here | Click here | Click here | Click here |
| REF5030A-Q1 | Click here | Click here | Click here | Click here | Click here |
| REF5040A-Q1 | Click here | Click here | Click here | Click here | Click here |
| REF5045A-Q1 | Click here | Click here | Click here | Click here | Click here |
| REF5050A-Q1 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Trademarks

All trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| REF5020AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5020 A |
| REF5020AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5020 A |
| REF5025AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5025 A |
| REF5025AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5025 A |
| REF5030AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5030 A |
| REF5030AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5030 A |
| REF5040AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5040 A |
| REF5040AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5040 A |
| REF5045AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5045 A |
| REF5045AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5045 A |
| REF5050AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5050 A |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| REF5050AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RFQ 5050 A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

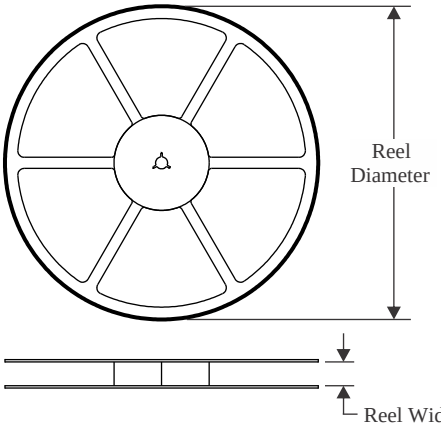
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

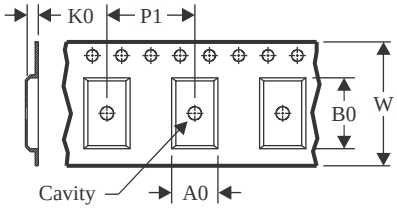
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

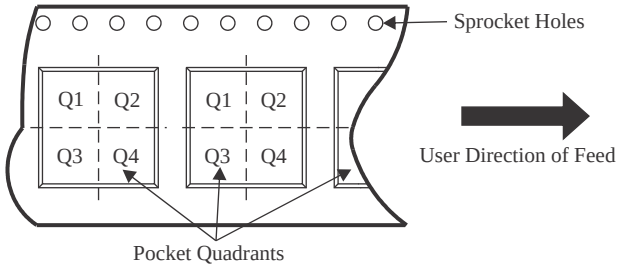



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

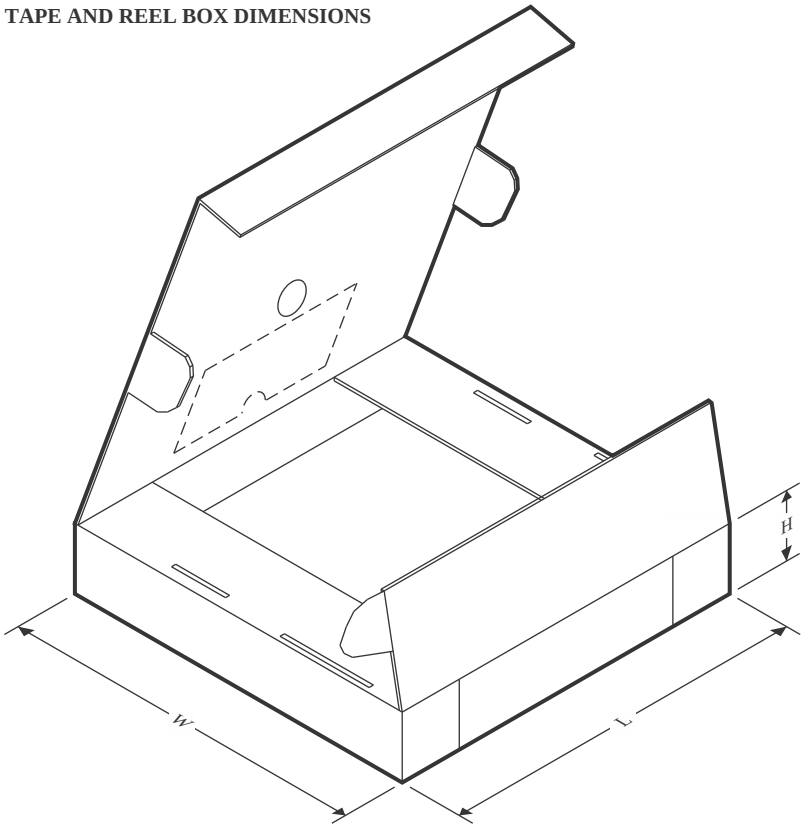
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

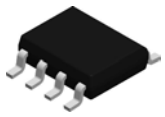
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REF5020AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5020AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5025AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5025AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5030AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5030AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5040AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5045AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5045AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| REF5050AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| REF5020AQDRQ1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REF5020AQDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| REF5025AQDRQ1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REF5025AQDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| REF5030AQDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| REF5030AQDRQ1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REF5040AQDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| REF5045AQDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| REF5045AQDRQ1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REF5050AQDRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

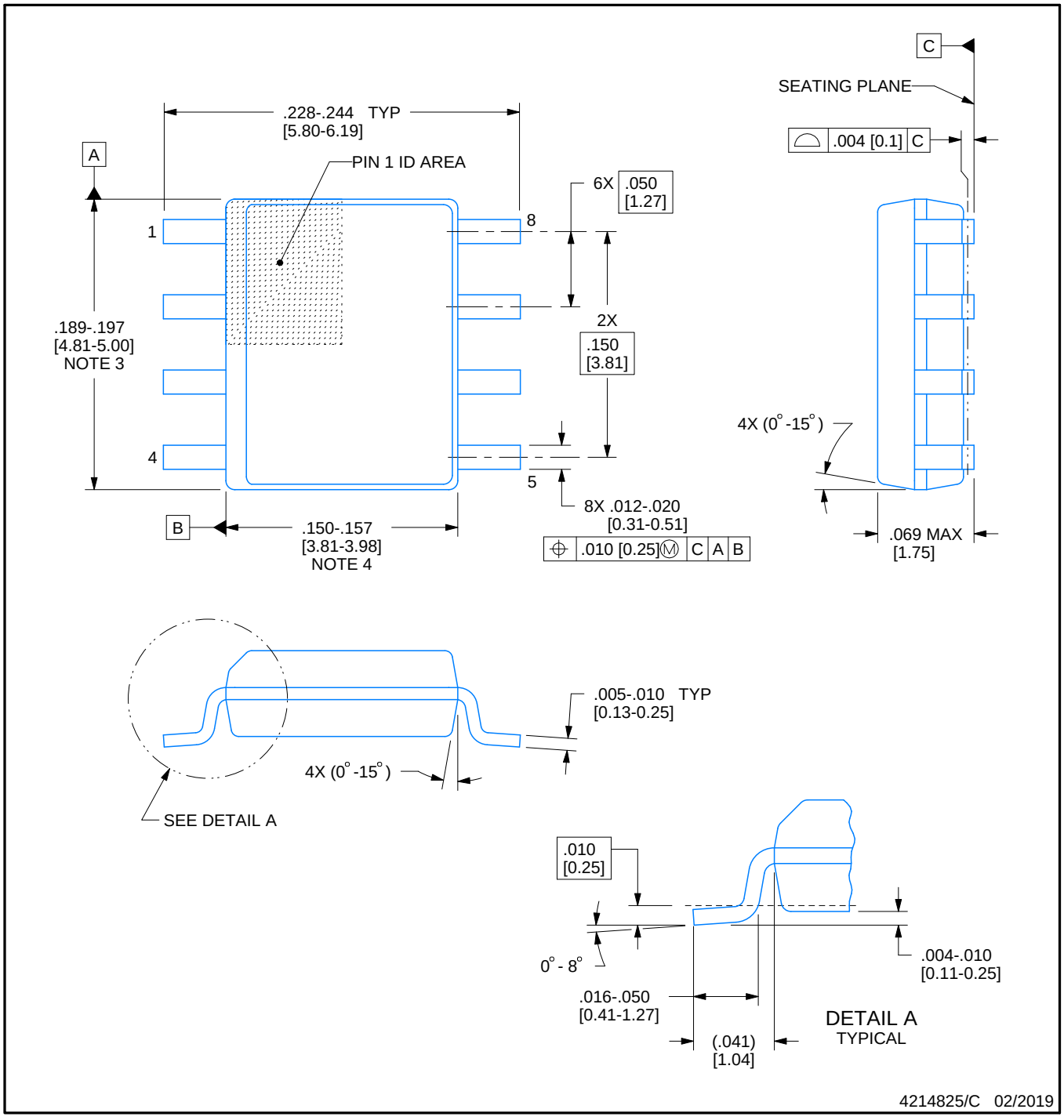


# PACKAGE OUTLINE

## D0008A

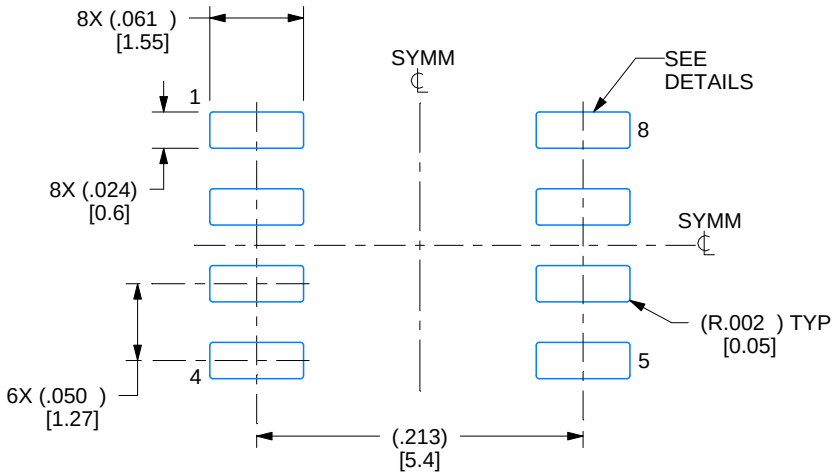
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

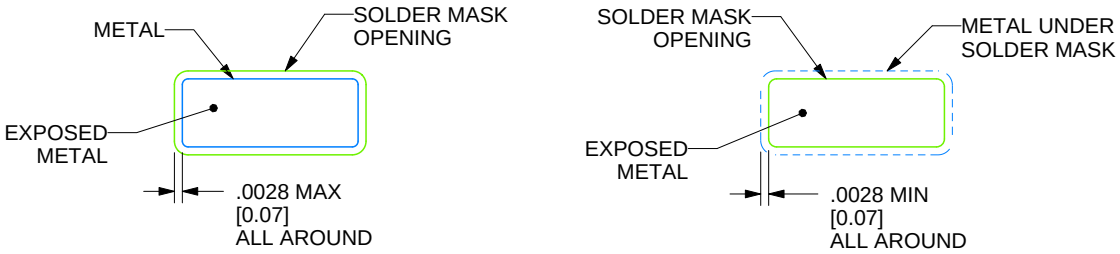



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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NOTES: (continued)

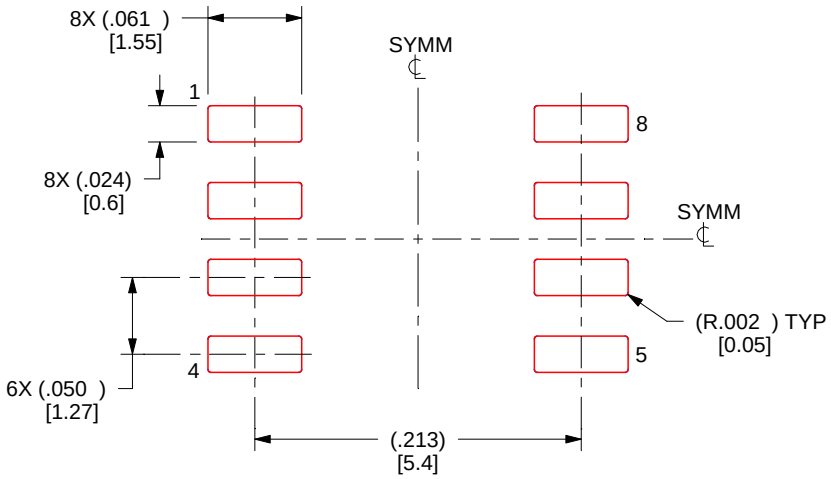
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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