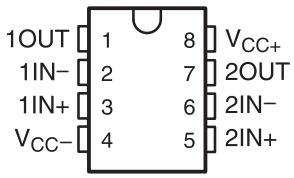
DUAL AUDIO OPERATIONAL AMPLIFIER

Check for Samples: RC4580-Q1

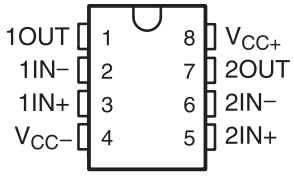
FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Operating Voltage . . . ±2 V to ±18 V**
- **Low Noise Voltage . . . 0.8 μVrms (TYP)**
- **Wide GBW . . . 12 MHz (TYP)**
- **Low THD . . . 0.0005% (TYP)**
- **Slew Rate . . . 5 V/μs (TYP)**
- **Suitable for Automotive Applications Such As Audio Preamplifier, Active Filter, Headphone Amplifier, Industrial Measurement Equipment**
- **Drop-In Replacement for NJM4580**
- **Pin and Function Compatible With LM833, NE5532, NJM4558/9, and NJM4560/2/5**

D PACKAGE
SOIC – 8
(TOP VIEW)



PW PACKAGE
TSSOP – 8
(TOP VIEW)



DESCRIPTION

The RC4580-Q1 device is a dual operational amplifier that is designed optimally for audio applications, such as improving tone control. It offers low noise, high gain bandwidth, low harmonic distortion, and high output current. All of these features make the device ideally suited for audio electronics, such as audio preamplifiers and active filters, as well as industrial measurement equipment. When high output current is required, the RC4580-Q1 device can be used as a headphone amplifier. Due to its wide operating supply voltage, the RC4580-Q1 device can also be used in low-voltage applications.

ORDERING INFORMATION(1)

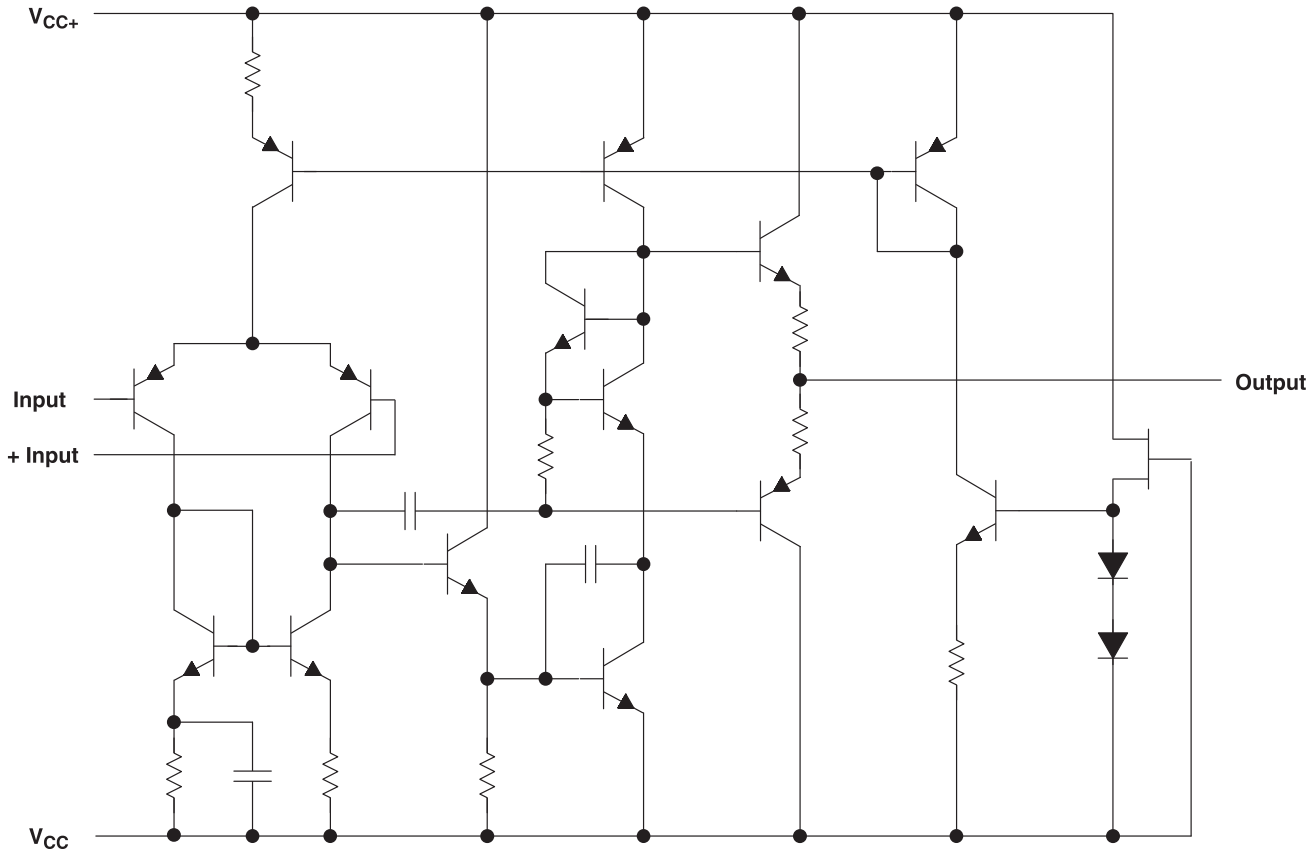
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2000	RC4580QDRQ1	R4580Q
–40°C to 125°C	TSSOP - PW	Reel of 2000	RC4580QPWRQ1	R4580Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Figure 1. EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		±18	V
	Input voltage (any input)		±15	V
V_{ID}	Differential input voltage		±30	V
	Output current		±50	mA
T_A	Ambient temperature range	–40	125	°C
T_{stg}	Storage temperature range	–60	125	°C
Electrostatic Discharge (ESD) Ratings	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		RC4580-Q1		UNIT
		D (8 PINS)	PW (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	109	163	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	55.7	38	
θ_{JB}	Junction-to-board thermal resistance	49	90.6	
ψ_{JT}	Junction-to-top characterization parameter	10.6	1.3	
ψ_{JB}	Junction-to-board characterization parameter	48.6	88.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
V_{CC-}		–2	–16	
V_{ICR}	Input common-mode voltage range	–13.5	13.5	V
T_A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = < 10 kΩ		0.5	3	mV
I_{IO}	Input offset current			5	200	nA
I_{IB}	Input bias current			100	500	nA
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	90	110		dB
V_{CM}	Output voltage swing	R_L ≥ 2 kΩ	±12	±13.5		V
V_{ICR}	Common-mode input voltage		±12	±13.5		V
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ	80	110		dB
k_{SVR}	Supply-voltage rejection ratio[1]	R_S ≤ 10 kΩ	80	110		dB
I_{CC}	Total supply current (all amplifiers)			6	9	mA

(1) Measured with $V_{CC\pm}$ varied simultaneously

OPERATING CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	R_L ≥ 2 kΩ	5	V/µs
GBW	Gain-bandwidth product	f = 10 kHz	12	MHz
THD	Total harmonic distortion	V_O = 5 V, R_L = 2 kΩ, f = 1 kHz, A_{VD} = 20 dB	0.0005%	
V_n	Equivalent input noise voltage	RIAA, R_S ≤ 2.2 kΩ, 30-kHz LPF	0.8	µVrms

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

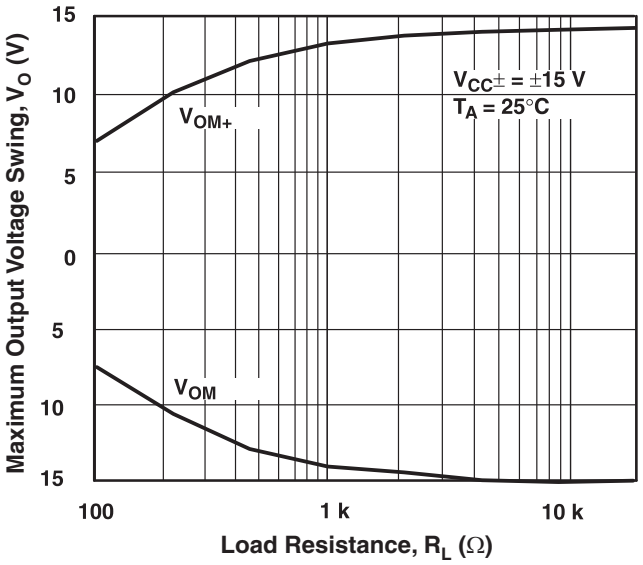


Figure 2.

MAXIMUM OUTPUT VOLTAGE SWING
vs
FREQUENCY

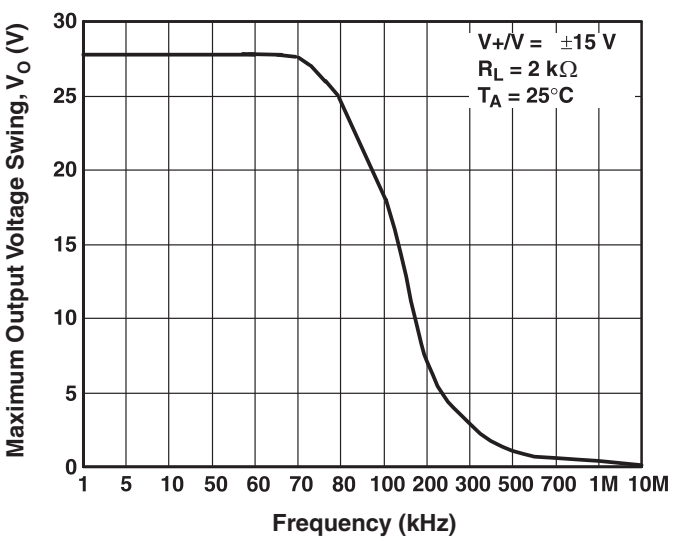


Figure 3.

OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

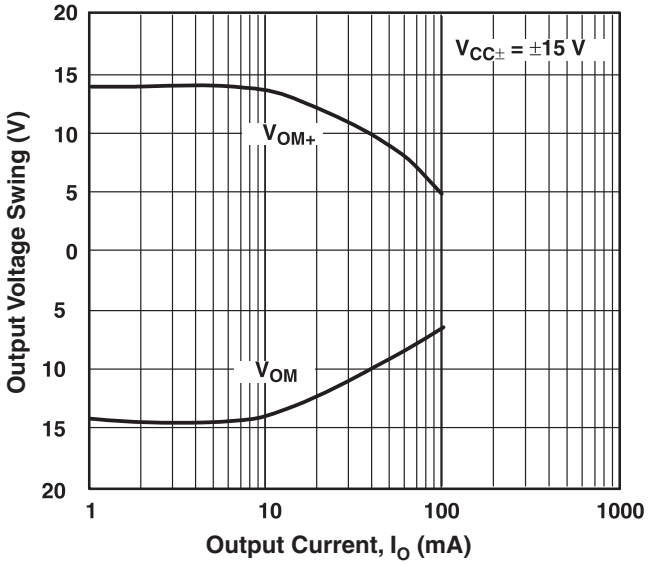


Figure 4.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

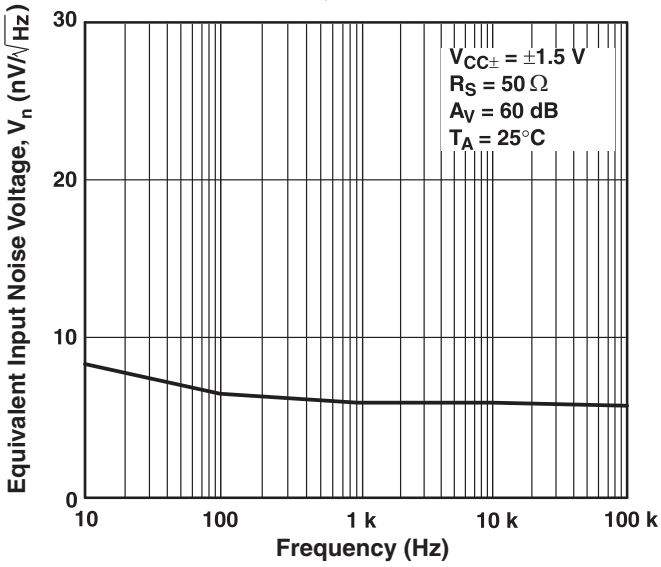


Figure 5.

TYPICAL CHARACTERISTICS (continued)

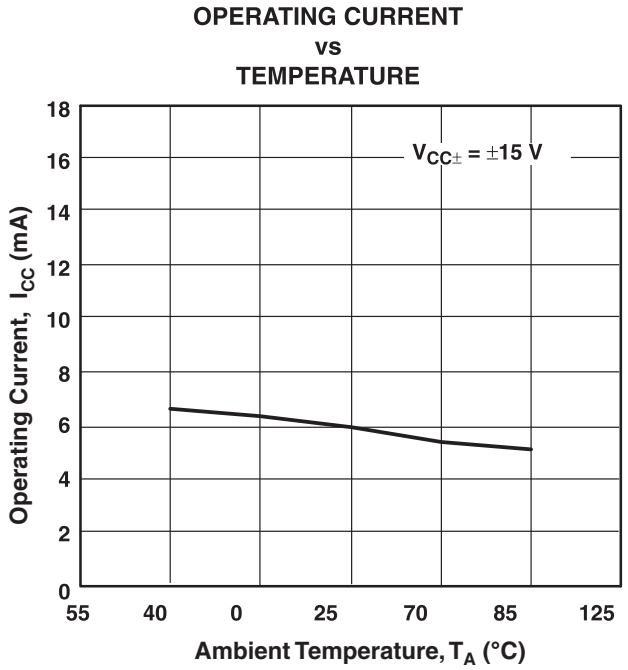


Figure 6.

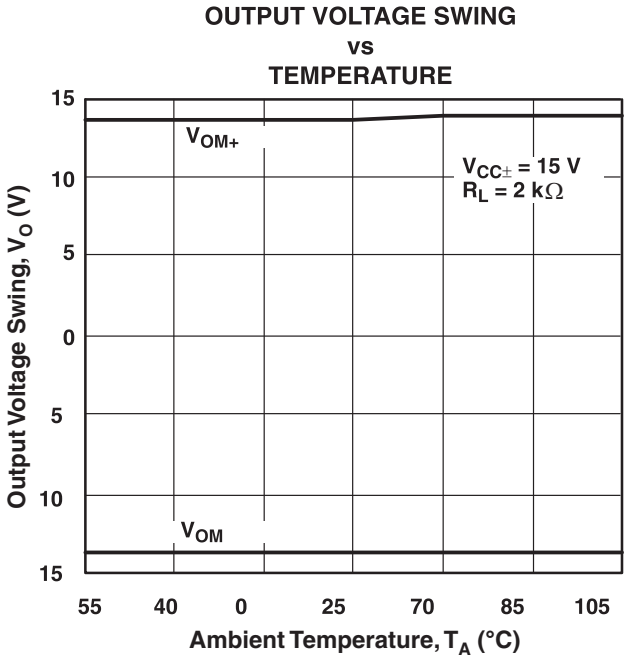


Figure 7.

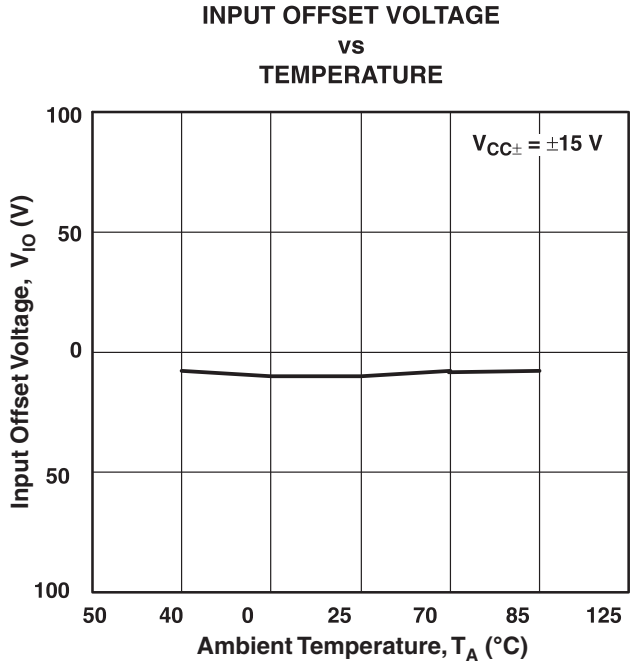


Figure 8.

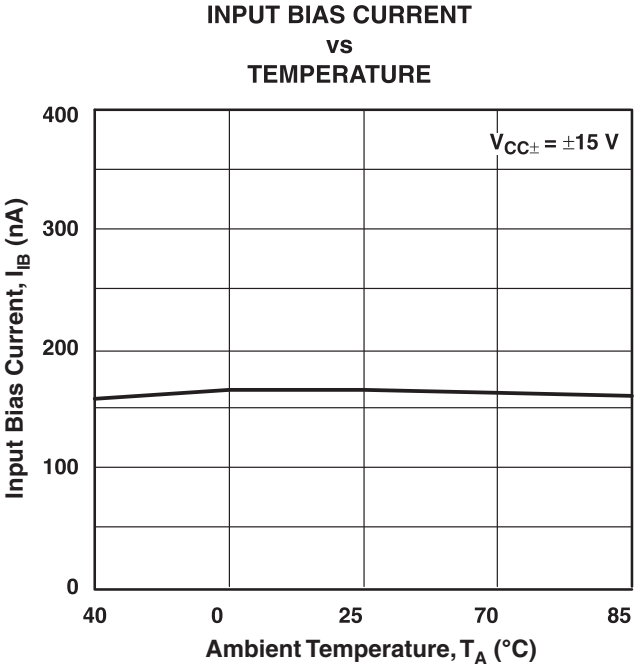


Figure 9.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM OUTPUT VOLTAGE SWING vs OPERATING VOLTAGE

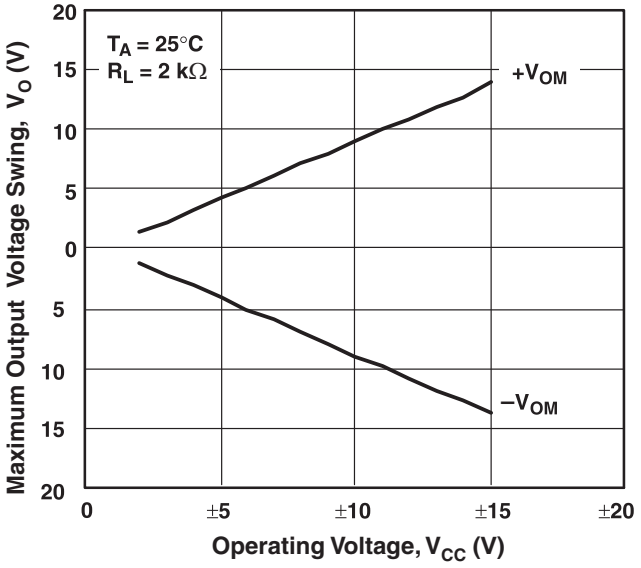


Figure 10.

OPERATING CURRENT vs OPERATING VOLTAGE

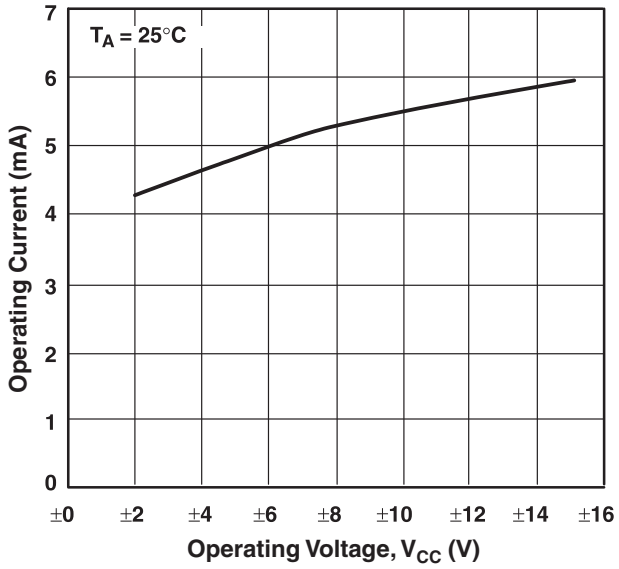


Figure 11.

TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE

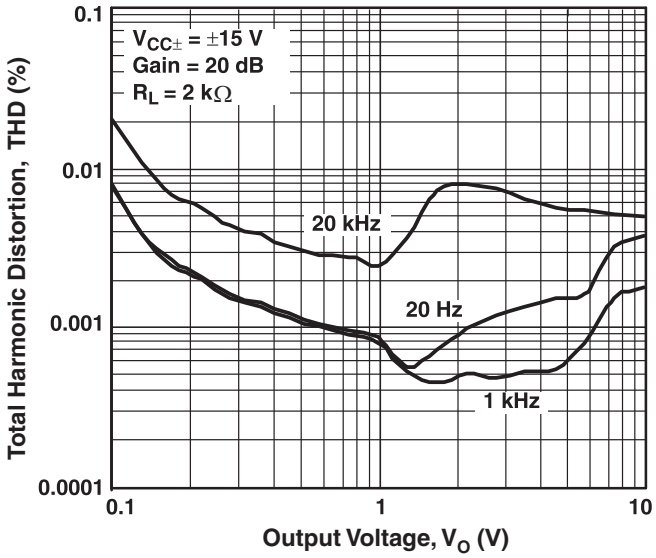


Figure 12.

VOLTAGE GAIN, PHASE vs FREQUENCY

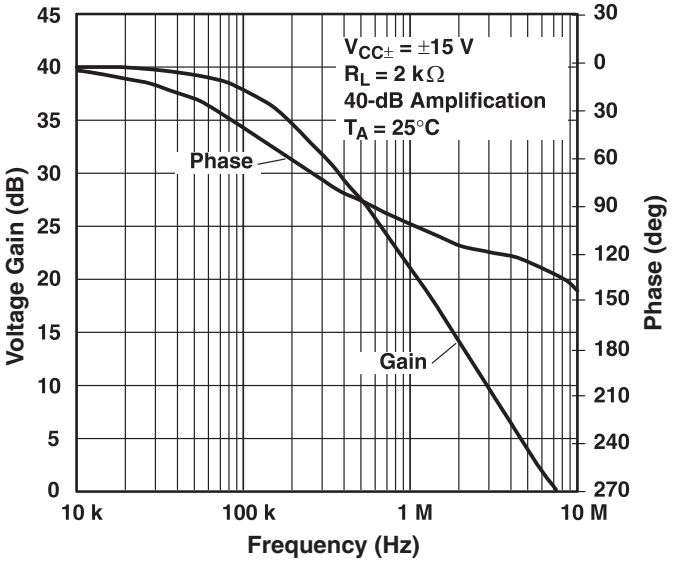


Figure 13.

REVISION HISTORY

Changes from Original (December 2010) to Revision A **Page**

- Added AEC-Q100 info to the features; changed Suitable for Applications to Suitable for Automotive Applications 1
- Added PW pinout drawing 1
- Added second row for PW package to Ordering Information table 1
- Added ESDS 2
- Changed T_J to T_A 2
- Removed θ_{JA} row from Abs Max table because it is also listed in the thermal table 2
- Added ESD ratings to Abs Max table 2
- Added thermal table 3
- Changed T_A = 25°C to T_A = –40°C to 125°C in condition statement for Elec Char table and Op Char table 3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RC4580QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580Q
RC4580QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580Q
RC4580QPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580Q
RC4580QPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF RC4580-Q1 :

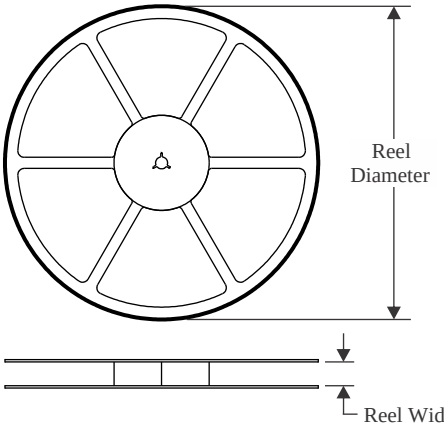
- Catalog : RC4580

NOTE: Qualified Version Definitions:

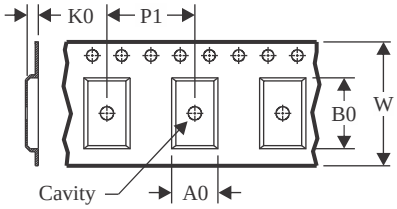
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

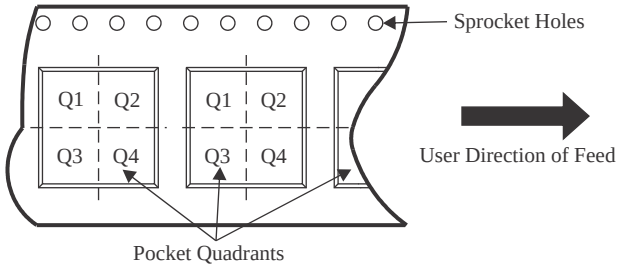


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

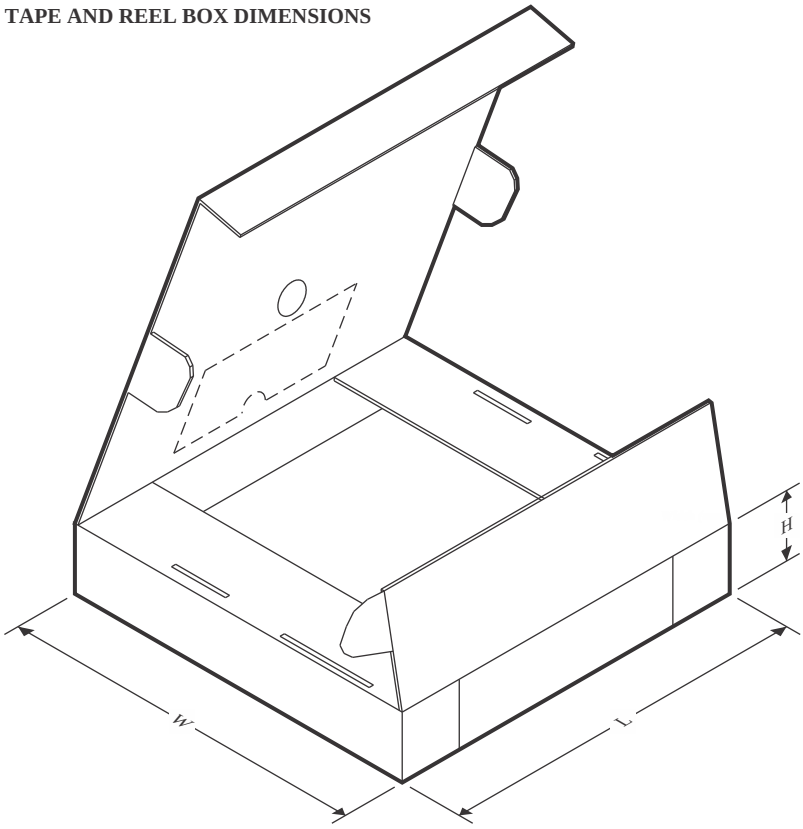
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

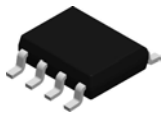
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4580QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4580QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
RC4580QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

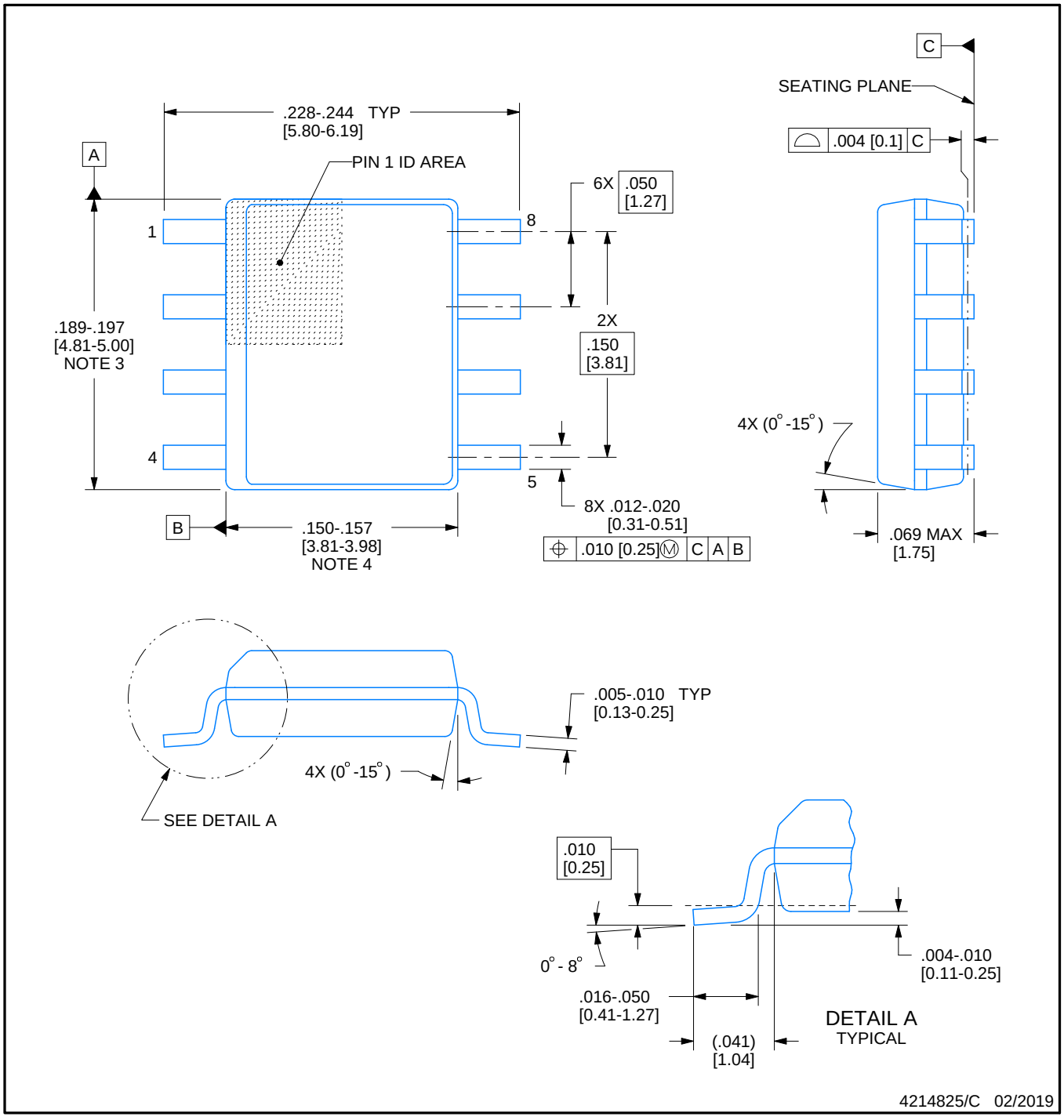


PACKAGE OUTLINE

D0008A

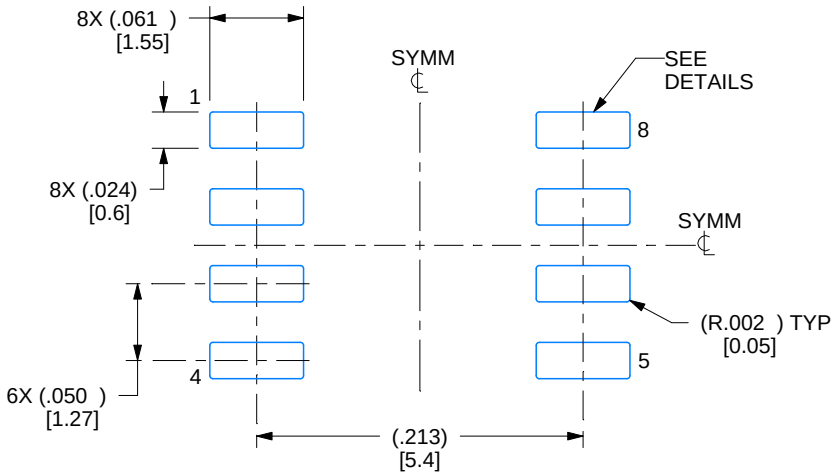
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

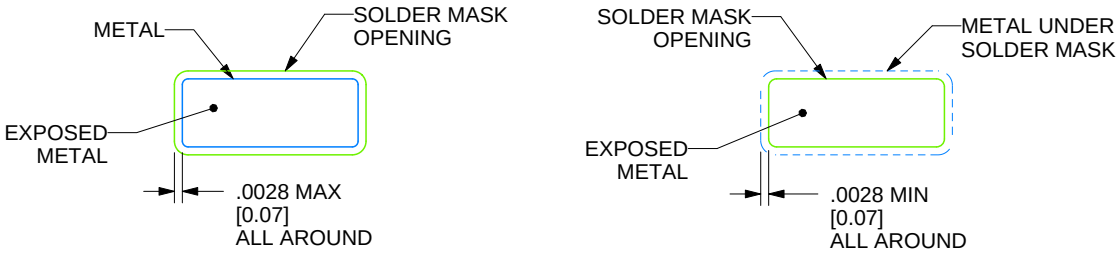


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

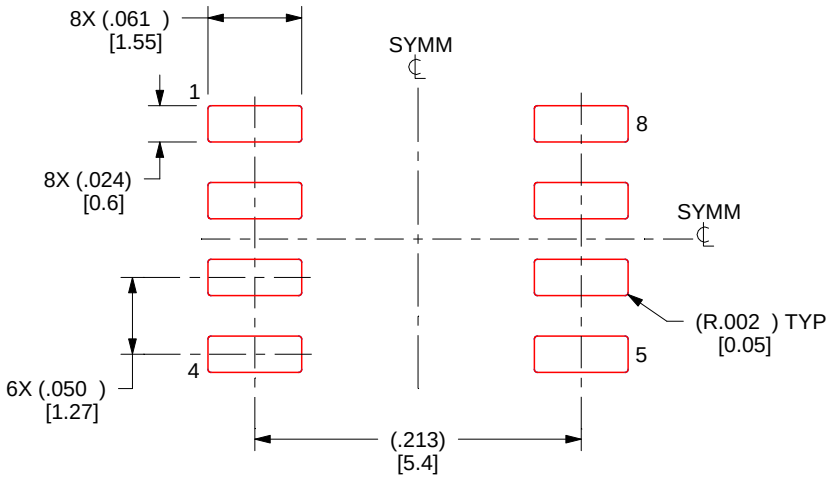
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

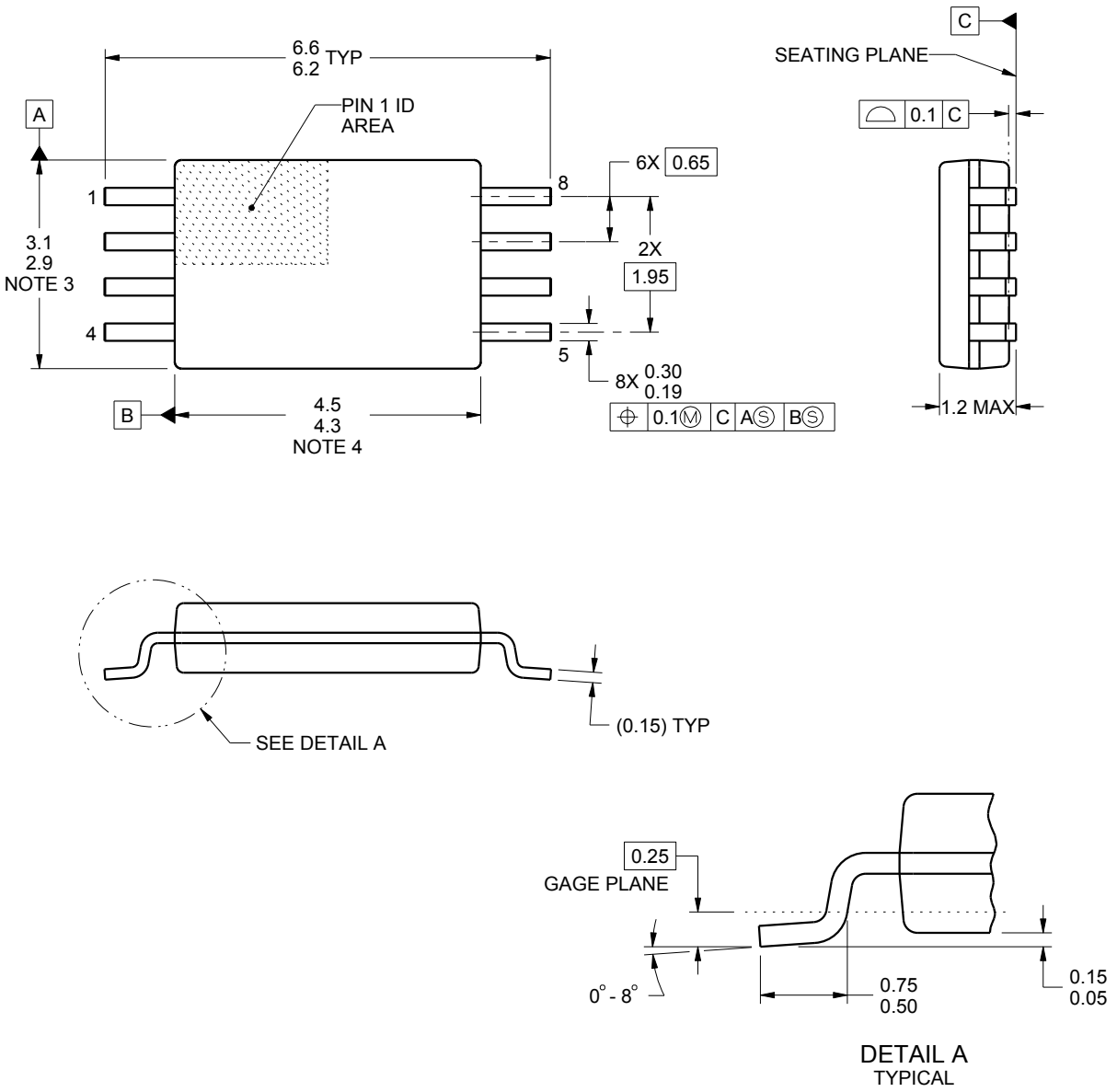
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

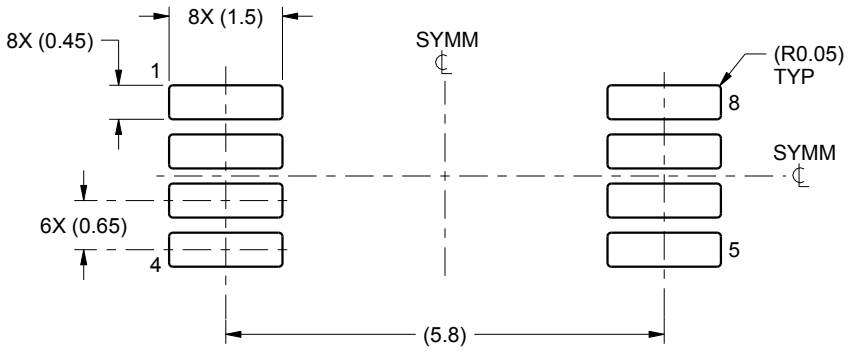
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

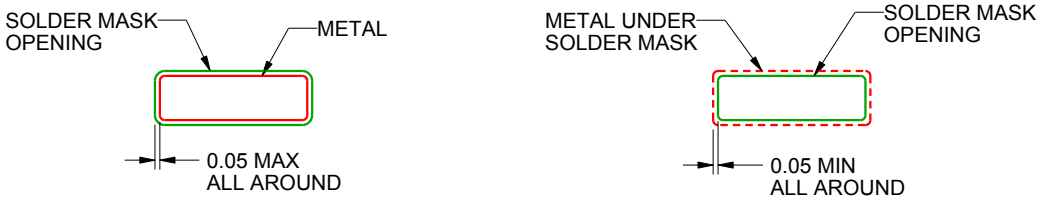


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

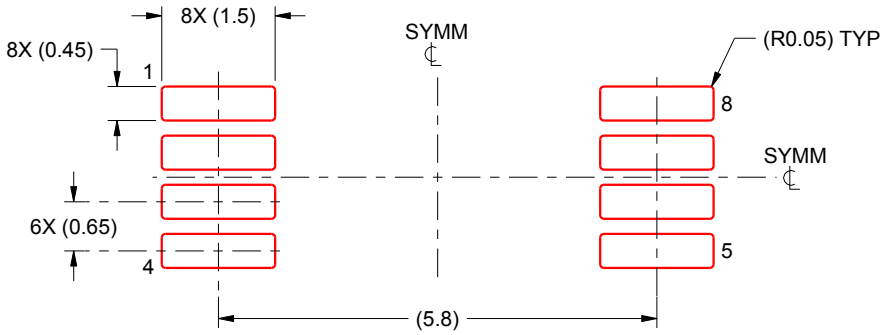


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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