DUAL AUDIO OPERATIONAL AMPLIFIER

FEATURES

- **Operating Voltage . . . ±2 V to ±18 V**
- **Low Noise Voltage . . . 1.2 μVrms (Typ)**
- **Wide GBW . . . 15 MHz (Typ)**
- **Low THD . . . 0.05% (Typ)**
- **Slew Rate . . . 5.5 V/μsec (Typ)**
- **Suitable for Applications Such as Audio Preamplifier, Active Filter, Headphone Amplifier, Industrial Measurement Equipment**

DESCRIPTION/ORDERING INFORMATION

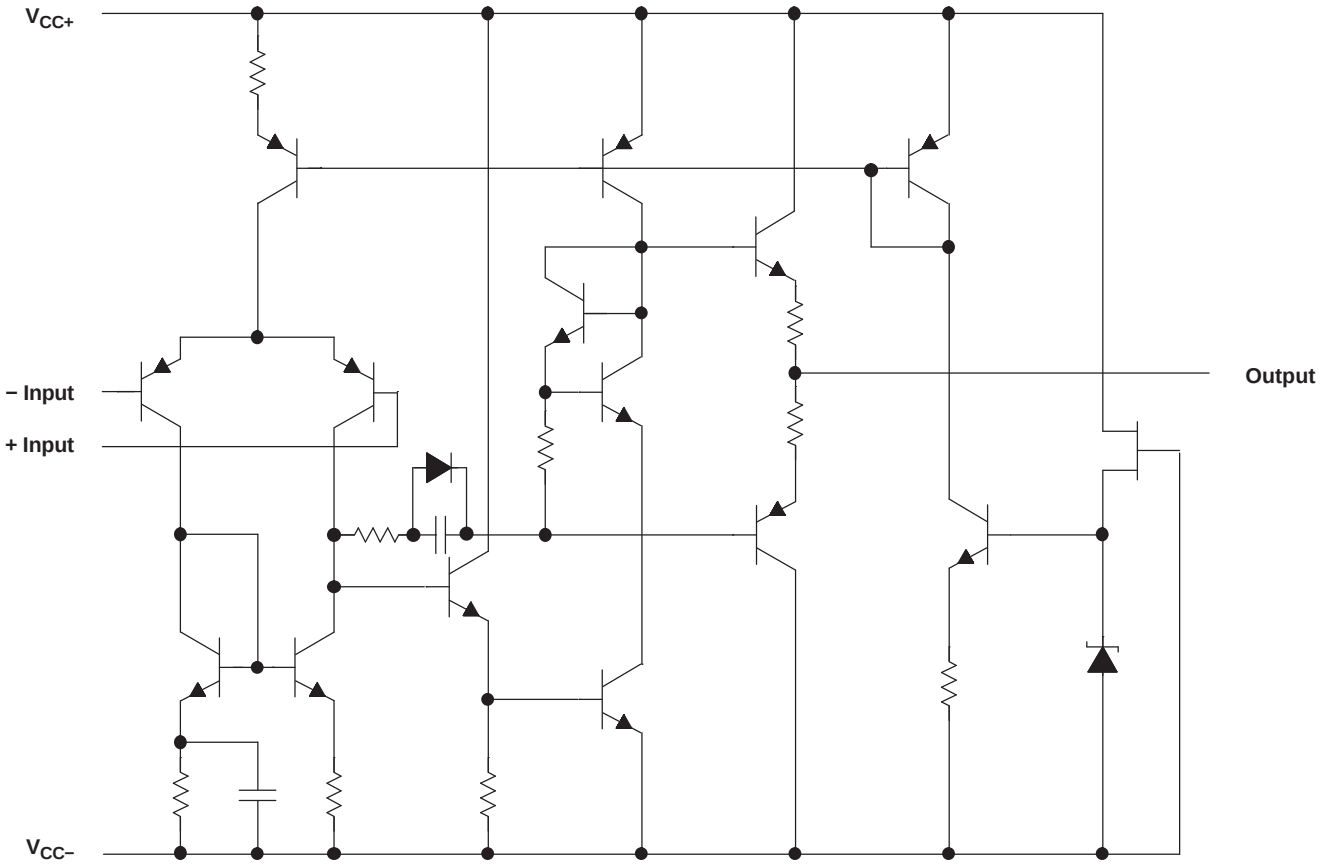
The RC4560 is a high-gain, wide-bandwidth, dual operational amplifier capable of driving 20 V peak-to-peak into 400-Ω loads. The RC4560 combines many of the features of the RC4558, but with wider bandwidth and higher slew rate, making this device ideal for active filters, data and telecommunications, and many instrumentation applications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – P	Tube of 50	RC4560IP	RC4560IP
	SOIC – D	Tube of 75	RC4560ID	R4560I
		Reel of 2500	RC4560IDR	
	TSSOP – PW	Tube of 150	RC4560IPW	R4560I
		Reel of 2000	RC4560IPWR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

$V_{CC\pm}$	Supply voltage		±18 V
	Input voltage (any input)		±15 V
	Output current		±50 mA
θ_{JA}	Package thermal impedance(2)(3)	D package	97°C/W
		P package	85°C/W
		PW package	149°C/W
T_J	Operating virtual junction temperature		150°C
T_{stg}	Storage temperature range		−60°C to 125°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
V_{CC-}		–2	–16	
V_{ID}	Differential input voltage		±30	V
V_{ICR}	Input common mode range	–14	14	V
T_A	Operating free-air temperature range	–40	85	°C

ELECTRICAL CHARACTERISTICS

$V_{CC±}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S ≤ 10 kΩ		0.5	6	mV
I_{IO}	Input offset current			5	200	nA
I_{IB}	Input bias current			40	500	nA
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	86	100		dB
r_i	Input resistance		0.3	5		MΩ
V_O	Output voltage swing	R_L ≥ 2 kΩ	±12	±14		V
		I_O = 25 mA	±10	±12.5		
V_{ICR}	Common-mode input voltage range		±12	±14		V
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ	70	90		dB
k_{SVR}	Supply-voltage rejection ratio (1)	R_S ≤ 10 kΩ	76.5	90		dB
I_{CC}	Supply current (all amplifiers)			4.3	5.7	mA

(1) Measured with $V_{CC±}$ differentially varied simultaneously from ±4 V to ±15 V

OPERATING CHARACTERISTICS

$V_{CC±}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain		5.5	V/µs
GBW	Gain bandwidth product		15	MHz
THD	Total harmonic distortion	V_O = 5 V, R_L = 2 kΩ, f = 1 kHz, A_{VD} = 20 dB	0.05	%
V_n	Equivalent input noise voltage	RIAA, R_S ≤ 2 kΩ, 30-kHz LPF	1.2	µVrms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RC4560ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	R4560I
RC4560IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I
RC4560IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I
RC4560IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	RC4560IP
RC4560IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	RC4560IP
RC4560IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	R4560I
RC4560IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I
RC4560IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

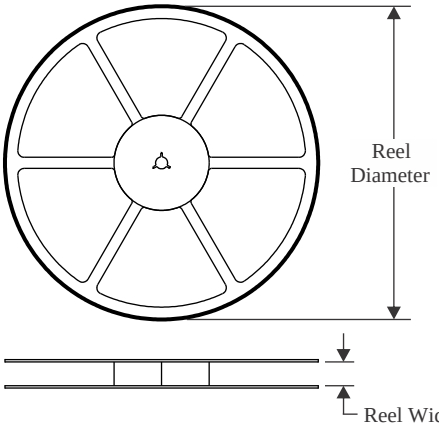
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

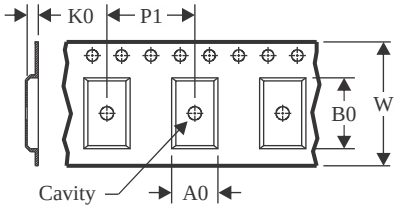
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

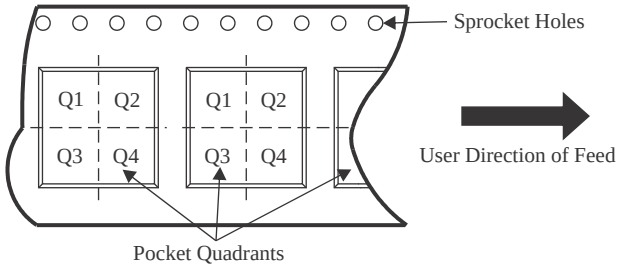


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

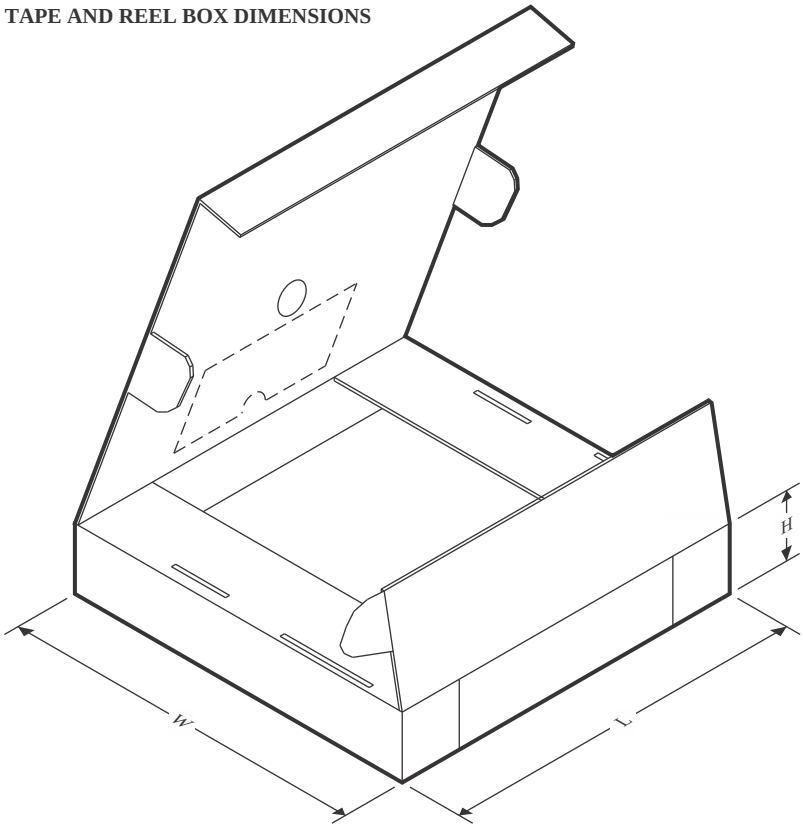
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4560IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4560IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

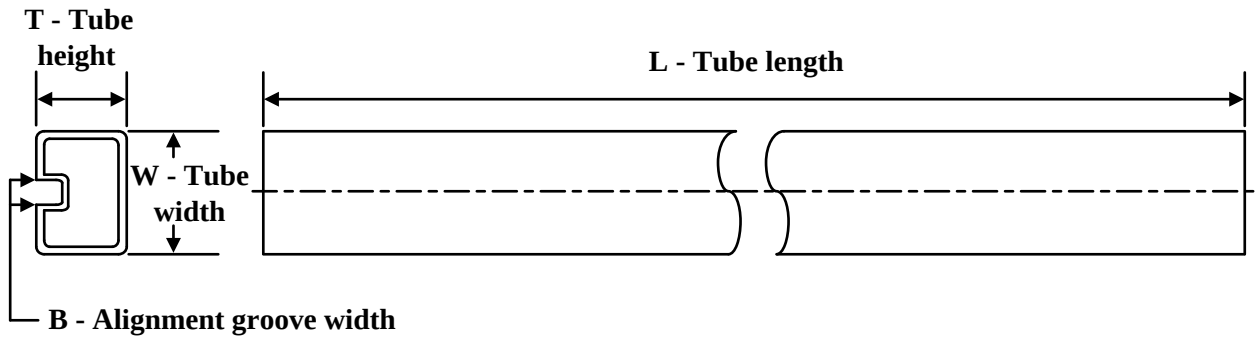
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

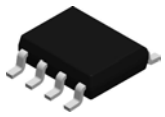
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4560IDR	SOIC	D	8	2500	353.0	353.0	32.0
RC4560IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
RC4560IP	P	PDIP	8	50	506	13.97	11230	4.32
RC4560IP.A	P	PDIP	8	50	506	13.97	11230	4.32

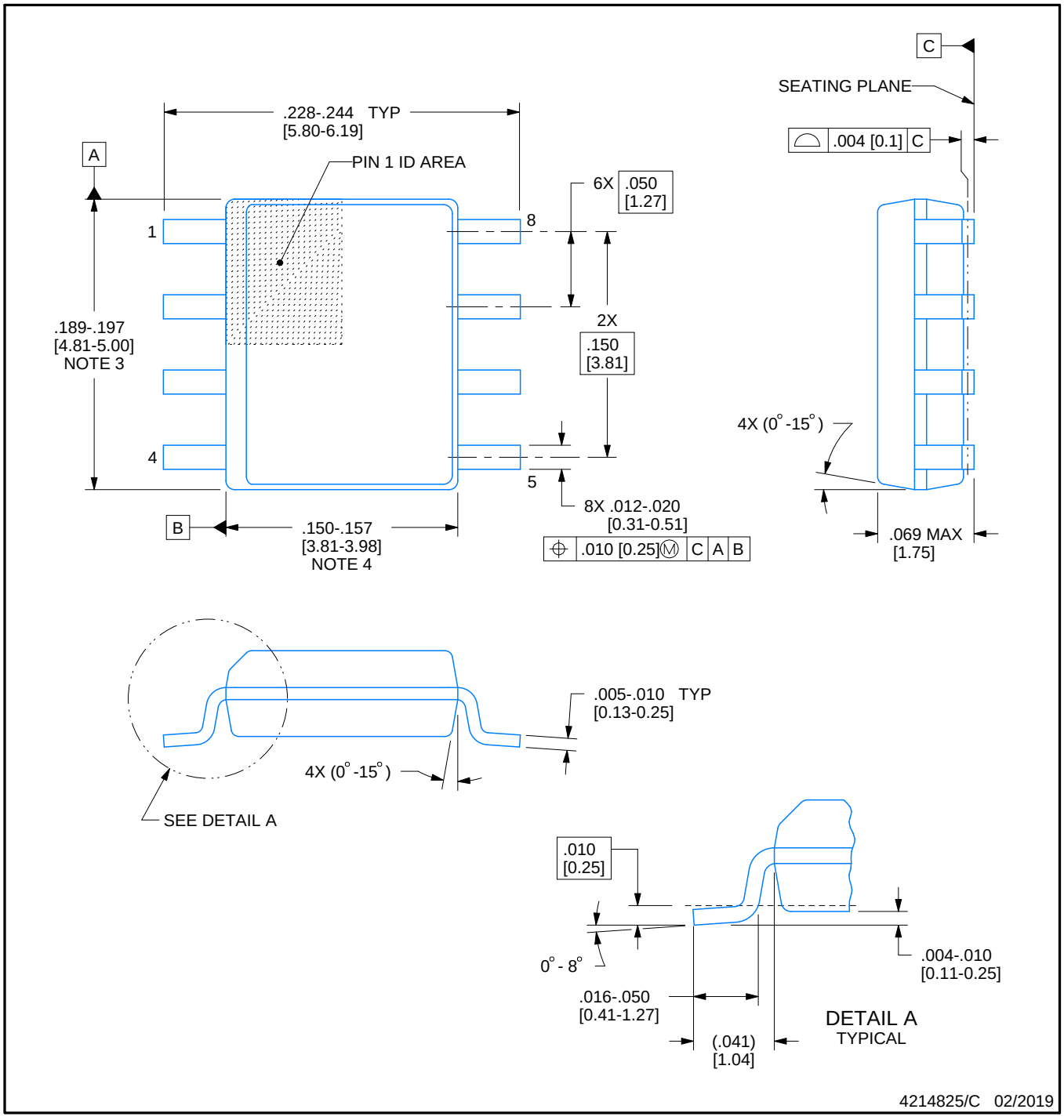


PACKAGE OUTLINE

D0008A

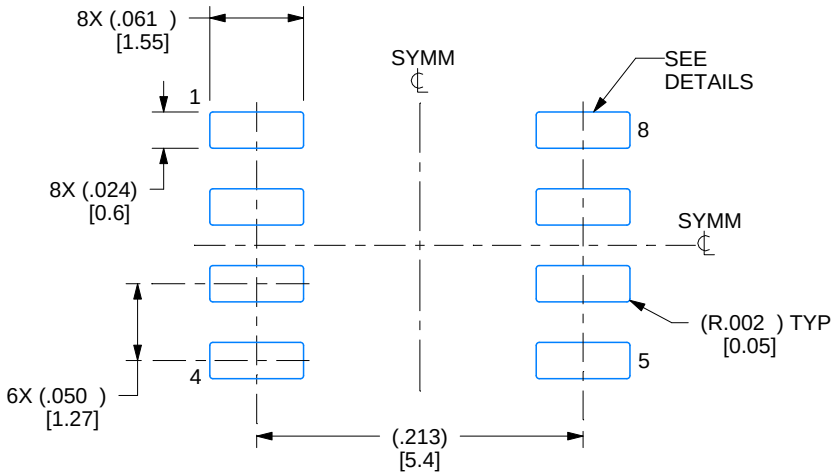
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

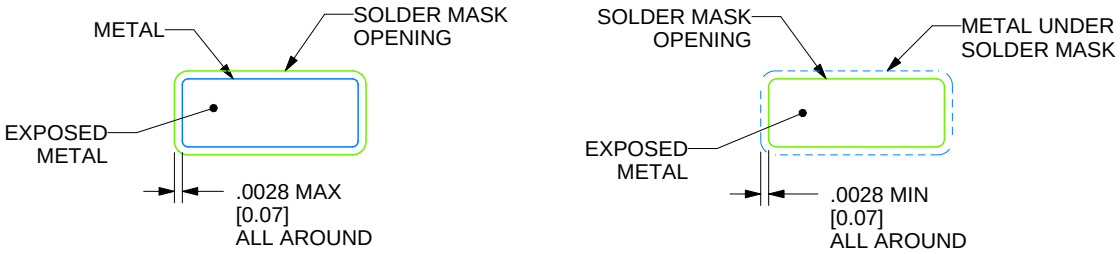


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

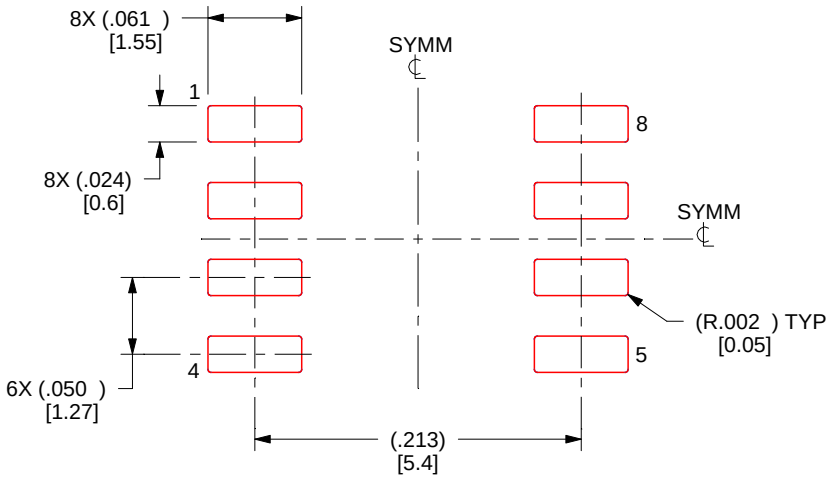
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



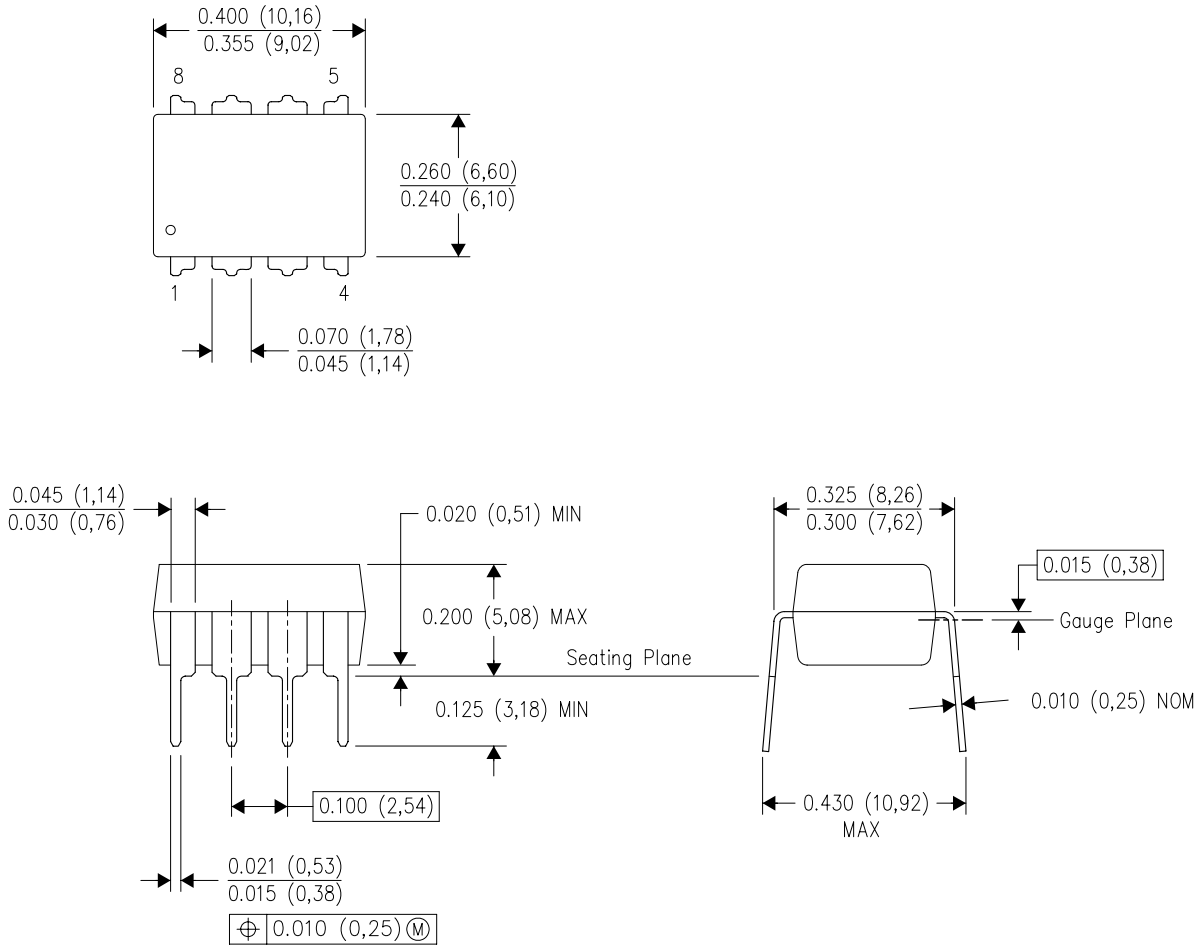
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



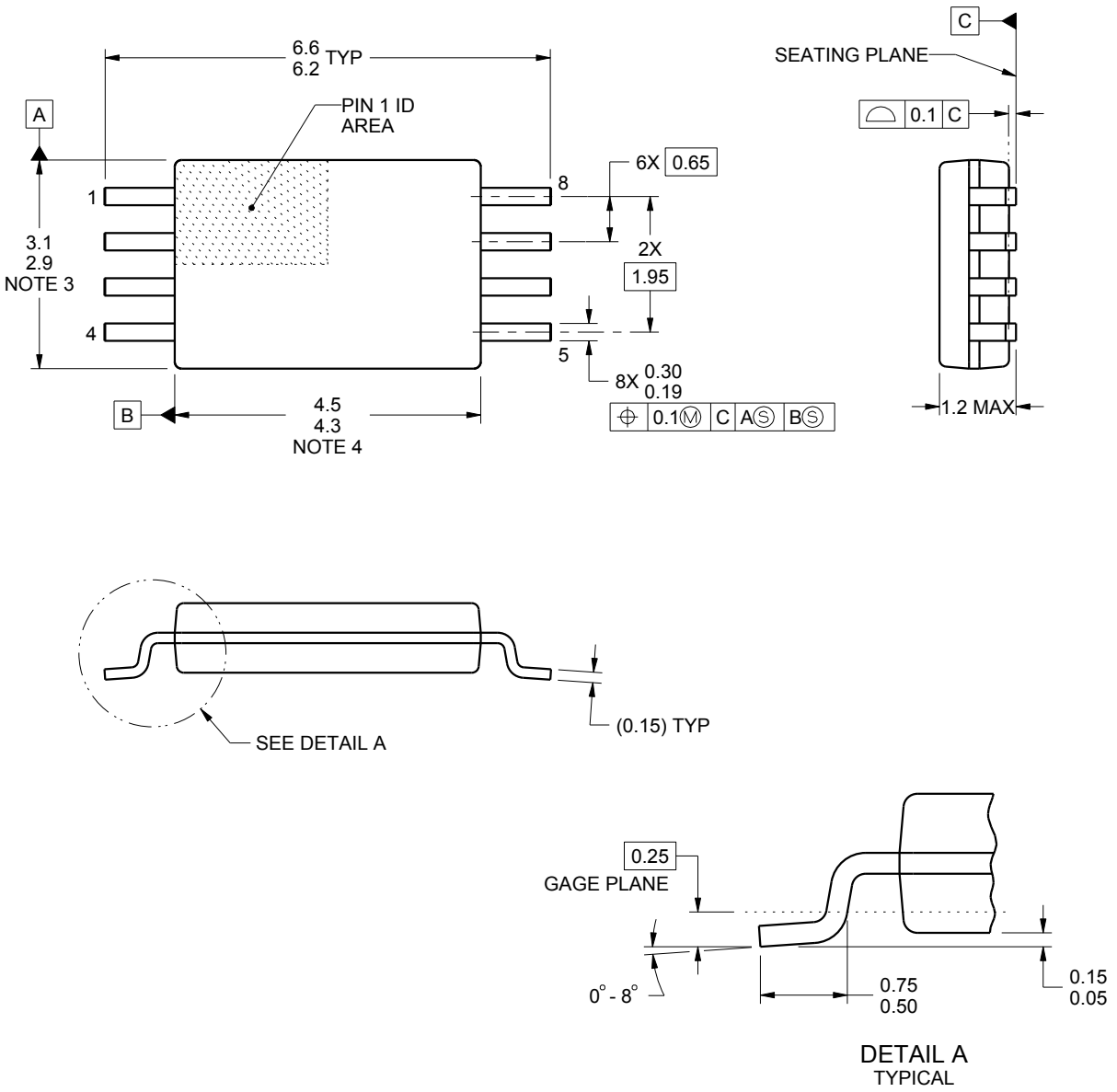
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

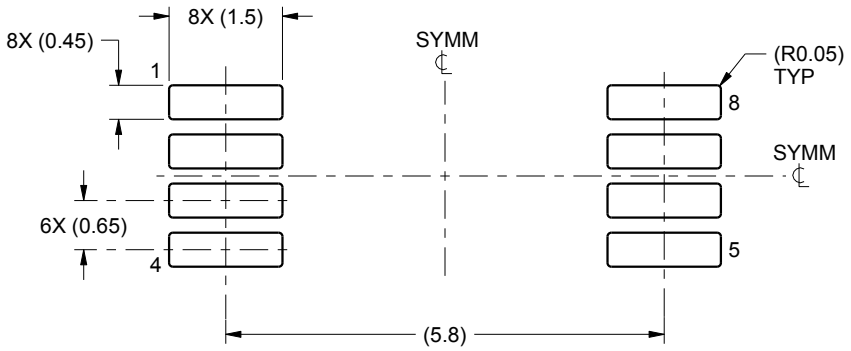
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

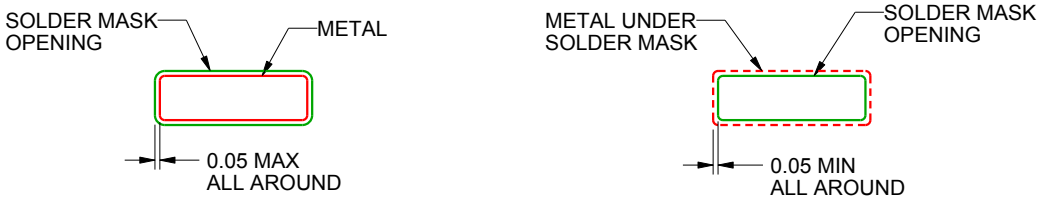


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

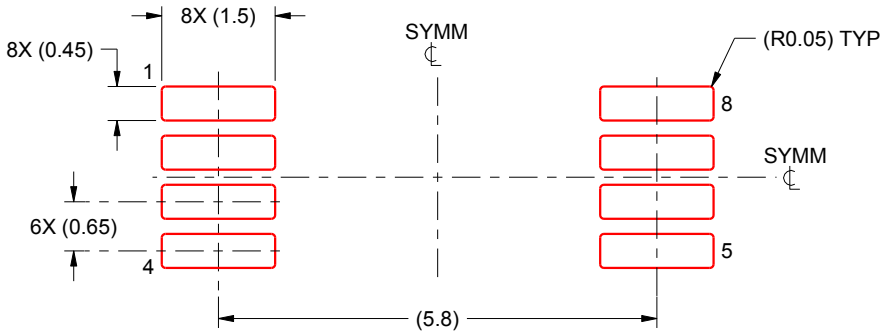


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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