SBOS317D − SEPTEMBER 2004 − REVISED AUGUST 2008

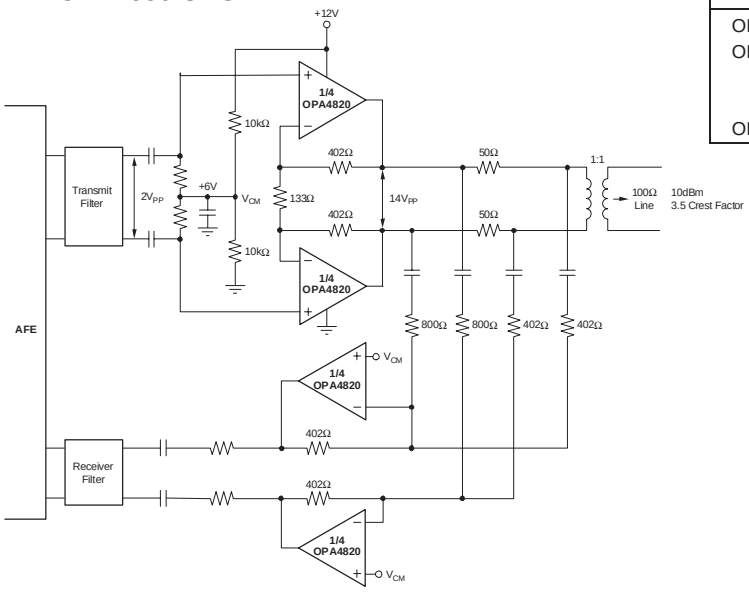
Quad, Unity-Gain Stable, Low-Noise, Voltage-Feedback Operational Amplifier

FEATURES

- **HIGH BANDWIDTH: 220MHz (G = +2)**
- **HIGH OUTPUT CURRENT: ±85mA**
- **LOW INPUT NOISE: 2.5nV/√Hz**
- **LOW SUPPLY CURRENT: 5.7mA/ch**
- **FLEXIBLE SUPPLY VOLTAGE:**
  ±2V to ±6.3V Dual Supply
  +4V to +12.6V Single Supply
- **EXCELLENT DC ACCURACY:**
  Maximum 25°C Input Offset Voltage = 0.8mV
  Maximum 25°C Input Offset Current = 500nA

APPLICATIONS

- **LOW-COST VIDEO LINE DRIVERS**
- **ADC PREAMPS**
- **ACTIVE FILTERS**
- **LOW-NOISE INTEGRATORS**
- **PORTABLE TEST EQUIPMENT**
- **OPTICAL CHANNEL AMPLIFIERS**
- **LOW-POWER, BASEBAND AMPLIFIERS**
- **CCD IMAGING CHANNEL AMPLIFIERS**
- **OPA4650 UPGRADE**



Low-Noise Transceiver Interface

DESCRIPTION

The OPA4820 provides a wideband, unity-gain stable, voltage-feedback amplifier with a very low input noise voltage and high output current using a low 5.7mA/ch supply current. At unity-gain, the OPA4820 gives > 600MHz bandwidth with < 1 dB peaking. The OPA4820 complements this high-speed operation with excellent DC precision in a low-power device. A worst-case input offset voltage of ±0.8mV and an offset current of ±500nA give excellent absolute DC precision for pulse amplifier applications.

Minimal input and output voltage swing headroom allow the OPA4820 to operate on a single +5V supply with > $2V_{PP}$ output swing. While not a rail-to-rail (RR) output, this swing will support most emerging analog-to-digital converter (ADC) input ranges with lower power and noise than typical RR output op amps.

Exceptionally low dG/dP (0.01%/0.03°) supports low-cost composite video line driver applications. Existing designs can use the industry-standard quad pinout SO-14 package while emerging high-density portable applications can use the TSSOP-14.

RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	FEATURES
OPA354	OPA2354	—	OPA4354	CMOS RR Output
OPA690	OPA2690	OPA3690	—	High Slew Rate
—	OPA2652	—	—	SOT23-8
—	OPA2822	—	—	Low-Noise
OPA820	—	—	—	Single Channel

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

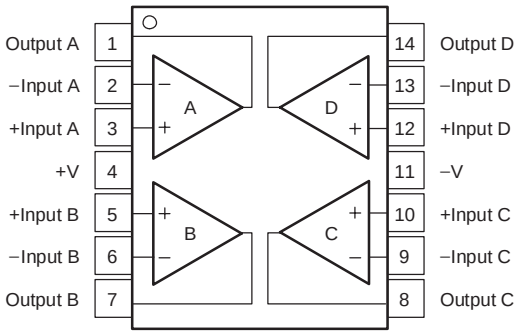
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA4820	SO-14	D	−45°C to +85°C	OPA4820	OPA4820ID	Rails, 58
″	″	″	″	″	OPA4820IDR	Tape and Reel, 2500
OPA4820	TSSOP-14	PW	−45°C to +85°C	OPA4820	OPA4820IPWT	Tape and Reel, 250
″	″	″	″	″	OPA4820IPWR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet or see the TI website at www.ti.com.

PIN CONFIGURATION

TOP VIEW **SO, TSSOP**



OPA4820

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

At $R_F = 402\Omega$, $R_L = 100\Omega$, and GND = +2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA4820ID, IPW				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, $V_O = 0.1V_{PP}$, $R_F = 25\Omega$	650				MHz	typ	C
	G = +2, $V_O = 0.1V_{PP}$	220	150	140	135	MHz	min	B
	G = +10, $V_O = 0.1V_{PP}$	27	21	19	18	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	250	200	185	180	MHz	min	B
Peaking at a Gain of 1	$V_O = 0.1V_{PP}$, $R_F = 25\Omega$	1				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O = 0.1V_{PP}$	33				MHz	typ	C
Large-Signal Bandwidth	G = +2, $2V_{PP}$	80				MHz	typ	C
Slew Rate	G = +2, 2V Step	240	190	184	178	V/µs	min	B
Rise Time and Fall TIme	G = +2, V_O = 2V Step	1.5				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	22				ns	typ	C
Settling Time to 0.1%	G = +2, V_O = 2V Step	18				ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 200\Omega$	−84	−80	−79	−78	dBc	max	B
	$R_L \geq 500\Omega$	−90	−85	−83	−81	dBc	max	B
3rd-Harmonic	$R_L = 200\Omega$	−92	−87	−86	−85	dBc	max	B
	$R_L \geq 500\Omega$	−105	−100	−97	−95	dBc	max	B
Input Voltage Noise	f > 100kHz	2.5	2.7	2.8	2.9	nV/√Hz	max	B
Noninverting Input Current Noise	f > 100kHz	1.7	2.6	2.8	3.0	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.003				%	typ	C
Differential Phase	G = +2, NTSC, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.06				°	typ	C
All Hostile Crosstalk, Input-Referred	3 Channels Driven at 5MHz, $1V_{PP}$ 4th Channel Measured	−61				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, $R_L = 100\Omega$	66	**62**	61	60	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.25	**±0.8**	±1.2	±1.5	mV	max	A
Average Input Offset Voltage Drift	V_{CM} = 0V			8	10	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	−9	**−20**	−22	−26	µA	max	A
Average Input Bias Current Drift	V_{CM} = 0V			30	50	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±100	**±500**	±800	±900	nA	max	A
Inverting Input Bias Current Drift	V_{CM} = 0V			5	5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)(5)		±4.0	**±3.8**	±3.7	±3.6	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V, Input-Referred	85	**76**	75	73	dB	min	A
Input Impedance, Differential Mode	V_{CM} = 0V	18 || 0.8				kΩ ||pF	typ	C
Input Impedance, Common-Mode	V_{CM} = 0V	6 ||1.0				MΩ ||pF	typ	C
OUTPUT								
Output Voltage Swing	$R_L \geq 500\Omega$	±3.7	**±3.5**	±3.45	±3.4	V	min	A
	$R_L = 100\Omega$	±3.6	**±3.5**	±3.45	±3.4	V	min	A
Output Current	V_O = 0	±85	**±70**	±65	±60	mA	min	A
Short-Circuit Output Current	Output Shorted to Ground	±110				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.04				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6.3**	±6.3	±6.3	V	max	A
Minimum Operating Voltage		±2				V	typ	C
Maximum Quiescent Current	$V_S = \pm 5V$	22.6	**23.4**	25	25.8	mA	max	A
Minimum Quiescent Current	$V_S = \pm 5V$	22.6	**21.8**	20.2	19.4	mA	min	A
Power-Supply Rejection Ratio (−PSRR)	Input-Referred	72	**64**	63	62	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IPW		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-14	Junction-to-Ambient	100				°C/W	typ	C
PW TSSOP-14	Junction-to-Ambient	110				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +28°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω to 2.5V, and G = +2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA4820ID, IPW				UNITS	MIN/ MAX	TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, V_O = 0.1V_{PP}, R_F = 25Ω	520				MHz	typ	C
	G = +2, V_O = 0.1V_{PP}	210	148	135	130	MHz	min	B
	G = +10, V_O = 0.1V_{PP}	25	18	17	16	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	230	180	170	160	MHz	min	B
Peaking at a Gain of 1	V_O = 0.1V_{PP}, R_F = 25Ω	2				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	67				MHz	typ	C
Slew Rate	G = +2, V_O = 2V Step	190	135	130	125	V/µs	min	B
Rise Time and Fall Time	G = +2, V_O = 2V Step	1.8				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	25				ns	typ	C
Settling Time to 0.1%	G = +2, V_O = 2V Step	22				ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 200Ω	−79	−75	−74	−73	dBc	max	B
	R_L ≥ 500Ω	−83	−79	−77	−75	dBc	max	B
3rd-Harmonic	R_L = 200Ω	−94	−87	−86	−85	dBc	max	B
	R_L ≥ 500Ω	−98	−95	−93	−92	dBc	max	B
Input Voltage Noise	f > 100kHz	2.5	2.8	2.9	3.0	nV/√Hz	max	B
Noninverting Input Current Noise	f > 100kHz	1.6	2.5	2.7	2.9	pA/√Hz	max	B
All Hostile Crosstalk, Input-Referred	3 Channels Driven at 5MHz, 1V_{PP} 4th Channel Measured	−61				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 2.5V, R_L = 100Ω	65	**60**	59	58	dB	min	A
Input Offset Voltage	V_{CM} = 2.5V	±0.35	**±1.3**	±1.7	±2.0	mV	max	A
Average Input Offset Voltage Drift	V_{CM} = 2.5V			8	10	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	−8	**−18**	−20	−24	µA	max	A
Average Input Bias Current Drift	V_{CM} = 2.5V			30	50	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±100	**±500**	±800	±900	µA	max	A
Inverting Input Bias Current Drift	V_{CM} = 2.5V			5	5	nA/°C	max	B
INPUT								
Least Positive Input Voltage		0.9	**1.1**	1.2	1.3	V	min	A
Most Positive Input Voltage		4.4	**4.1**	4.0	3.9	V	max	A
Common-Mode Rejection Ratio (CMRR)(5)	V_{CM} = 2.5V, Input-Referred	83	**74**	73	72	dB	min	A
Input Impedance, Differential-Mode	V_{CM} = 2.5V	15 ||1				kΩ ||pF	typ	C
Input Impedance, Common-Mode	V_{CM} = 2.5V	5 ||1.3				MΩ ||pF	typ	C
OUTPUT								
Least Positive Output Voltage	R_L ≥ 500Ω to 2.5V	3.9	**3.8**	3.75	3.7	V	min	A
	R_L = 100Ω to 2.5V	3.8	**3.7**	3.65	3.6	V	min	A
Most Negative Output Voltage	R_L ≥ 500Ω to 2.5V	1.2	**1.3**	1.35	1.4	V	min	A
	R_L = 100Ω to 2.5V	1.2	**1.3**	1.35	1.4	V	min	A
Output Current	V_O = 2.5V	±75	**±60**	±55	±50	mA	min	A
Short-Circuit Output Current	Output Shorted to Ground	±105				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.04				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		+5				V	typ	C
Maximum Operating Voltage			**+12.6**	+12.6	+12.6	V	max	A
Minimum Operating Voltage		+4				V	typ	C
Maximum Quiescent Current	V_S = +5V, 4 Channels	20.4	**22.2**	22.6	23.0	mA	max	A
Minimum Quiescent Current	V_S = +5V, 4 Channels	20.4	**18.0**	17.4	16.8	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	68				dB	typ	C
THERMAL CHARACTERISTICS								
Specification: ID, IPW		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-14	Junction-to-Ambient	100				°C/W	typ	C
PW TSSOP-14	Junction-to-Ambient	110				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +13°C at high temperature limit for over temperature.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

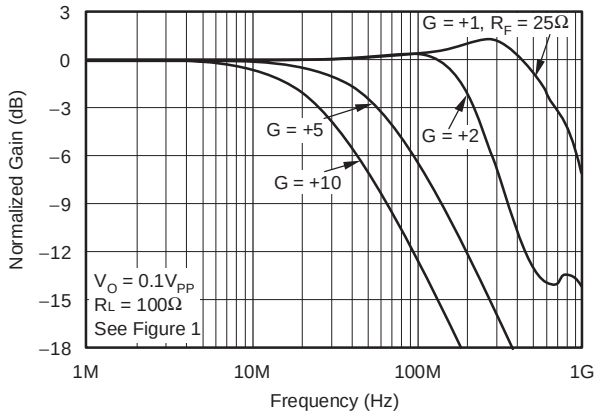
(4) Current considered positive out of pin.

(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

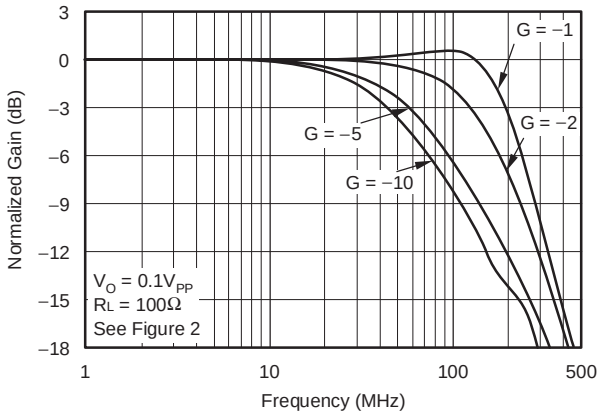
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

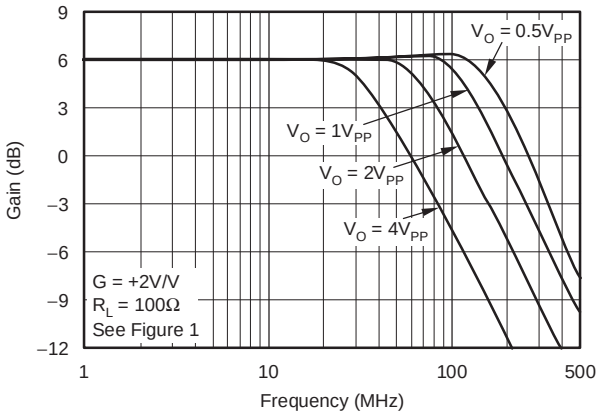
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



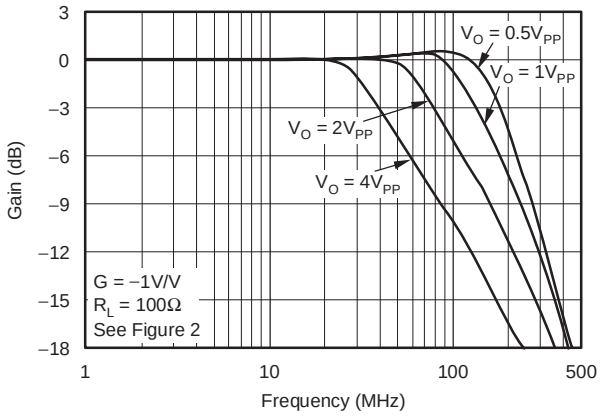
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



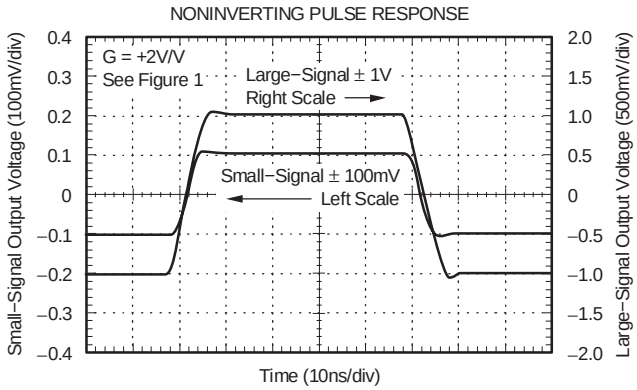
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



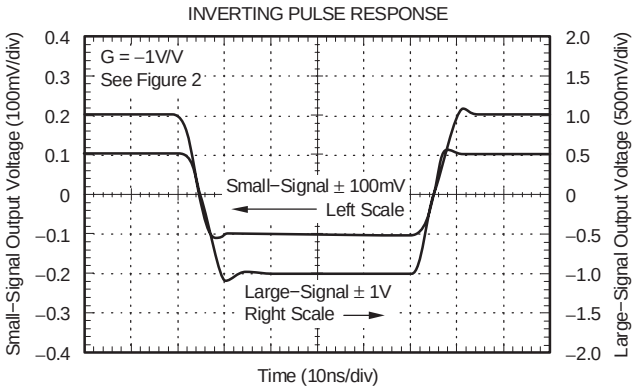
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



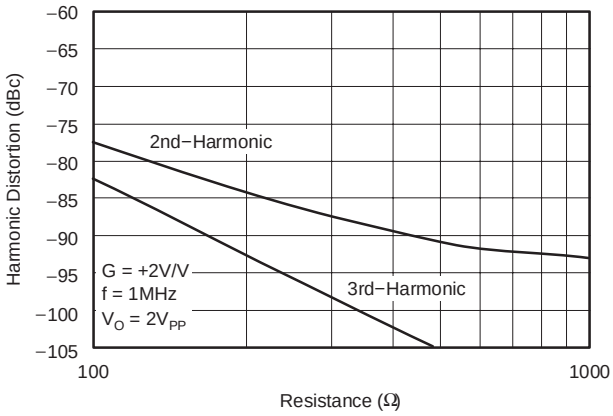
INVERTING PULSE RESPONSE



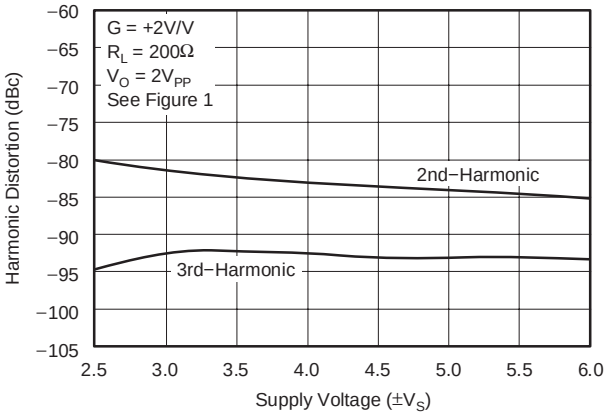
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

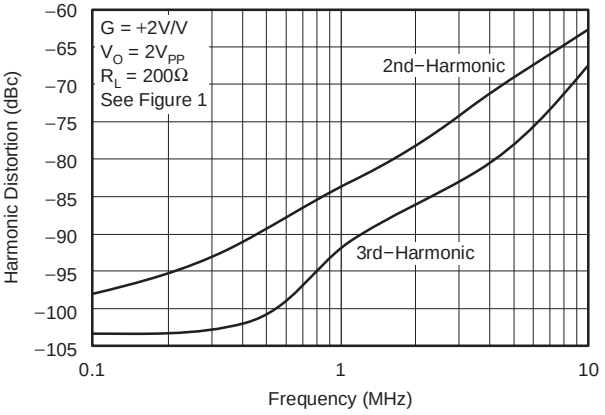
HARMONIC DISTORTION vs LOAD RESISTANCE



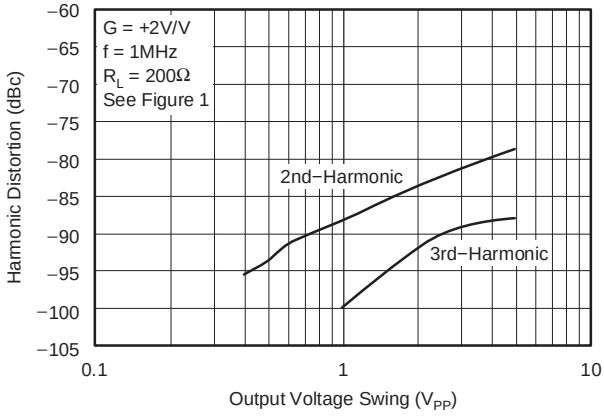
1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



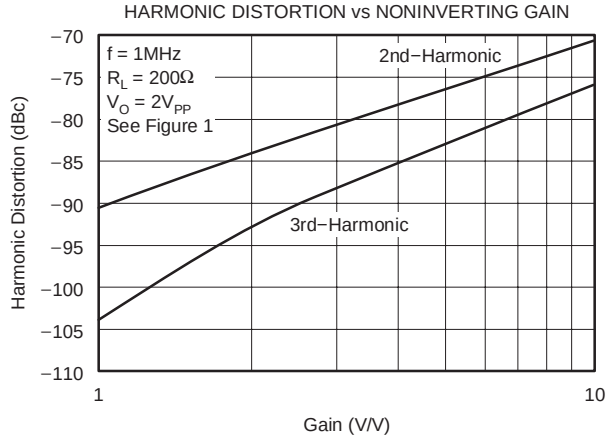
HARMONIC DISTORTION vs FREQUENCY



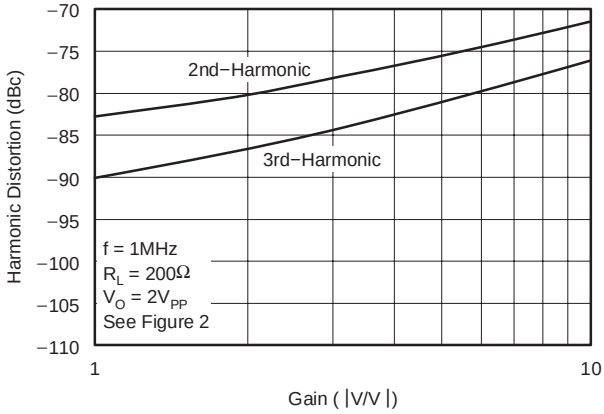
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



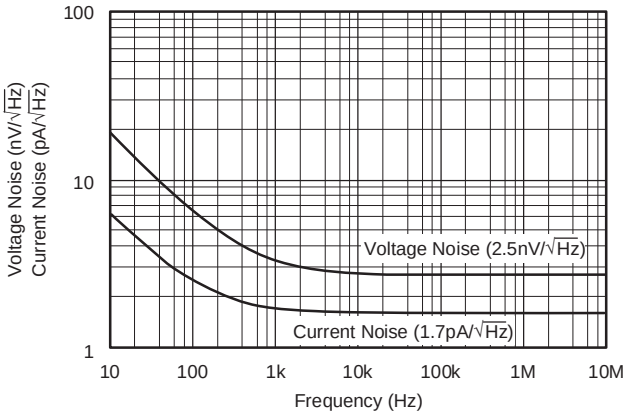
HARMONIC DISTORTION vs INVERTING GAIN



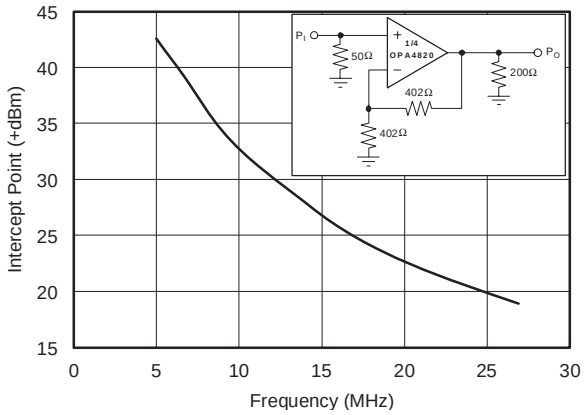
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

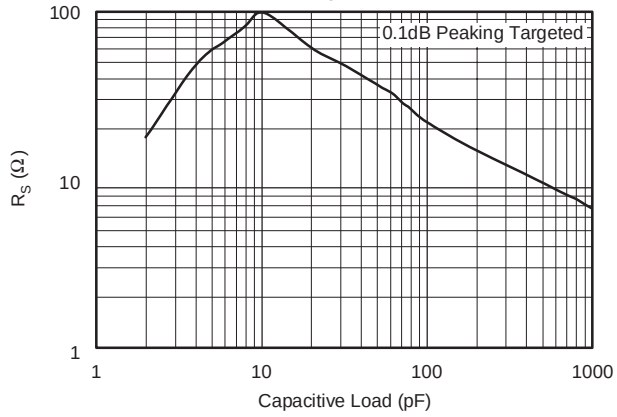
INPUT VOLTAGE AND CURRENT NOISE



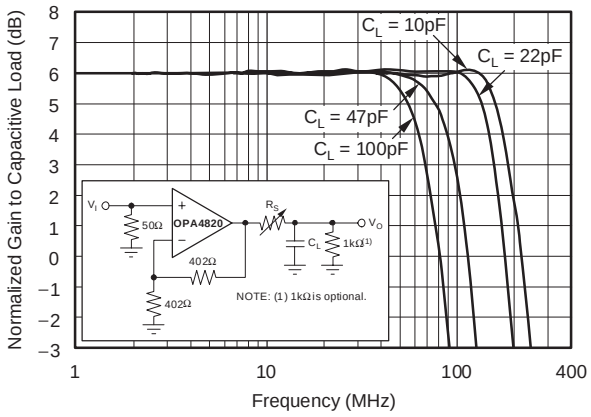
TWO−TONE, 3RD−ORDER
INTERMODULATION INTERCEPT



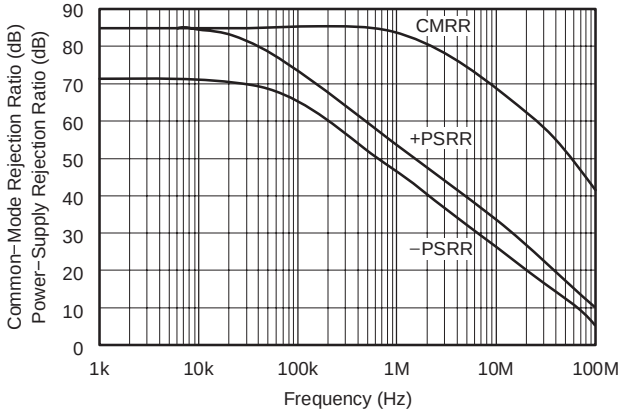
RECOMMENDED R_S vs CAPACITIVE LOAD



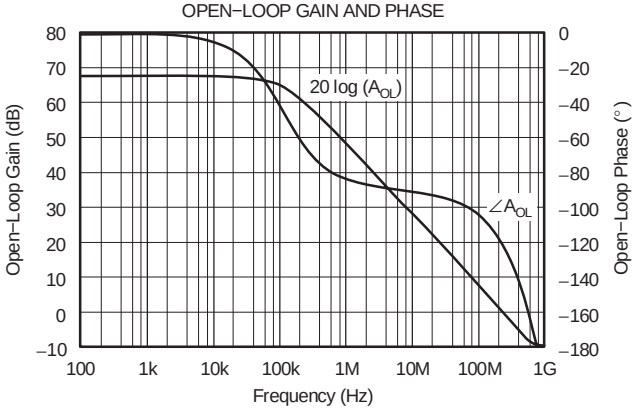
FREQUENCY RESPONSE vs CAPACITIVE LOAD



CMRR AND PSRR vs FREQUENCY



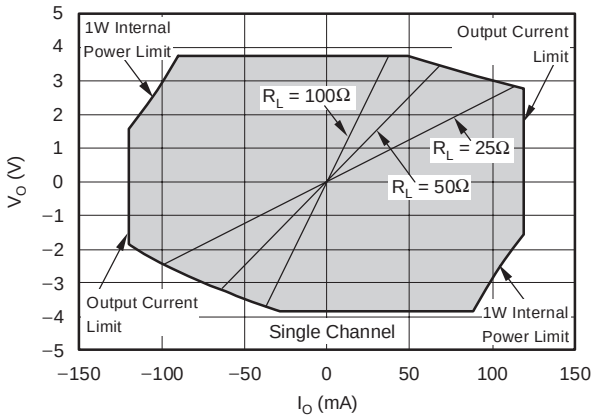
OPEN−LOOP GAIN AND PHASE



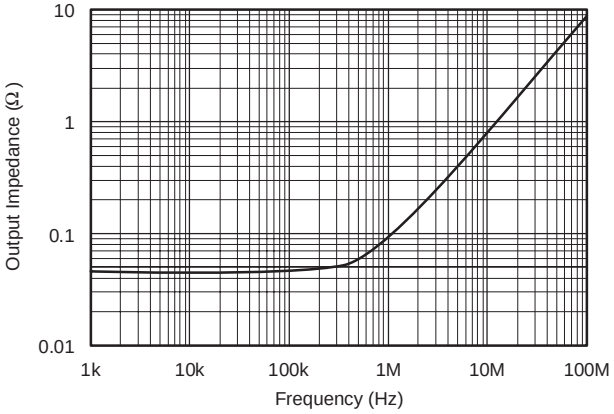
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted.

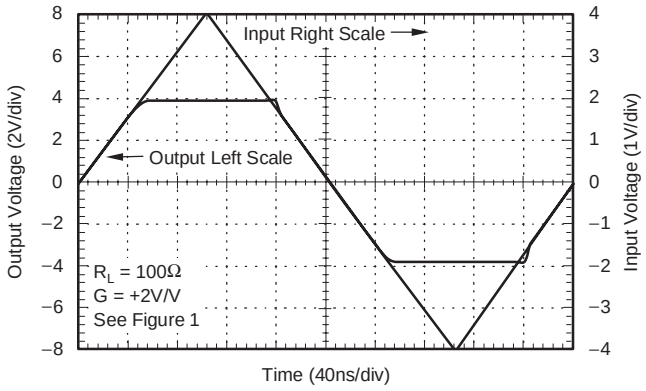
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



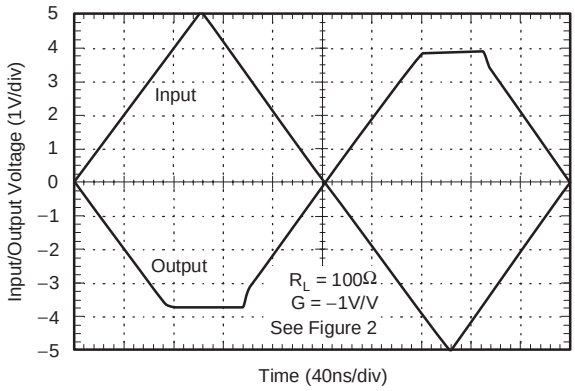
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



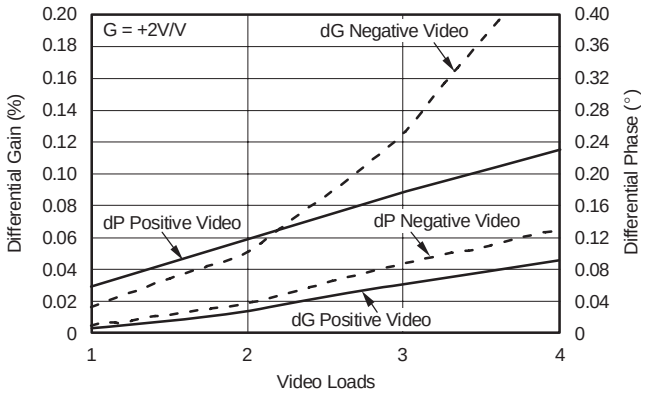
NONINVERTING OVERDRIVE RECOVERY



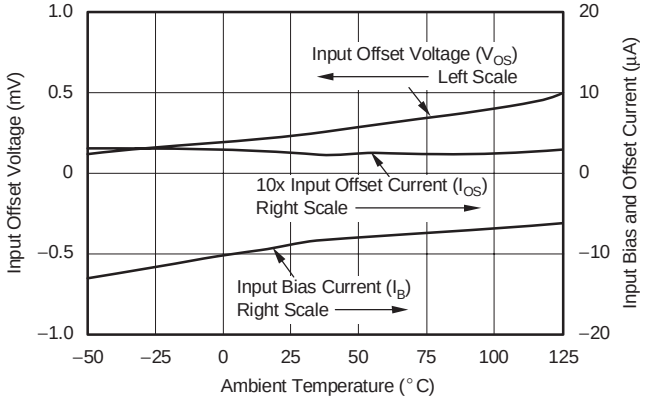
INVERTING OVERDRIVE RECOVERY



COMPOSITE VIDEO dG/dP



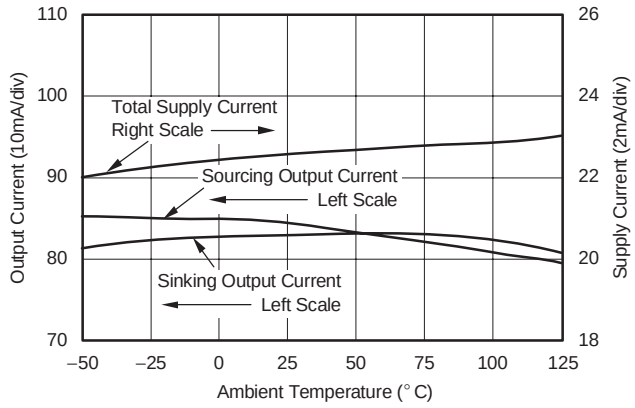
TYPICAL DC DRIFT OVER TEMPERATURE



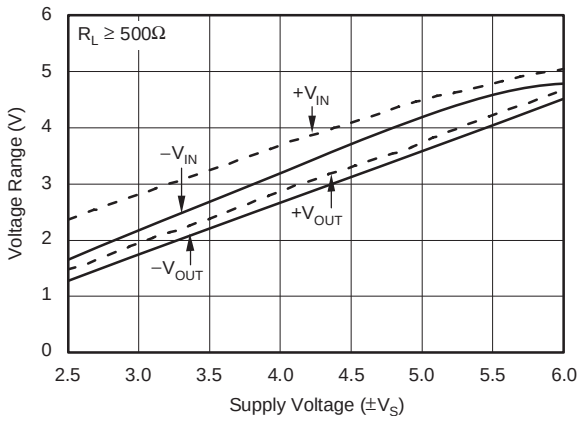
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted.

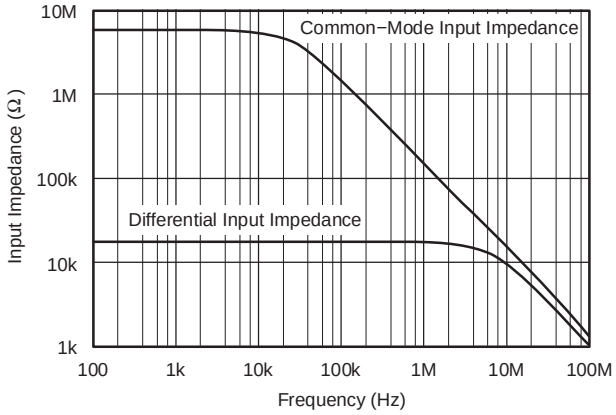
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



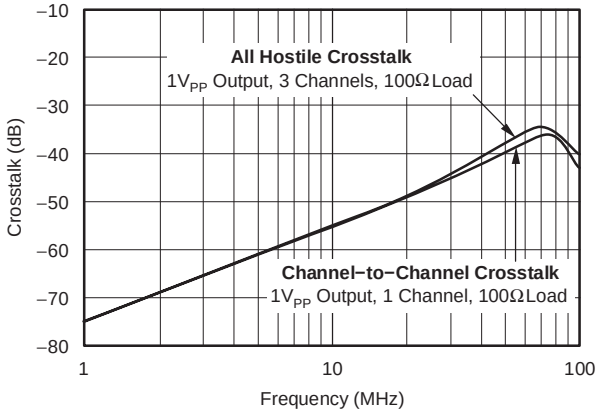
COMMON−MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



COMMON−MODE AND DIFFERENTIAL INPUT IMPEDANCE



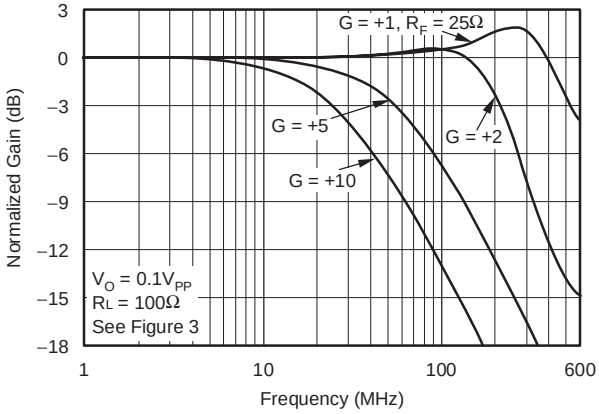
CROSSTALK vs FREQUENCY



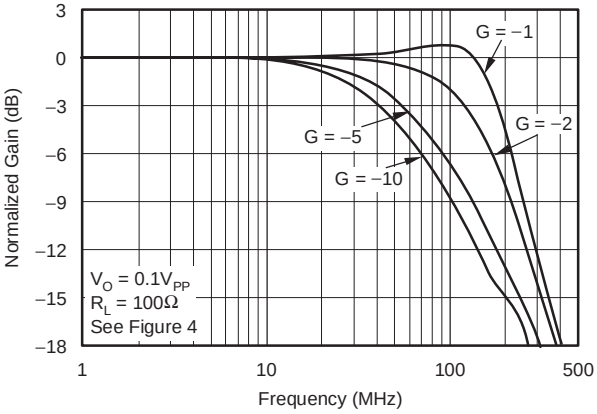
TYPICAL CHARACTERISTICS: V_S = +5V

R_F = 402Ω, R_L = 100Ω to V_S/2, and G = +2, unless otherwise noted.

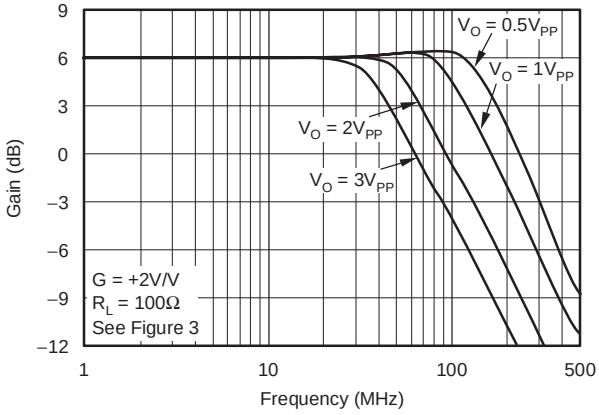
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



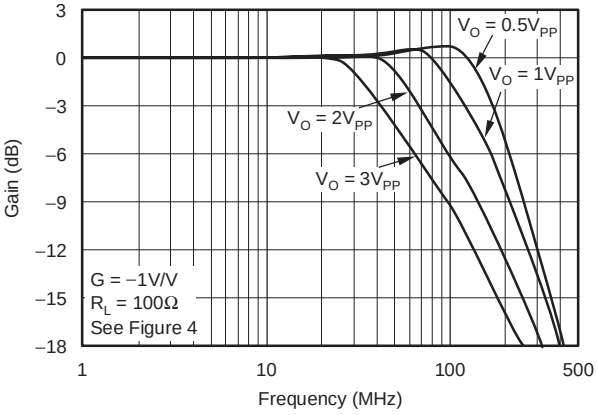
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



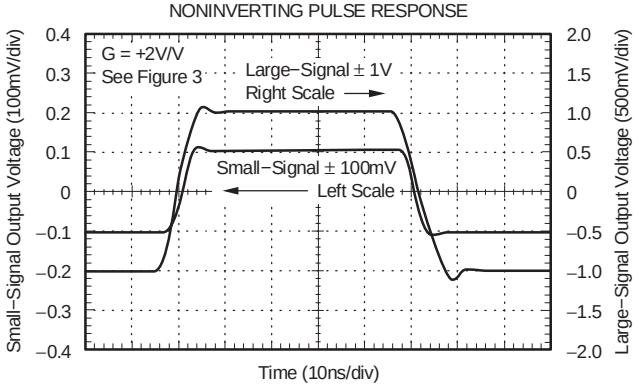
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



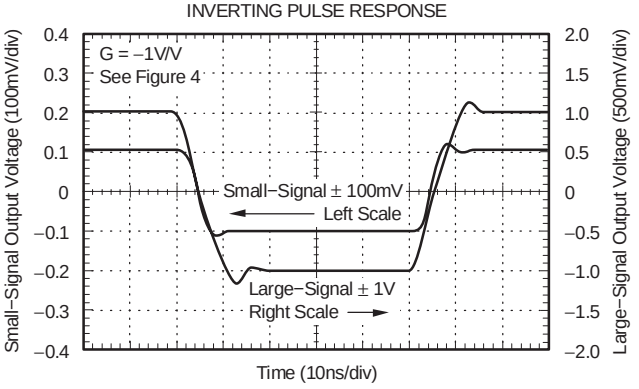
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



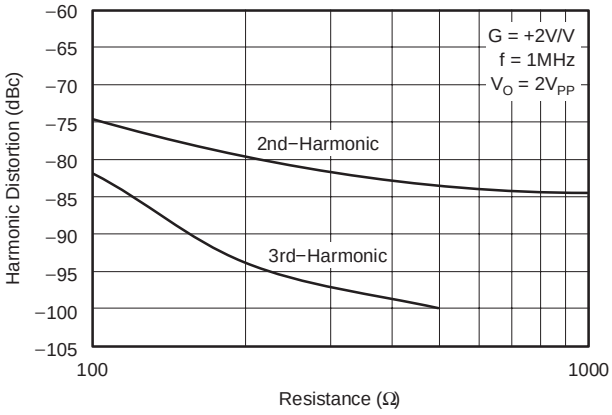
INVERTING PULSE RESPONSE



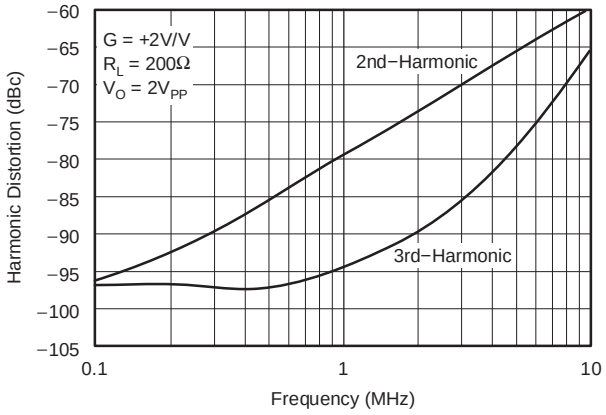
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

R_F = 402Ω, R_L = 100Ω to V_S/2, and G = +2, unless otherwise noted.

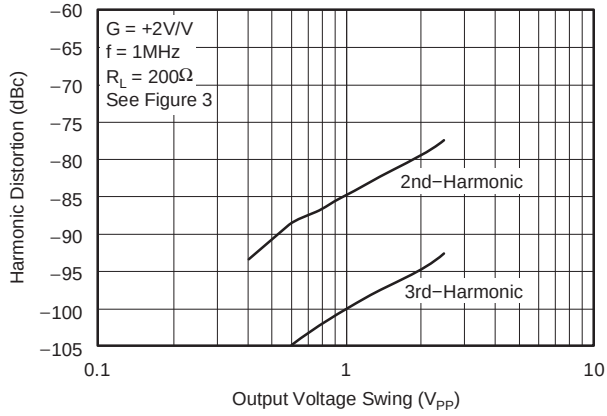
HARMONIC DISTORTION vs LOAD RESISTANCE



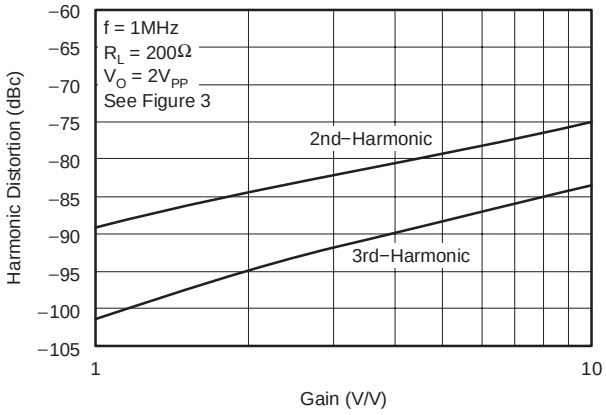
HARMONIC DISTORTION vs FREQUENCY



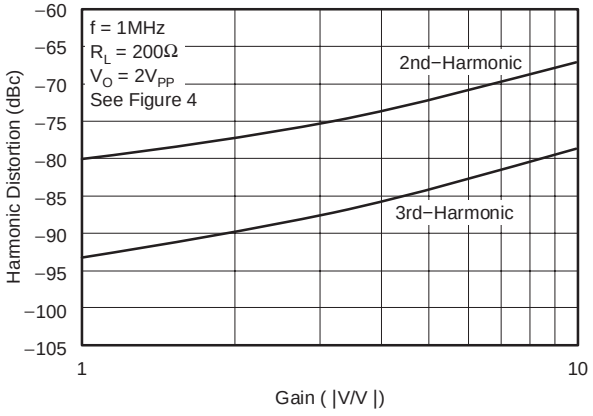
HARMONIC DISTORTION vs OUTPUT VOLTAGE



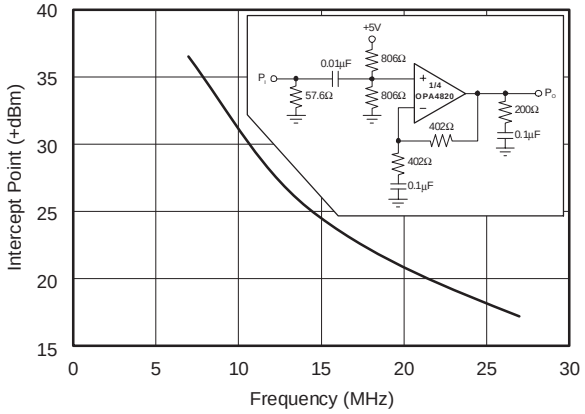
HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN



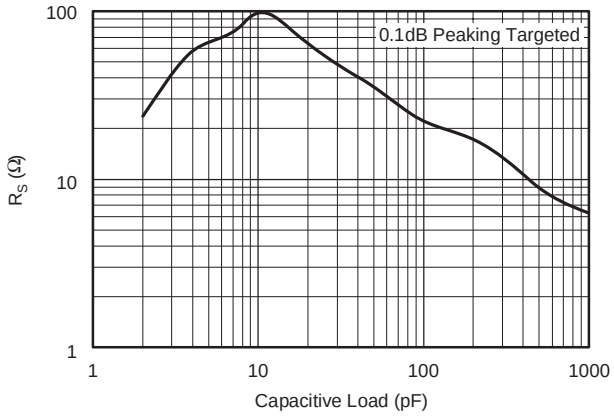
TWO−TONE, 3RD−ORDER
INTERMODULATION INTERCEPT



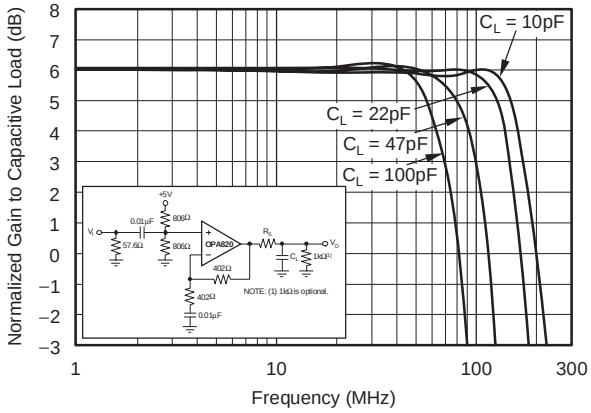
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

R_F = 402Ω, R_L = 100Ω to V_S/2, and G = +2, unless otherwise noted.

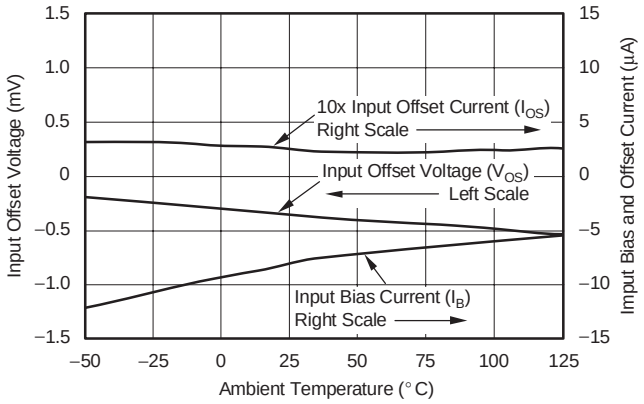
RECOMMENDED R_S vs CAPACITIVE LOAD



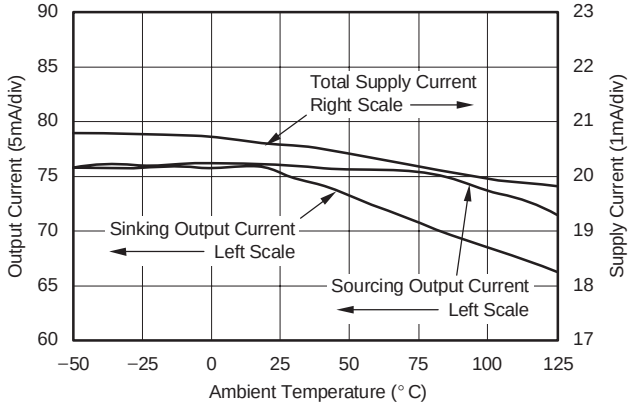
FREQUENCY RESPONSE vs CAPACITIVE LOAD



TYPICAL DC DRIFT OVER TEMPERATURE



SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The combination of speed and dynamic range offered by the OPA4820 is easily achieved in a wide variety of application circuits, providing that simple principles of good design are observed. For example, good power-supply decoupling, as shown in Figure 1, is essential to achieve the lowest possible harmonic distortion and smooth frequency response.

Proper printed circuit board (PCB) layout and careful component selection will maximize the performance of the OPA4820 in all applications, as discussed in the following sections of this data sheet.

Figure 1 shows the gain of +2 configuration used as the basis for most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance and with measurement equipment presenting 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swings at the output pin (V_O in Figure 1). The 100Ω load, combined with the 804Ω total feedback network load, presents the OPA4820 with an effective load of approximately 90Ω in Figure 1.

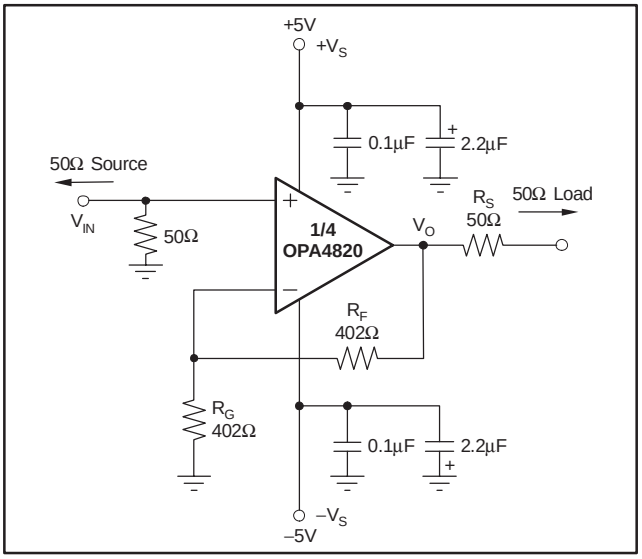


Figure 1. Gain of +2, High-Frequency Application and Characterization Circuit

WIDEBAND INVERTING OPERATION

Operating the OPA4820 as an inverting amplifier has several benefits and is particularly useful when a matched 50Ω source and input impedance is required. Figure 2 shows the inverting gain of −1 circuit used as the basis of the inverting mode Typical Characteristics.

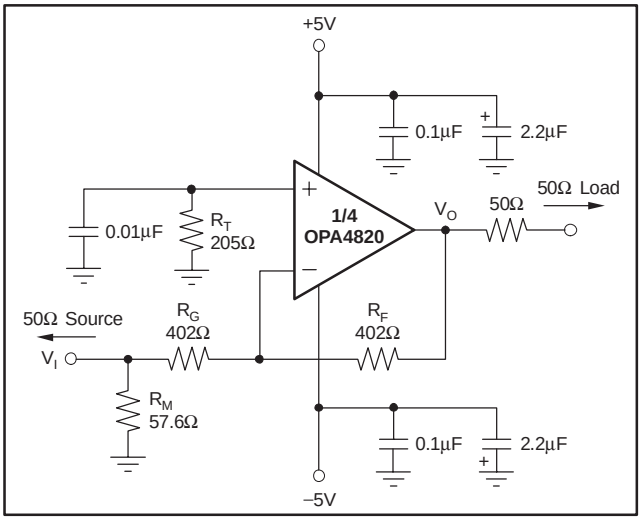


Figure 2. Inverting G = −1 Specifications and Test Circuit

In the inverting case, just the feedback resistor appears as part of the total output load in parallel with the actual load. For the 100Ω load used in the Typical Characteristics, this gives a total load of 80Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case 402Ω for a gain of −1) while an additional input matching resistor (R_M) can be used to set the total input impedance equal to the source if desired. In this case, R_M = 57.6Ω in parallel with the 402Ω gain setting resistor gives a matched input impedance of 50Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 2.

The OPA4820 offers extremely good DC accuracy as well as low noise and distortion. To take full advantage of that DC precision, the total DC impedance looking out of each of the input nodes must be matched to get bias current cancellation. For the circuit of Figure 2, this requires the 205Ω resistor shown to ground on the noninverting input. The calculation for this resistor includes a DC-coupled 50Ω source impedance along with R_G and R_M. Although this resistor will provide cancellation for the bias current, it must be well decoupled (0.01µF in Figure 2) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 2 will far exceed the bandwidth at that same gain magnitude for the noninverting circuit of Figure 1. This occurs due to the lower *noise gain* for the circuit of Figure 2 when the 50Ω source impedance is included in the analysis. For instance, at a signal gain of −10 (R_G = 50Ω, R_M = open, R_F = 499Ω) the noise gain for the circuit of Figure 2 will be 1 + 499Ω/(50Ω + 50Ω) = 6 as a result of adding the 50Ω source in the noise gain equation. This gives considerable higher bandwidth than the noninverting gain of +10. Using the 240MHz gain bandwidth product for the OPA4820, an inverting gain of −10 from a 50Ω source to a 50Ω R_G gives 42MHz bandwidth, whereas the noninverting gain of +10 gives 27MHz.

WIDEBAND SINGLE-SUPPLY OPERATION

Figure 3 shows the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis for the +5V only Electrical and Typical Characteristics. The key requirement for single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 0.9V of the negative supply and 0.6V of the positive supply, giving a $3.5V_{PP}$ input signal range. The input impedance matching resistor (57.6Ω) used in Figure 3 is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1. This puts the input DC bias voltage (2.5V) on the output as well. On a single +5V supply, the output voltage can swing to within 1.3V of either supply pin while delivering more than 60mA output current giving 2.4V output swing into 100Ω (5.6dBm maximum at a matched 50Ω load).

Figure 4 shows the AC-coupled, single +5V supply, gain of −1V/V circuit configuration used as a basis for the +5V only Typical Characteristic curves. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.01µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC blocked by the input capacitor, will also appear at the output pin.

The single-supply test circuits of Figure 3 and Figure 4 show +5V operation. These same circuits can be used over a single-supply range of +4V to +12.6V. Operating on a single +12V supply, with the Absolute Maximum Supply voltage specification of +13V, gives adequate design margin for the typical ±5% supply tolerance.

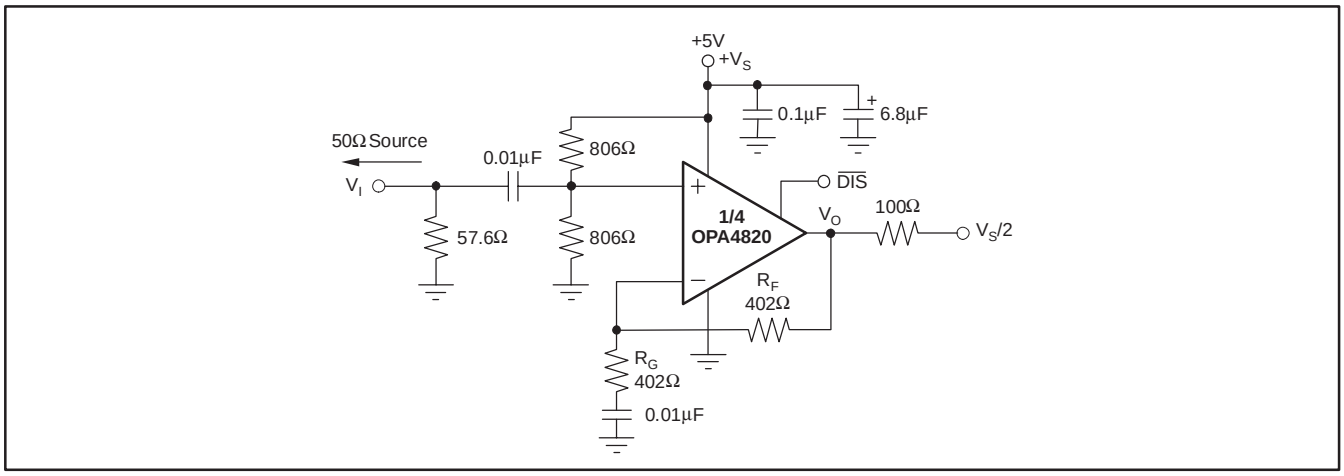


Figure 3. AC-Coupled, G = +2V/V, Single-Supply Specifications and Test Circuit

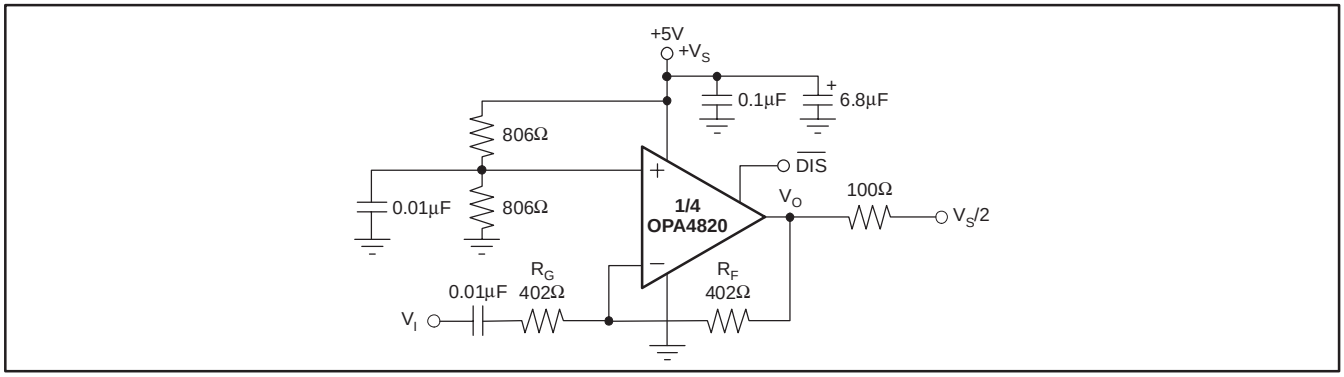


Figure 4. AC-Coupled, G = −1V/V, Single-Supply Specifications and Test Circuit

DIFFERENTIAL INTERFACE APPLICATIONS

Dual and quad op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either ADC input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA4820. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting differential I/O applications.

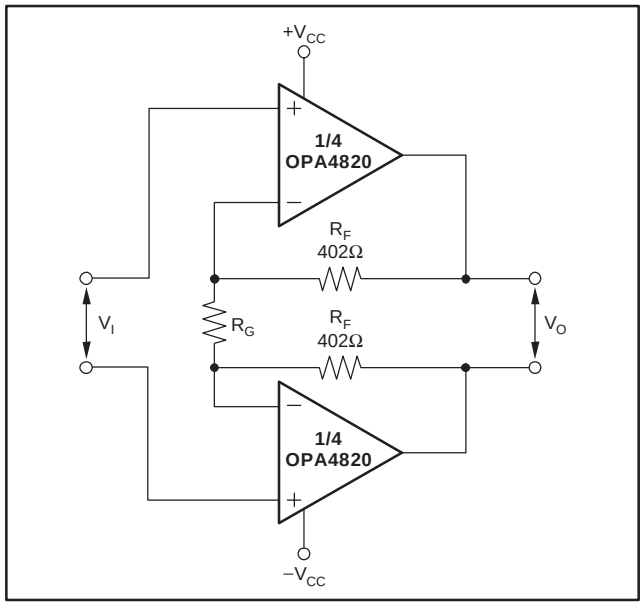


Figure 5. Noninverting Differential I/O Amplifier

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the amplifier gain. The differential signal gain for the circuit of Figure 5 is:

$$\frac{V_O}{V_I} = A_D = 1 + 2 \times \frac{R_F}{R_G} \qquad (1)$$

Figure 5 shows the recommended value of 402Ω. However, the gain may be adjusted using just the R_G resistor.

Various combinations of single-supply or AC-coupled gains can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through R_G, giving that voltage a common-mode gain of 1 to the output.

Figure 6 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become the input resistance for the source. This provides a better noise performance than the noninverting configuration, but does limit the flexibility in setting the input impedance separately from the gain.

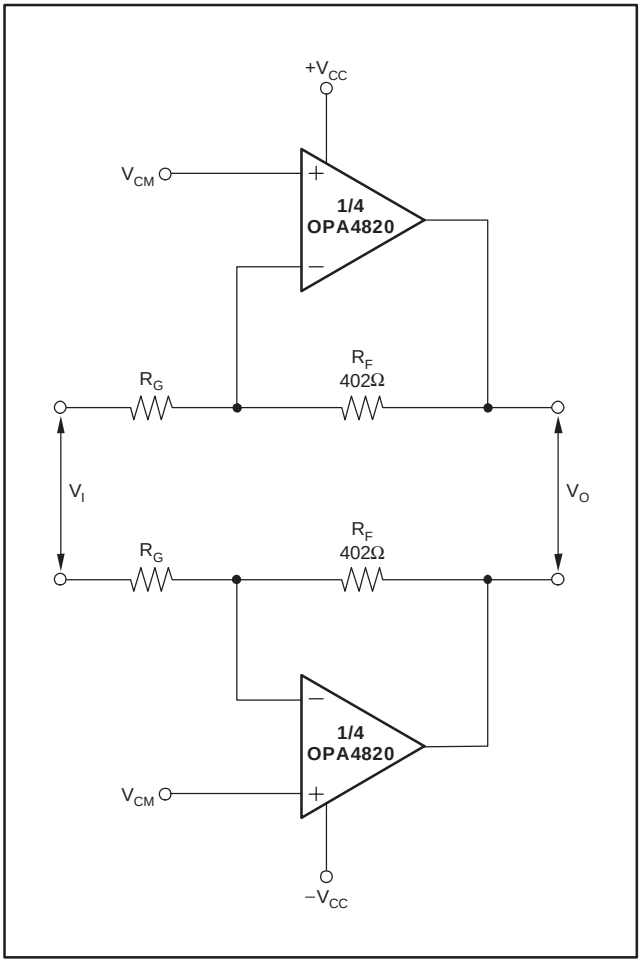


Figure 6. Inverting Differential I/O Amplifier

The two noninverting inputs provide an easy common-mode control input. This is particularly useful if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving an easy common-mode control for single-supply operation. The input resistors may be adjusted to the desired gain but will also be changing the input impedance as well. The differential gain for this circuit is:

$$\frac{V_O}{V_I} = -\frac{R_F}{R_G} \qquad (2)$$

DC-COUPLED SINGLE-TO-DIFFERENTIAL CONVERSION

The previous differential output circuits were set up to receive a differential input as well as provide a differential output. Figure 7 shows one way to provide a single to differential conversion, with DC coupling, and independent output common-mode control using a quad op amp.

The circuit of Figure 7 provides several useful features for isolating the input signal from the final outputs. Using the first amplifier as a simple noninverting stage gives an independent adjustment on R_I (to set the source loading) while the gain can be easily adjusting in this stage using the R_G resistor. The next stage allows a separate output common-mode level to be set up. The desired output common-mode voltage, V_{CM}, is cut in half and applied to the noninverting input of the 2nd stage. The signal path in this stage sees a gain of −1 while this ($1/2 \times V_{CM}$) voltage sees a gain of +2. The output of this 2nd stage is then the original common-mode voltage plus the inverted signal from the output of the first stage. The 2nd stage output appears directly at the output of the noninverting final stage. The inverting node of the inverting output stage is also biased to the common-mode voltage, equal to the common-mode voltage appearing at the output of the 2nd stage, creating no current flow and placing the desired V_{CM} at the output of this stage as well. Both the positive and negative output are shown in Figure 8.

LOW-POWER, DIFFERENTIAL I/O, 4th-ORDER ACTIVE FILTER

The OPA4820 can give a very capable gain block for active filters. The quad design lends itself very well to differential active filters. Where the filter topology is looking for a simple gain function to implement the filter, the noninverting configuration is preferred to isolate the filter elements from the gain elements in the design. Figure 9 shows an example of a 10MHz, 4th-order Butterworth, low-pass Sallen-Key filter. The design places the higher Q stage first to allow the lower Q 2nd stage to roll off the peaked noise of the first stage. The resistor values have been adjusted slightly to account for the amplifier group delay.

While this circuit is bipolar, using ±5V supplies, it can easily be adapted to single-supply operation. This will add two real zeroes in the response, transforming this circuit into a bandpass. The frequency response for the filter of Figure 9 is shown in Figure 10.

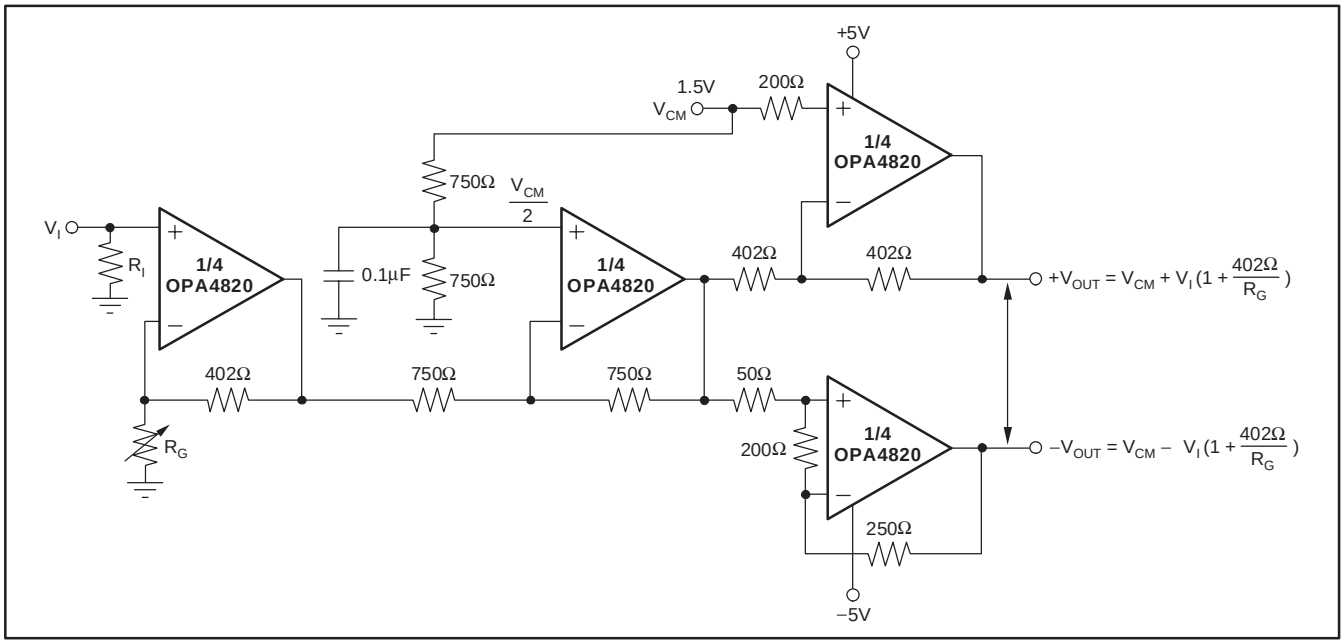


Figure 7. Precision, DC-Coupled, Single-to-Differential Conversion

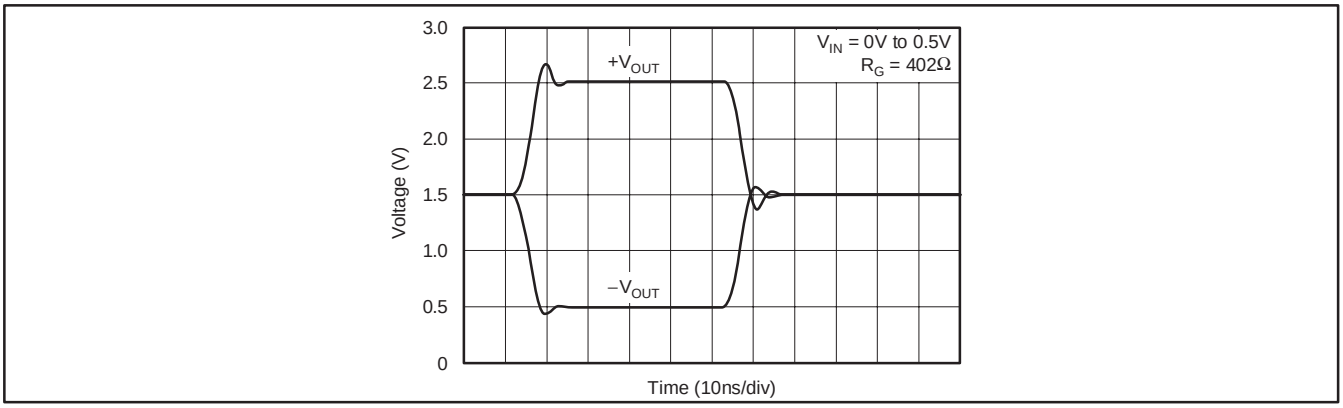


Figure 8. Pulse Response for Figure 7 Schematic

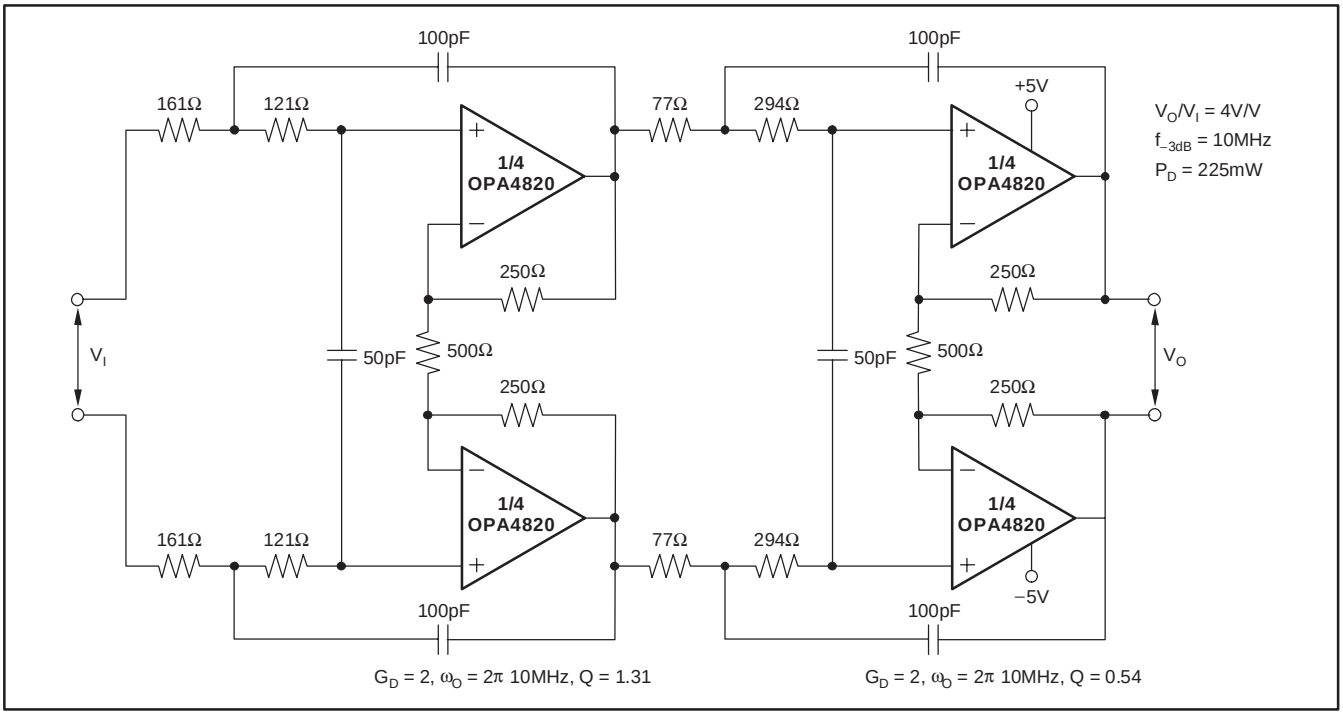


Figure 9. Low-Power, Differential I/O, 4th-Order Butterworth Active Filter

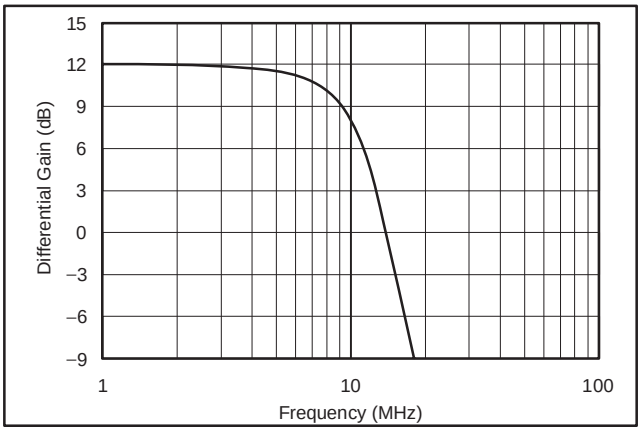


Figure 10. Differential 4th-Order, 10MHz Butterworth Filter

LOW-POWER xDSL TRANSCEIVER INTERFACE

With four amplifiers available, the quad OPA4820 can meet the needs for both differential driver and receiver in a low-power xDSL line interface design. A simplified design example is shown on the front page. Two amplifiers are used as a noninverting differential driver while the other two implement the driver echo cancellation and receiver amplifier function. This example shows a single +12V design where the drive side is taking a $2V_{PP}$ maximum input from the transmit filter and providing a differential gain of 7, giving a maximum $14V_{PP}$ differential output swing. This is coupled through 50Ω matching resistors and a 1:1 transformer to give a maximum $7V_{PP}$ on a 100Ω line. This $7V_{PP}$ corresponds to a 10dBm line power with a 3.5 crest factor.

The differential receiver is configured as an inverting summing stage where the outputs of the driver are cancelled prior to appearing at the output of the receive amplifiers. This is done by summing the output voltages for the drive amplifiers and their attenuated and inverted levels (at the transformer input) into the inverting inputs of each receiver amplifier. The resistor values are set (see the circuit on the front page) to give perfect drive signal cancellation if the drive signal is attenuated by 1/2, going from the drive amplifier outputs to the transformer input. The signal received through the transformer has a gain of 1 through the receive amplifiers. Higher gain could easily be provided by scaling the resistors summing into the inverting inputs of the receiver amplifiers down while keeping the same ratio between them.

DUAL-CHANNEL, DIFFERENTIAL ADC DRIVER

Where a low-noise, single-supply, interface to a differential input +5V ADC is required, the circuit of Figure 11 can provide a high dynamic range, medium gain interface for dual high-performance ADCs. The circuit of Figure 11 uses two amplifiers in the differential inverting configuration. The common-mode voltage is set on the noninverting inputs to the supply midscale. In this example, the input signal is coupled in through a 1:2 transformer. This provides both signal gain, single to differential conversion, and a reduction in noise figure. To show a 50Ω input impedance at the input to the transformer, two 200Ω resistors are required on the transformer secondary. These two resistors are also the amplifier gain elements. Since the same DC voltage appears on both inverting nodes in the circuit of Figure 11, no DC current will flow through the transformer, giving a DC gain of 1 to the output for this common-mode voltage, V_{CM}.

The circuit of Figure 11 is particularly suitable for a moderate resolution dual ADC used as I/Q samplers. The optional 500Ω resistors to ground on each amplifier output can be added to improve the 2nd- and 3rd-harmonic distortion by > 15dB if higher dynamic range is required. The 5mA added output stage current significantly improves linearity if that is required. The measured 2nd-harmonic distortion is consistently lower than the 3rd-harmonics for this balanced differential design. It is particularly helpful for this low-power design if there are no grounds in the signal path after the low-level signal at the transformer input. The two pull-down resistors do show a signal path ground and should be connected at the same physical point to ground, in order to eliminate imbalanced ground return currents from degrading 2nd-harmonic distortion.

VIDEO LINE DRIVING

Most video distribution systems are designed with 75Ω series resistors to drive a matched 75Ω cable. In order to deliver a net gain of 1 to the 75Ω matched load, the amplifier is typically set up for a voltage gain of +2, compensating for the 6dB attenuation of the voltage divider formed by the series and shunt 75Ω resistors at either end of the cable.

The circuit of Figure 1 applies to this requirement if all references to 50Ω resistors are replaced by 75Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional DC loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 1 to be reduced from 402Ω to 335Ω. In either case, both the gain flatness and the differential gain/phase performance of the OPA4820 will provide exceptional results in video distribution applications. Differential gain and phase measure the change in overall small-signal gain and phase for the color sub-carrier frequency (3.58MHz in NTSC systems) versus changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA4820, with the typical 150Ω load of a single matched video cable, shows less than 0.003%/0.06° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance would be observed for multiple video signals (see Figure 12).

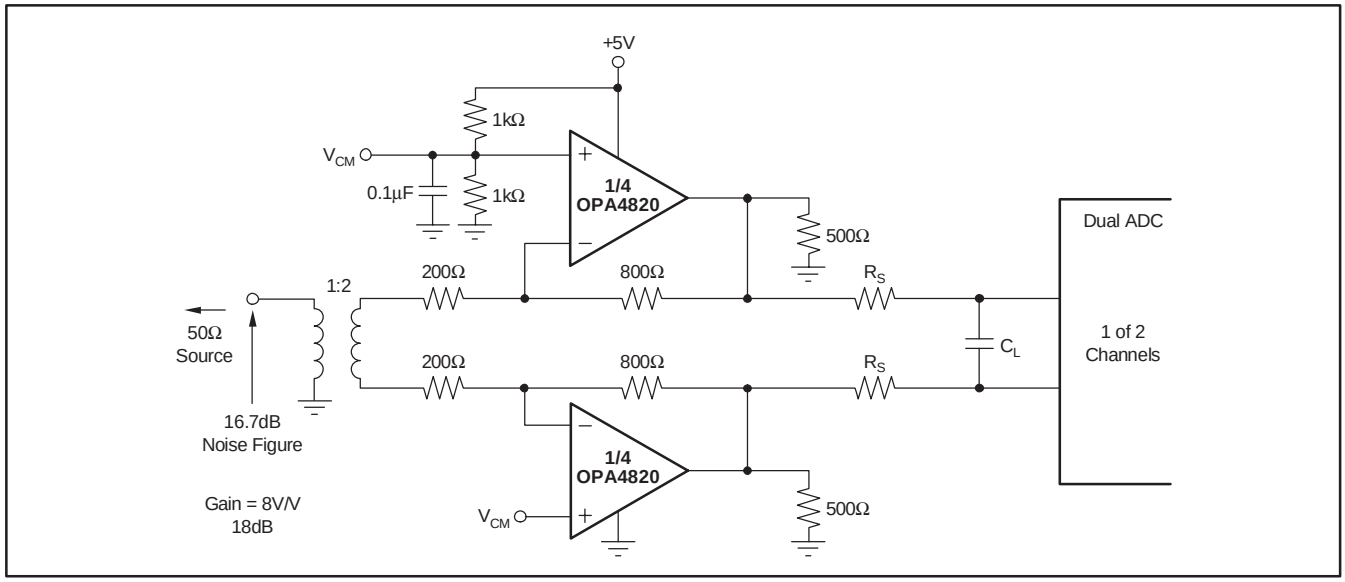


Figure 11. Single-Supply Differential ADC Driver (1 of 2 channels)

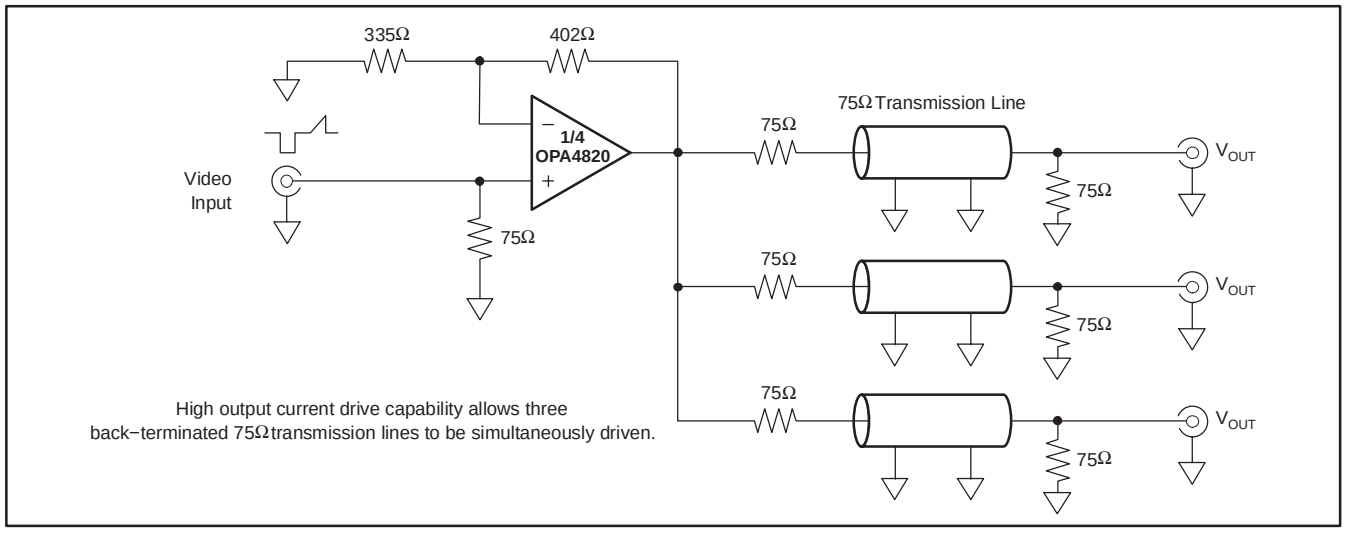


Figure 12. Video Distribution Amplifier

SINGLE OP AMP DIFFERENTIAL AMPLIFIER

The voltage-feedback architecture of the OPA4820, with its high common-mode rejection ratio (CMRR), will provide exceptional performance in differential amplifier configurations. Figure 13 shows a typical configuration. The starting point for this design is the selection of the R_F value in the range of 200Ω to 2kΩ. Lower values reduce the required R_G, increasing the load on the V_2 source and on the OPA4820 output. Higher values increase output noise as well as the effects of parasitic board and device capacitances. Following the selection of R_F, R_G must be set to achieve the desired inverting gain for V_2. Remember that the bandwidth will be set approximately by the gain bandwidth product (GBP) divided by the noise gain ($1 + R_F/R_G$). For accurate differential operation (that is, good CMRR), the ratio R_2/R_1 must be set equal to R_F/R_G.

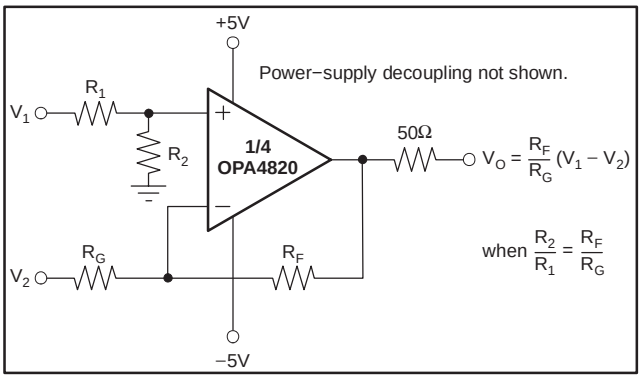


Figure 13. High-Speed, Single Differential Amplifier

Usually, it is best to set the absolute values of R_2 and R_1 equal to R_F and R_G, respectively; this equalizes the divider resistances and cancels the effect of input bias currents. However, it is sometimes useful to scale the values of R_2 and R_1 in order to adjust the loading on the driving source, V_1. In most cases, the achievable low-frequency CMRR will be limited by the accuracy of the resistor values. The 85dB CMRR of the OPA4820 itself will not determine the overall circuit CMRR unless the resistor ratios are matched to better than 0.003%. If it is necessary to trim the CMRR, then R_2 is the suggested adjustment point.

4-CHANNEL DAC TRANSIMPEDANCE AMPLIFIER

High-frequency Digital-to-Analog Converters (DACs) require a low-distortion output amplifier to retain their SFDR performance into real-world loads. See Figure 14 for a single-ended output drive implementation. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground-summing junction of the OPA4820, which is set up as a transimpedance stage or *I-V converter*. The unused current output of the DAC is connected to ground. If the DAC requires its outputs to be terminated to a compliance voltage other than ground for operation, then the appropriate voltage level may be applied to the noninverting input of the OPA4820.

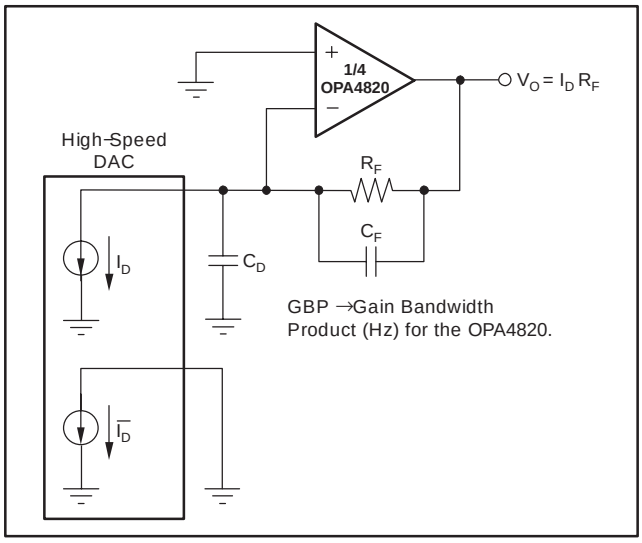


Figure 14. Wideband, Low-Distortion DAC Transimpedance Amplifier

The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D) will produce a zero in the noise gain for the OPA4820 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise-gain peaking. To achieve a flat transimpedance frequency response, this pole in the feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (3)$$

which will give a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \quad (4)$$

ACTIVE FILTERS

Most active filter topologies will have exceptional performance using the broad bandwidth and unity-gain stability of the OPA4820. Topologies employing capacitive feedback require a unity-gain stable, voltage-feedback op amp. Sallen-Key filters simply use the op amp as a noninverting gain stage inside an RC network. Either current- or voltage-feedback op amps may be used in Sallen-Key implementations.

Figure 15 shows an example Sallen-Key low-pass filter, in which the OPA4820 is set up to deliver a low-frequency gain of +2. The filter component values have been selected to achieve a maximally-flat Butterworth response with a 5MHz, −3dB bandwidth. The resistor values have been slightly adjusted to compensate for the effects of the 240MHz bandwidth provided by the OPA4820 in this configuration. This filter may be combined with the ADC driver suggestions to provide moderate (2-pole) Nyquist filtering, limiting noise, and out-of-band harmonics into the input of an ADC. This filter will deliver the exceptionally low harmonic distortion required by high SFDR ADCs such as the ADS850 (14-bit, 10MSPS, 82dB SFDR).

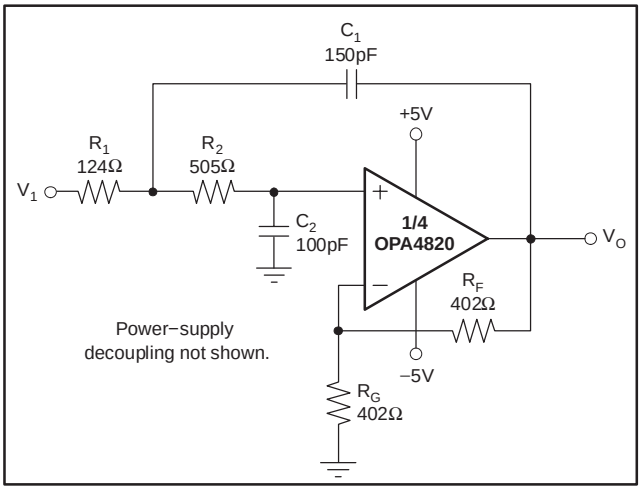


Figure 15. 5MHz Butterworth Low-Pass Active Filter

Another type of filter, a high-Q bandpass filter, is shown in Figure 16. The transfer function for this filter is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{s\frac{R_3+R_4}{R_1R_4C_1}}{s^2 + s\frac{1}{R_1C_1} + \frac{R_3}{R_2R_4R_5C_1C_2}} \quad (5)$$

with $$\omega_O{}^2 = \frac{R_3}{R_2R_4R_5C_1C_2} \quad (6)$$

and $$\frac{\omega_O}{Q} = \frac{1}{R_1C_1} \quad (7)$$

For the values chosen in Figure 16:

$$f_O = \frac{\omega_O}{2\pi} \simeq 1\text{MHz} \quad (8)$$

and Q = 100

See Figure 17 for the frequency response of the filter shown in Figure 16.

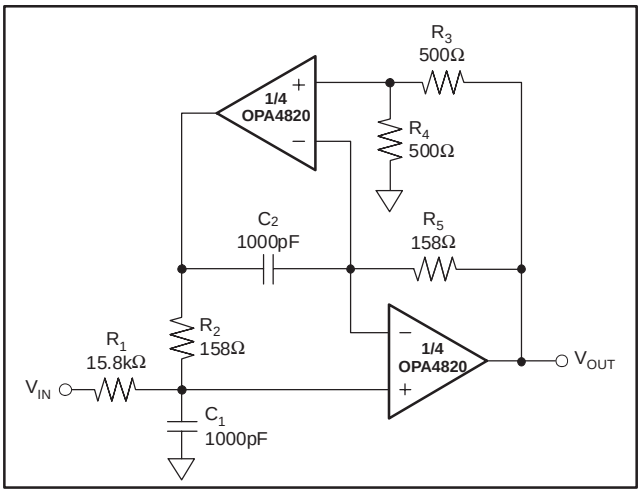


Figure 16. High-Q 1MHz Bandpass Filter

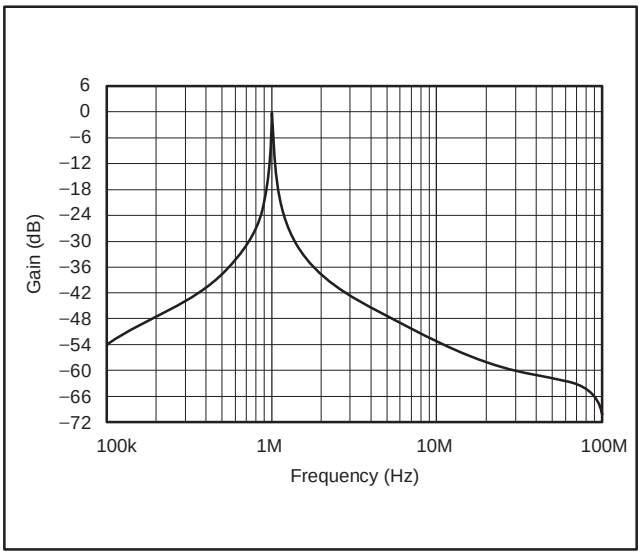


Figure 17. High-Q 1MHz Bandpass Filter Frequency Response

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA4820 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in the table below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA4820ID	SO-14	DEM-OPA-SO-4A	SBOU016
OPA4820IPW	TSSOP-14	DEM-OPA-TSSOP-4A	SBOU017

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA4820 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA4820 and its circuit designs. This is particularly true for video and R_F amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA4820 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small-signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA4820 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain-setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. Usually, the feedback resistor value should be between 200Ω and 1kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA4820. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response. A 25Ω feedback resistor is suggested for A_V = +1V/V.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 1) to be less than about 200Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward

response. Assuming a 2pF total parasitic on the inverting node, holding R_F || R_G < 200Ω will keep this pole above 400MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 2). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH vs GAIN

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low signal gains, most amplifiers will exhibit a more complex response with lower phase margin. The OPA4820 is optimized to give a maximally-flat, 2nd-order Butterworth response in a gain of 2. In this configuration, the OPA4820 has approximately 64° of phase margin and will show a typical −3dB bandwidth of 240MHz. When the phase margin is 64°, the closed-loop bandwidth is approximately $\sqrt{2}$ greater than the value predicted by dividing GBP by the noise gain. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 27MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 250MHz.

OUTPUT DRIVE CAPABILITY

The OPA4820 has been optimized to drive the demanding load of a doubly-terminated transmission line. When a 50Ω line is driven, a series 50Ω into the cable and a terminating 50Ω load at the end of the cable are used. Under these conditions, the cable impedance will appear resistive over a wide frequency range, and the total effective load on the OPA4820 is 100Ω in parallel with the resistance of the feedback network. The electrical characteristics show a ±3.6V swing into this load—which will then be reduced to a ±1.8V swing at the termination resistor. The ±75mA output drive over temperature provides adequate current drive margin for this load. Higher voltage swings (and lower distortion) are achievable when driving higher impedance loads.

A single video load typically appears as a 150Ω load (using standard 75Ω cables) to the driving amplifier. The OPA4820 provides adequate voltage and current drive to support up to three parallel video loads (50Ω total load) for an NTSC signal. With only one load, the OPA4820 achieves an exceptionally low 0.01%/0.03° dG/dP error.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. A high-speed, high open-loop gain amplifier like the OPA4820 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended *R_S vs Capacitive Load* and the resulting frequency response at the load. The criterion for setting the recommended resistor is maximum bandwidth, flat frequency response at the load. Since there is now a passive low-pass filter between the output pin and the load capacitance, the response at the output pin itself is typically somewhat peaked, and becomes flat after the roll-off action of the RC network. This is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the amplifier's swing limit. Such clipping would be most likely to occur in pulse response applications where the frequency peaking is manifested as an overshoot in the step response.

Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA4820. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA4820 output pin (see the *Board Layout* section).

DISTORTION PERFORMANCE

The OPA4820 is capable of delivering an exceptionally low distortion signal at high frequencies and low gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100dB dynamic range. The OPA4820 distortion does not rise above −90dBc until either the signal level exceeds 0.9V and/or the fundamental frequency exceeds 500kHz. **Distortion in the audio band is ≤ −100dBc.**

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is the sum of $R_F + R_G$, whereas in the inverting configuration this is just R_F (see Figure 1). Increasing the output voltage swing increases harmonic distortion directly. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again, a 6dB increase in gain will increase the 2nd- and 3rd-harmonic by 6dB even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases because of the roll-off in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 100kHz. Starting from the −85dBc 2nd-harmonic for $2V_{PP}$ into 200Ω, G = +2 distortion at 1MHz (from the Typical Characteristics), the 2nd-harmonic distortion will not show any improvement below 100kHz and will then be:

−85dB − 20log (1MHz/100kHz) = −105dBc

NOISE PERFORMANCE

The OPA4820 complements its low harmonic distortion with low input noise terms. Both the input-referred voltage noise and the two input-referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 18 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 9 shows the general form for this output noise voltage using the terms presented in Figure 18.

$$E_O = \sqrt{\left[E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right]NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (9)$$

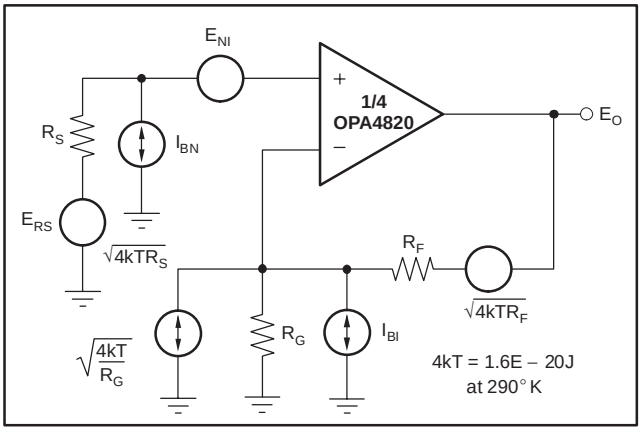


Figure 18. Op Amp Noise Analysis Model

Dividing this expression by the noise gain (NG = 1 + R_F/R_G) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 10.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (10)$$

Evaluating these two equations for the OPA4820 circuit presented in Figure 1 will give a total output spot noise voltage of 6.44nV/√Hz and an equivalent input spot noise voltage of 3.22nV/√Hz.

DC OFFSET CONTROL

The OPA4820 can provide excellent DC signal accuracy because of its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA4820 has a moderately high input bias current (9μA typ into the pins) but with a very close match between the two input currents—typically 100nA input offset current. The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 175Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this will increase the source impedance for the noninverting input bias current to 200Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F \parallel R_G$), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402Ω feedback resistor, this output error will now be less than ±0.5μA × 402Ω = ±208μV at 25°C.

THERMAL ANALYSIS

The OPA4820 will not require heatsinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using all channels of an OPA4820IPW (TSSOP-14 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C.

$$P_D = 10V(25.8mA) + 4 \times [5^2/(4 \times (100\Omega \parallel 800\Omega))] = 539mW$$

$$\text{Maximum } T_J = +85°C + (539mW \times 110°C/W) = 144°C$$

This maximum operating junction temperature is below the absolute maximum junction temperature. Most junction temperatures in applications will be lower since an absolute worst-case output stage power was assumed in this calculation.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the OPA4820 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA4820. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load-driving considerations. It has been suggested here that a good starting point for design would be to set $R_G \parallel R_F = 200\Omega$. Using this setting will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA4820 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA4820 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA4820 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA4820 onto the board.

INPUT AND ESD PROTECTION

The OPA4820 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 19.

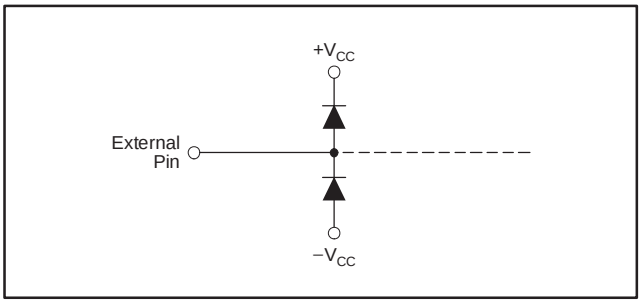


Figure 19. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA4820), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Figure 20 shows an example protection circuit for I/O voltages that may exceed the supplies.

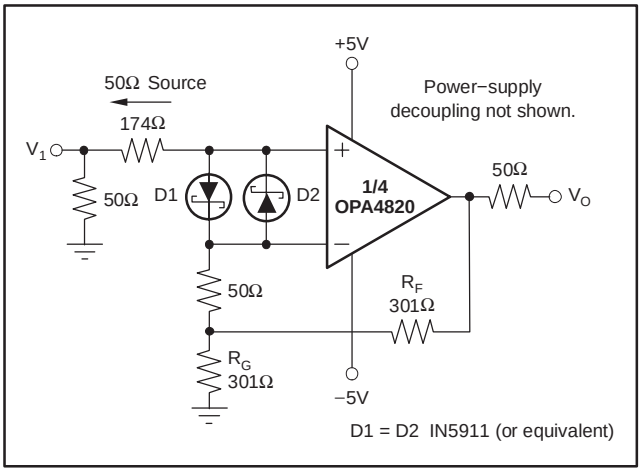


Figure 20. Gain of +2 with Input Protection

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/08	D	2	Absolute Maximum Ratings	Changed Storage Temperature minimum value from −40°C to −65°C.
6/06	C	21	Design-In Tools	Demonstration fixture numbers changed.
		26	Application Information	Added Revision History table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4820ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4820
OPA4820ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4820
OPA4820IDG4	Active	Production	SOIC (D) | 14	50 | TUBE	-	Call TI	Call TI	-40 to 85	
OPA4820IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4820
OPA4820IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4820
OPA4820IPWR	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4820
OPA4820IPWR.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4820
OPA4820IPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4820
OPA4820IPWT.A	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4820

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

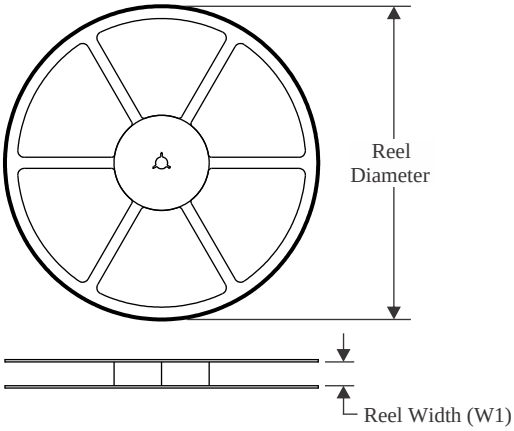
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

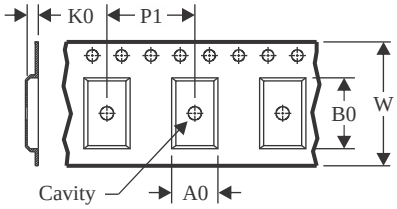
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

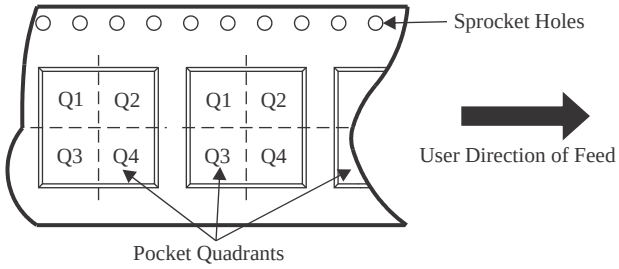


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

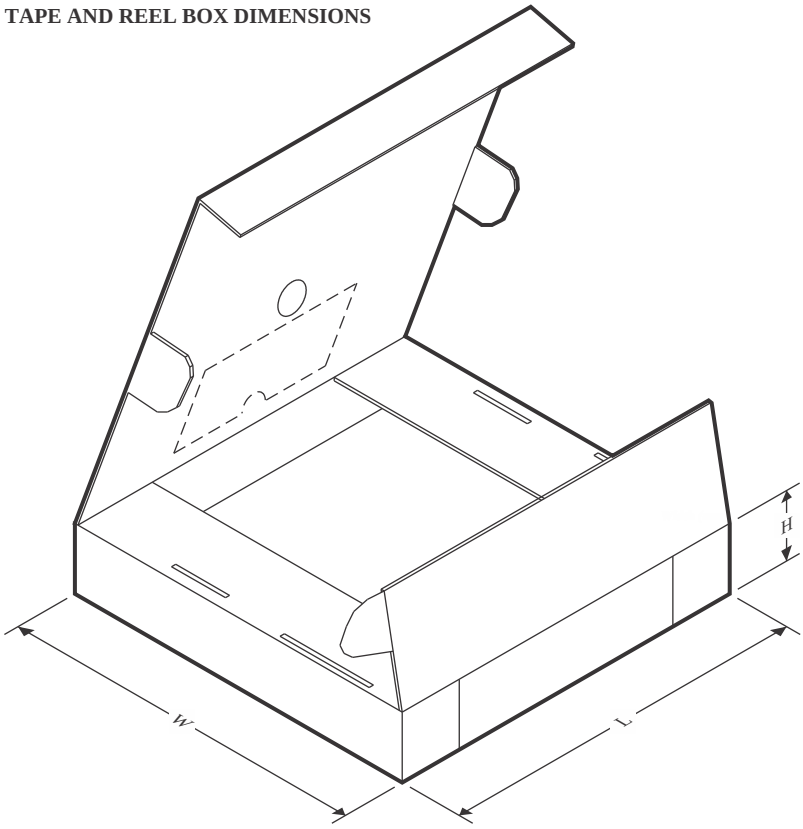
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4820IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4820IPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4820IPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

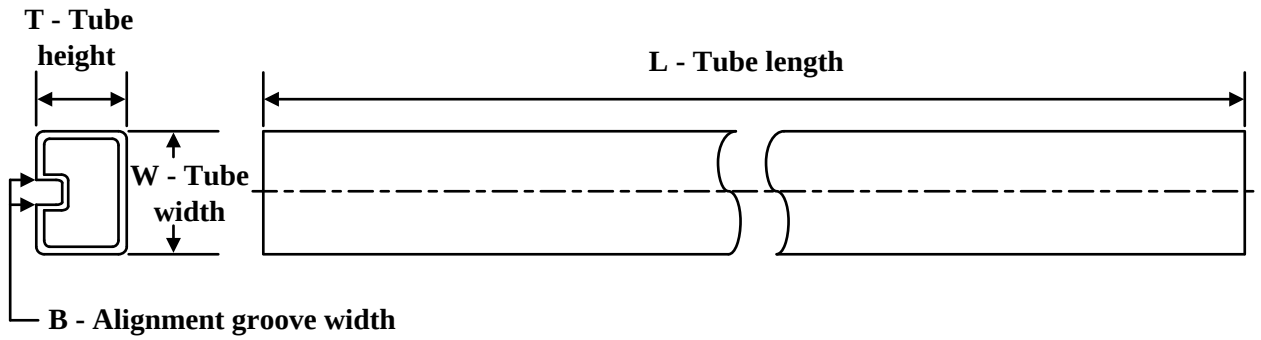
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4820IDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4820IPWR	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA4820IPWT	TSSOP	PW	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

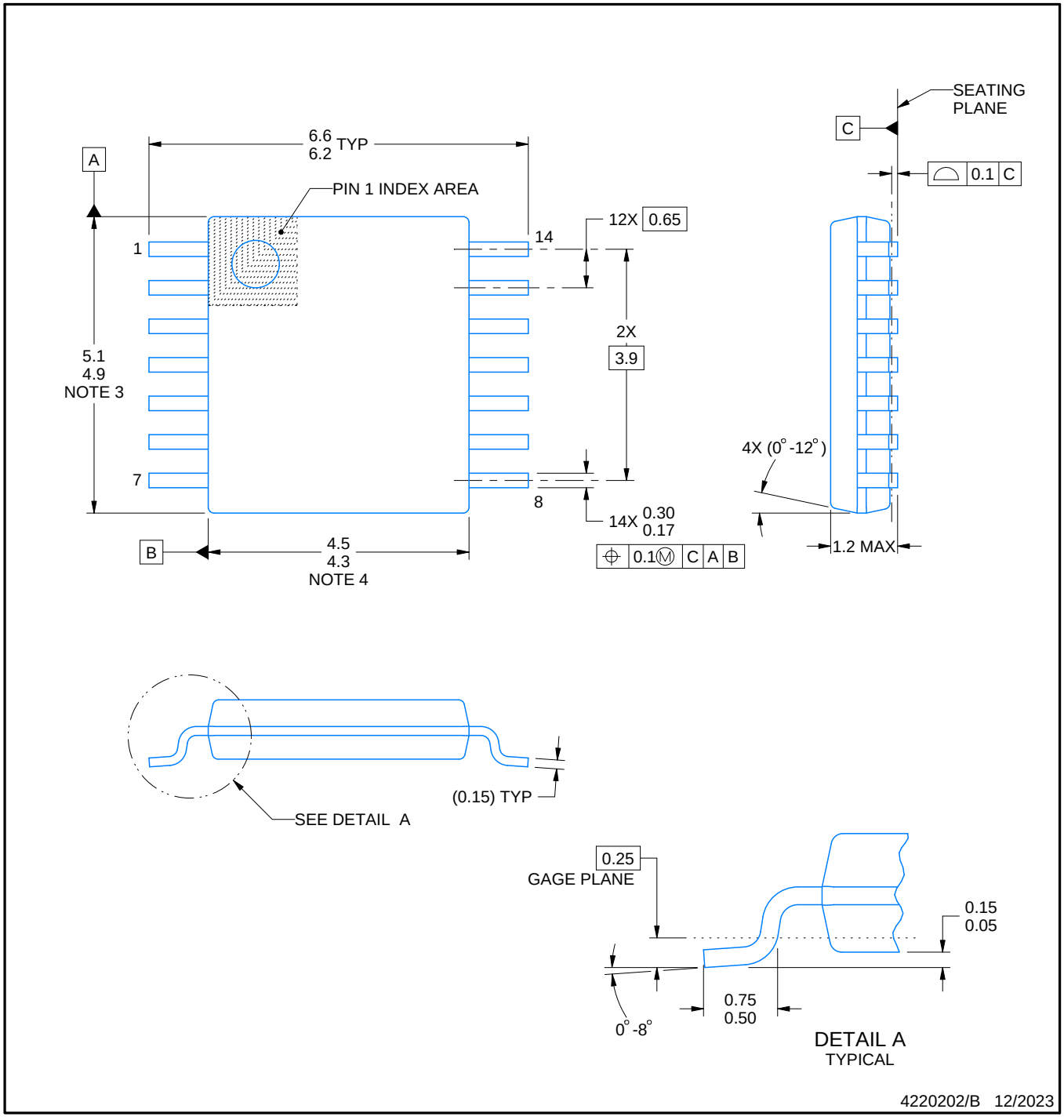
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA4820ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4820ID.A	D	SOIC	14	50	506.6	8	3940	4.32

PACKAGE OUTLINE

PW0014A

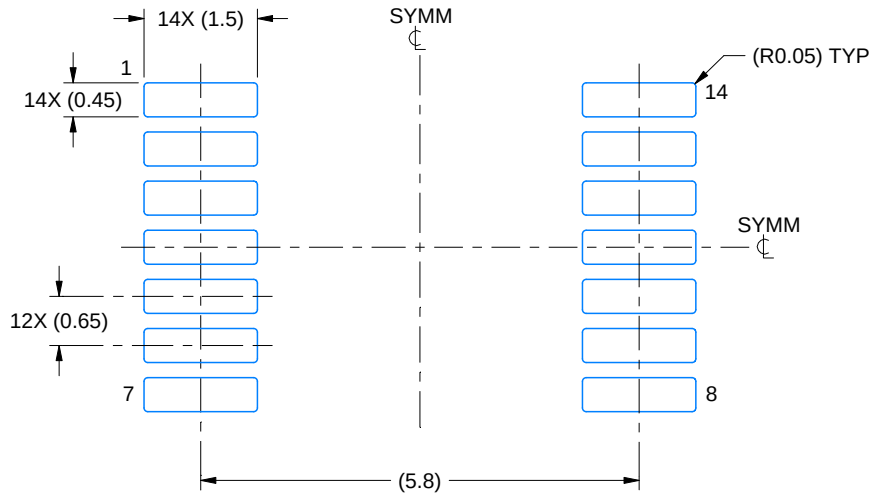
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

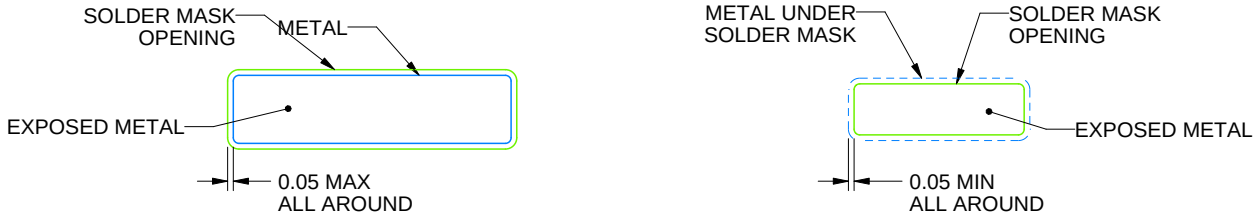


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

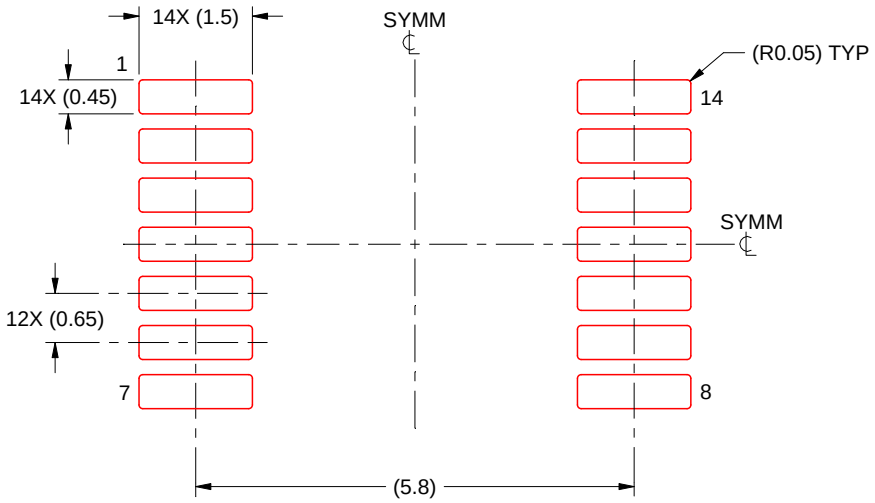


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

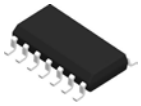


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

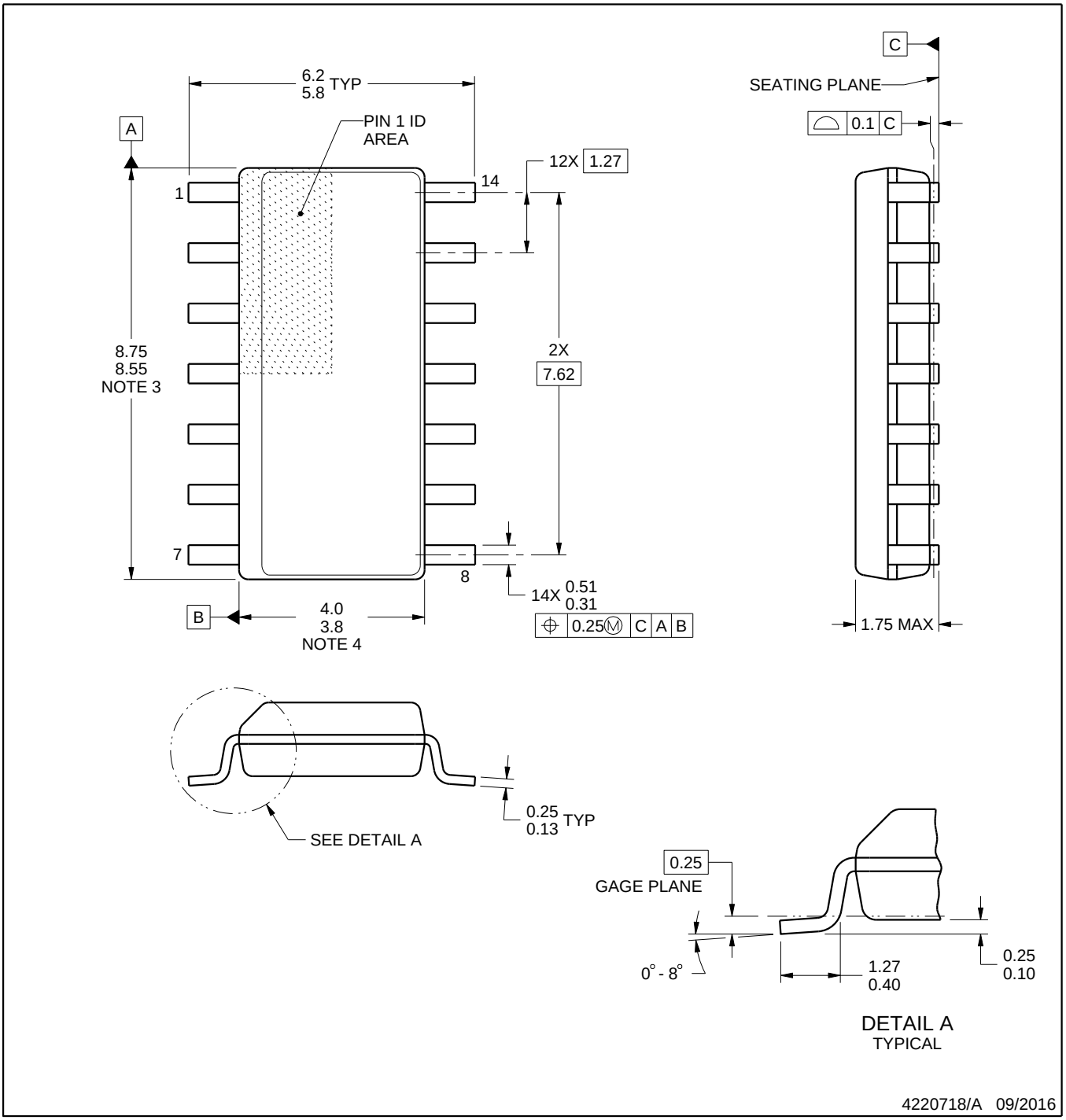


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

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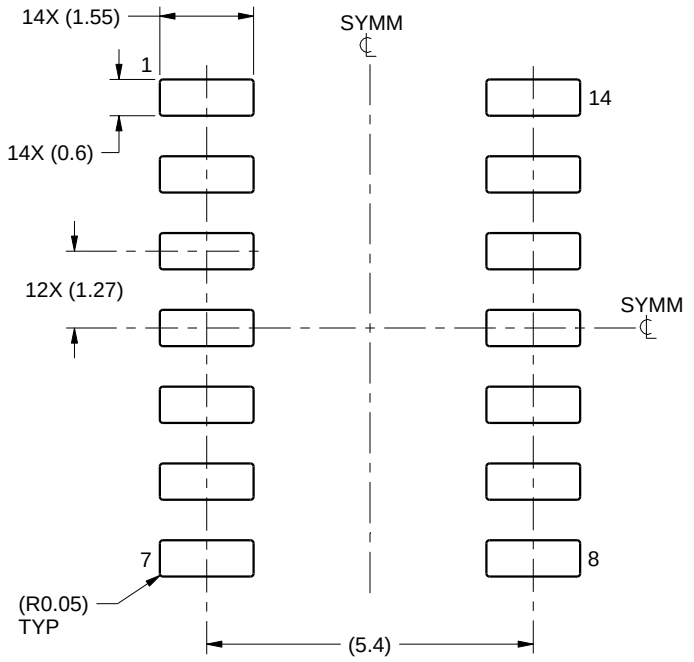
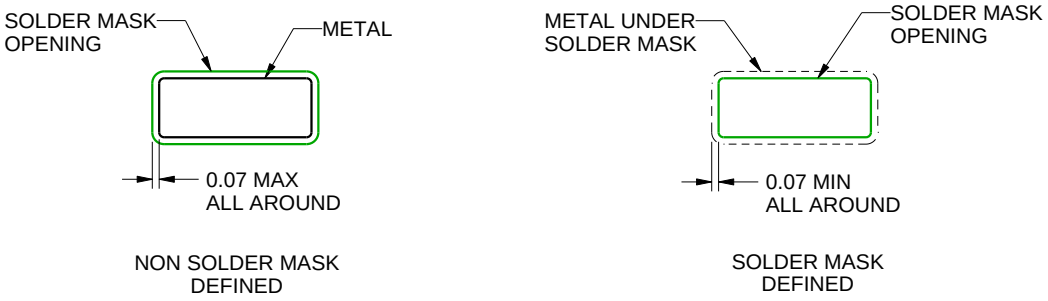
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

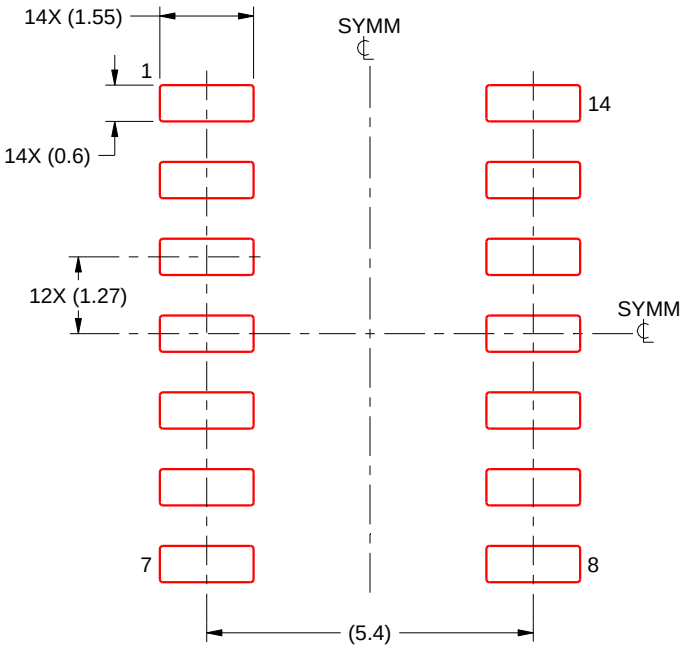
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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