OPAx205 4μV、0.08μV/°C 低功耗超 β 双极 e-trim™ 运算放大器

1 特性

- e-trim™ 运算放大器性能
  - 低失调电压：25μV（最大值），15μV（最大值，高等级）
  - 低失调电压漂移：±0.5μV/°C（典型值），±0.2μV/°C（最大值，高等级）
- 超 β 输入
  - 输入偏置电流：500 pA（最大值）
  - 输入电流噪声：110fA/√Hz
- 低噪声
  - 0.1 至 10Hz：$0.2μV_{PP}$
  - 电压噪声：7.2nV/√Hz
- A_{OL}、CMRR 和 PSRR：> 126dB（全温度范围）
- 增益带宽积：3.6MHz
- 低静态电流：240μA（最大值）
- 压摆率：4V/μs
- 过载功率限制器
- 轨到轨输出
- EMI 和 RFI 已滤除的输入
- 宽电源电压范围：4.5V 至 36V
- 温度范围：–40°C 至 +125°C
- 提供标准等级 (OPAx205A) 和高等级（OPA2205，预发布）
- OPA206 和 OPA2206 提供 ±40V 过压保护

2 应用

- 流量变送器
- 串式逆变器
- 数据采集 (DAQ)
- 源测量单元 (SMU)
- 实验室和现场仪表
- 电池测试
- 模拟输入模块
- 压力变送器

3 说明

OPA205、OPA2205 和 OPA4205 (OPAx205) 是业界通用 OPAx277 系列的新一代版本。OPA206 和 OPA2206 是使用相同运算放大器内核的相关器件，但具有高于电源电压 ±40V 的输入过压保护的额外特性。这些器件是具有超 β 输入的精密双极 e-trim™ 运算放大器。TI 的专有微调技术用于实现 ±4μV（±2μV，高等级）的典型输入失调电压和 ±0.08μV（±0.04μV，高等级）的典型输入失调电压漂移。

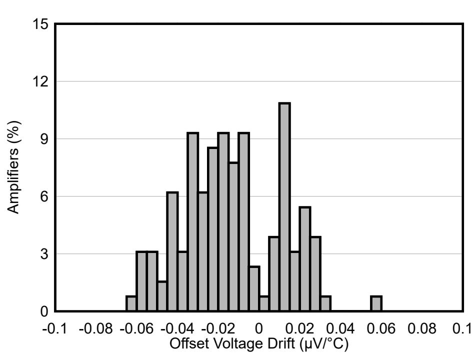
OPAx205 采用双极工艺设计，可针对仅 220μA 的静态电流提供 3.6MHz 增益带宽。这些器件还可在 1kHz 下实现仅 7.2nV/√Hz 的低电压噪声密度。得益于超 β 输入，OPAx205 具有 100pA（典型值）的超低输入偏置电流和 110fA/√Hz 的电流噪声密度。

OPAx205 的高性能使这些器件成为了高精度和低功耗系统的理想选择，例如流量和压力变送器、便携式数据采集 (DAQ) 系统和高密度源测量单元 (SMU)。

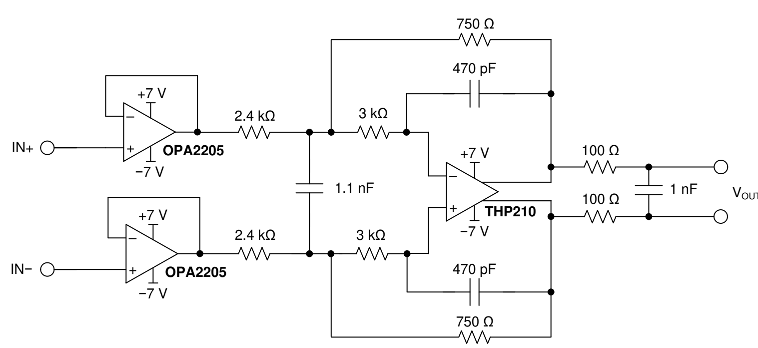
器件信息

器件型号	通道	封装[1]
OPA205	单通道	D（SOIC，8）
OPA2205[2]	双通道	D（SOIC，8）
	双通道	DGK（VSSOP，8）
OPA4205	四通道	D（SOIC，14）
	四通道	PW（TSSOP，14）

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 高等级版本为预发布信息（而非量产数据）。



OPAx205 失调电压漂移



OPA2205 典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (December 2022) to Revision F (March 2023) — **Page**

- 更改了标题以与标准级器件规格保持一致 1
- 添加了 OPA2205 D（SOIC，8）封装和相关内容作为量产数据 1
- 添加了 OPA4205 D（SOIC，14）封装和相关内容作为量产数据 1
- Changed maximum input bias from ±0.4 nA to ±0.5 nA 21
- Changed offset and offset drift values to match standard-grade device specifications in *Detailed Design Description* 26
- Changed Figure 9-6 to show correct VS+ connection 29

Changes from Revision D (September 2022) to Revision E (December 2022) — **Page**

- 添加了 OPA4205 TSSOP 封装和相关内容作为量产数据 1
- Changed typical input offset voltage from 8 µV to 4 µV in *Electrical Characteristics* 8
- Changed maximum input offset voltage from 50 µV to 25 µV in *Electrical Characteristics* 8
- Changed maximum input offset voltage over temperature from 80 µV to 55 µV in *Electrical Characteristics* 8
- Changed typical input offset voltage from 8 µV to 4 µV in *Electrical Characteristics* 10
- Changed maximum input offset voltage from 50 µV to 25 µV in *Electrical Characteristics* 10
- Changed maximum input offset voltage over temperature from 80 µV to 55 µV in *Electrical Characteristics* 10

Changes from Revision C (July 2022) to Revision D (September 2022) — **Page**

- 将 OPA205 (SOIC) 从“预发布”更改为“量产数据”（正在供货） 1

Changes from Revision B (August 2021) to Revision C (July 2022) — **Page**

- 添加了 OPA205 D (SOIC) 封装作为预告信息（预发布） 1

Changes from Revision A (May 2021) to Revision B (August 2021)	Page
• Changed Figure 6-22, *Voltage Noise Density vs Frequency*, to show voltage noise density instead of current noise density	12

Changes from Revision * (April 2020) to Revision A (May 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将 OPA2205 从“预告信息（预发布）”更改为“量产数据（正在供货）”	1
• Changed both *Electrical Characteristics* tables to show differentiated performance between OPA2205 (high grade) and OPA2205A (standard grade)	8

5 Pin Configuration and Functions

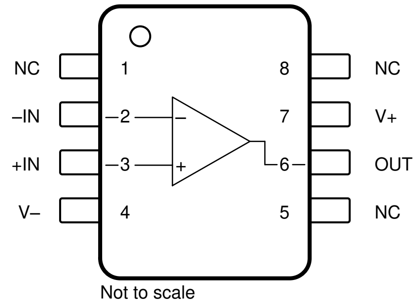


图 5-1. OPA205 D Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions: OPA205

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
– IN	2	Input	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	Output	Output
V+	7	—	Positive (highest) power supply
V –	4	—	Negative (lowest) power supply

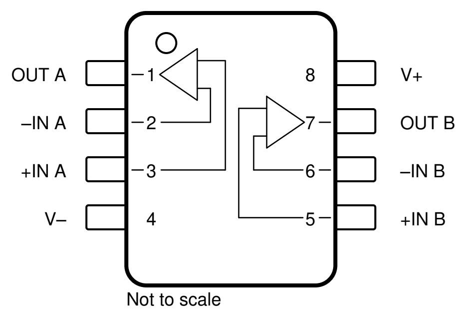


图 5-2. OPA2205 DGK Package, 8-Pin VSSOP and D Package, 8-pin SOIC (Top View)

表 5-2. Pin Functions: OPA2205

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
– IN A	2	Input	Inverting input, channel A
+IN B	5	Input	Noninverting input, channel B
– IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	—	Positive (highest) power supply
V –	4	—	Negative (lowest) power supply

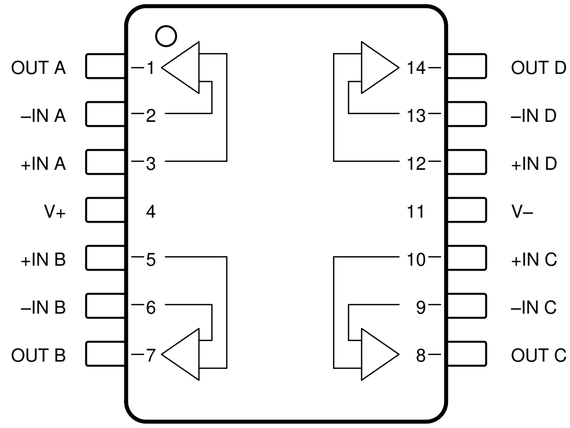


图 5-3. OPA4205 PW Package, 14-Pin TSSOP and D Package, 14-Pin SOIC (Top View)

Pin Functions: OPA4205

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
– IN C	9	Input	Inverting input, channel C
– IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply		40	V
		Dual supply		±20	
	Signal input pin voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		±0.5	
	Signal input pin current			±10	mA
	Output short-circuit[(2)]		Continuous		
T_A	Operating temperature		–40	150	°C
T_J	Junction temperature			150	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[((2))]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T_A	Operating temperature		–40		125	°C

6.4 Thermal Information: OPA205

THERMAL METRIC[(1)]		OPA205 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.5	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.0	℃/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	℃/W
ψ_{JB}	Junction-to-board characterization parameter	64.3	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	℃/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2205

THERMAL METRIC[(1)]		OPA2205		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	175.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	63.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.3	97.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.8	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.5	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4205

THERMAL METRIC[(1)]		OPA4205		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	117.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.5	36.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.9	58.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics: V_S = ±5 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA2205			±2	±15	μV
			T_A = –40°C to +125°C			±25	
		OPAx205A			±4	±25	
			T_A = –40°C to +125°C			±55	
dV_{OS}/dT	Input offset voltage drift	OPA2205	T_A = –40°C to +125°C		±0.04	±0.2	μV/°C
		OPAx205A	T_A = –40°C to +125°C		±0.08	±0.5	
PSRR	Power supply rejection ratio	OPA2205, V_S = ±2.25 V to ±18 V			±0.05	±0.25	μV/V
			T_A = –40°C to +125°C			±0.5	
		OPAx205A, V_S = ±2.25 V to ±18 V			±0.05	±0.5	
			T_A = –40°C to +125°C			±1	
	Channel separation, (dual, quad)	f = dc			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I_B	Input bias current	OPA2205			±0.1	±0.4	nA
			T_A = 0°C to 85°C			±0.6	
			T_A = –40°C to +125°C			±0.9	
		OPAx205A			±0.1	±0.5	
			T_A = 0°C to 85°C			±0.75	
			T_A = –40°C to +125°C			±1	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.5	
		T_A = –40°C to +125°C				±0.6	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz			7.4		$nV/\sqrt{Hz}$
		f = 100 kHz			7.2		
		f = 1 kHz			7.2		
i_n	Input current noise density	f = 1 kHz			110		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	OPA2205, (V–) + 1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		124	140		dB
		OPAx205A, (V–) + 1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		124	140		
INPUT IMPEDANCE							
Z_{ID}	Differential				9 || 4.4		MΩ || pF
Z_{ICM}	Common-mode				300 || 4.4		GΩ || pF

6.7 Electrical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	OPA2205, T_A = –40°C to +125°C, (V–) + 200 mV < V_O < (V+) – 200 mV	R_L = 10 kΩ	126	132		dB
			R_L = 2 kΩ	126	130		
		OPAx205A, T_A = –40°C to +125°C, (V–) + 200 mV < V_O < (V+) – 200 mV	R_L = 10 kΩ	126	132		
			R_L = 2 kΩ	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3.6		MHz
SR	Slew rate	4-V step, gain = –1			3.2		V/μs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			67		degrees
t_S	Settling time	To 0.024% (12-bit), 4-V step, gain = 1, C_L = 30 pF	Falling		2.2		μs
			Rising		2.8		
	Overload recovery time	Gain = –10			0.3		μs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, gain = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%
OUTPUT							
	Voltage output swing from rail	A_{OL} > 126 dB	R_L = 10 kΩ	(V–) + 0.2		(V+) – 0.2	V
			R_L = 2 kΩ	(V–) + 0.2		(V+) – 0.2	
		T_A = –40°C to +125°C, R_L = 10 kΩ		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current				±25		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
R_O	Open-loop output impedance				See Typical Characteristics		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			220	240	μA
			T_A = –40°C to +125°C			310	

6.8 Electrical Characteristics: V_S = ±15 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA2205			±2	±15	µV
			T_A = –40°C to +125°C			±25	
		OPAx205A			±4	±25	
			T_A = –40°C to +125°C			±55	
dV_{OS}/dT	Input offset voltage drift	OPA2205	T_A = –40°C to +125°C		±0.04	±0.2	µV/°C
		OPAx205A	T_A = –40°C to +125°C		±0.08	±0.5	
PSRR	Power supply rejection ratio	OPA2205, V_S = ±2.25 V to ±18 V			±0.05	±0.25	µV/V
			T_A = –40°C to +125°C			±0.5	
		OPAx205A, V_S = ±2.25 V to ±18 V			±0.05	±0.5	
			T_A = –40°C to +125°C			±1	
	Channel separation, (dual, quad)	f = dc			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I_B	Input bias current	OPA2205			±0.1	±0.4	nA
			T_A = 0°C to 85°C			±0.6	
			T_A = –40°C to +125°C			±0.9	
		OPAx205A			±0.1	±0.5	
			T_A = 0°C to 85°C			±1	
			T_A = –40°C to +125°C			±1.2	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.8	
		T_A = –40°C to +125°C				±0.9	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz			7.4		$nV/\sqrt{Hz}$
		f = 100 Hz			7.2		
		f = 1 kHz			7.2		
i_n	Input current noise density	f = 1 kHz			110		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	OPA2205, (V–) + 1 V < V_{CM} < (V+) – 1.4 V		126	140		dB
			T_A = –40°C to +125°C	124	140		
		OPAx205A, (V–) + 1 V < V_{CM} < (V+) – 1.4 V		126	140		
			T_A = –40°C to +125°C	124	140		
INPUT IMPEDANCE							
Z_{ID}	Differential				9 || 4.4		MΩ || pF
Z_{ICM}	Common-mode				300 || 4.3		GΩ || pF

6.8 Electrical Characteristics: V_S = ±15 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	OPA2205, T_A = –40°C to +125°C	R_L = 10 kΩ, (V–) + 200 mV < V_O < (V+) – 200 mV	132	135		dB
			R_L = 2 kΩ, (V–) + 350 mV < V_O < (V+) – 350 mV	132	135		
		OPAx205A, T_A = –40°C to +125°C	R_L = 10 kΩ, (V–) + 200 mV < V_O < (V+) – 200 mV	126	132		
			R_L = 2 kΩ, (V–) + 350 mV < V_O < (V+) – 350 mV	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 30 pF			3.6		MHz
SR	Slew rate	10-V step, gain = –1			4		V/µs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			58		degrees
t_S	Settling time	To 0.024% (12-bit), 10-V step, gain = 1, C_L = 30 pF	Falling		2.8		µs
			Rising		4.5		
	Overload recovery time	Gain = –10			0.2		µs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, gain = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%
OUTPUT							
	Voltage output swing from rail	A_{OL} > 126 dB	R_L = 10 kΩ	(V–) + 0.2		(V+) – 0.2	V
			R_L = 2 kΩ	(V–) + 0.35		(V+) – 0.35	
		T_A = –40°C to +125°C, R_L = 10 kΩ		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current				±25		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
R_O	Open-loop output impedance				See Typical Characteristics		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			220	240	µA
			T_A = –40°C to +125°C			310	

6.9 Typical Characteristics

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

表 6-1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution at 25°C	图 6-1
Offset Voltage at 125°C	图 6-2
Offset Voltage at –40°C	图 6-3
Offset Voltage vs Temperature	图 6-4
Offset Voltage Drift Distribution	图 6-5
Offset Voltage vs Output Voltage	图 6-6
Offset Voltage vs Power Supply Voltage	图 6-7
Power-Supply Rejection Ratio vs Temperature	图 6-8
Power-Supply and Common-Mode Rejection Ratio vs Frequency	图 6-9
Common-Mode Rejection Ratio vs Temperature	图 6-10
Offset Voltage vs Common-Mode Voltage	图 6-11
Offset Voltage vs V_{CM} at Low Supply	图 6-12
Offset Voltage vs V_{CM} at High Supply	图 6-13
Open-Loop Gain and Phase vs Frequency	图 6-14
Open-Loop Gain vs Swing From the Rail	图 6-15
Open-Loop Gain vs Temperature	图 6-16
Closed-Loop Gain vs Frequency	图 6-17
Input Bias Production Distribution	图 6-18
Input Bias vs Common-Mode Voltage	图 6-19
Input Bias and Input Offset Current vs Temperature	图 6-20
Input Offset Current Production Distribution	图 6-21
Voltage Noise Density vs Frequency	图 6-22
0.1-Hz to 10-Hz Noise	图 6-23
Total Harmonic Distortion + Noise Ratio vs Frequency	图 6-24
Total Harmonic Distortion + Noise Ratio vs Output Amplitude	图 6-25
Current Noise vs Frequency	图 6-26
Maximum Output Voltage vs Frequency	图 6-27
Output Voltage Swing vs Output Sourcing Current	图 6-28
Output Voltage Swing vs Output Sinking Current	图 6-29
Open-Loop Output Impedance vs Frequency	图 6-30
No Phase Reversal	图 6-31
Small-Signal Overshoot vs Capacitive Load, Gain = +1	图 6-32
Small-Signal Overshoot vs Capacitive Load, Gain = –1	图 6-33
Phase Margin vs Capacitive Load	图 6-34
Positive Overload Recovery, Gain = –1	图 6-35
Negative Overload Recovery, Gain = –1	图 6-36
Settling Time	图 6-37
Small-Signal Step Response, Gain = +1	图 6-38
Small-Signal Step Response, Gain = –1	图 6-39
Large-Signal Step Response, Gain = +1	图 6-40
Large-Signal Step Response, Gain = –1	图 6-41
Short-Circuit Current vs Temperature	图 6-42
Electromagnetic Interference Rejection (EMIRR)	图 6-43
Quiescent Current vs Supply Voltage	图 6-44

6.9 Typical Characteristics

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

表 6-1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Quiescent Current vs Temperature	图 6-45

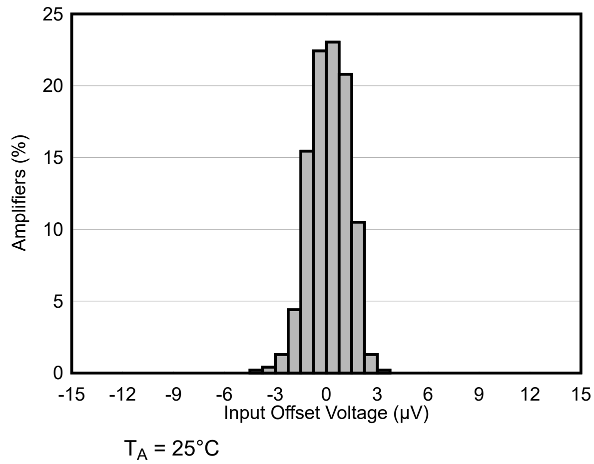


图 6-1. Offset Voltage Production Distribution at 25°C

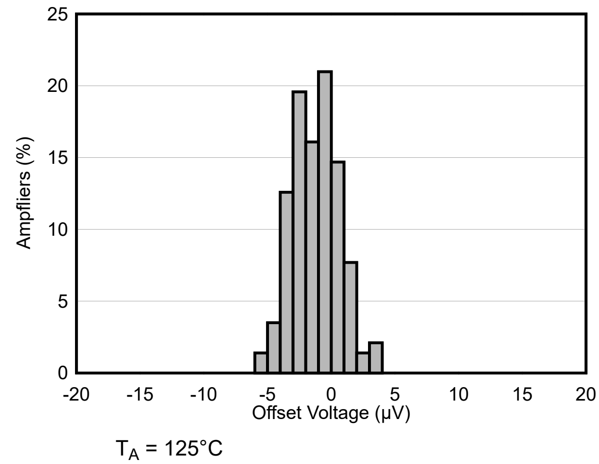


图 6-2. Offset Voltage Distribution at 125°C

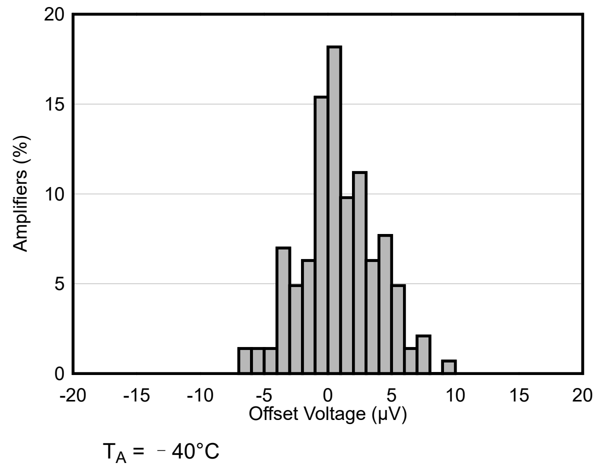


图 6-3. Offset Voltage Distribution at -40°C

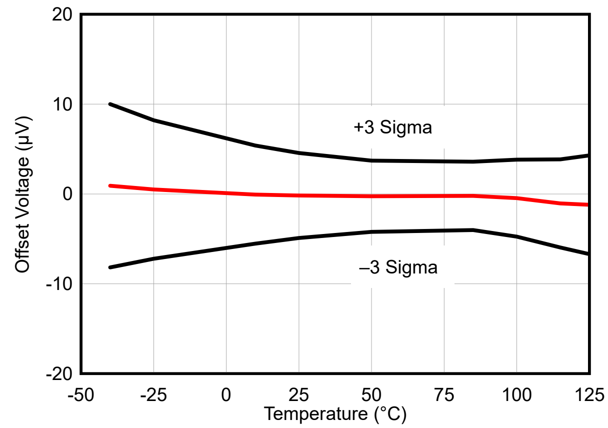


图 6-4. Offset Voltage vs Temperature

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

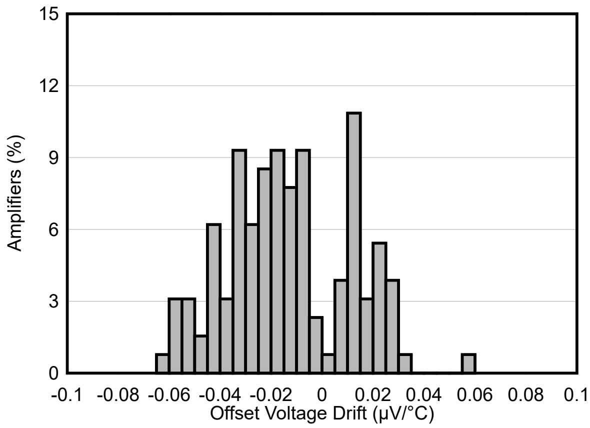


图 6-5. Offset Voltage Drift Distribution

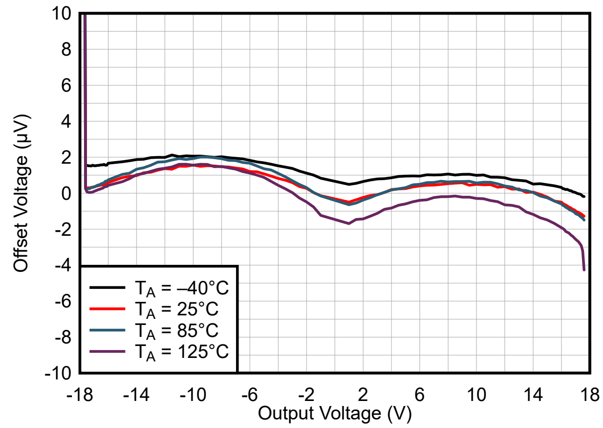


图 6-6. Offset Voltage vs Output Voltage

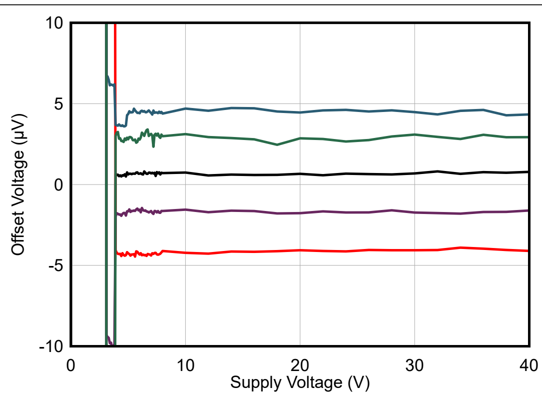


图 6-7. Offset Voltage vs Power Supply Voltage

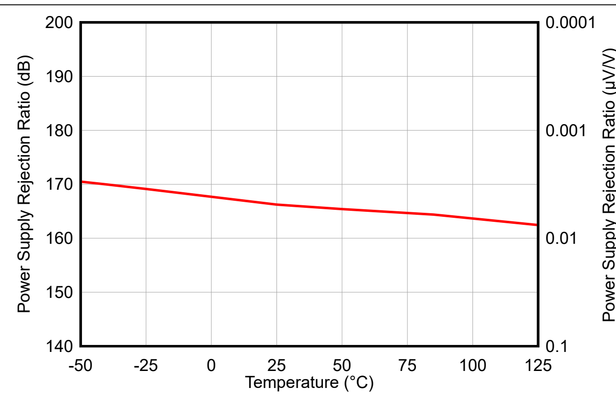


图 6-8. Power-Supply Rejection Ratio vs Temperature

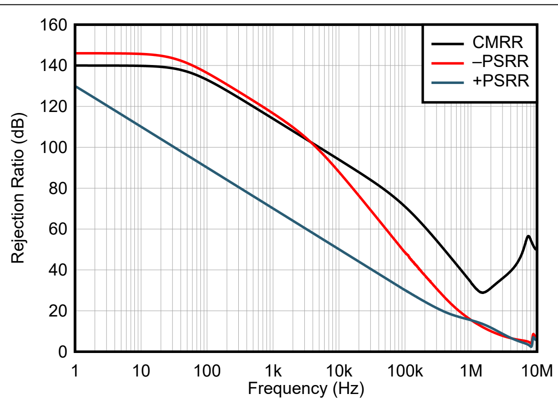


图 6-9. Power-Supply and Common-Mode Rejection Ratio vs Frequency

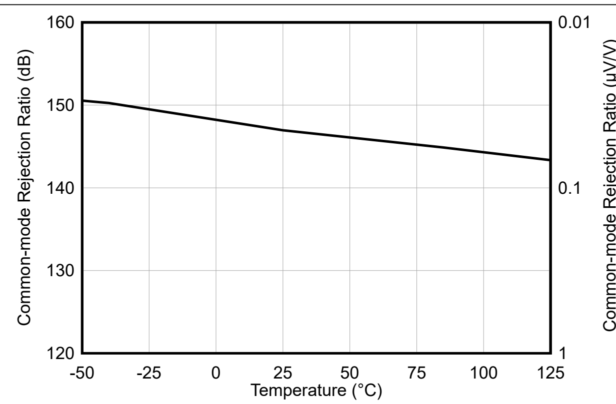


图 6-10. Common-Mode Rejection Ratio vs Temperature

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

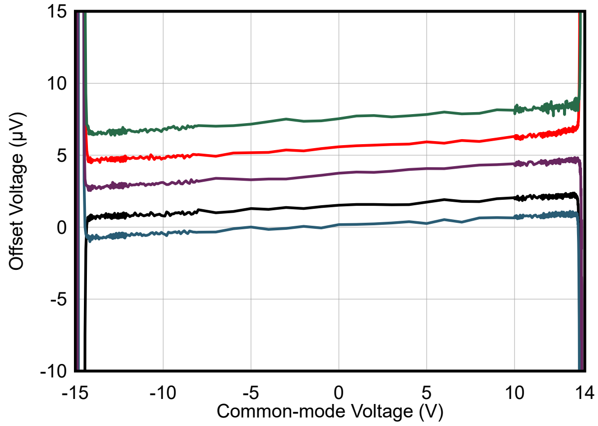


图 6-11. Offset Voltage vs Common-Mode Voltage

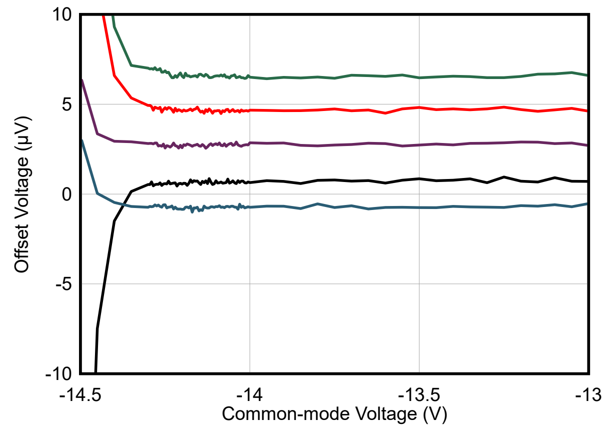


图 6-12. Offset Voltage vs V_{CM} at Low Supply

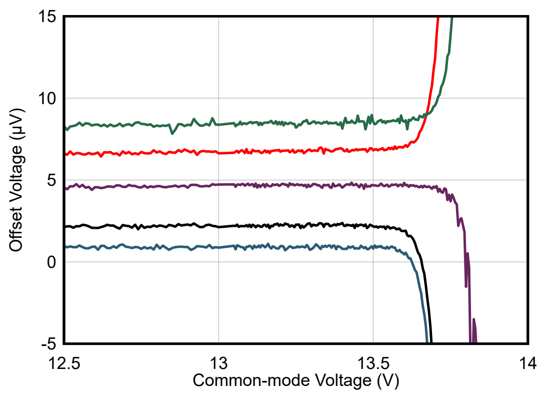


图 6-13. Offset Voltage vs V_{CM} at High Supply

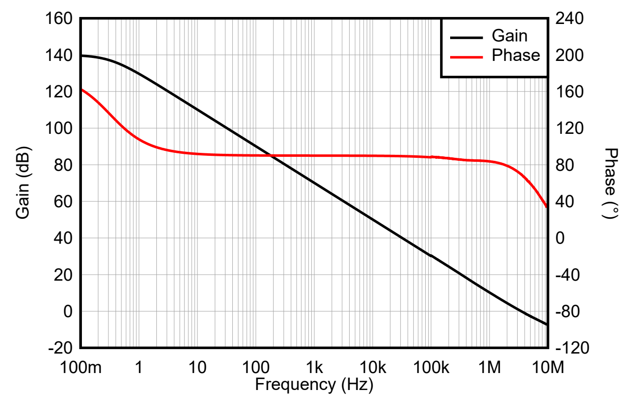


图 6-14. Open-Loop Gain and Phase vs Frequency

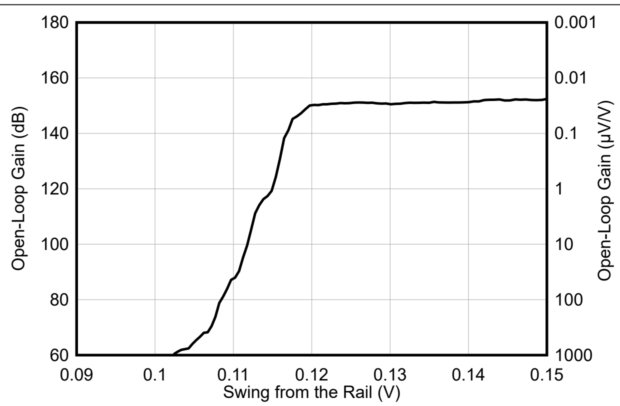


图 6-15. Open-Loop Gain vs Swing From the Rail

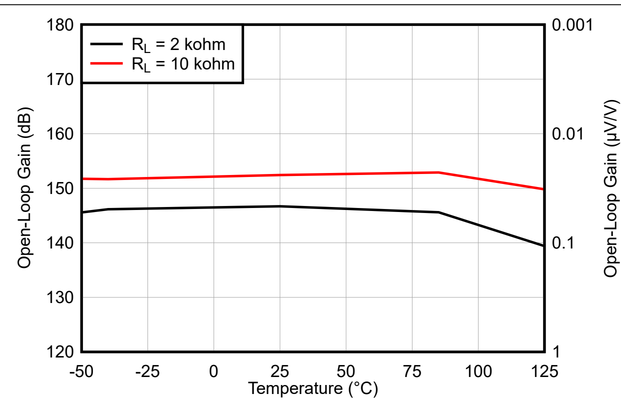


图 6-16. Open-Loop Gain vs Temperature

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

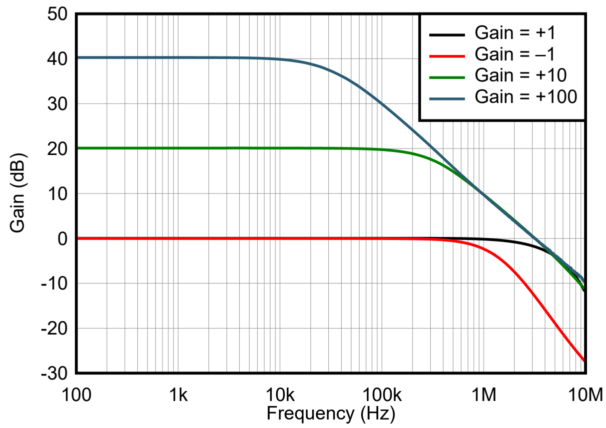


图 6-17. Closed-Loop Gain vs Frequency

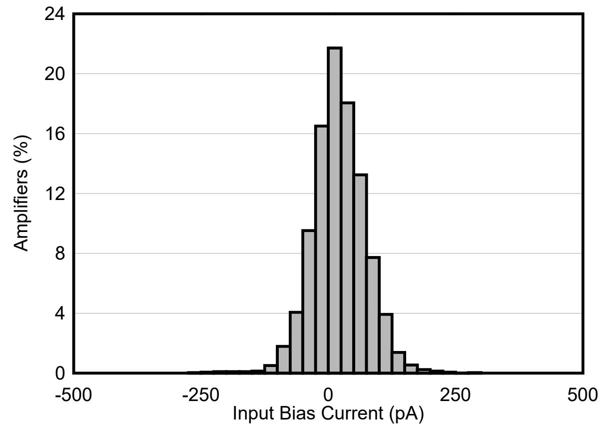


图 6-18. Input Bias Production Distribution

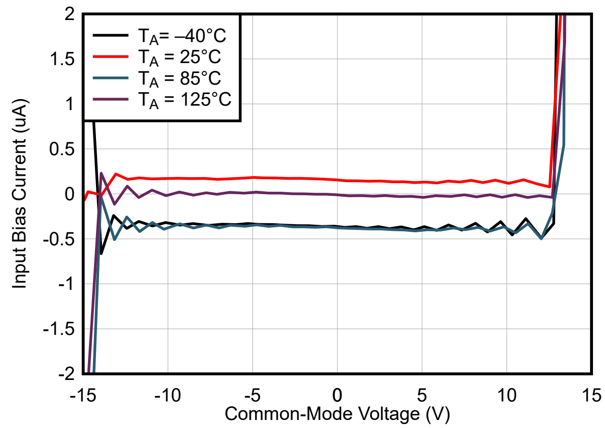


图 6-19. Input Bias vs Common-Mode Voltage

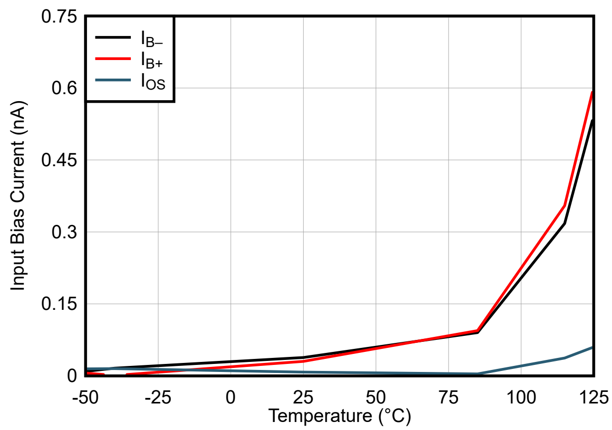


图 6-20. Input Bias and Input Offset Current vs Temperature

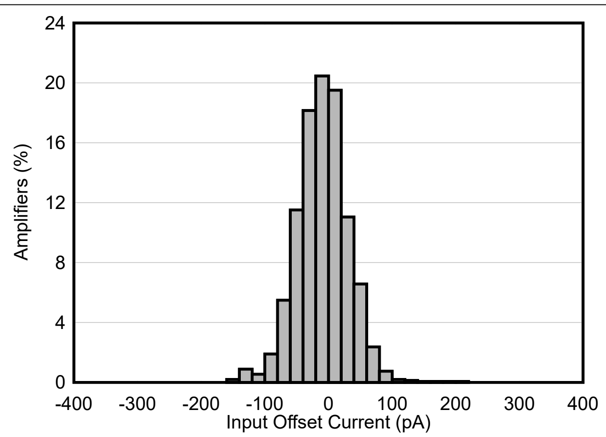


图 6-21. Input Offset Current Production Distribution

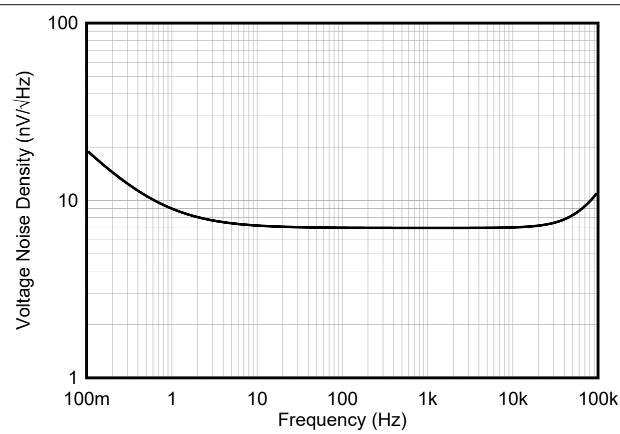


图 6-22. Voltage Noise Density vs Frequency

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

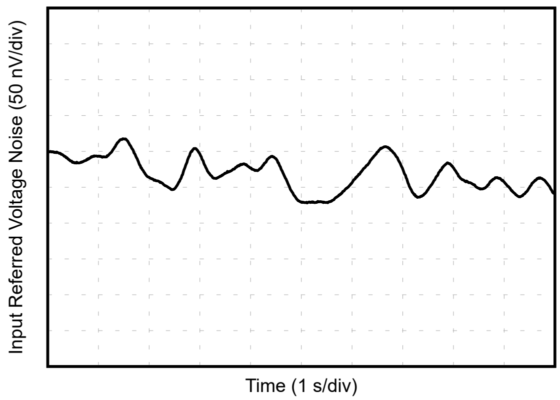


图 6-23. 0.1-Hz to 10-Hz Noise

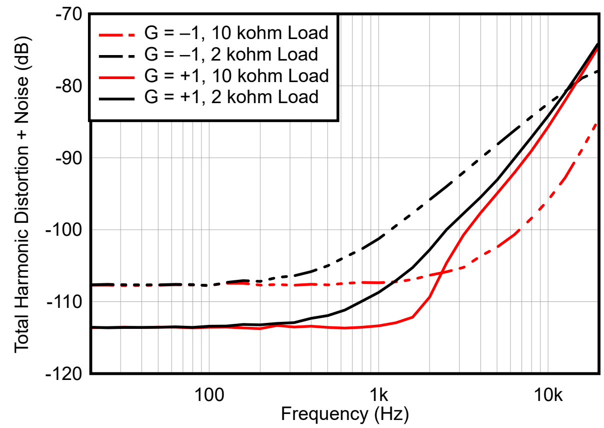


图 6-24. Total Harmonic Distortion + Noise Ratio vs Frequency

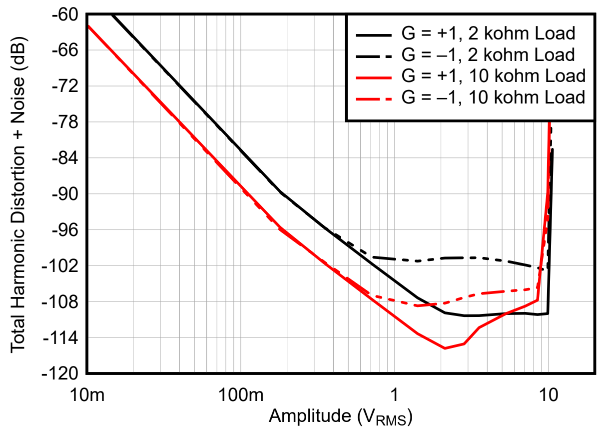


图 6-25. Total Harmonic Distortion + Noise Ratio vs Output Amplitude

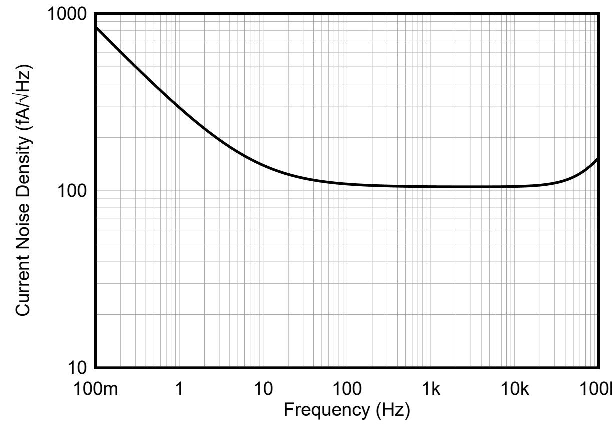


图 6-26. Current Noise vs Frequency

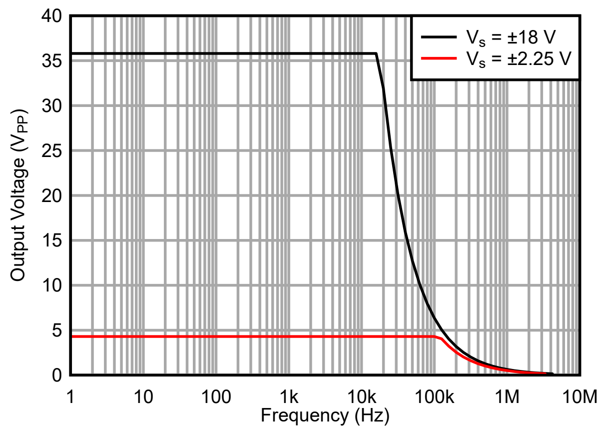


图 6-27. Maximum Output Voltage vs Frequency

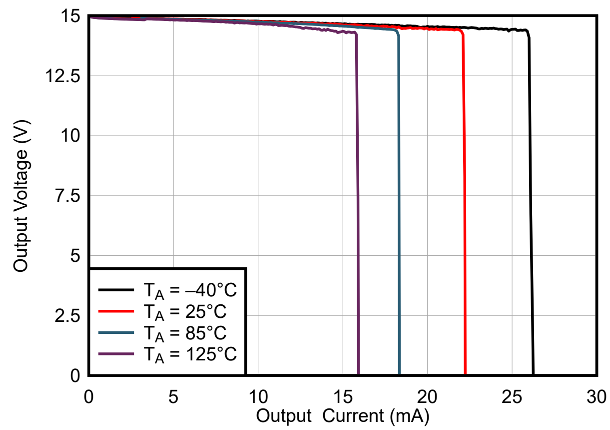


图 6-28. Output Voltage Swing vs Output Sourcing Current

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

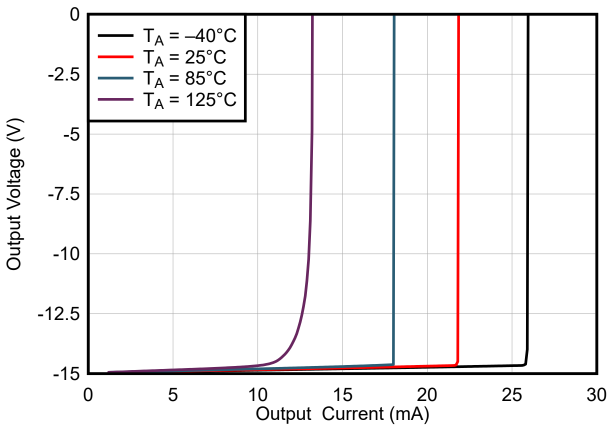


图 6-29. Output Voltage Swing vs Output Sinking Current

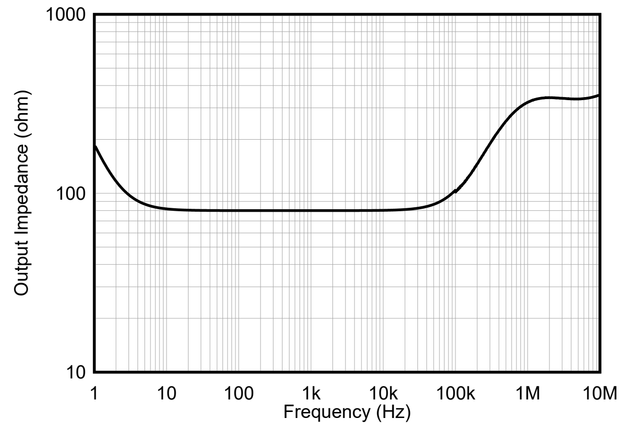


图 6-30. Open-Loop Output Impedance vs Frequency

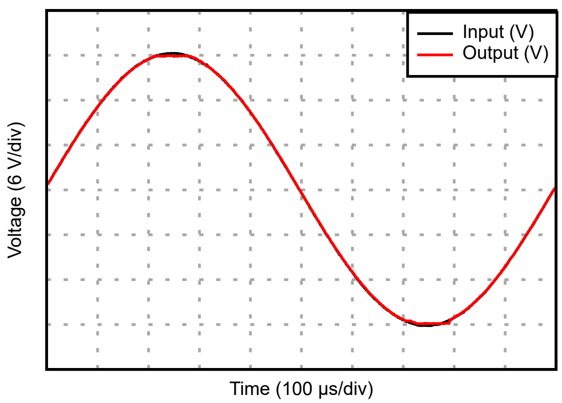


图 6-31. No Phase Reversal

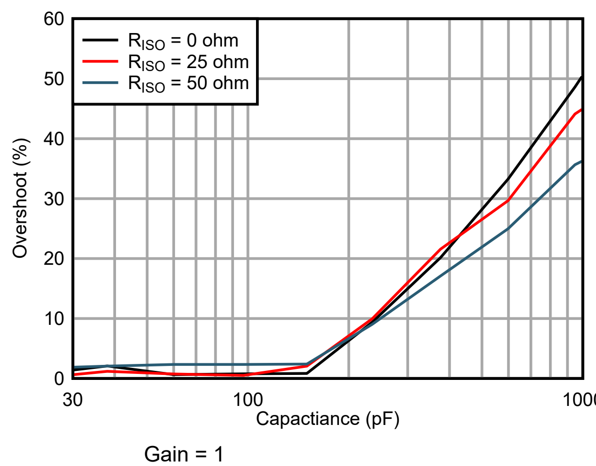


图 6-32. Small-Signal Overshoot vs Capacitive Load, Gain = +1

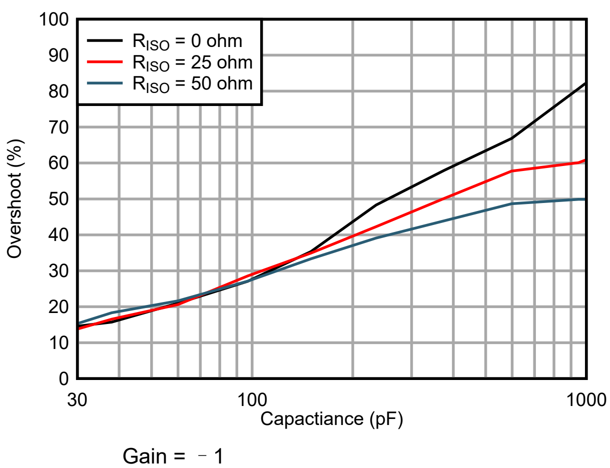


图 6-33. Small-Signal Overshoot vs Capacitive Load, Gain = －1

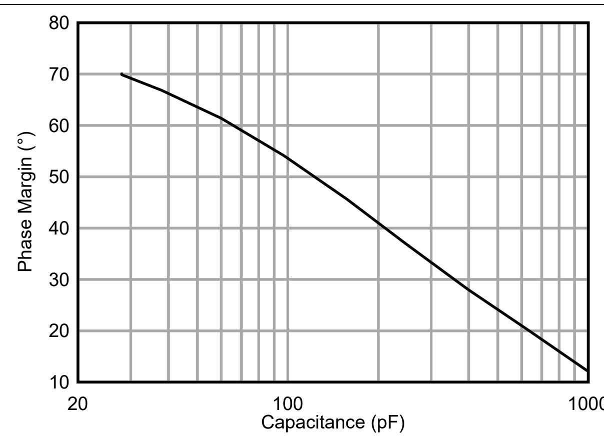
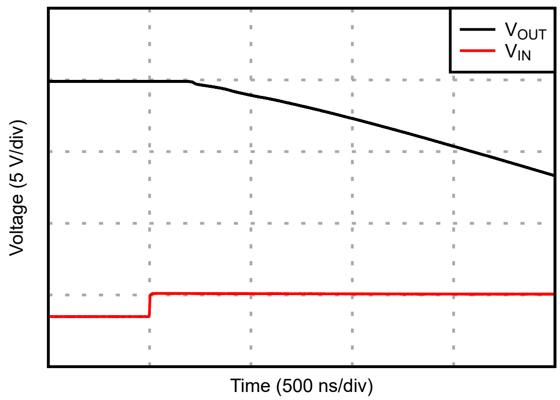


图 6-34. Phase Margin vs Capacitive Load

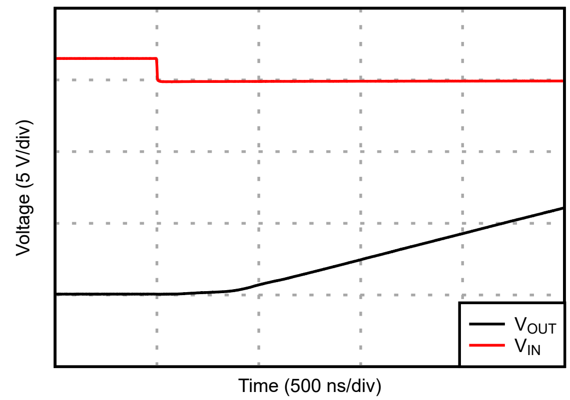
6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)



Gain = –1

图 6-35. Positive Overload Recovery, Gain = –1



Gain = –1

图 6-36. Negative Overload Recovery, Gain = –1

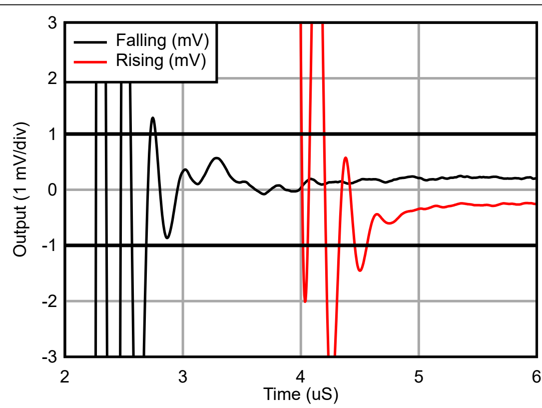
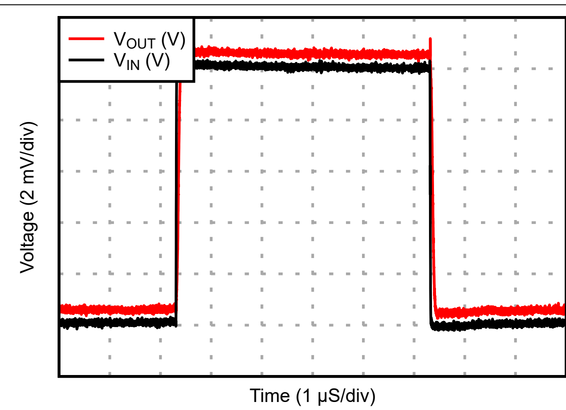
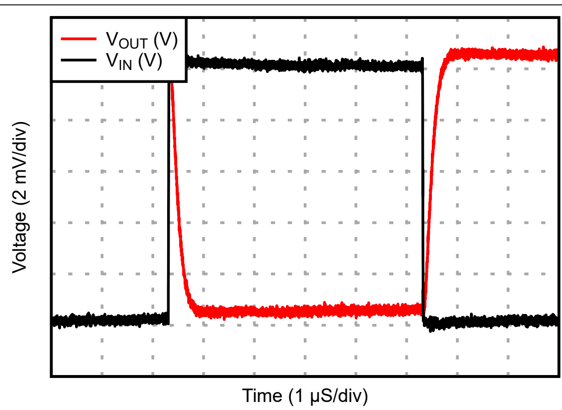


图 6-37. Settling Time



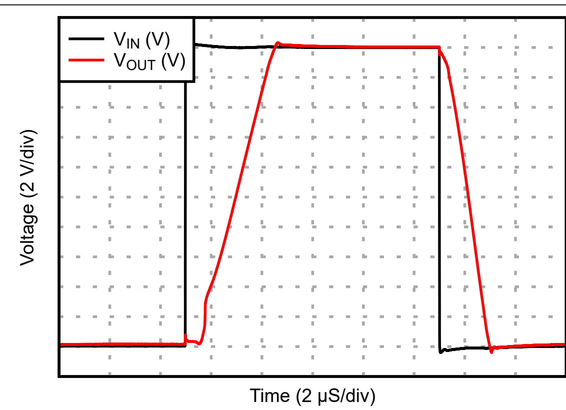
Gain = 1

图 6-38. Small-Signal Step Response, Gain = +1



Gain = –1

图 6-39. Small-Signal Step Response, Gain = –1

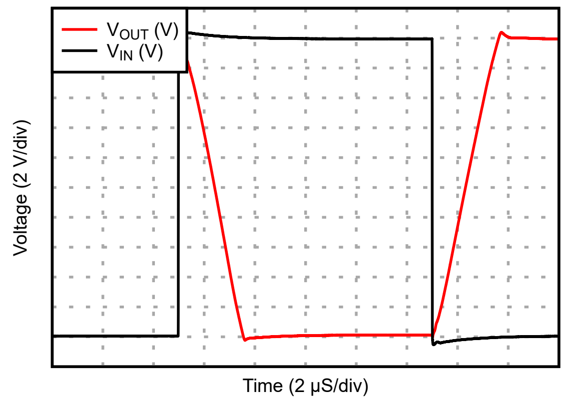


Gain = 1

图 6-40. Large-Signal Step Response, Gain = +1

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)



Gain = –1

图 6-41. Large-Signal Step Response, Gain = –1

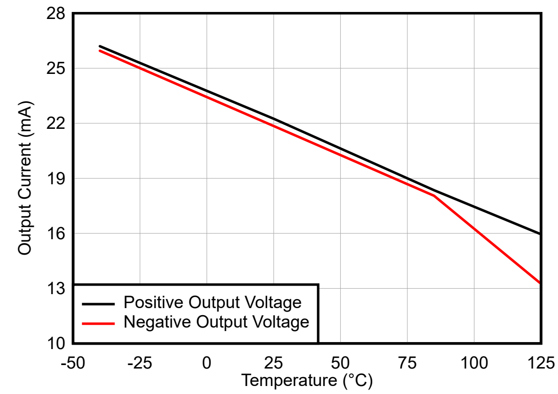


图 6-42. Short-Circuit Current vs Temperature

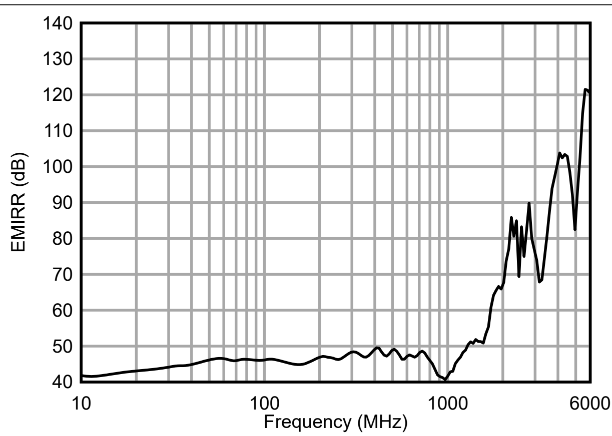


图 6-43. Electromagnetic Interference Rejection

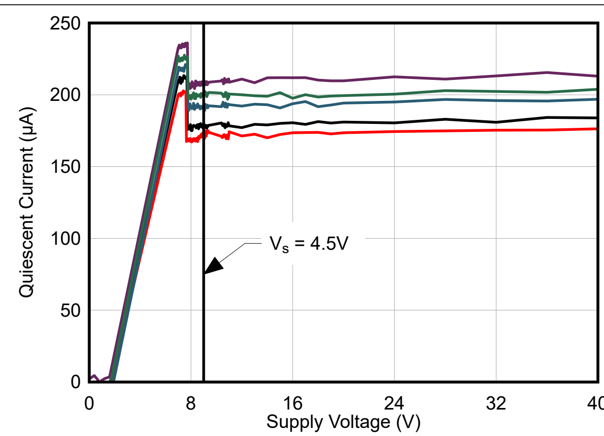


图 6-44. Quiescent Current vs Supply Voltage

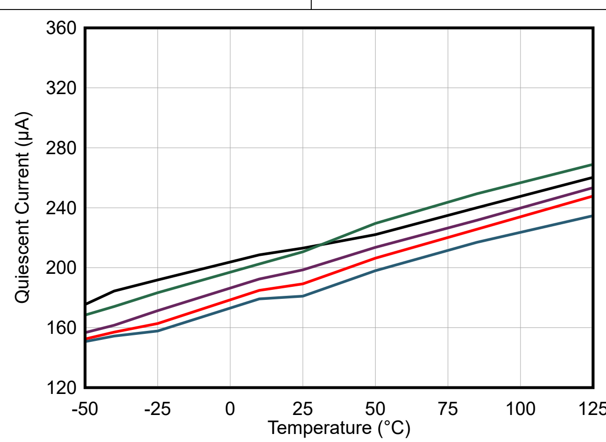


图 6-45. Quiescent Current vs Temperature

7 Parameter Measurement Information

7.1 Typical Specifications and Distributions

To design a more robust circuit, designers often have questions about a typical specification of an amplifier. As a result of natural variations in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, such as the input bias current of an amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions. Circuit designers can leverage this information to guard-band their system, even when there is no minimum or maximum specification in the *Electrical Characteristics*.

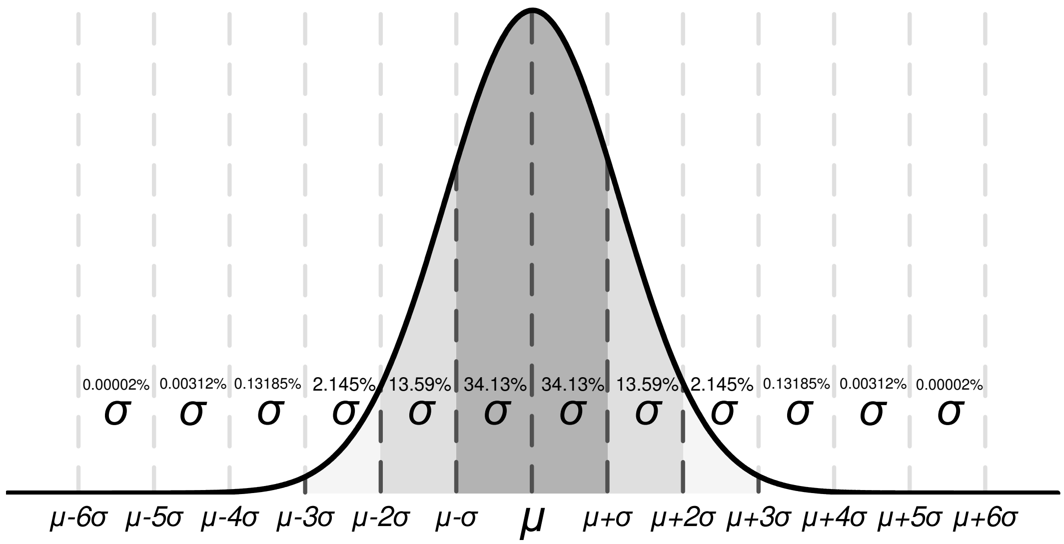


图 7-1. Ideal Gaussian Distribution

图 7-1 shows an example distribution, where *μ*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ* – σ to *μ* + σ).

Depending on the specification, values listed in the *typical* column of *Electrical Characteristics* are represented in different ways. As a general guideline, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (for example, input bias current), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Use this chart to calculate the approximate probability of a specification in a unit. For example, the OPAx205 typical input bias current is ±0.1 nA; therefore, 68.2% of all devices are expected to have an input bias from ±0.1 nA. At 4 σ, 99.9937% of the distribution has an input bias less than ±0.28 nA, which means that 0.0063% of the population is outside of these limits, and corresponds to approximately 1 in 15,873 units.

Units that are found to exceed any tested minimum or maximum specifications are removed from production material. For example, the OPAx205 have a maximum input bias of ±0.5 nA at 25°C. Although this value corresponds to approximately 6 σ (approximately 1 in 500 million units), TI removes any unit with a larger input bias from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for your application, and design worst-case conditions using this value. Use this information to only estimate the performance of a device.

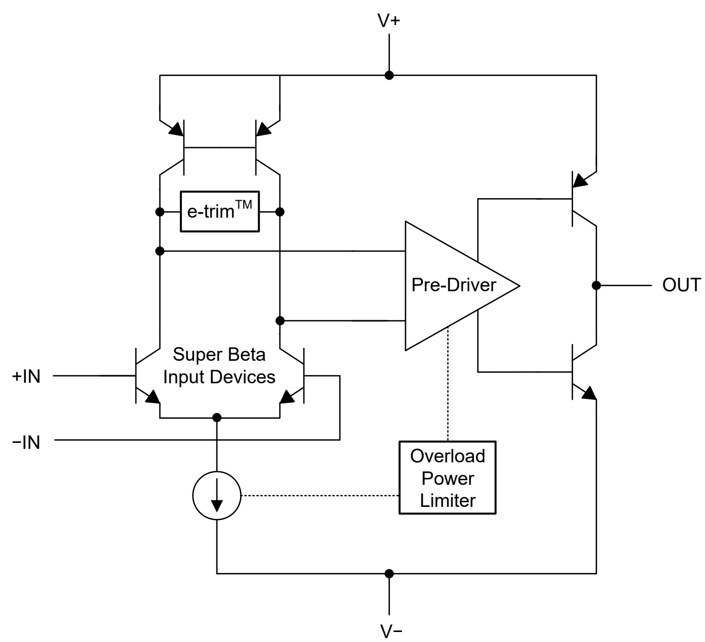
8 Detailed Description

8.1 Overview

The OPAx205 are the first 36-V bipolar, e-trim operational amplifiers that uses a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device has been assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. These devices also feature super-beta inputs that decrease the input bias current and input current noise.

The following section shows the simplified diagram of the OPAx205.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Offset Trimming

The OPAx205 are the industry's first e-trim operational amplifiers built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the input transistors. The offset can be minimized using laser-trimming performed during the manufacturing process while the devices are still in the bare silicon form. However, when the silicon is packaged, the packaging process introduces additional offset due to mechanic stresses. TI's new trimming processes are used to trim the offset after the packaging process is complete to minimize both inherent and package-induced offsets. After trimming, communication is disabled to make sure the amplifiers operate properly in the final system.

A comparison between production offset values for the industry-popular, laser-trimmed OPA2277 and the OPAx205 proprietary trim can be seen in 图 8-1 and 图 8-2.

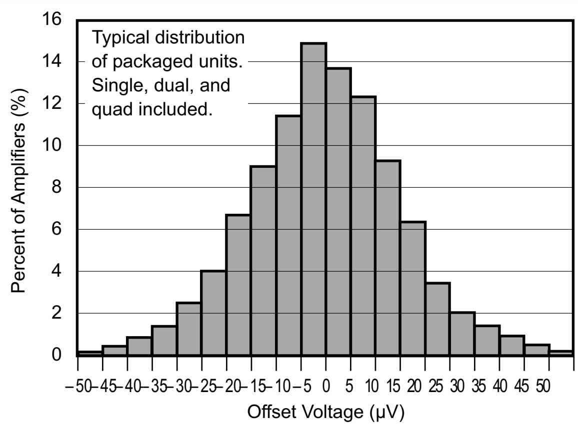


图 8-1. OPA2277 Laser-Trimmed Operational Amplifier Offset

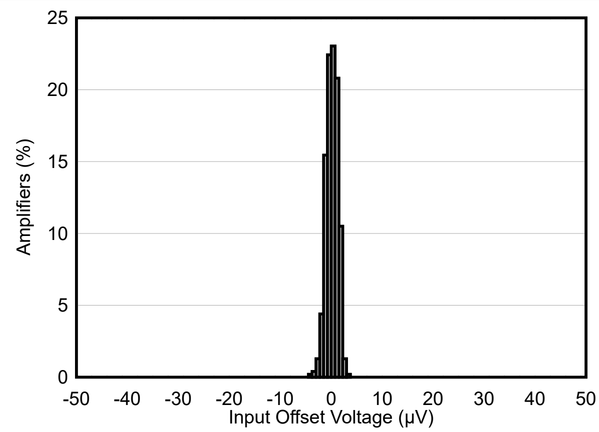


图 8-2. OPAx205 e-trim™ Operational Amplifier Offset

The OPAx205 are also trimmed at two temperatures to minimize the input offset voltage drift over temperature. The final performance of the offset drift can be seen in 图 8-3.

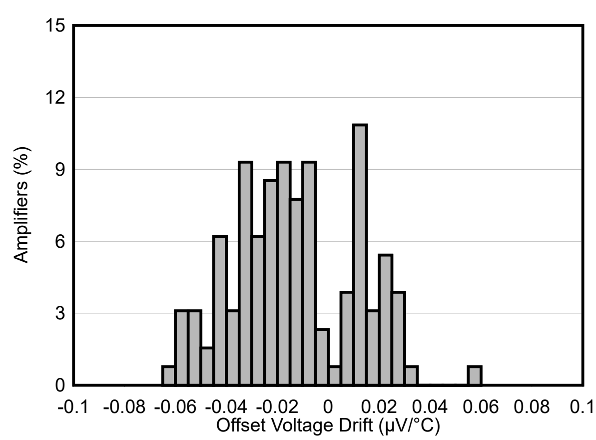


图 8-3. OPAx205 e-trim™ Operational Amplifier Drift

8.3.2 Lower Input Bias With Super-Beta Inputs

The OPAx205 have a super-beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super-beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super-beta input reduces the input bias current of the amplifier. In addition, the super-beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of the OPA2277 and the OPAx205 super-beta input bias currents can be seen in 图 8-4 and 图 8-5.

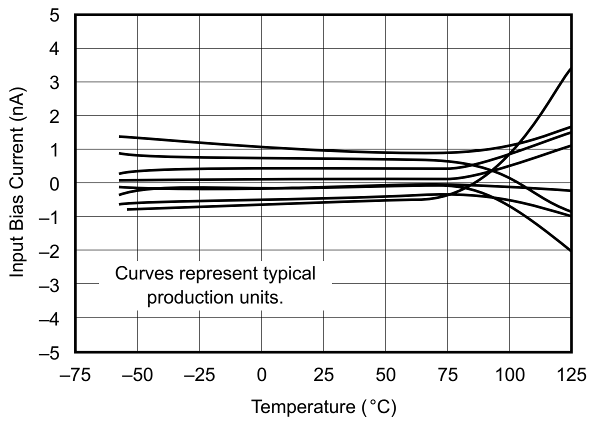


图 8-4. OPA2277 Input Bias Current

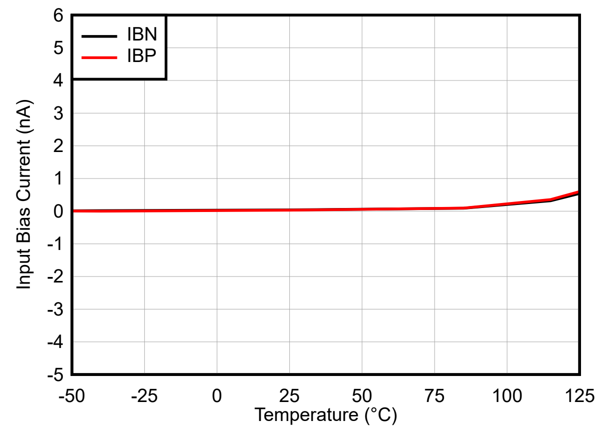


图 8-5. OPAx205 Super-Beta Input Bias Current

8.3.3 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (that is, the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPAx205 have an advanced output stage design that eliminates this problem. When the output voltage reaches either supply (V+ or V–), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by large external transient voltage.

8.3.4 EMI Rejection

The OPAx205 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources, such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the *EMI Rejection Ratio of Operation Amplifiers* application report.

8.4 Device Functional Modes

The OPAx205 have a single functional mode and are operational with any supply between 4.5 V (±2.25 V) and 36 V (±18 V).

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The OPAx205 are unity-gain stable operational amplifiers with very low offset voltage, offset voltage drift, voltage noise, current noise and power consumption. These features make this device family a great choice for a variety of space-constrained and power-constrained systems.

9.2 Typical Applications

9.2.1 High-Precision Signal-Chain Input Buffer

A common application for the OPAx205 is an input buffer for the signal chain of a data acquisition (DAQ) or field instrumentation system. This amplifier family is selected because of the low offset and drift that maintain system accuracy across a variety of operating conditions. The low power consumption of the OPAx205 enables the device to be used in battery-operated or high-density applications, where thermal dissipation is difficult. The low 1/f (flicker) noise and broadband noise allow for higher-accuracy signal chains, such as those using a 24-bit delta-sigma analog-to-digital converter (ADC). If a higher sampling rate is needed, the OPAx205 can be paired with a fully differential amplifier, such as the THP210, to drive the ADC inputs. 图 9-1 shows the OPA2205 configured as an input buffer to a differential ADC driver.

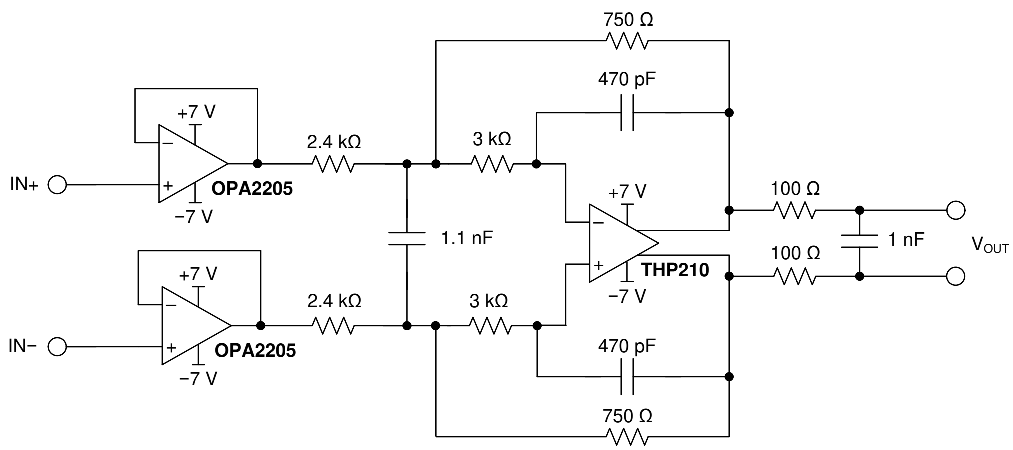


图 9-1. OPA2205 Configured as a DAQ Input Buffer

9.2.1.1 Design Requirements

The design requirements for this application are:

- Input range: ±10 V
- Input frequency: 10 kHz
- Output voltage: ±3.3 V
- Quiescent current: < 1.5 mA

9.2.1.2 Detailed Design Procedure

In this application, the input signal ranges from – 10 V to +10 V with a frequency of up to 10 kHz. Because of possible portable-use cases for this data acquisition system (DAQ), low power consumption is required to minimize battery drain and thermal dissipation requirements.

To maintain high system accuracy the OPA2205 is selected as input buffers. This device is selected because of the high dc precision (4 µV offset and 0.08 µV/°C offset drift), low flicker noise (0.2 µVpp), and low quiescent current (220 µA). The buffers are followed by a high-precision, fully differential amplifier such as the THP210, which is capable of accurately driving a 24-bit, fully differential ADC such as the ADS127L01.

9.2.1.3 Application Curves

The gain plot for this system can be seen in 图 9-2. This plot shows proper attenuation of the ±10-V signal to the target ±3.3-V output, and adequate bandwidth to support the input frequency range.

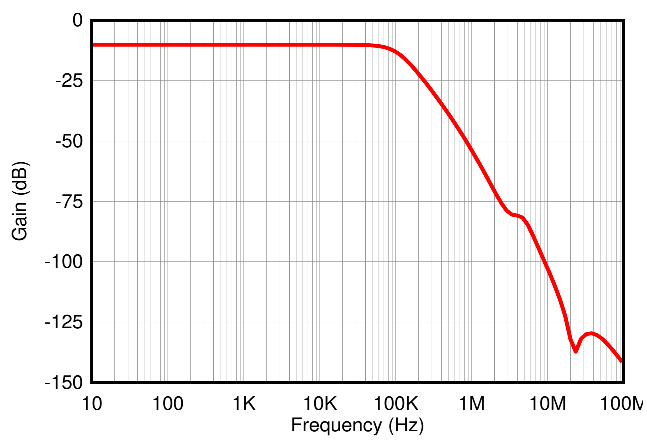


图 9-2. Gain Plot of DAQ Front End

9.2.2 Discrete, Two-Op-Amp Instrumentation Amplifier

图 9-3 shows the OPA2205 configured as a two-op-amp, discrete instrumentation amplifier. This configuration allows for a differential signal measurement, such as the signal from a load cell, with higher input impedance to the signal chain than most monolithic instrumentation amplifiers. The strong ac and dc performance of the OPA2205 enables high accuracy measurements.

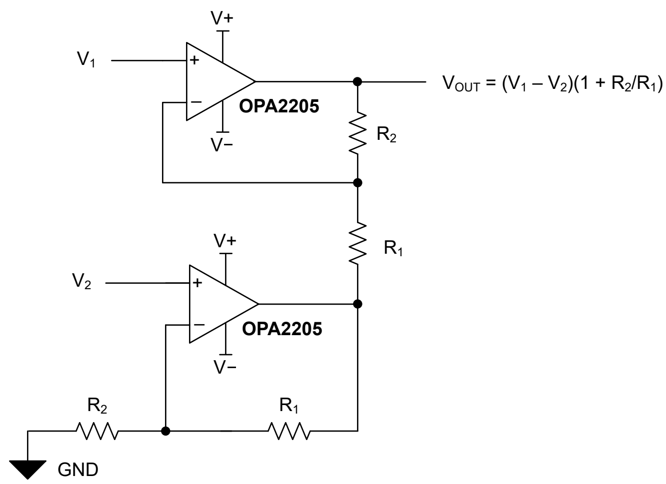


图 9-3. OPA2205 Configured as a Two-Op-Amp, Discrete Instrumentation Amplifier

9.2.3 Second-Order Low-Pass Filter

The OPAx205 has a very-low broadband voltage noise of only 7.2 nV/$\sqrt{Hz}$ and flicker noise of 0.2 µV_{PP} given the low power consumption of only 220 µA, making this device an excellent choice for low-power filter applications. 图 9-4 is an example of one channel of the OPAx205 configured as a second-order low-pass filter with a cutoff frequency of 50 kHz.

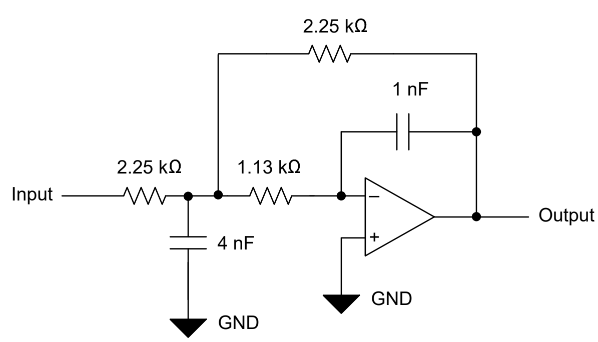


图 9-4. Second-Order Low-Pass Filter

9.3 Power Supply Recommendations

The OPAx205 operate with a power supply between 4.5 V to 36 V (±2.25 V to ±18 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in 节 6.9.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 9.4.1.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 9-5, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.4.2 Layout Example

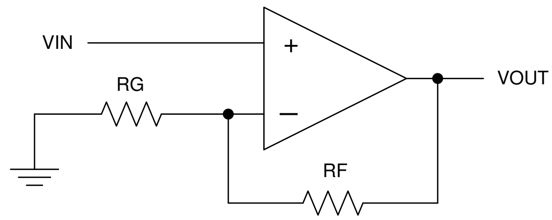


图 9-5. Schematic Representation

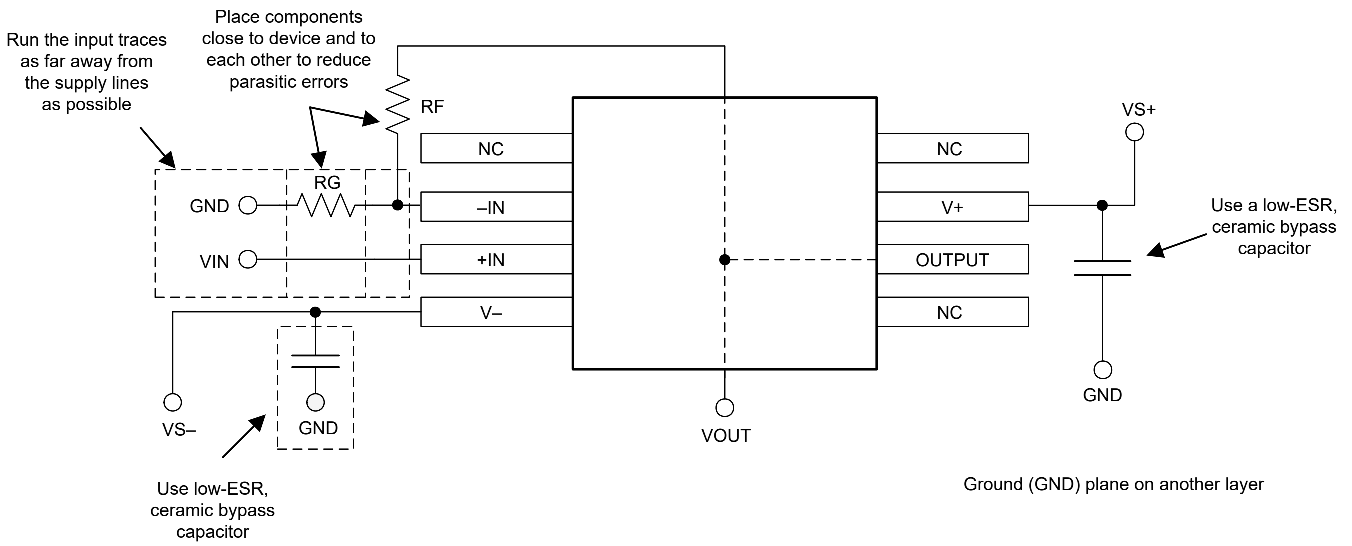


图 9-6. Operational Amplifier Board Layout for Noninverting Configuration

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

The following evaluation modules are available:

- DIP-ADAPTER-EVM
- DIYAMP-EVM

10.1.1.1 PSpice® for TI

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

10.2 文档支持

10.2.1 相关文档

请参阅以下相关文档：

- 德州仪器 (TI)，*DIP-ADAPTER-EVM* 用户指南
- 德州仪器 (TI)，*DIYAMP-SOIC-EVM* 用户指南

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.5 Trademarks

e-trim™ and TI E2E™ are trademarks of Texas Instruments.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
所有商标均为其各自所有者的财产。

10.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA205ADR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP205A
OPA205ADR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP205A
OPA205ADT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP205A
OPA205ADT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP205A
OPA2205ADGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5
OPA2205ADGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5
OPA2205ADGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5
OPA2205ADGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5
OPA2205ADR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2205A
OPA2205ADR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2205A
OPA2205ADT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2205A
OPA2205ADT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2205A
OPA4205ADR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4205A
OPA4205ADR.B	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
OPA4205ADT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4205A
OPA4205ADT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
OPA4205APWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4205A
OPA4205APWR.B	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
OPA4205APWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4205A
OPA4205APWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

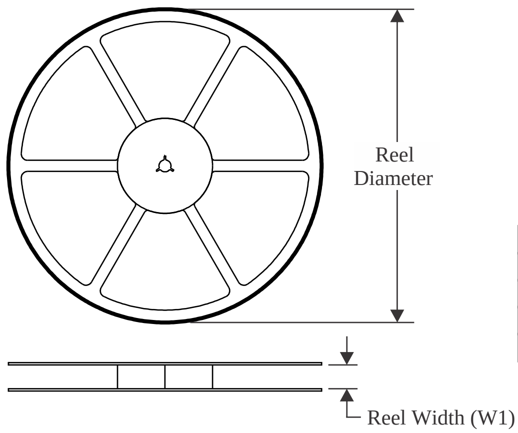
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

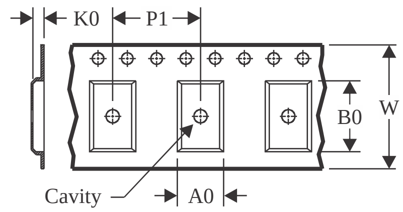
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

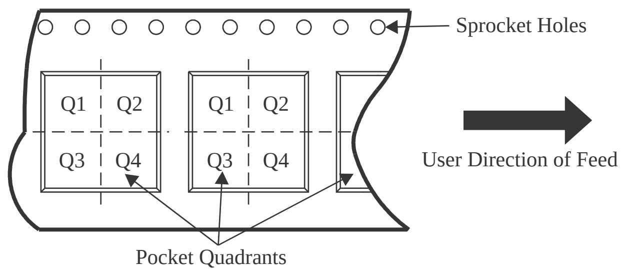


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

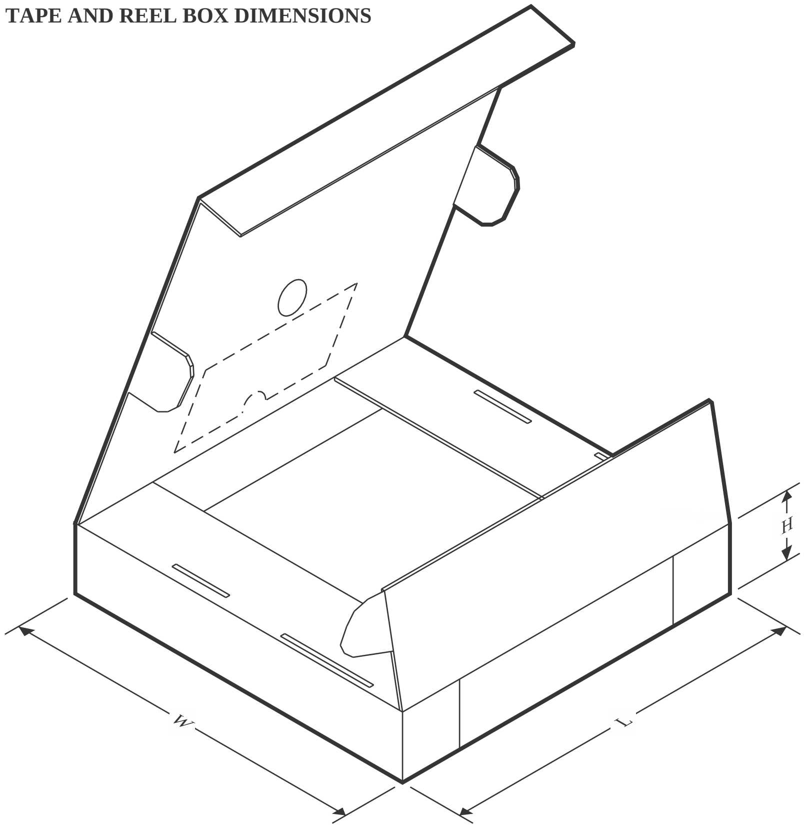
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

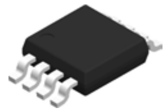
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA205ADR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA205ADT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2205ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2205ADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2205ADR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2205ADT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4205ADR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4205ADT	SOIC	D	14	250	180.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

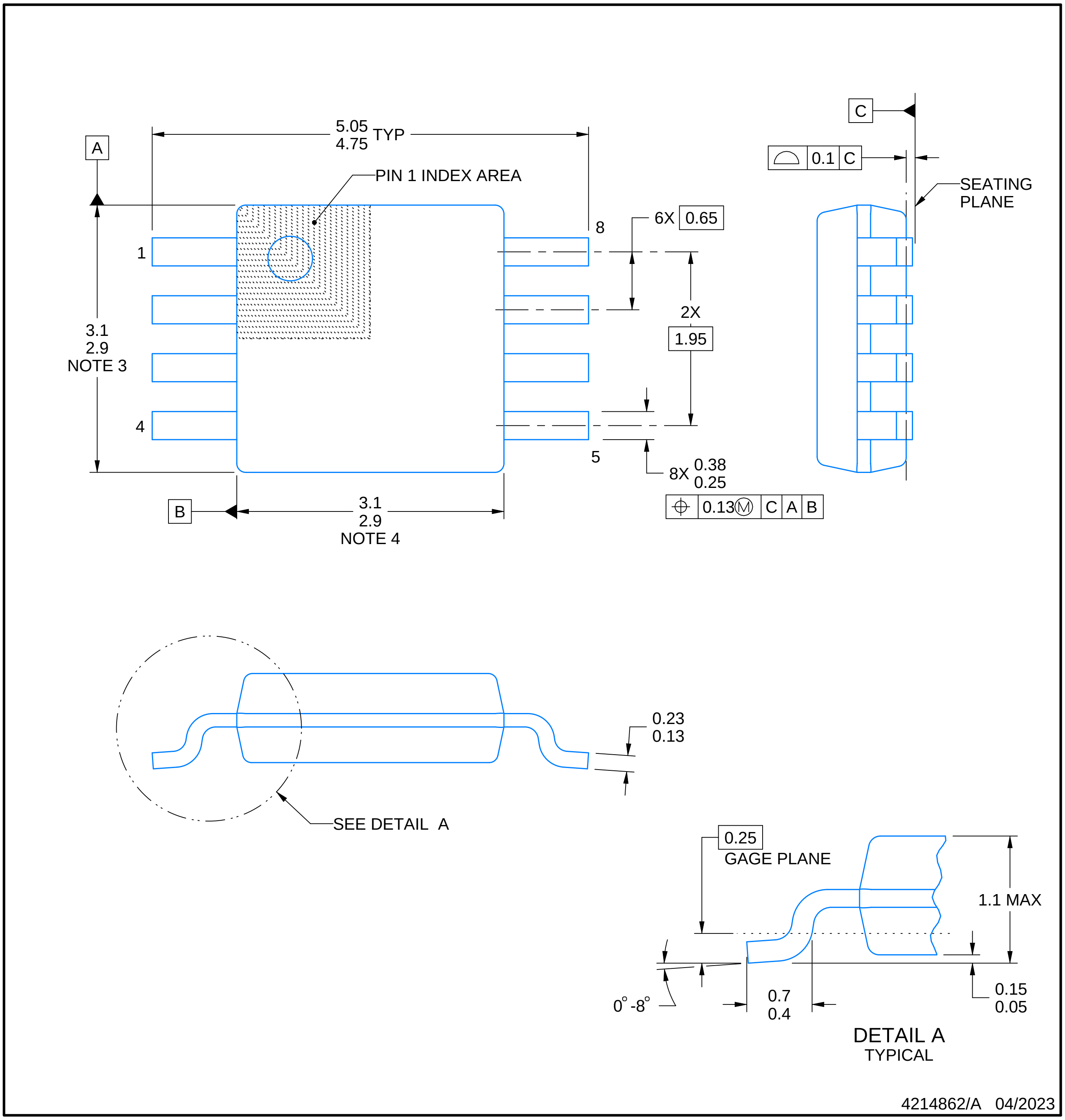
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA205ADR	SOIC	D	8	3000	353.0	353.0	32.0
OPA205ADT	SOIC	D	8	250	213.0	191.0	35.0
OPA2205ADGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2205ADGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2205ADR	SOIC	D	8	3000	353.0	353.0	32.0
OPA2205ADT	SOIC	D	8	250	213.0	191.0	35.0
OPA4205ADR	SOIC	D	14	3000	353.0	353.0	32.0
OPA4205ADT	SOIC	D	14	250	213.0	191.0	35.0



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

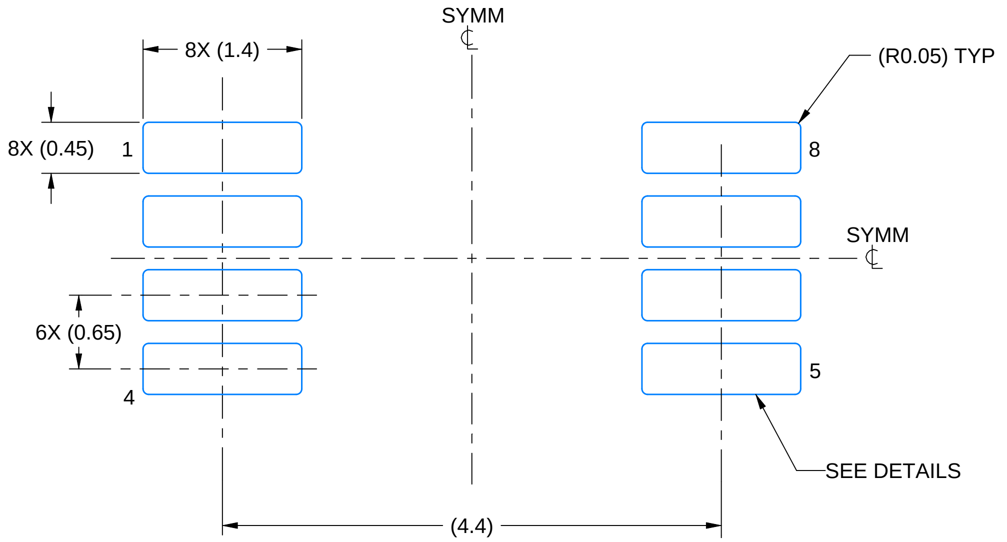
SMALL OUTLINE PACKAGE



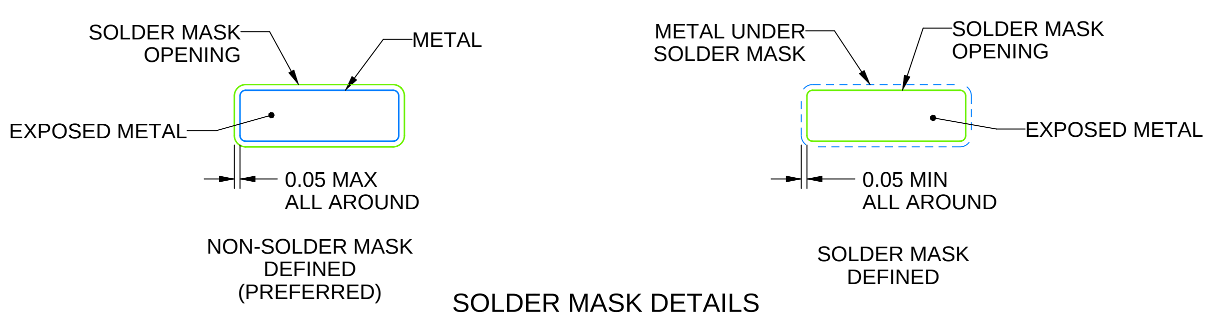
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

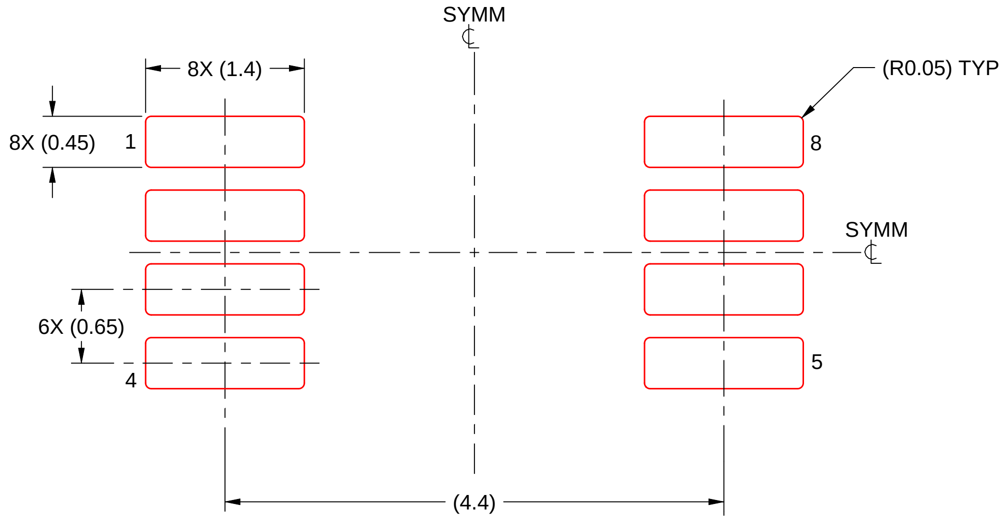


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

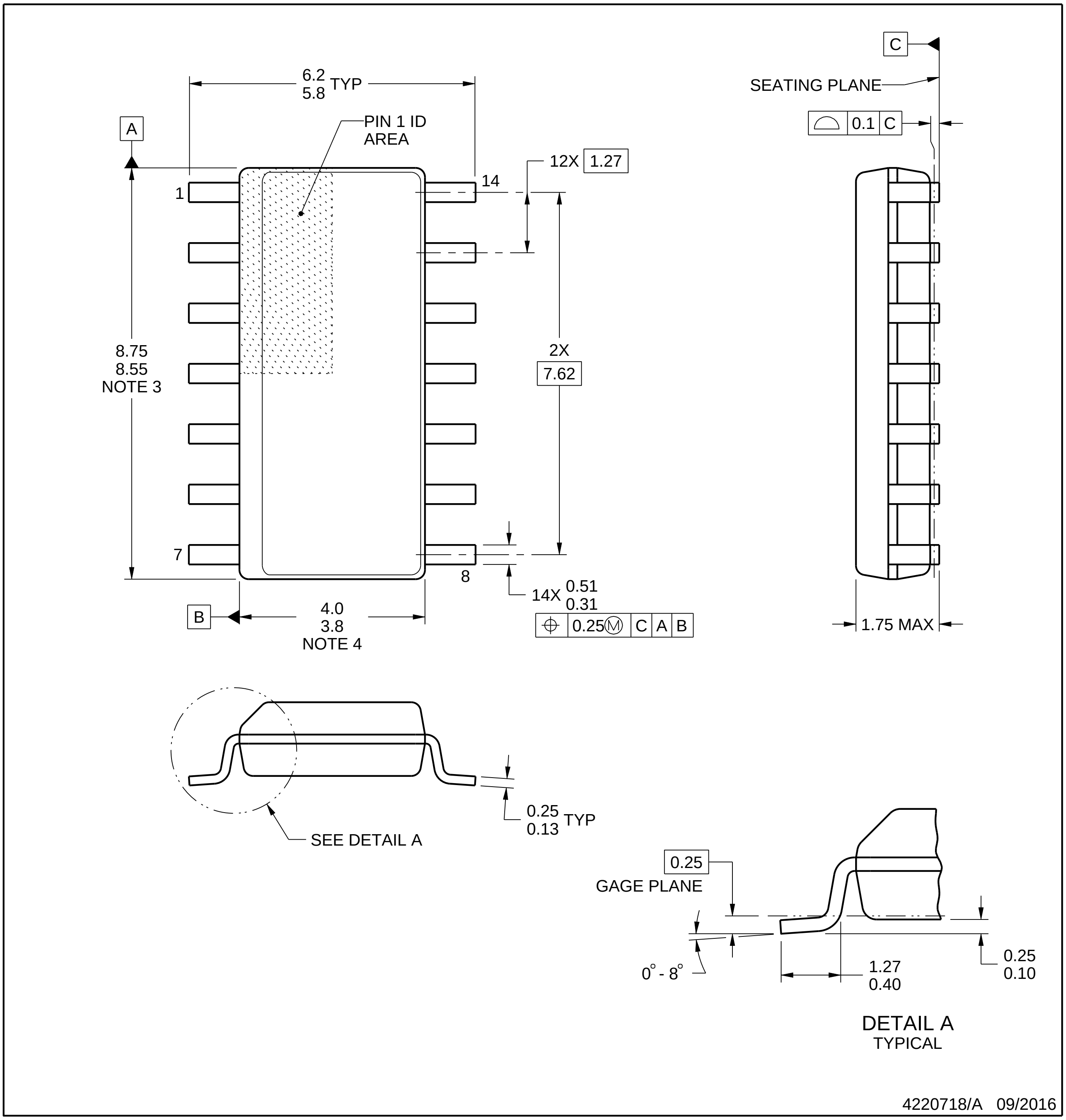


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

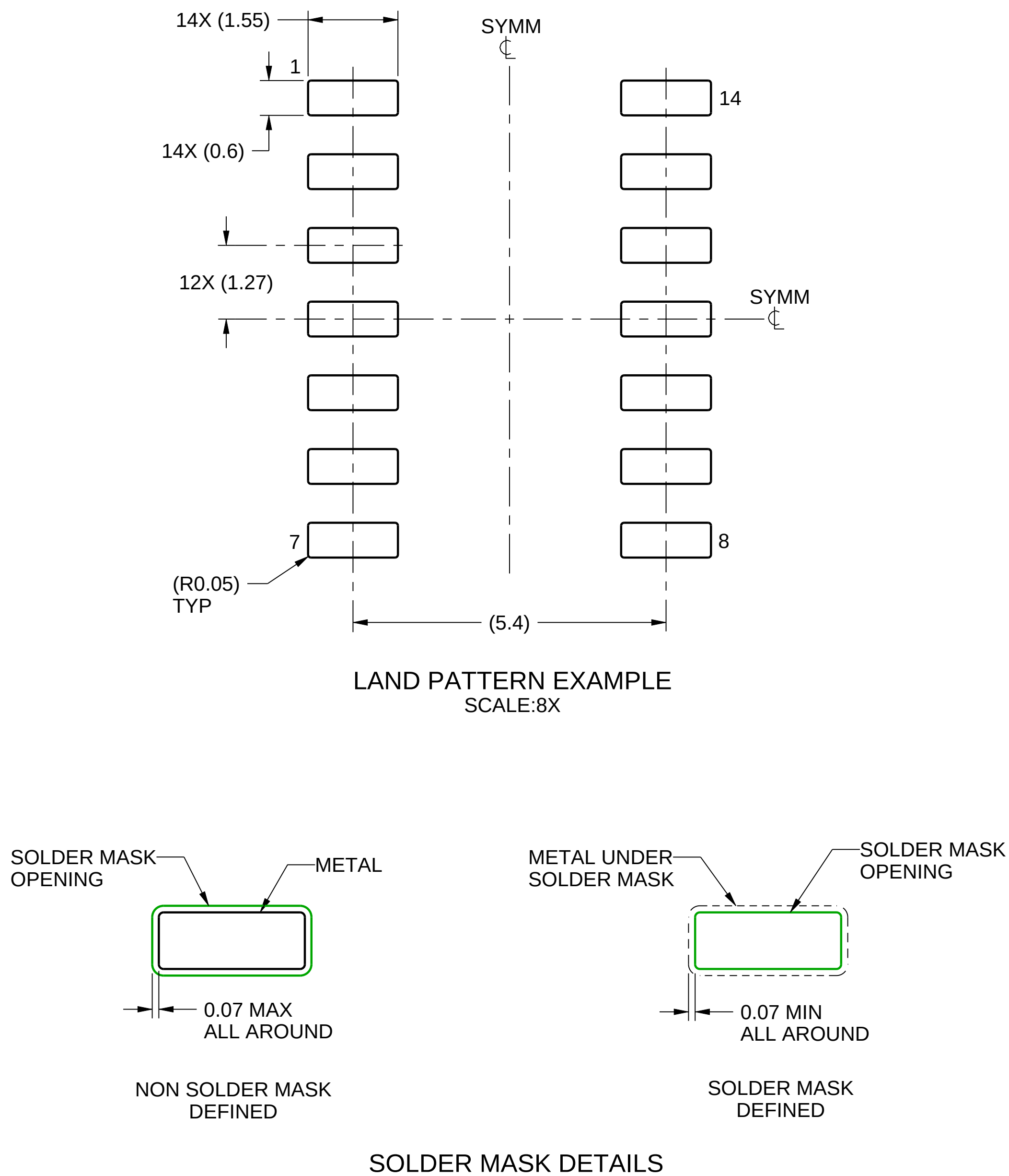
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



NOTES:

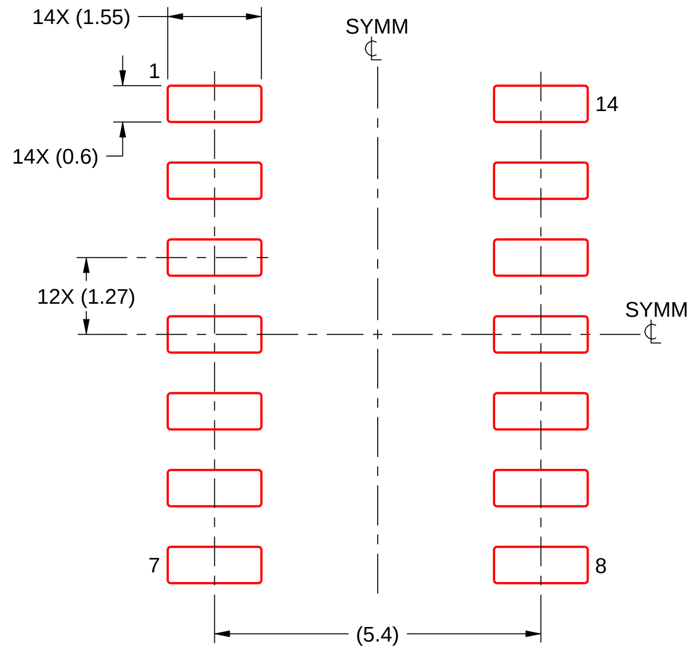
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

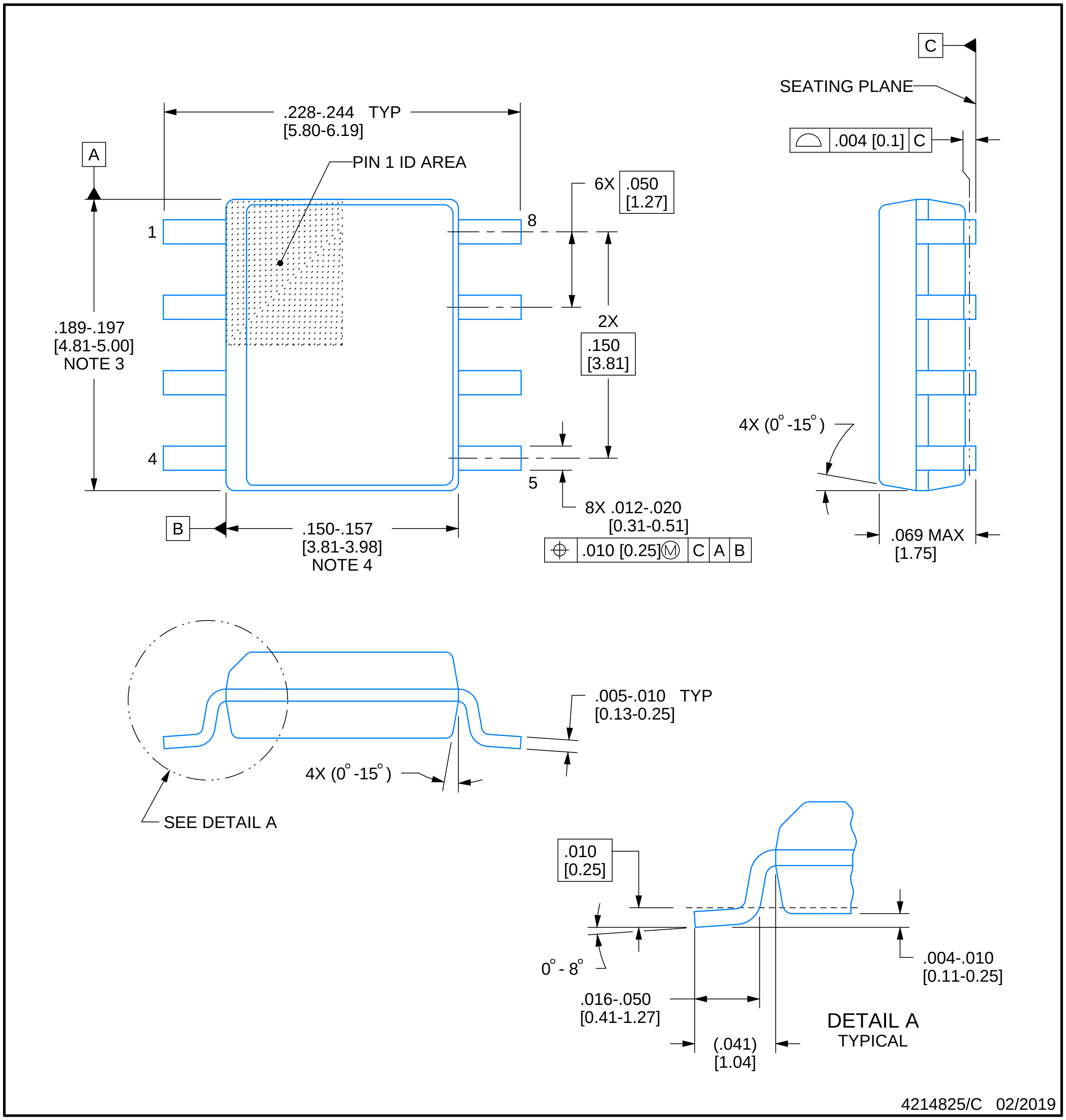


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

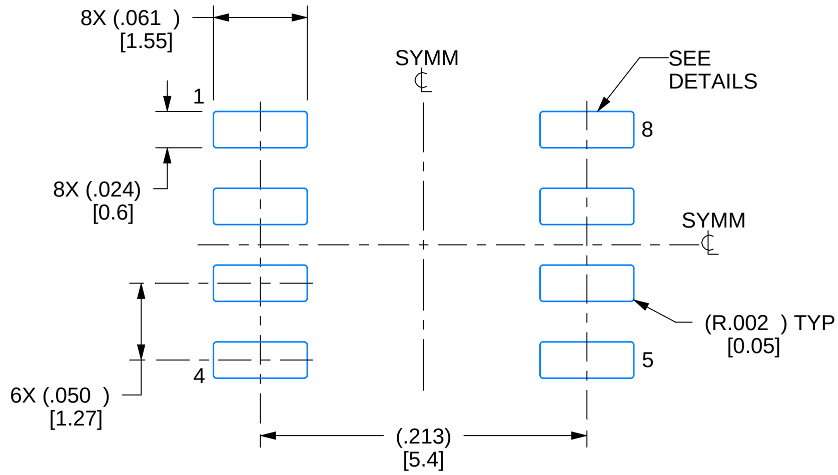
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

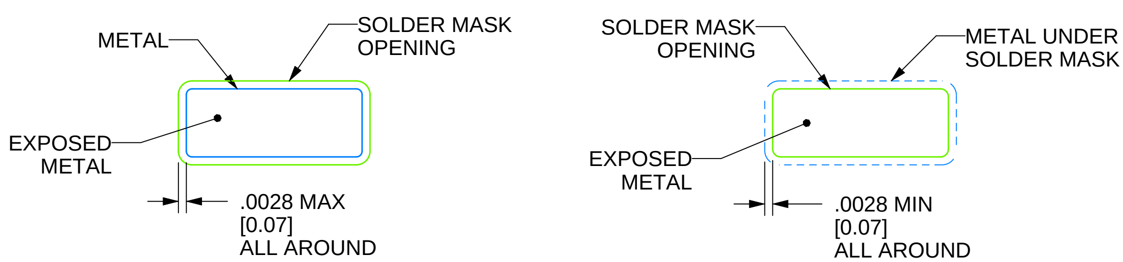


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

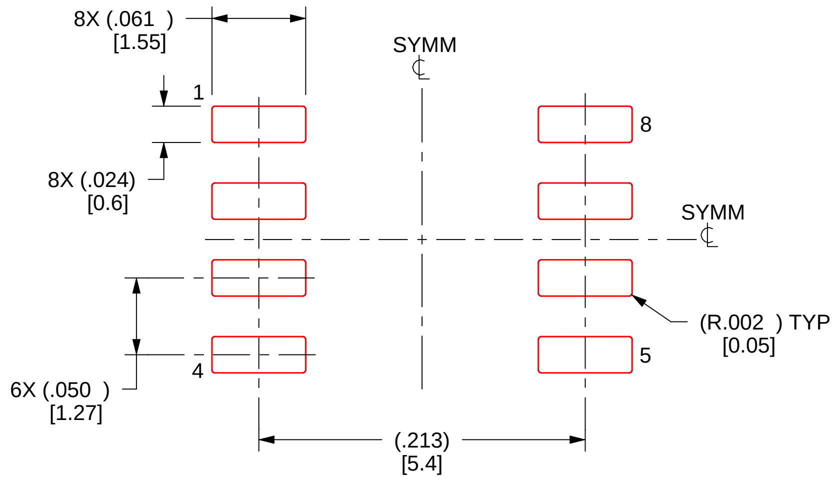
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

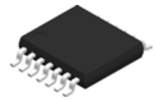


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

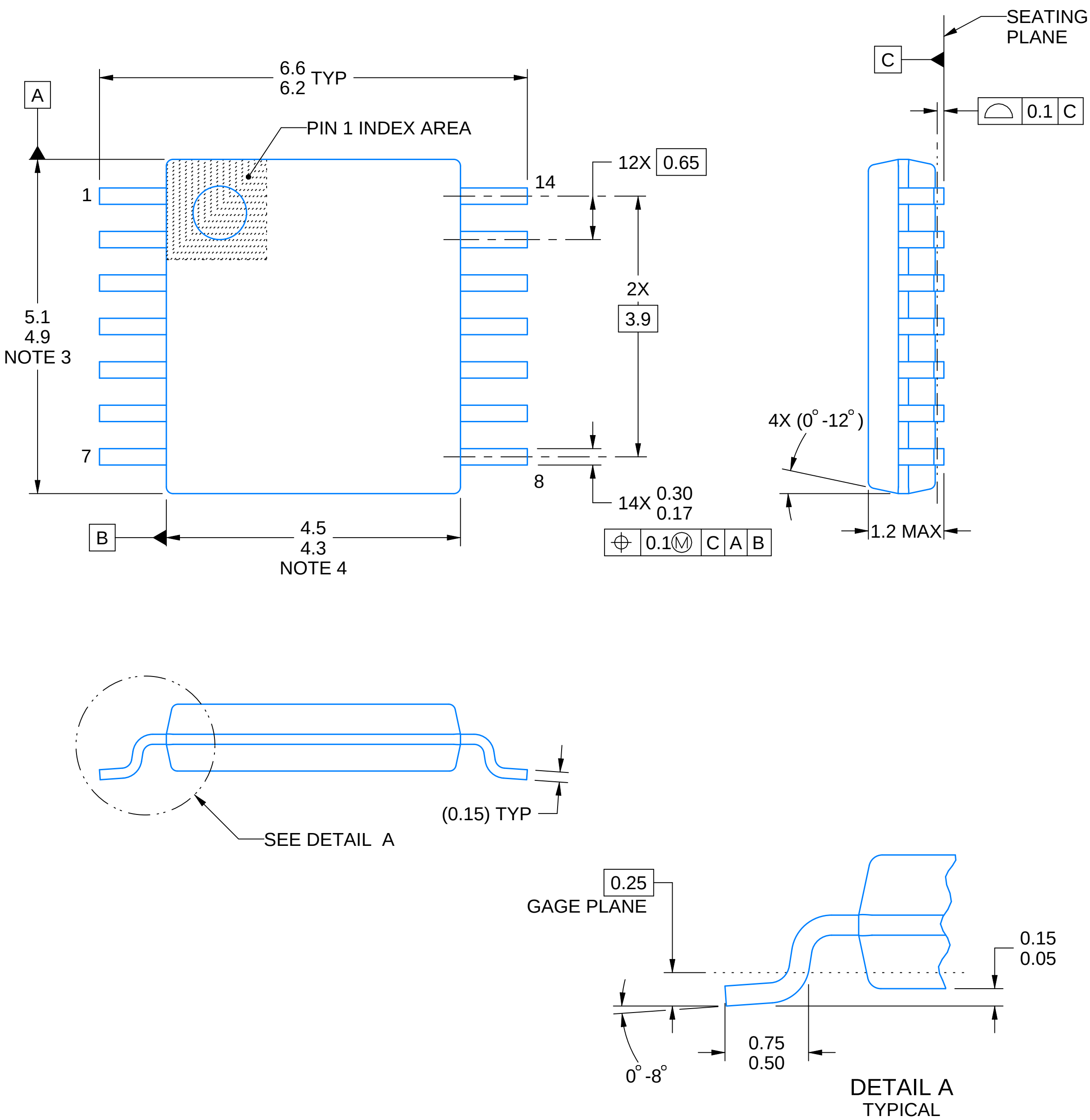
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

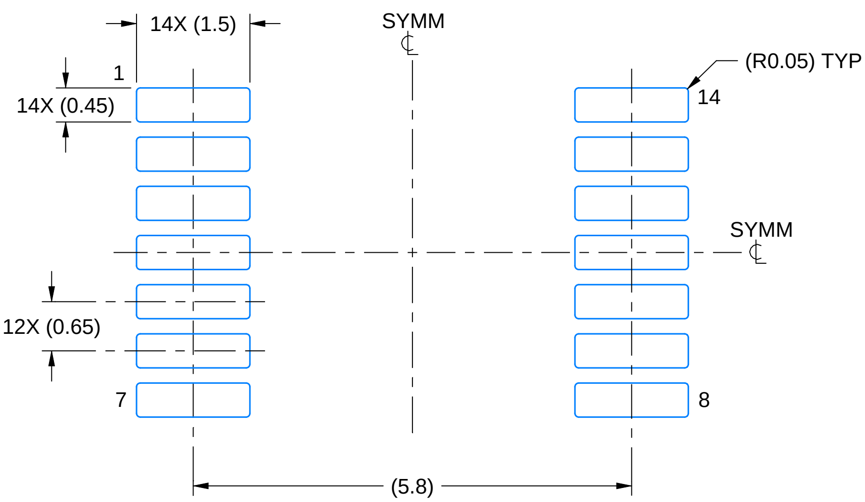
SMALL OUTLINE PACKAGE



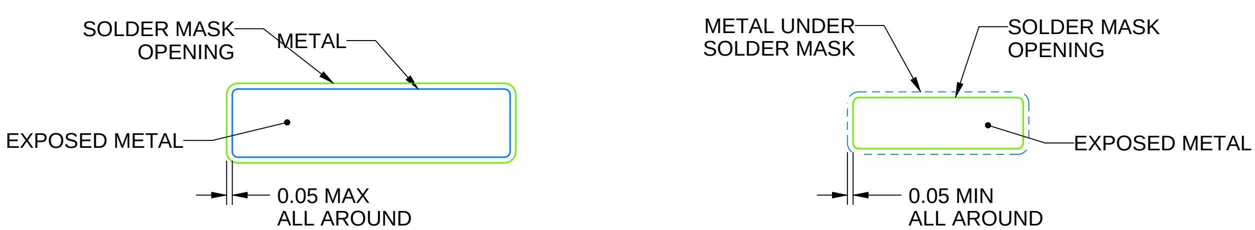
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

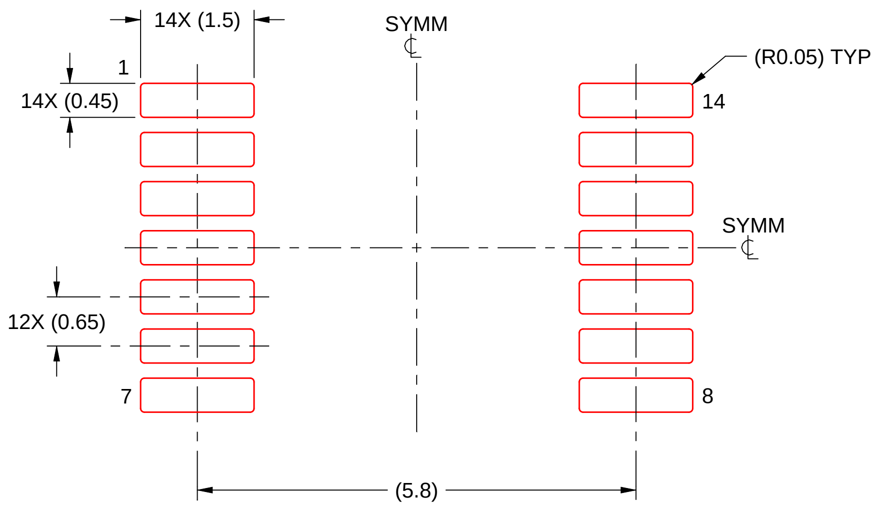
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265