OPA2333-Q1 汽车类 1.8V 微功耗 CMOS 零温漂运算放大器

1 特性

- 符合面向汽车应用的 AEC 标准
  - 温度等级 1：–40°C 至 +125°C，T_A
- 低失调电压：23μV（最大值）
- 0.01Hz 至 10Hz 噪声：1.1μV_{PP}
- 静态电流：17μA
- 单电源供电
- 电源电压：1.8V 至 5.5V
- 轨至轨输入/输出
- 封装：8 引脚 SOIC 和 VSSOP

2 应用

- 泵
- 位置传感器
- 车辆乘员检测传感器
- 制动系统
- 安全气囊

3 说明

这款 CMOS 运算放大器 OPA2333-Q1 使用专有自动校准技术，可在随时间推移和温度变化的同时提供超低的失调电压（10μV，最大值）以及几乎为零的温漂。这些高精度、低静态电流微型放大器可提供高阻抗输入（共模范围在电源轨基础上向外扩展了 100mV）和轨至轨输出（摆幅在相对于电源轨 50mV 以内）。此器件可以使用低至 1.8V (±0.9V) 和高达 5.5V (±2.75V) 的单电源或双电源，并且针对低电压、单电源运行情况进行了优化。

OPA2333-Q1 提供出色的高共模抑制比 (CMRR)，而不存在与传统互补输入级关联的交叉。该设计可在驱动模数转换器 (ADC) 的过程中实现优异的性能，而不会降低微分线性。

OPA2333-Q1 的额定工作温度范围为 –40°C 至 +125°C。

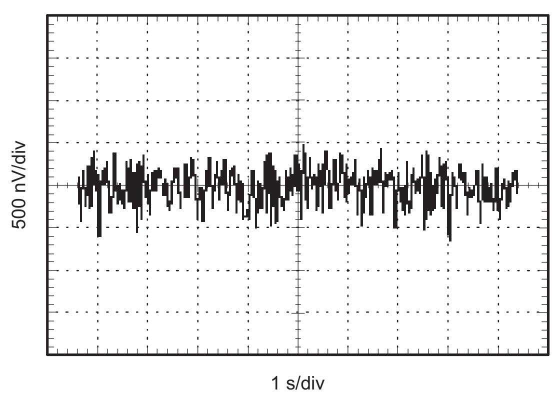
添加了

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
OPA2333-Q1	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

0.1Hz 至 10Hz 噪声



目录

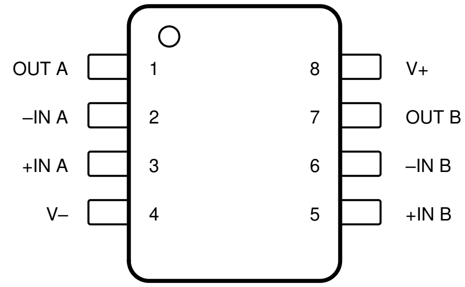
4 修订历史记录

Changes from Revision A (June 2010) to Revision B **Page**

- 已添加 *器件信息* 表、*引脚功能* 表、*ESD 额定值* 表、*建议运行条件* 表、*热性能信息* 表、*特性 说明* 部分、*器件功能模式* 部分，*应用和实施* 部分，*电源相关建议* 部分，*布局* 部分，*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 .. 1
- Changed input offset voltage (over full temp range) from 22 µV to 15 µV in *Electrical Characteristics* table ... 5
- Added maximum value of 0.05 µV/°C to the V_{OS} drift parameter in the *Electrical Characteristics* table ... 5
- Deleted *Thermal resistance* parameter from *Electrical Characteristics* table ... 5

5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Channel A output
2	–IN A	I	Channel A inverting input
3	+IN A	I	Channel A noninverting input
4	V–	—	Negative (lowest) supply voltage
5	+IN B	I	Channel B noninverting input
6	–IN B	I	Channel B inverting input
7	OUT B	O	Channel B output
8	V+	—	Positive (highest) supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage		7	V
V_I	Input voltage, signal input pins[2]	–0.3	(V+) + 0.3	V
	Output short-circuit[3]	Continuous		
T_A	Operating free-air temperature	–40	125	°C
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short circuit to ground, one amplifier per package

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Specified supply voltage	1.8		5.5	V
T_A	Specified free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA2333-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	180.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.0	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_S = 1.8 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		2	10	µV
		V_S = 5 V, T_A = –40°C to +125°C			15	µV
dV_{OS}/d_T	V_{OS} drift	V_S = 5 V, T_A = –40°C to 125°C		0.02	0.05	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5.5 V, T_A = –40°C to +125°C		1	6	µV/V
	Long-term stability (1)			1 (1)		µV
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±70	±200	pA
		T_A = –40°C to +125°C		±150		pA
I_{OS}	Input offset current			±140	±400	pA
NOISE						
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz		1.1		$µV_{PP}$
i_n	Input current noise	f = 10 Hz		100		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode supply voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	102	130		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ, T_A = –40°C to +125°C	104	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = 1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	R_L = 10 kΩ		30	50	mV
		R_L = 10 kΩ, T_A = –40°C to +125°C			85	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive					
	(2)Open-loop output impedance	f = 350 kHz, I_O = 0 A		2		kΩ
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 A		17	25	µA
		I_O = 0 A, T_A = –40°C to +125°C			30	µA
	Turn-on time	V_S = 5 V		100		µs

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.
(2) See the *Typical Characteristics* section.

6.6 Typical Characteristics

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

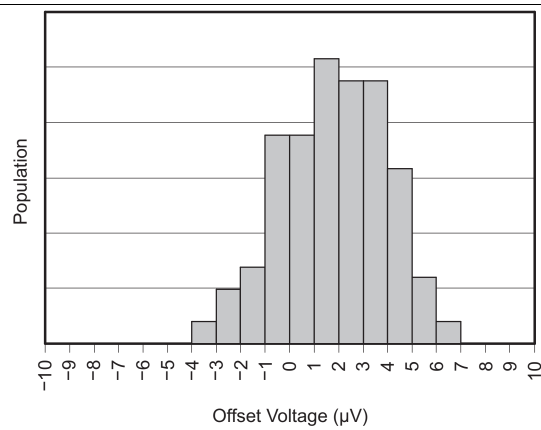


Figure 1. Offset Voltage Production Distribution

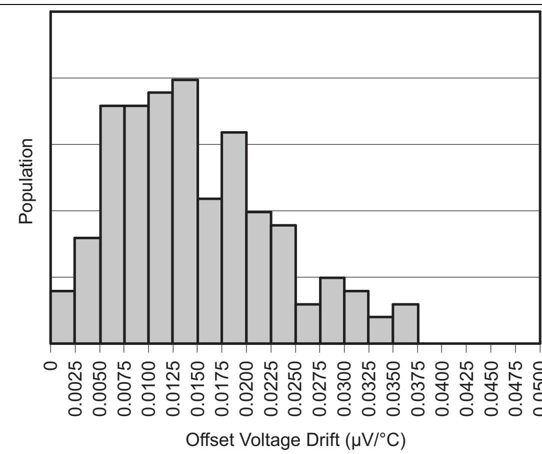


Figure 2. Offset Voltage Drift Production Distribution

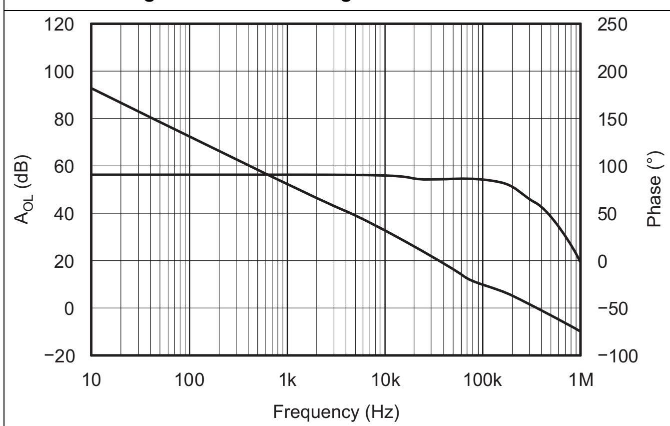


Figure 3. Open-Loop Gain vs Frequency

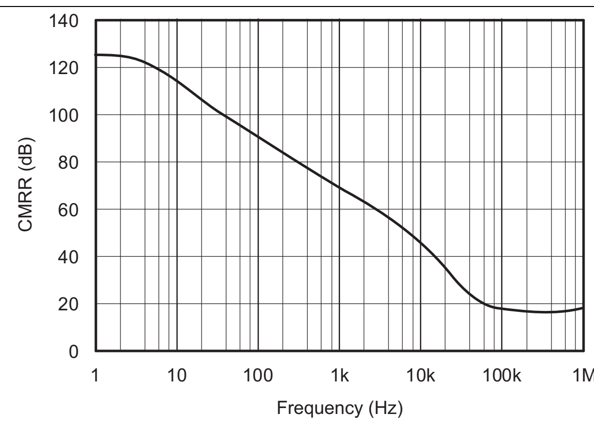


Figure 4. Common-Mode Rejection Ratio vs Frequency

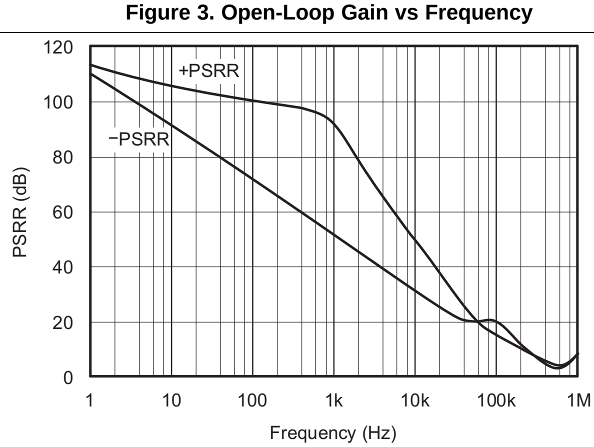


Figure 5. Power-Supply Rejection Range vs Frequency

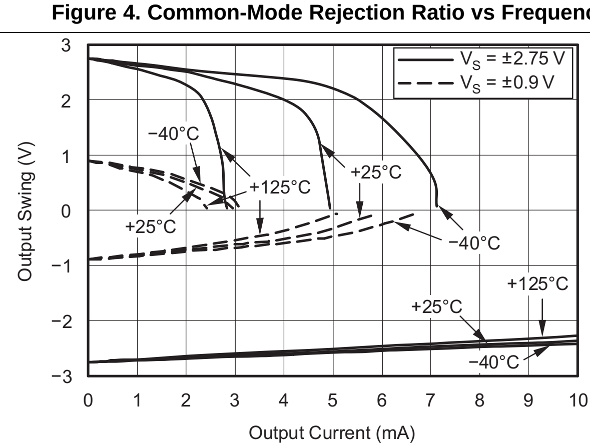


Figure 6. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

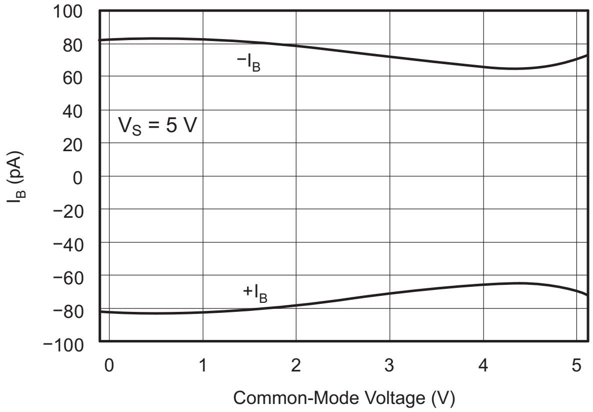


Figure 7. Input Bias Current vs Common-Mode Voltage

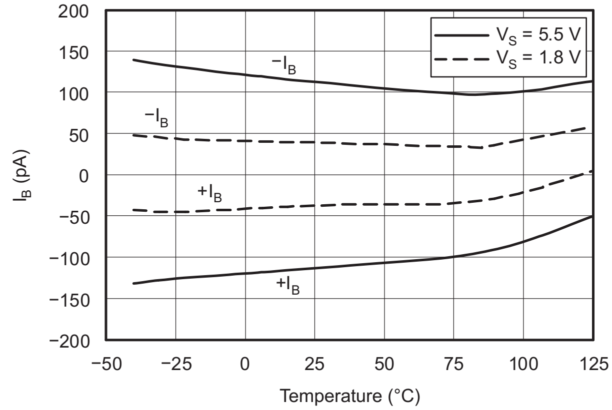


Figure 8. Input Bias Current vs Temperature

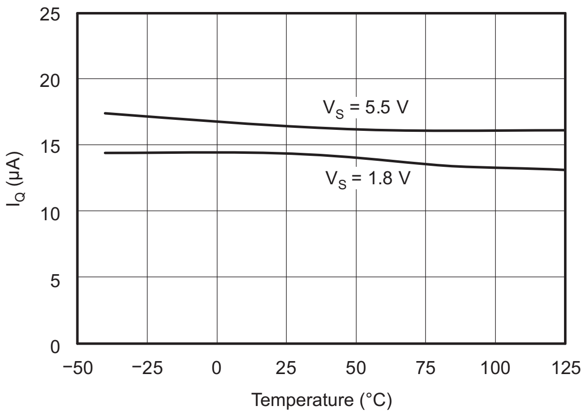


Figure 9. Quiescent Current vs Temperature

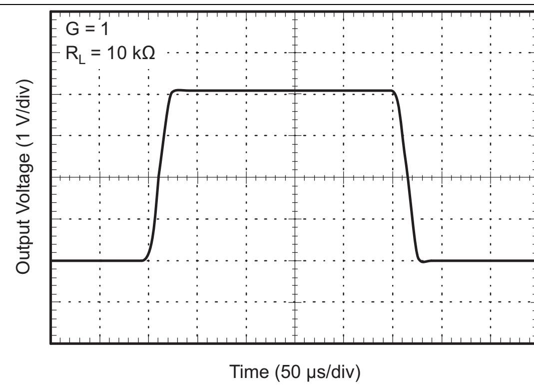


Figure 10. Large-Signal Step Response

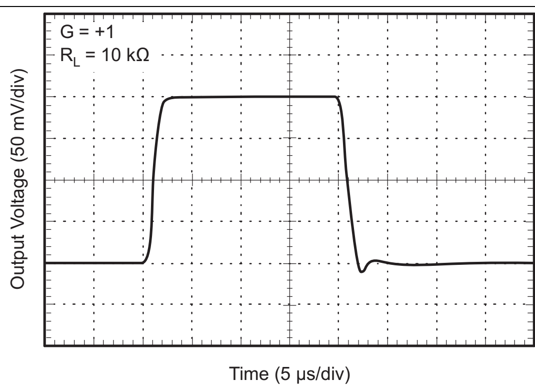


Figure 11. Small-Signal Step Response

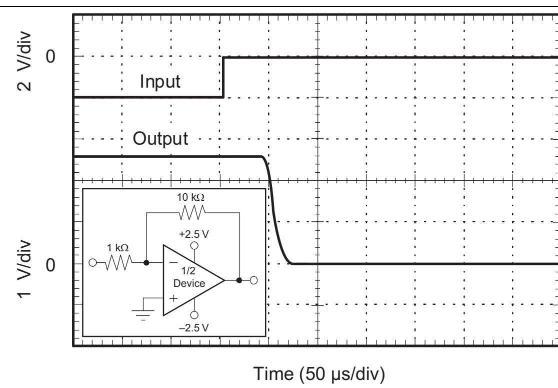


Figure 12. Positive Over-Voltage Recovery

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted)

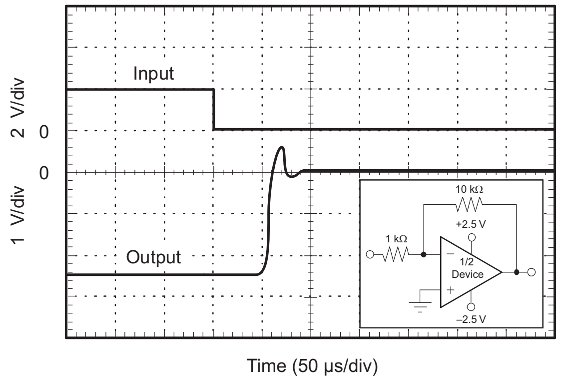


Figure 13. Negative Over-Voltage Recovery

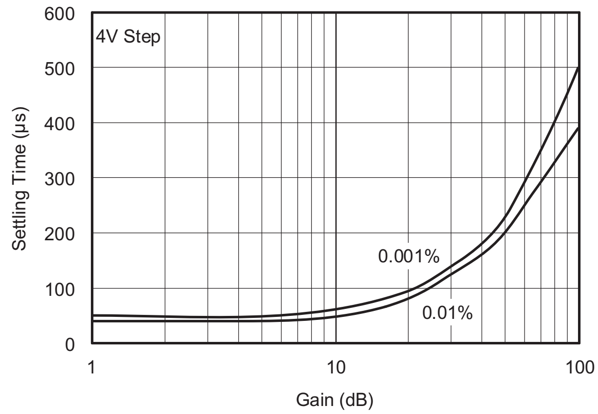


Figure 14. Settling Time vs Closed-Loop Gain

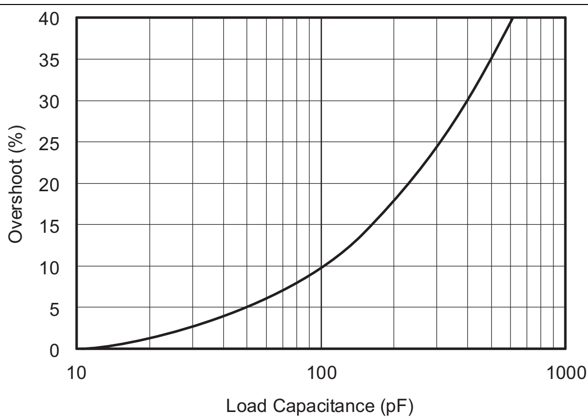


Figure 15. Small-Signal Overshoot vs Load Capacitance

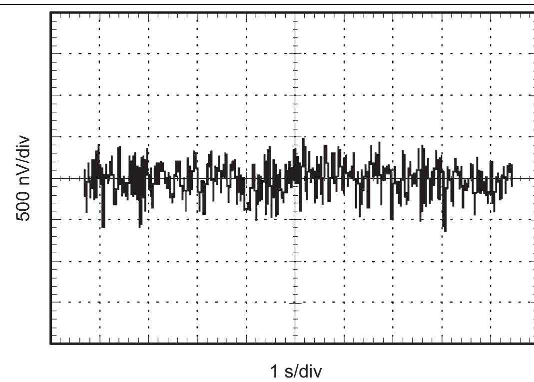


Figure 16. 0.1-Hz to 10-Hz Noise

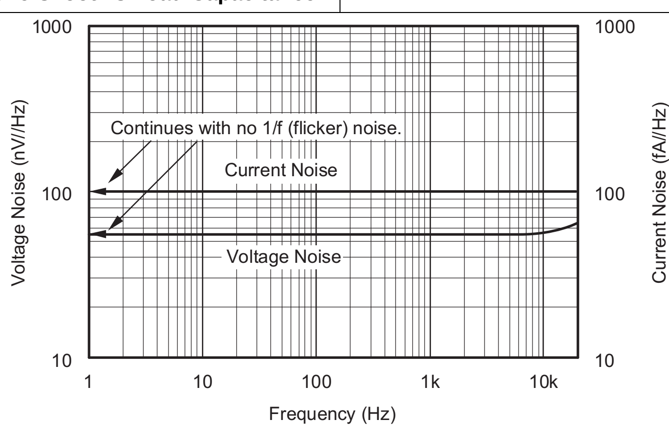


Figure 17. Current and Voltage Spectral Density vs Frequency

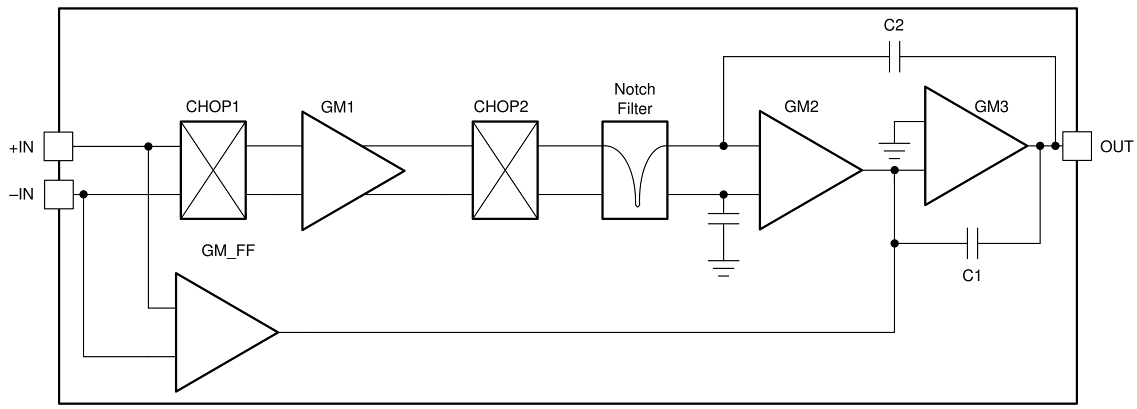
7 Detailed Description

7.1 Overview

The OPA2333-Q1 device is a zero-drift, low-power, rail-to-rail input and output operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low offset voltage and near-zero offset voltage drift.

The OPA2333-Q1 is unity-gain stable and free from unexpected output phase reversal. The device uses a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature.

7.2 Functional Block Diagram

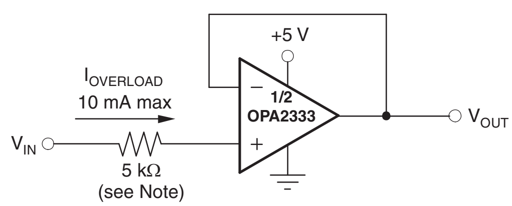


7.3 Feature Description

7.3.1 Rail-to-Rail Input Voltage

The OPA2333-Q1 input common-mode voltage range extends 0.1 V beyond the supply rails. The device is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is approximately 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor (see Figure 18).



NOTE: A current-limiting resistor required if the input voltage exceeds the supply rails by ≥ 0.5 V.

Figure 18. Input Current Protection

7.3.2 Internal Offset Correction

The OPA2333-Q1 op amps use an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8 µs using a proprietary technique. At power up, the amplifier requires approximately 100 µs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.4 Device Functional Modes

The OPA2333-Q1 has a single functional mode. The device is powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2333-Q1 is a unity-gain stable, precision operational amplifier with very low offset voltage drift. The device is also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but does not reach ground. The output of the OPA2333-Q1 can be made to swing to ground or slightly below on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 19).

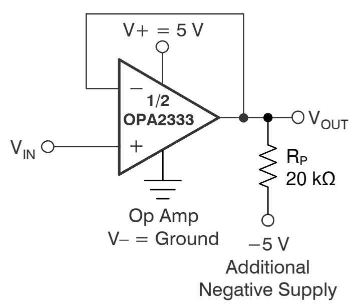


Figure 19. V_{OUT} Range to Ground

The OPA2333-Q1 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA2333-Q1 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ.

NOTE

This configuration increases the current consumption by several hundreds of microamps.

Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

8.2 Typical Application

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 20 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 21 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333-Q1 device facilitate excellent dc accuracy for the circuit.

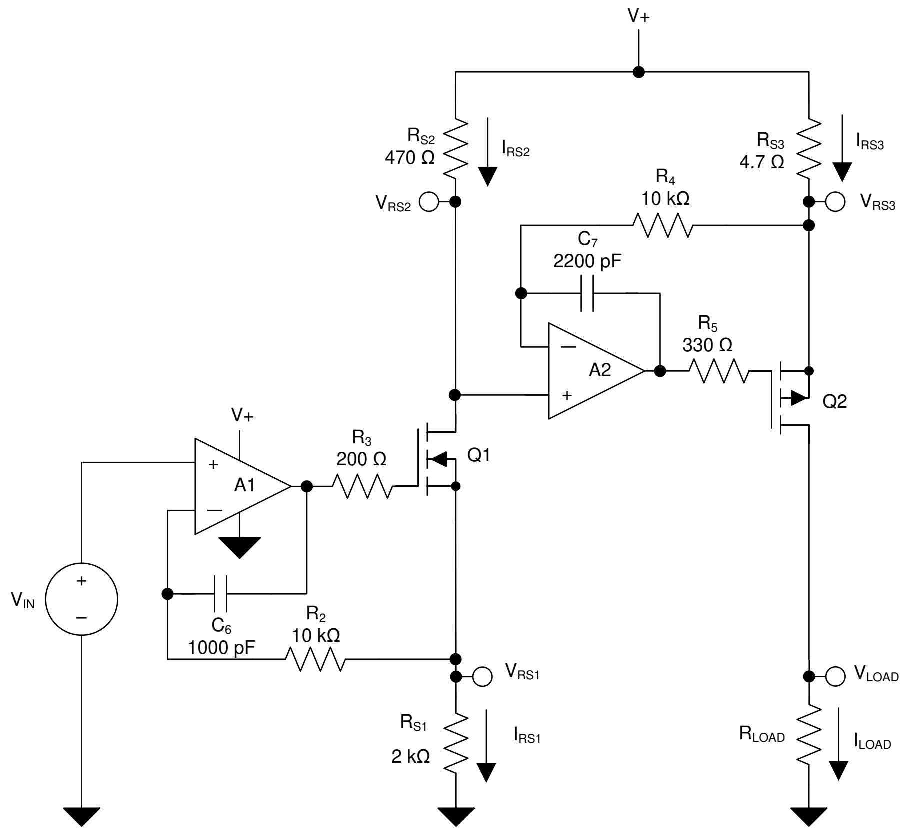


Figure 20. High-Side Voltage-to-Current (V-I) Converter

Typical Application (continued)

8.2.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V dc
- Input: 0 V to 2 V dc
- Output: 0 mA to 100 mA dc

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2333-Q1 CMOS operational amplifier is a high-precision, 5-µV offset, 0.05-µV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2333-Q1 uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2333-Q1 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in the *High-Side V-I Converter* reference design.

8.2.1.3 Application Curve

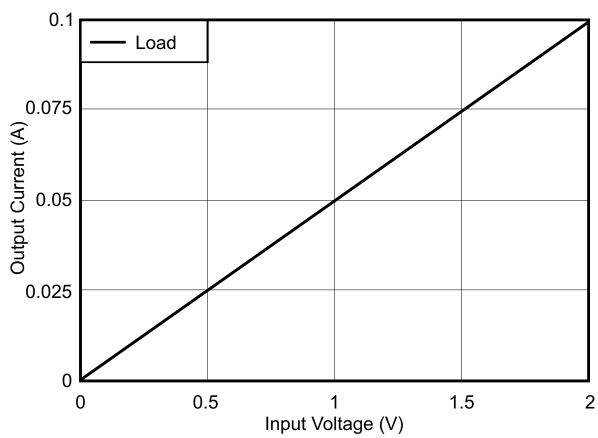


Figure 21. Measured Transfer Function for High-Side V-I Converter

Typical Application (continued)

8.2.1.4 Single Op Amp Bridge Amplifier

Figure 22 shows the basic configuration for a bridge amplifier.

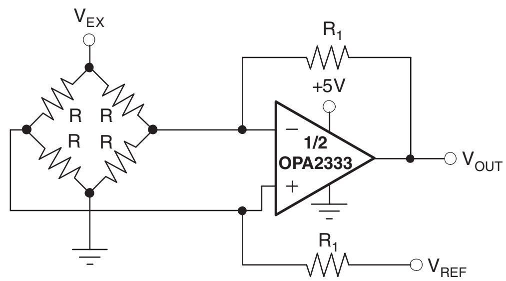
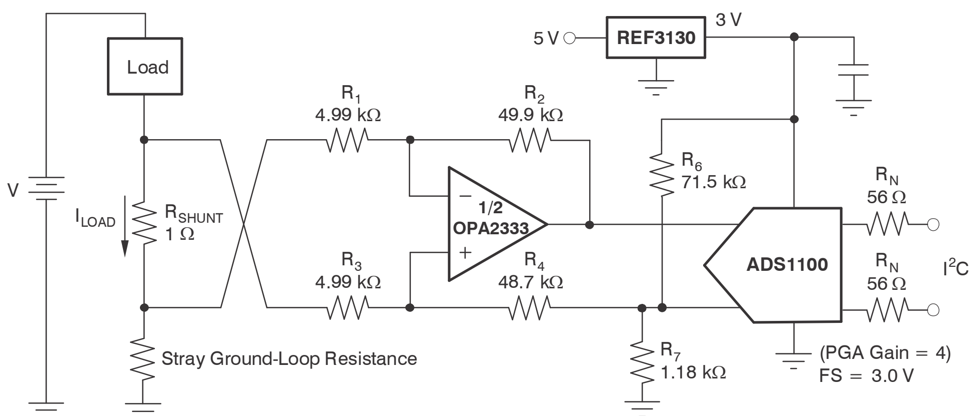


Figure 22. Single Op-Amp Bridge Amplifier

8.2.1.5 Low-Side Current Monitor

A low-side current shunt monitor is shown in Figure 23. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Because the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.



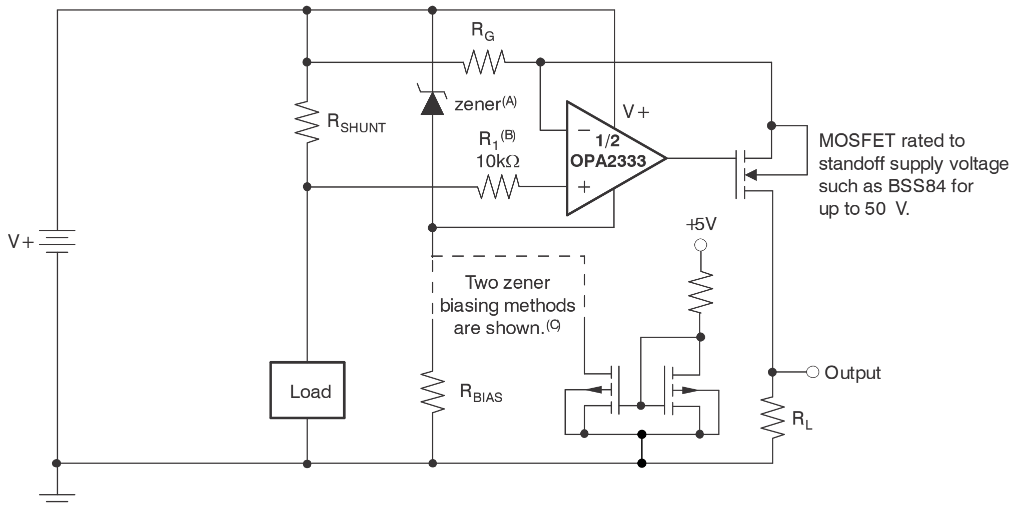
NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 23. Low-Side Current Monitor

Typical Application (continued)

8.2.1.6 High-Side Current Monitor

Figure 24 shows the use case for a precision single-supply amplifier for a high-side current sensing circuit.



A. Zener rated for op amp supply capability (that is, 5.1 V for the OPA2333).

B. Current-limiting resistor.

C. Choose a Zener biasing resistor or dual NMOSFETs (FDG6301N, NTJD4001N, or Si1034).

Figure 24. High-Side Current Monitor

8.2.1.7 Precision Instrumentation Amplifier

Figure 25 shows a three op amp implementation for a high-CMRR instrumentation amplifier..

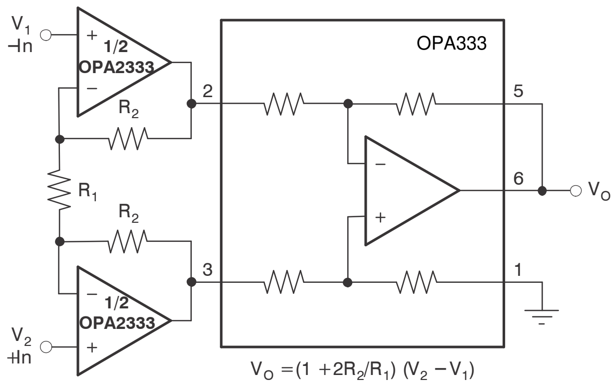


Figure 25. Precision Instrumentation Amplifier

9 Power Supply Recommendations

The OPA2333-Q1 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages greater than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors near the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more details on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA2333-Q1 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low-thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 µV/°C or higher, depending on materials used.

10.2 Layout Example

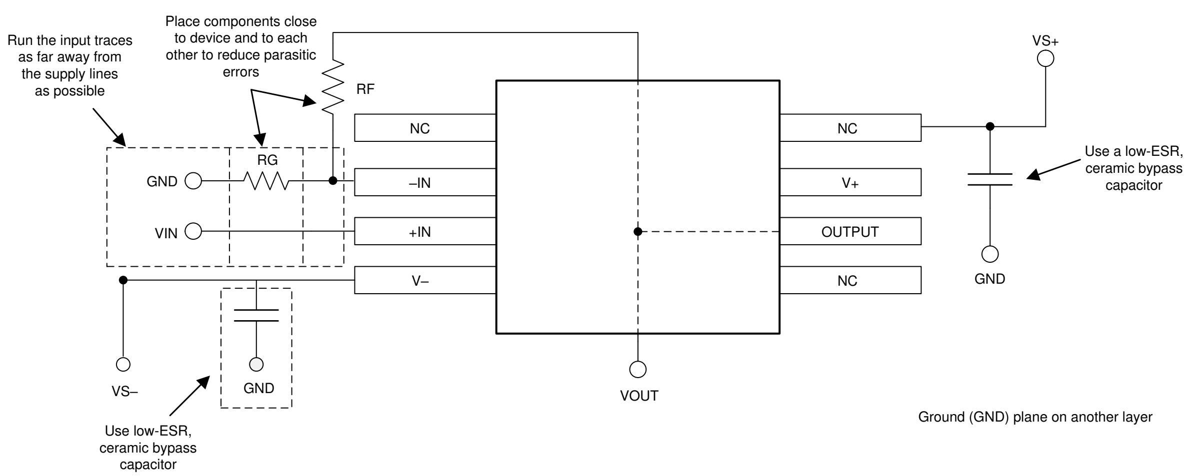


Figure 26. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《ADS1100 自校准 16 位模数转换器》* 数据表
- 德州仪器 (TI)，*《REF31xx 15ppm/°C 最大值、100μA、SOT-23 系列电压基准》* 数据表
- 德州仪器 (TI)，*《INAx321 微功耗、单电源 CMOS 仪表放大器》* 数据表
- 德州仪器 (TI)，*《INA32x 高精度、轨至轨 I/O 仪表放大器》* 数据表

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商标

E2E is a trademark of Texas Instruments.
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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2333AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	OCOQ
OPA2333AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OCOQ
OPA2333AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	02333Q
OPA2333AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	02333Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2333-Q1 :

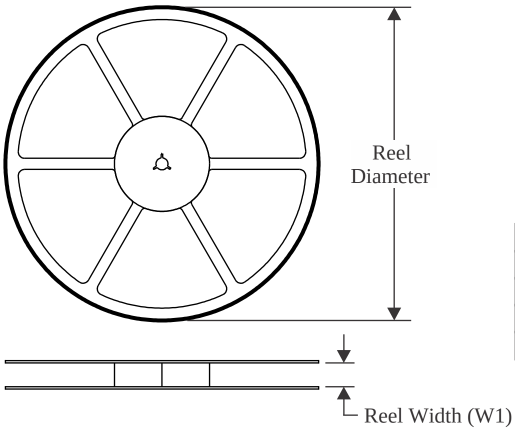
- Catalog : OPA2333

NOTE: Qualified Version Definitions:

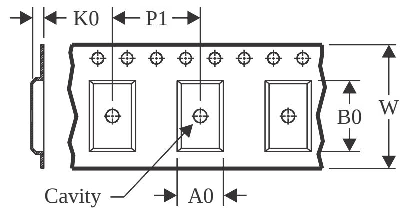
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

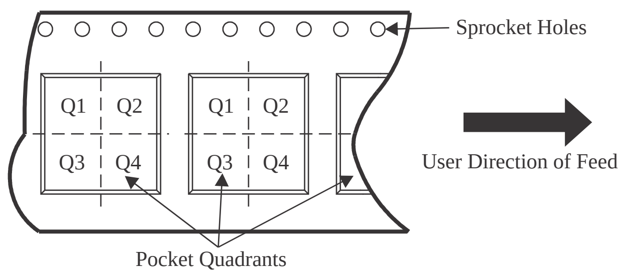


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

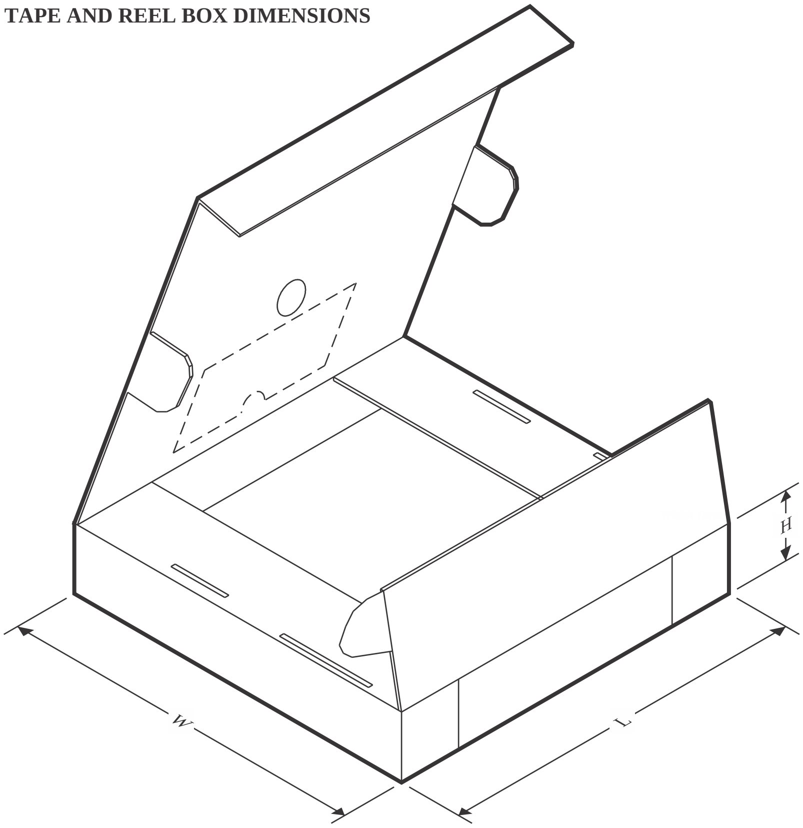
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

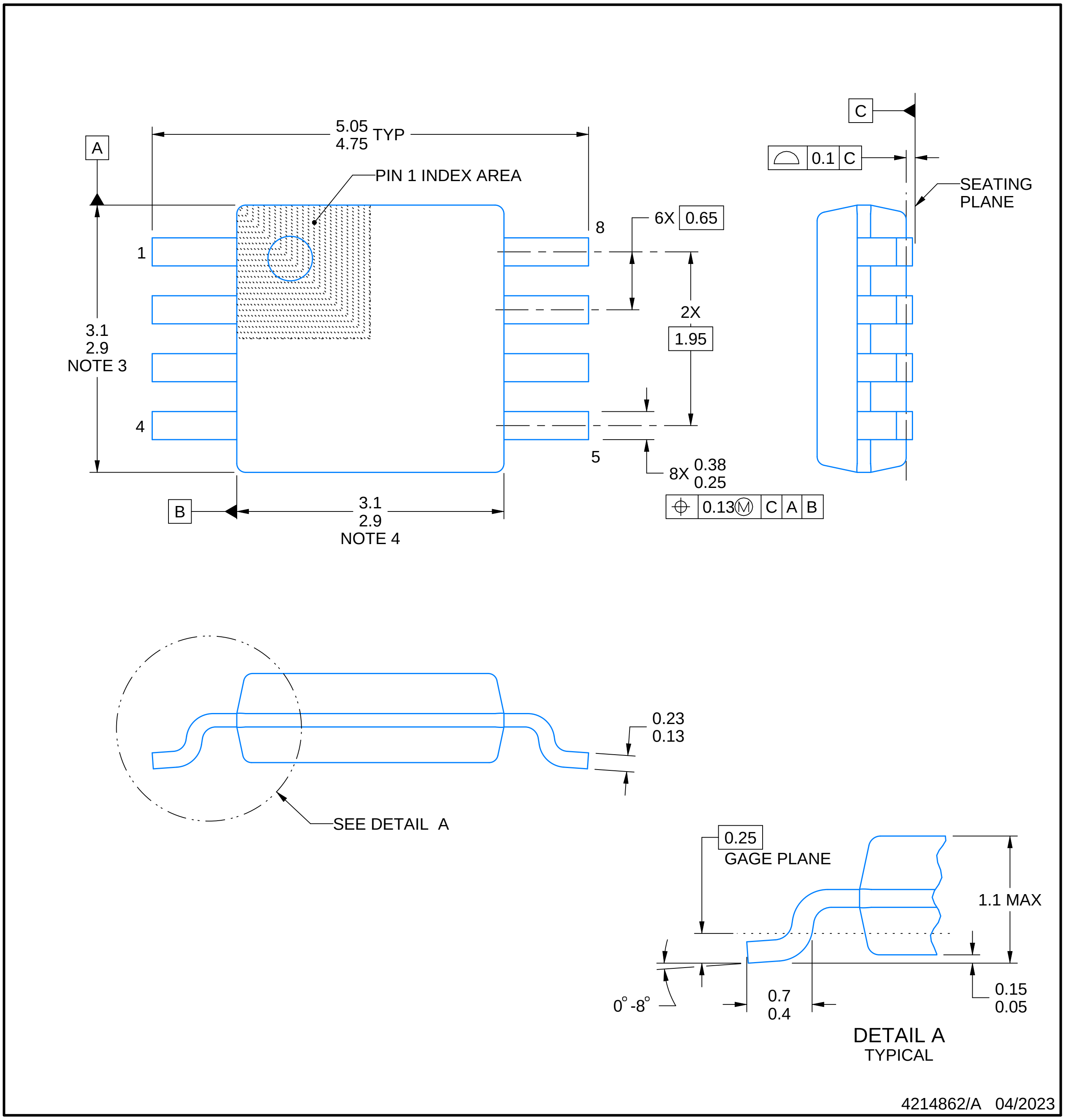
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
OPA2333AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333AQDGKRQ1	VSSOP	DGK	8	2500	367.0	367.0	38.0
OPA2333AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

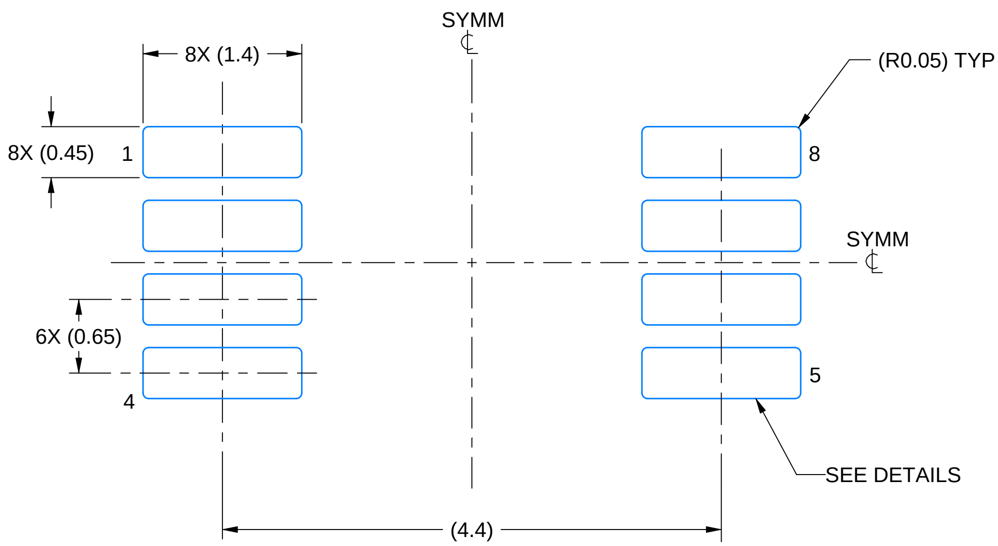


4214862/A 04/2023

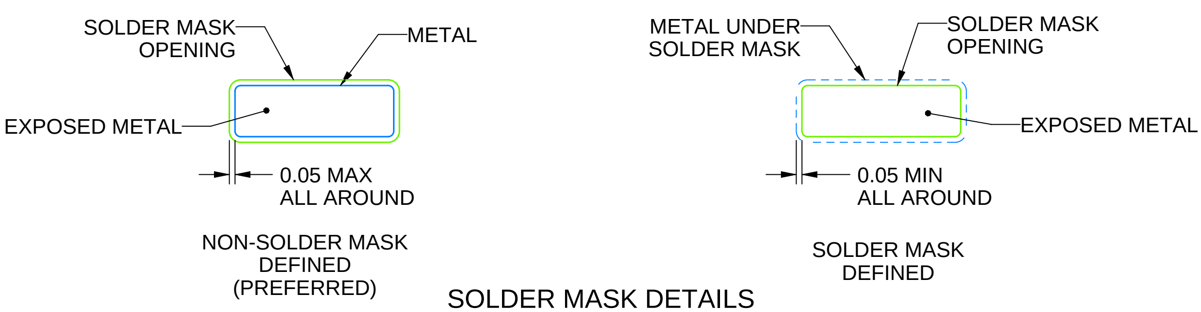
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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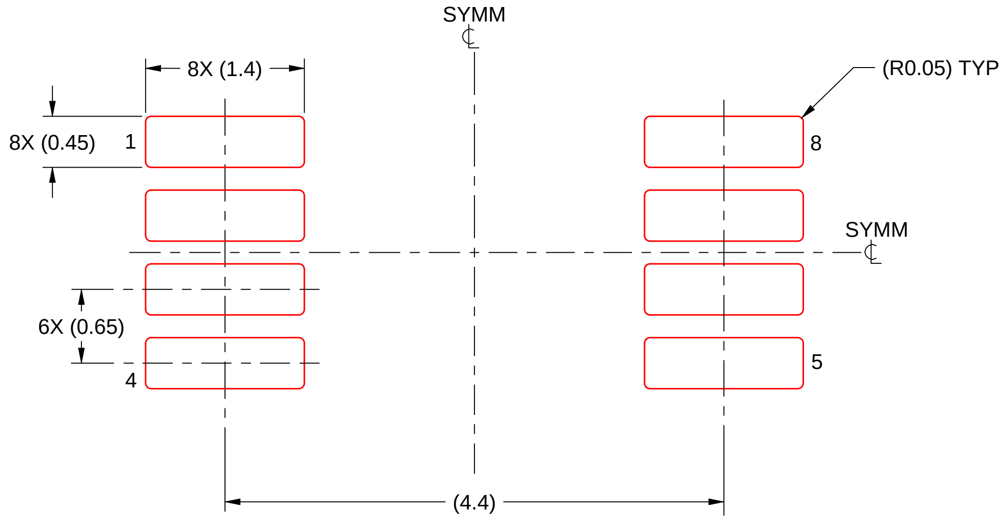
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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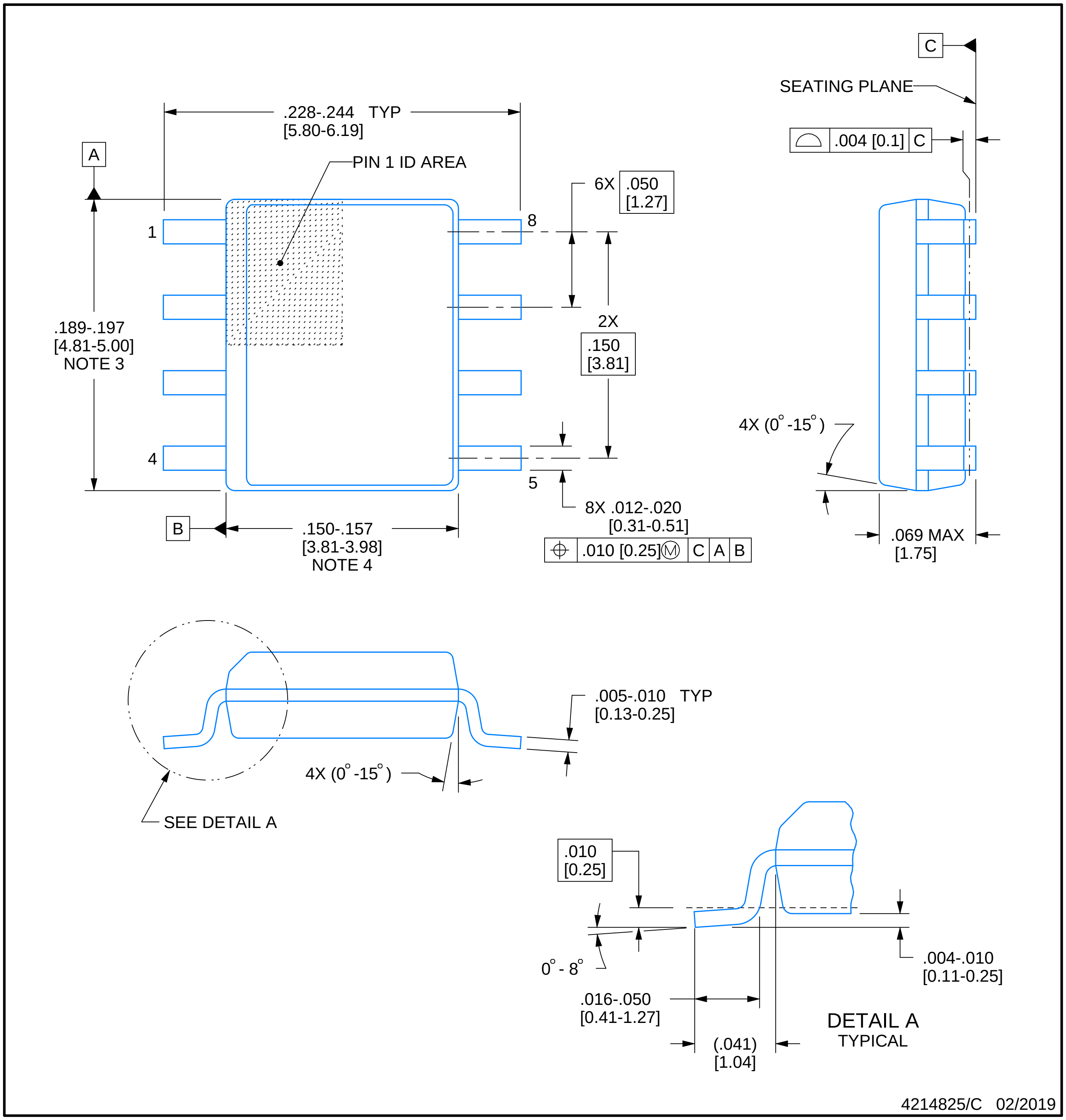
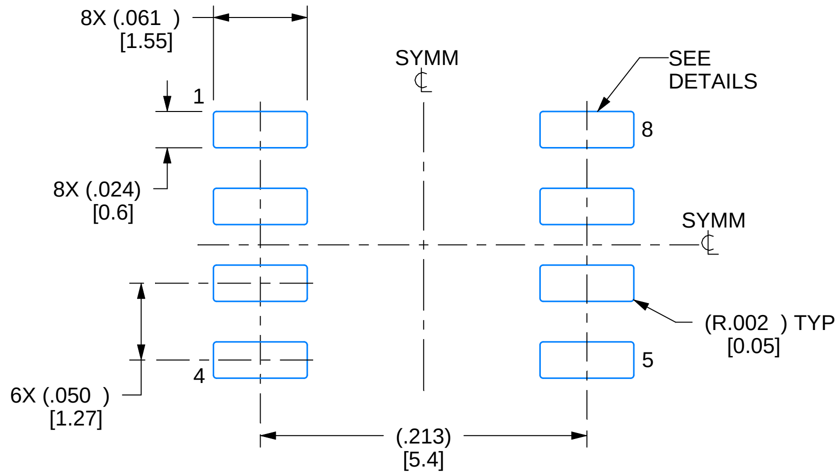
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

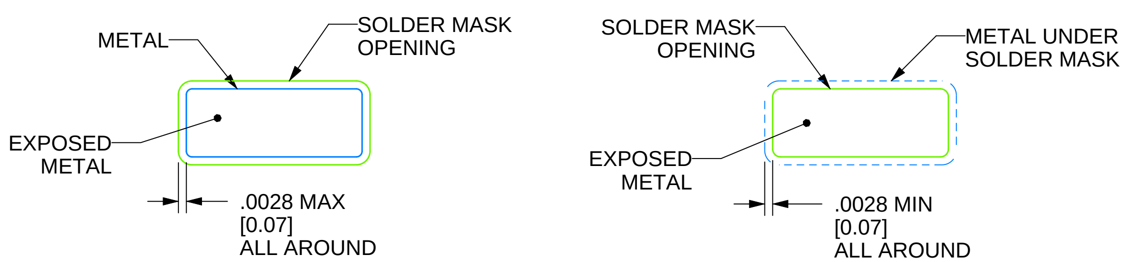


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

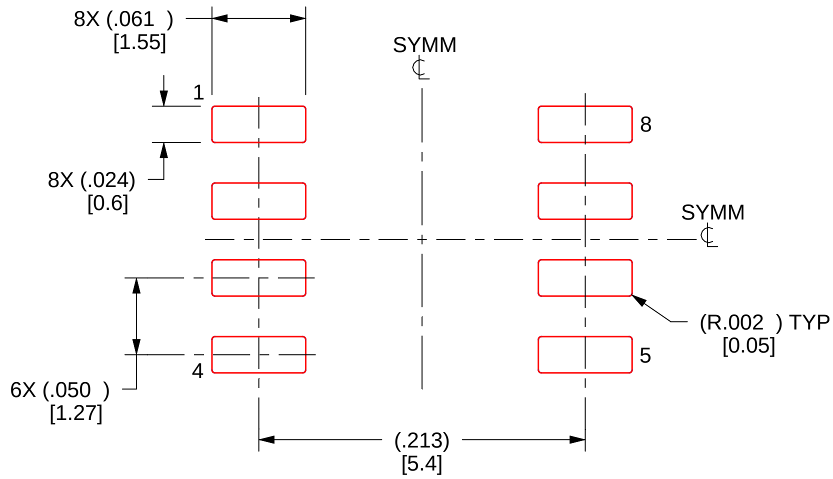
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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