OPAx320-Q1 高精度 20MHz 0.9pA 低噪声 RRIO CMOS 运算放大器

1 特性

- 符合汽车应用 标准
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：–40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 零交叉失真时的精度：
  - 低偏移电压：150μV（最大值）
  - 高共模抑制比 (CMRR)：114dB
  - 轨到轨 I/O
- 低输入偏置电流：0.9pA（最大值）
- 低噪声：10kHz 时为 7nV/√Hz
- 高带宽：20MHz
- 转换率：10V/μs
- 静态电流：每通道 1.45mA
- 单电源电压范围：1.8V 到 5.5V
- 单位增益稳定
- 小型超薄小外形尺寸 (VSSOP) 封装

2 应用

- 汽车
- 高阻抗传感器信号调节
- 互阻抗放大器
- 测试和测量设备
- 可编程逻辑控制器 (PLC)
- 电机控制环路
- 通信
- 输入和输出 ADC 和 DAC 缓冲器
- 有源滤波器

3 说明

OPA320-Q1 和 OPA2320-Q1 (OPAx320-Q1) 器件是经过优化的新一代精密低压 CMOS 运算放大器 (op amps)，具有极低噪声和宽带宽。这些器件可在仅 1.45mA 的低静态电流下运行。

OPAx320-Q1 非常适用于低功耗、单电源类 应用。低噪声 (7nV/√Hz) 和高速运行特性使这些器件同样非常适合驱动采样模数转换器 (ADC)。其他 应用 包括信号调节和传感器放大。

OPAx320-Q1 具有零交叉失真的线性输入级，能够在整个输入范围内提供 114dB（典型值）的出色共模抑制比 (CMRR)。共模输入范围将正负电源电压分别扩展了 100mV。输出电压摆幅通常在 10mV 电源轨内。

此外，OPAx320-Q1 还具有 1.8V 至 5.5V 的宽电源电压范围，而且在整个电源电压范围内的 PSRR 都极为出色 (106dB)。这些 特性 使得 OPAx320-Q1 适用于直接从电池运行， 而无需调节的 高精度、低功耗类应用。

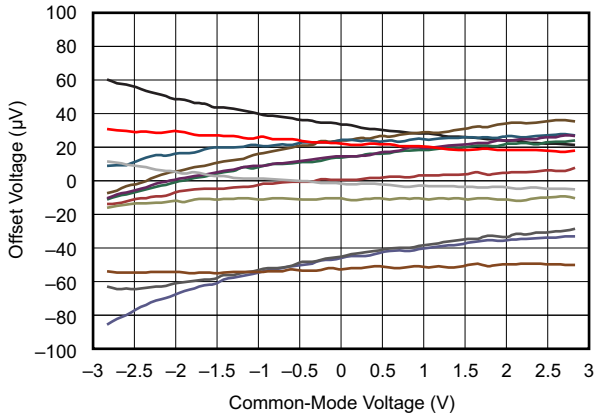
OPAx320-Q1 器件采用 8 引脚 VSSOP (DGK) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA320-Q1	SOT (5)	2.90mm x 1.60mm
OPA2320-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

零交叉失真：低偏移电压



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4 修订历史记录

Changes from Revision A (December 2016) to Revision B **Page**

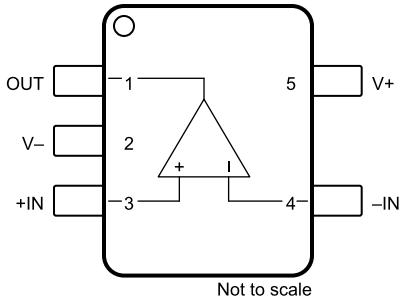
- Changed Figure 1 x-axis unit from mV to µV (typo) ... 7
- Changed Figure 2 x-axis unit from mV/°C to µV/°C (typo) ... 7
- Changed Figure 3 y-axis unit from mV to µV (typo) ... 7
- Changed Figure 14 y-axis unit from mV to µV (typo) ... 8
- Changed Figure 19 y-axis unit from W to Ω (typo) ... 9
- Changed Figure 25 y-axis unit from V/ms to V/µs (typo) ... 10
- Changed Figure 26 x-axis unit from ms to µs (typo) ... 10
- Changed Figure 27 x-axis unit from ms to µs (typo) ... 10
- Changed Figure 28 x-axis unit from ms to µs (typo) ... 10
- Changed Figure 35 x-axis unit from ms to µs (typo) ... 16

Changes from Original (September 2014) to Revision A **Page**

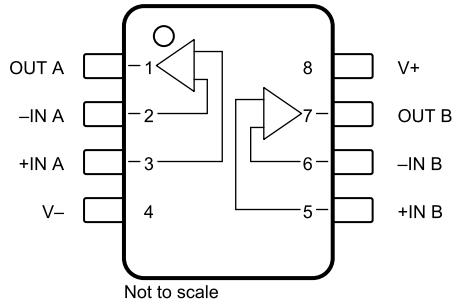
- 已添加 在文档中添加了 OPA320-Q1 器件 ... 1
- 已更改 在同时提及 OPA2320-Q1 和 OPAx320-Q1 器件的文档中，将 OPA2320-Q1 更改为了 OPAx320-Q1 ... 1
- 已更改 更改了说明部分的 首句 ： 添加了 *(OPA320-Q1、OPA2320-Q1)* ... 1
- 已添加 将 OPA320-Q1 添加到了*器件信息* 表 ... 1
- Added OPA320-Q1 device (SOT package) to *Pin Configuration and Functions* section: added OPA320-Q1 pin out to section and added relevant rows to *Pin Functions* table ... 3
- Changed format of *ESD Ratings* table: updated table to current standards, moved storage temperature parameter to *Absolute Maximum Ratings* table ... 4
- Changed *Supply voltage* parameter in *Recommended Operating Conditions* table: split apart single- and dual-supply values into separate rows ... 4
- Added OPA320-Q1 package to *Thermal Information* table ... 4
- Changed *Output Voltage Swing vs Output Current* figure ... 8
- Changed *Operational Amplifier Board Layout for Noninverting Configuration* figure ... 23

5 Pin Configuration and Functions

OPA320-Q1: DBV Package
5-Pin SOT
Top View



OPA2320-Q1: DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBV	DGK		
–IN	4	—	I	Inverting input
–IN A	—	2	I	Inverting input (channel A)
–IN B	—	6	I	Inverting input (channel B)
+IN	3	—	I	Noninverting input
+IN A	—	3	I	Noninverting input (channel A)
+IN B	—	5	I	Noninverting input (channel B)
OUT	1	—	O	Output
OUT A	—	1	O	Output (channel A)
OUT B	—	7	O	Output (channel B)
V–	2	4	—	Negative supply or ground (for single-supply operation)
V+	5	8	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V+ and V–		6	V
Voltage(2)	Signal input pins	$V_{(V–)}$ – 0.5	$V_{(V+)}$ + 0.5	V
Current(2)	Signal input pins	–10	10	mA
	Output short-circuit current(3)	Continuous		
Temperature	Operating, T_A	–40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed as *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	1.8		5.5	V
		Dual-supply	±0.9		±2.75	
T_A	Ambient operating temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA320-Q1 DBV (SOT) 5 PINS	OPA2320-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	174.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.7	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	95	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.2	93.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics:

V_S = 1.8 to 5.5 V or ±0.9 V to ±2.75 V; at T_A = 25°C, $R_{(L)}$ = 10 kΩ connected to V_S / 2, $V_{(CM)}$ = V_S / 2, V_O = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage			40	150	µV
	Input offset voltage versus temperature	V_S = 5.5 V, T_A = –40°C to +125°C		1.5	5	µV/°C
	Input offset voltage versus power supply	V_S = 1.8 to 5.5 V		5	20	µV/V
		V_S = 1.8 to 5.5 V, T_A = –40°C to +125°C		15		
	Input offset-voltage channel separation	At 1 kHz		130		dB
INPUT VOLTAGE						
$V_{(CM)}$	Common-mode voltage range		$V_{(V–)}$ – 0.1		$V_{(V+)}$ + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, $V_{(V–)}$ – 0.1 V < $V_{(CM)}$ < $V_{(V+)}$ + 0.1 V	100	114		dB
	Common-mode rejection ratio, over temperature	V_S = 5.5 V, $V_{(V–)}$ – 0.1 V < $V_{(CM)}$ < $V_{(V+)}$ + 0.1 V, T_A = –40°C to 125°C	96			dB
INPUT BIAS CURRENT						
I_{IB}	Input bias current			±0.2	±0.9	pA
	Input bias current, over temperature	T_A = –40°C to 85°C			±50	pA
		T_A = –40°C to 125°C			±400	
I_{IO}	Input offset current			±0.2	±0.9	pA
	Input offset current, over temperature	T_A = –40°C to 85°C			±50	pA
		T_A = –40°C to 125°C			±400	
NOISE						
$V_{I(n)}$	Input voltage noise	f = 0.1 to 10 Hz		2.8		$µV_{PP}$
	Input voltage noise density	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		
	Input current noise density	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
	Differential			5		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
$A_{(OL)}$	Open-loop voltage gain	0.1 V < V_O < $V_{(V+)}$ – 0.1 V, $R_{(L)}$ = 10 kΩ	114	132		dB
		0.1 V < V_O < $V_{(V+)}$ – 0.1 V, $R_{(L)}$ = 10 kΩ, T_A = –40°C to 125°C	100	130		
		0.2 V < V_O < $V_{(V+)}$ – 0.2 V, $R_{(L)}$ = 2 kΩ	108	123		
		0.2 V < V_O < $V_{(V+)}$ – 0.2 V, $R_{(L)}$ = 2 kΩ, T_A = –40°C to 125°C	96	130		
PM	Phase margin	V_S = 5 V, $C_{(L)}$ = 50 pF		47		°
FREQUENCY RESPONSE (V_S = 5 V, $C_{(L)}$ = 50 pF)						
GBP	Gain bandwidth product	Unity gain		20		MHz
SR	Slew rate	G = 1		10		V/µs
t_s	Settling time	To 0.1%, 2-V step, G = 1		0.25		µs
		To 0.01%, 2-V step, G = 1		0.32		
		To 0.0015%, 2-V step, G = 1 (1)		0.5		
	Overload recovery time	V_I × G > V_S		100		ns
THD+N	Total harmonic distortion + noise (2)	V_O = 4 V_{PP}, G = 1, f = 10 kHz, $R_{(L)}$ = 10 kΩ		0.0005%		
		V_O = 4 V_{PP}, G = 1, f = 10 kHz, $R_{(L)}$ = 600 kΩ		0.0011%		

(1) Based on simulation.
(2) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: (continued)

V_S = 1.8 to 5.5 V or ±0.9 V to ±2.75 V; at T_A = 25°C, $R_{(L)}$ = 10 kΩ connected to V_S / 2, $V_{(CM)}$ = V_S / 2, V_O = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from both rails	$R_{(L)}$ = 10 kΩ		10	20	mV
		$R_{(L)}$ = 10 kΩ, T_A = –40°C to 125°C			30	
		$R_{(L)}$ = 2 kΩ		25	35	
		$R_{(L)}$ = 2 kΩ, T_A = –40°C to 125°C			45	
$I_{(SC)}$	Short-circuit current	V_S = 5.5 V		±65		mA
$C_{(L)}$	Capacitive load drive		See *Typical Characteristics*			
	Open-loop output resistance	I_O = 0 mA, f = 1MHz		90		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5V		1.45	1.6	mA
		I_O = 0 mA, V_S = 5.5V, T_A = –40°C to 125°C			1.7	
	Power-on time	$V_{(V+)}$ = 0 to 5 V, to 90% I_Q level		28		µs
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–40		150	°C

6.6 Typical Characteristics

at T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ (unless otherwise noted)

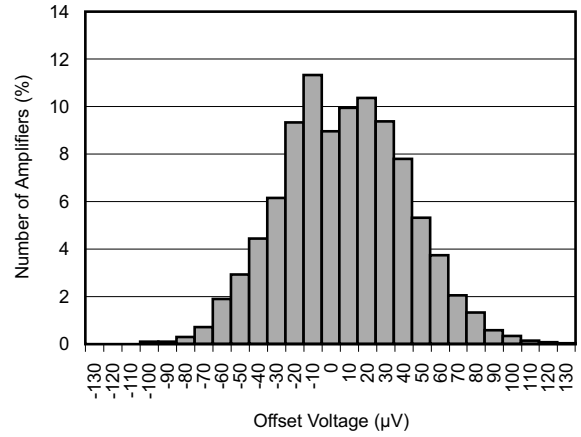


Figure 1. Offset Voltage Production Distribution

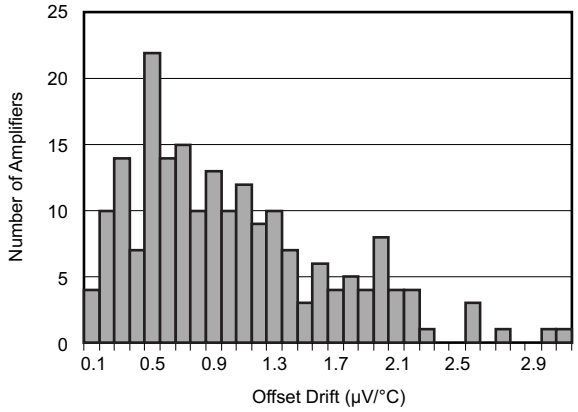
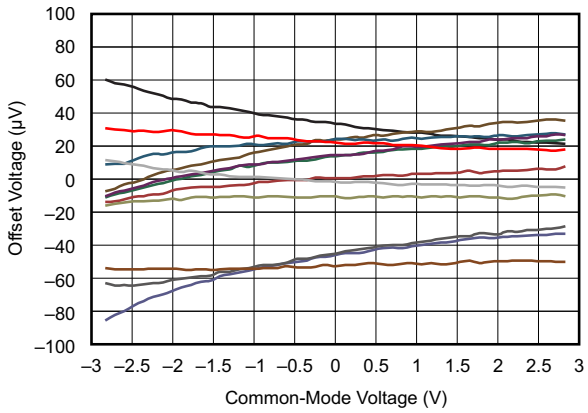
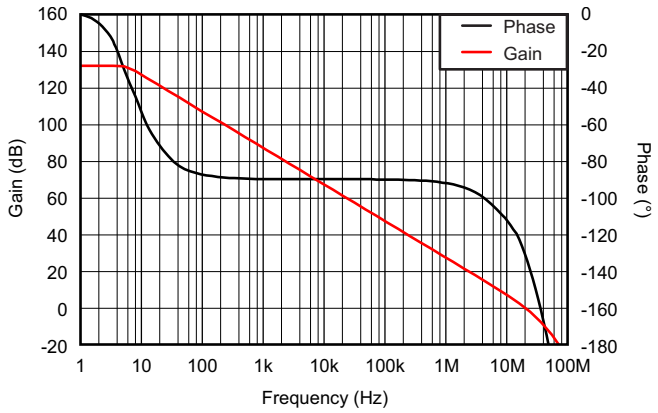


Figure 2. Offset Voltage Drift Distribution



Representative units, V_S = ±2.75 V

Figure 3. Offset Voltage vs Common-Mode Voltage



V_S = ±2.5 V, $C_{(L)}$ = 50 pF

Figure 4. Open-Loop Gain and Phase vs Frequency

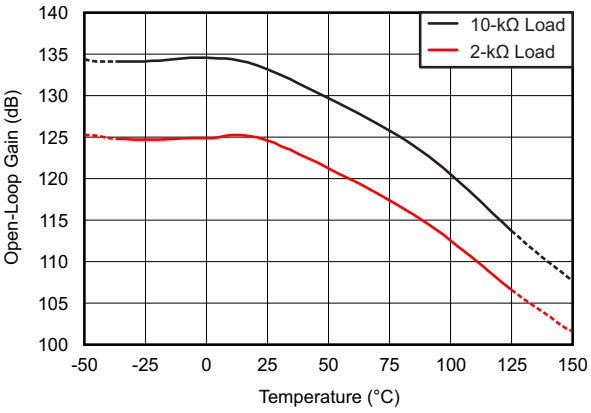


Figure 5. Open-Loop Gain vs Temperature

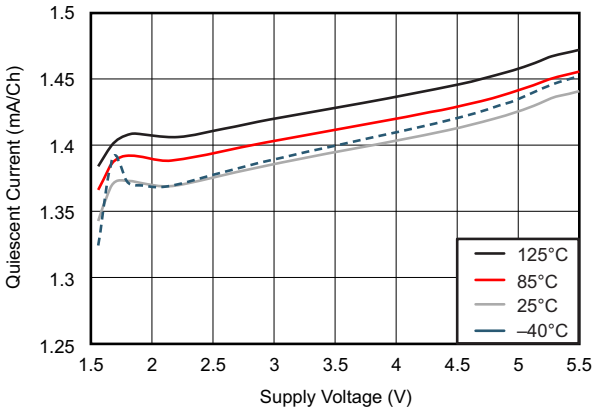


Figure 6. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ (unless otherwise noted)

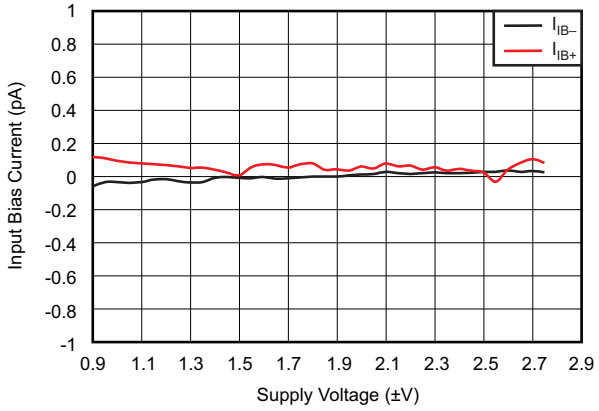


Figure 7. Input Bias Current vs Supply Voltage

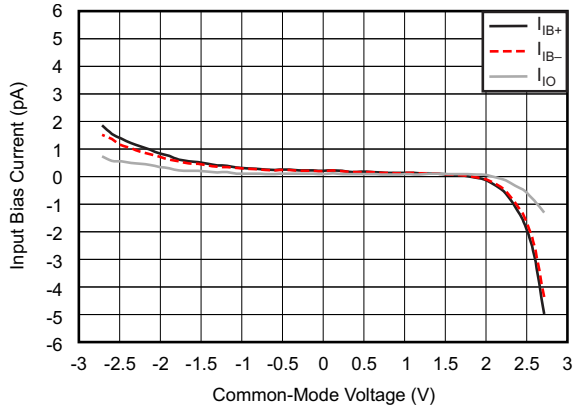


Figure 8. Input Bias Current vs Common-Mode Voltage

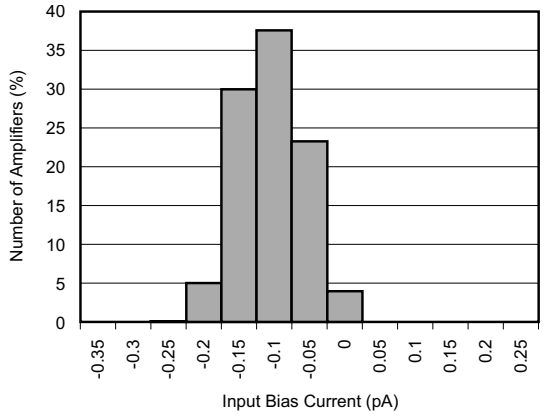


Figure 9. Input Bias Current Distribution

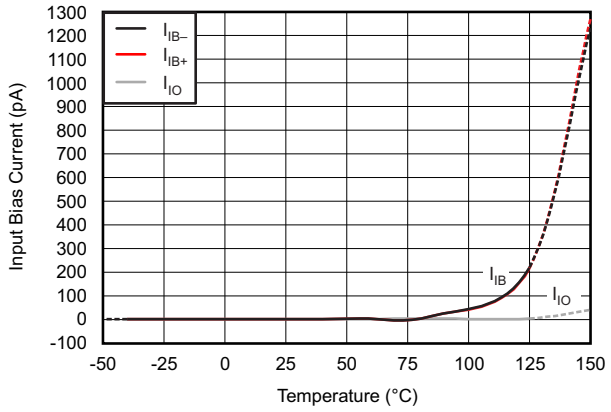


Figure 10. Input Bias Current vs Temperature

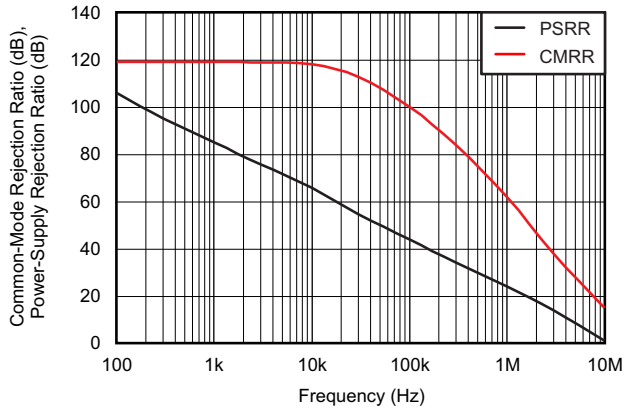
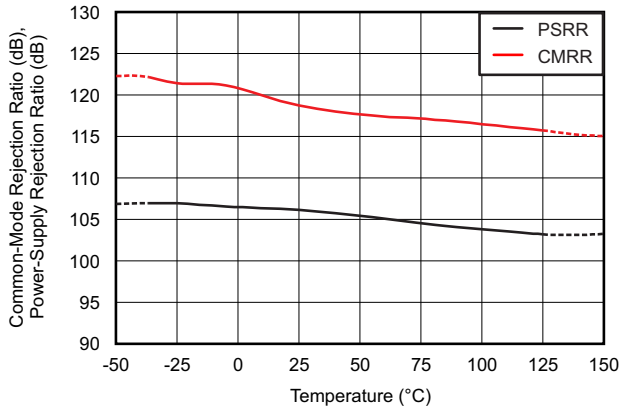


Figure 11. CMRR and PSRR vs Frequency

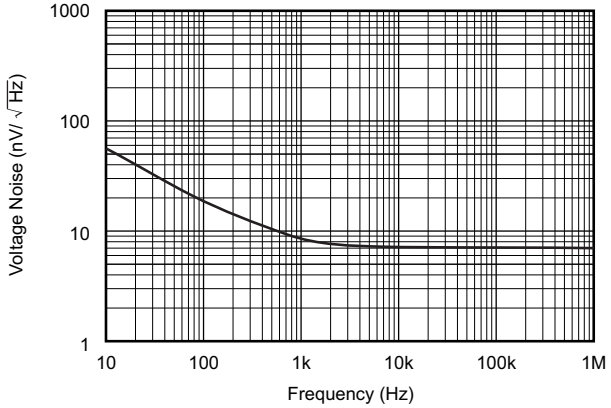


V_S = 1.8 to 5.5 V

Figure 12. CMRR and PSRR vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ (unless otherwise noted)



V_S = 1.8 to 5.5 V

Figure 13. Input Voltage Noise Spectral Density vs Frequency

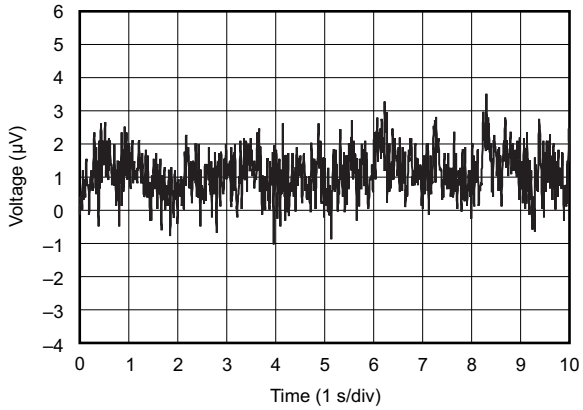
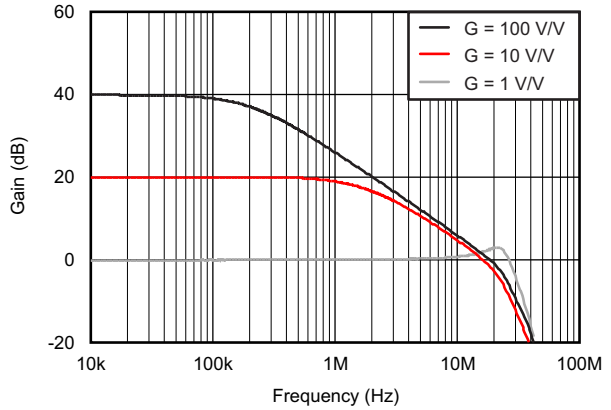
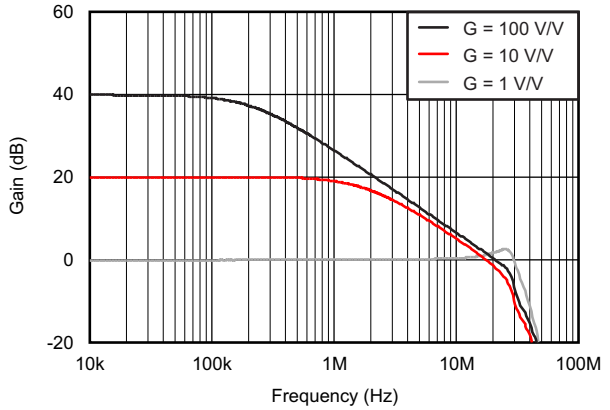


Figure 14. 0.1-Hz to 10-Hz Input Voltage Noise



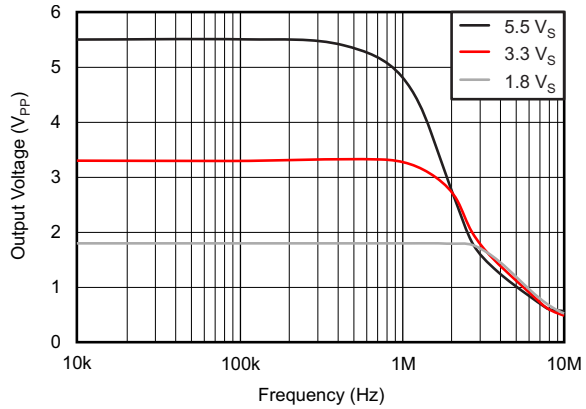
V_S = 1.8 V, $C_{(L)}$ = 50 pF, $R_{(L)}$ = 10 kΩ

Figure 15. Closed-Loop Gain vs Frequency



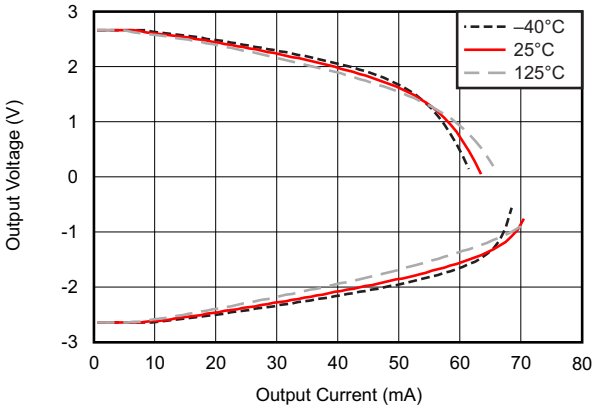
V_S = 5.5 V, $C_{(L)}$ = 50 pF, $R_{(L)}$ = 10 kΩ

Figure 16. Closed-Loop Gain vs Frequency



$C_{(L)}$ = 50 pF, $R_{(L)}$ = 10 kΩ

Figure 17. Maximum Output Voltage vs Frequency

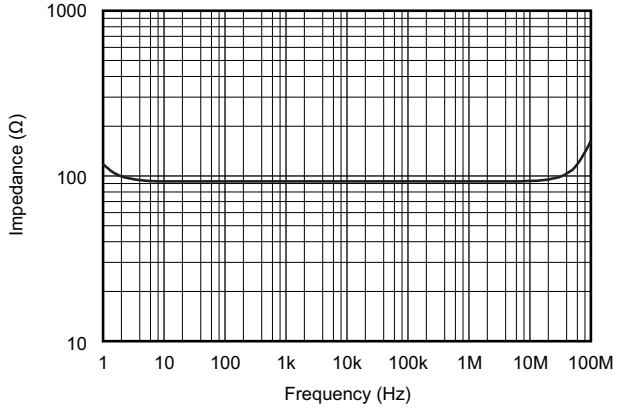


V_S = ±2.75 V

Figure 18. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ (unless otherwise noted)



V_S = ±2.75 V

Figure 19. Open-Loop Output Impedance vs Frequency

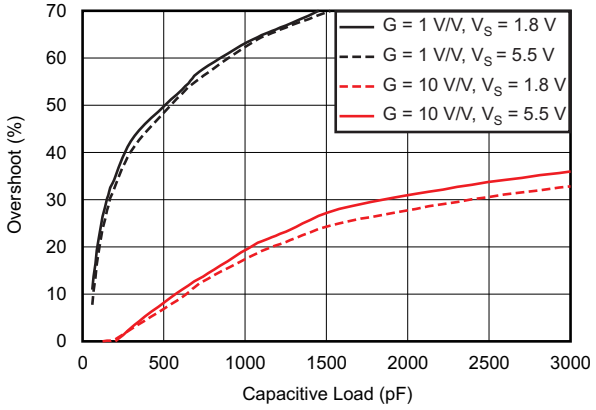
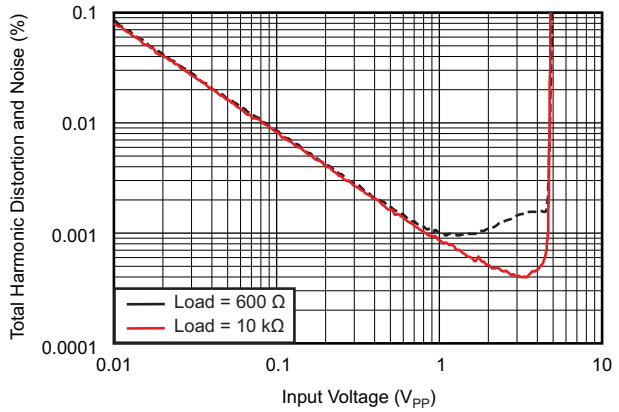
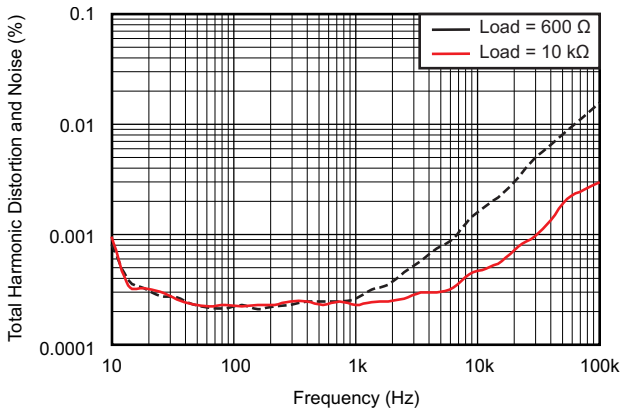


Figure 20. Small-Signal Overshoot vs Load Capacitance



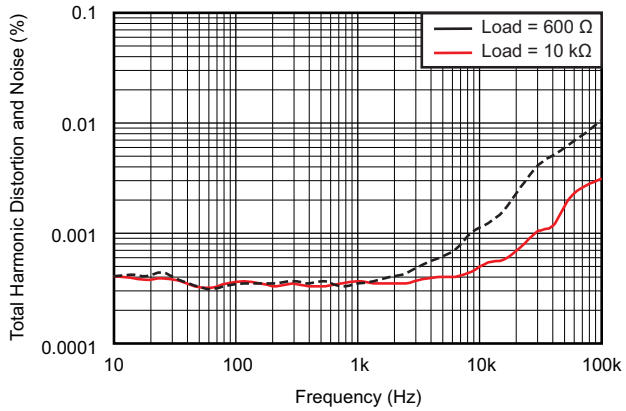
V_S = ±2.5 V, f = 10 kHz, G = 1 V/V

Figure 21. THD+N vs Amplitude



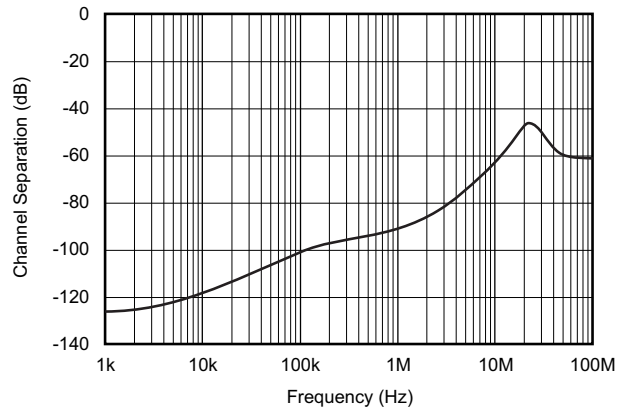
V_S = ±2.5 V, f = 10 kHz, G = 1 V/V, V_I = 2 V_{PP}

Figure 22. THD+N vs Frequency



V_S = ±2.5 V, f = 10 kHz, G = 1 V/V, V_I = 4 V_{PP}

Figure 23. THD+N vs Frequency

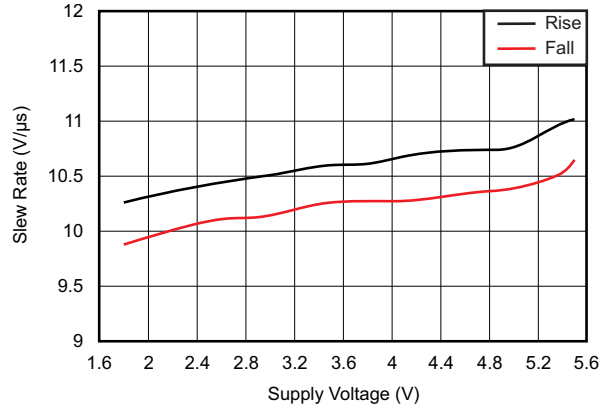


V_S = ±2.75 V

Figure 24. Channel Separation vs Frequency

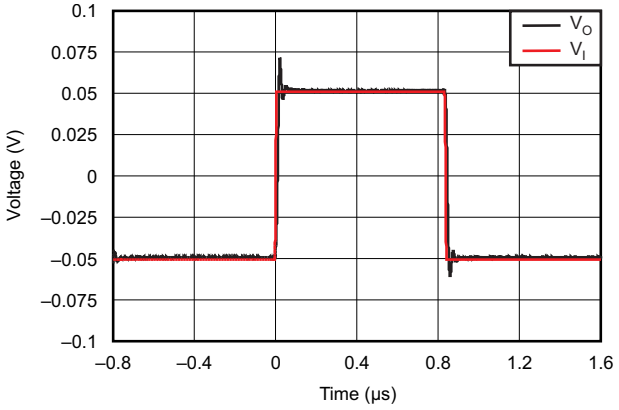
Typical Characteristics (continued)

at T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ (unless otherwise noted)



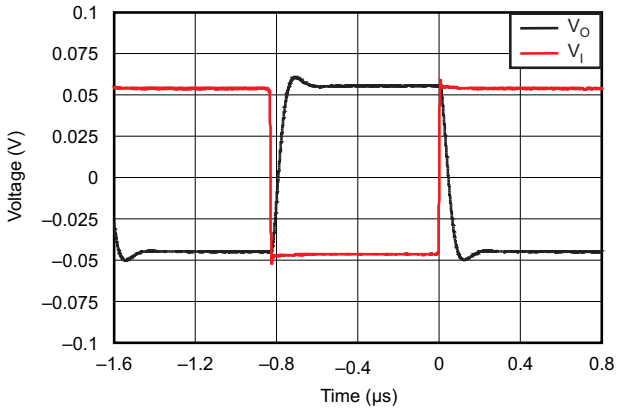
$C_{(L)}$ = 50 pF

Figure 25. Slew Rate vs Supply Voltage



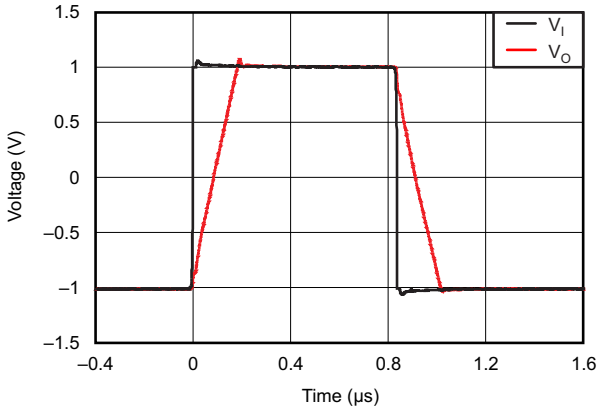
V_S = ±2.75 V, G = 1 V/V, V_I = 100 mV_{PP}

Figure 26. Small-Signal Step Response



V_S = ±2.75 V, G = –1 V/V, V_I = 100 mV_{PP}

Figure 27. Small-Signal Step Response



V_S = ±2.75 V, G = 1 V/V, V_I = 2 V_{PP}

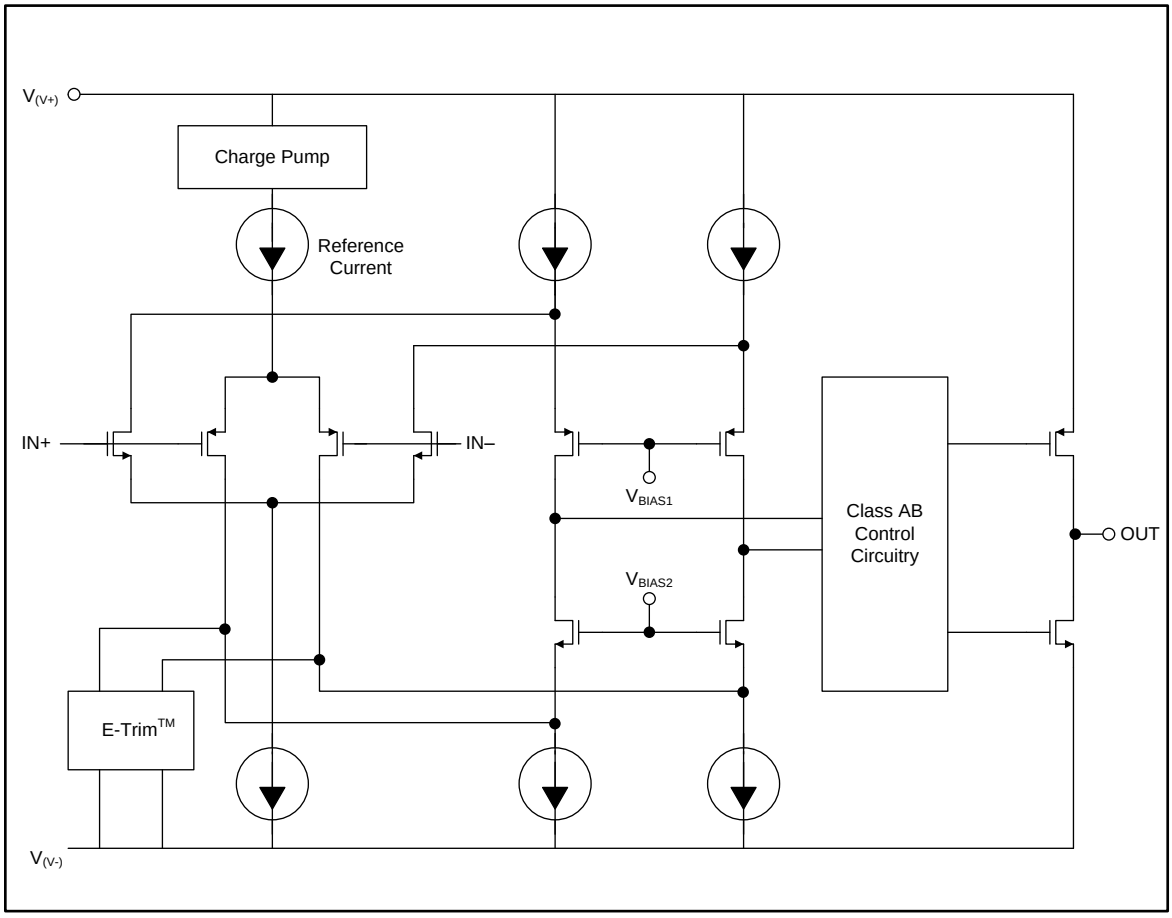
Figure 28. Large-Signal Step Response vs Time

7 Detailed Description

7.1 Overview

The OPA320-Q1 and OPA2320-Q1 (OPAx320-Q1) operational amplifiers (op amps) are unity-gain stable and operate on a single-supply voltage (1.8 V to 5.5 V), or a split supply voltage (±0.9 V to ±2.75 V), making these devices highly versatile and easy to use. The OPAx320-Q1 amplifiers are fully specified from 1.8 V to 5.5 V and over the extended temperature range of –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input and ESD Protection

The OPAx320-Q1 incorporate internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, provided that the current is limited to 10 mA, as stated in the *Absolute Maximum Ratings*. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 29 shows how a series input resistor ($R_{(S)}$) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

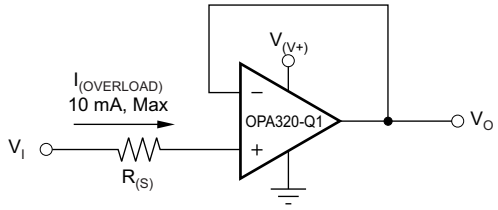
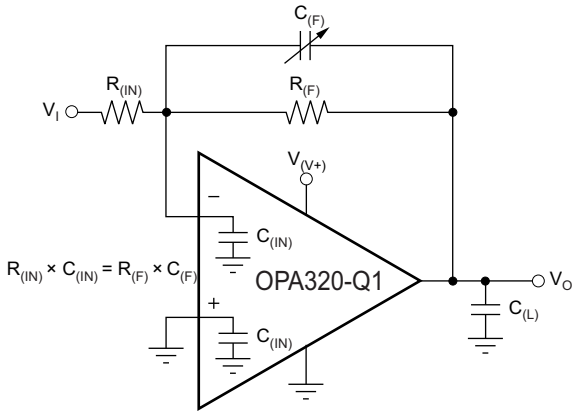


Figure 29. Input Current Protection

7.3.2 Feedback Capacitor Improves Response

For optimum settling time and stability with high-impedance feedback networks, adding a feedback capacitor across the feedback resistor, $R_{(FB)}$, as shown in Figure 30 may be necessary. This capacitor compensates for the zero created by the feedback network impedance and the OPAx320-Q1 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



NOTE: Where $C_{(IN)}$ is equal to the OPAx320-Q1 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 30. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor because input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 30, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPAx320-Q1 (9 pF, typical) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{(IN)} \times C_{(IN)} = R_{(FB)} \times C_{(FB)} \quad (1)$$

Where:

- $C_{(IN)}$ is equal to the OPAx320-Q1 input capacitance (sum of differential and common-mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

Feature Description (continued)

7.3.3 EMI Susceptibility And Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx320-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cut-off frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

7.3.4 Output Impedance

The open-loop output impedance of the OPAx320-Q1 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For example, with 130 dB (typical) of open-loop gain, the output impedance is reduced in unity-gain to less than 0.03 Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPAx320-Q1 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This in turn prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPAx320-Q1 have excellent capacitive load drive capability for op amps with the bandwidth.

7.3.5 Capacitive Load and Stability

The OPAx320-Q1 are designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx320-Q1 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPAx320-Q1 remain stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors ($C_{(L)}$ > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains; see Figure 32. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor ($R_{(S)}$), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 31.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, $R_{(L)}$ = 10 kΩ and $R_{(S)}$ = 20 Ω, the gain error is only about 0.2%. However, when $R_{(L)}$ is decreased to 600 Ω, which the OPAx320-Q1 are able to drive, the error increases to 7.5%.

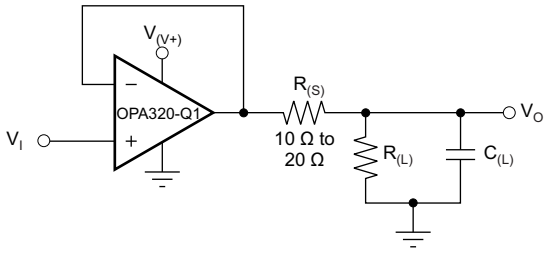


Figure 31. Improving Capacitive Load Drive

Feature Description (continued)

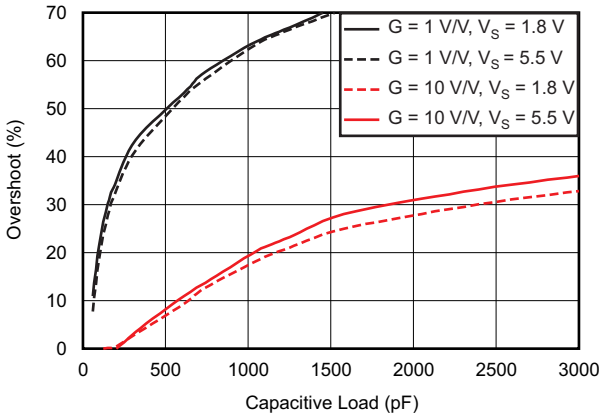


Figure 32. Small-Signal Overshoot versus Capacitive Load (100-mV_{PP} Output Step)

7.3.6 Overload Recovery Time

Overload recovery time is the time it takes the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 33 and Figure 34 show the positive and negative overload recovery times of the OPAx320-Q1, respectively. In both cases, the time elapsed before the OPAx320-Q1 come out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

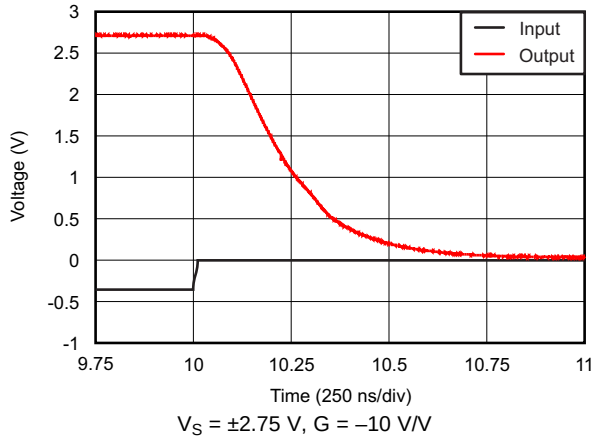


Figure 33. Positive Recovery Time

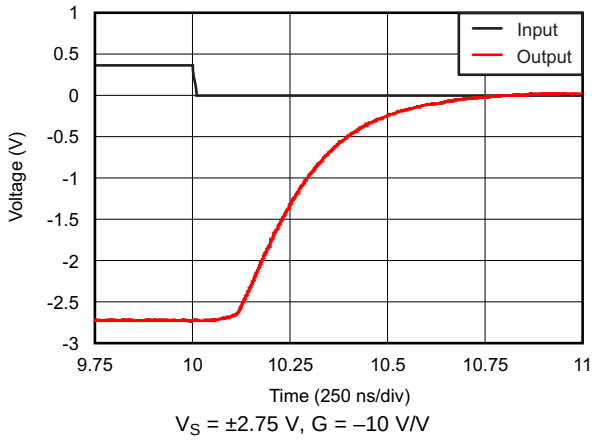


Figure 34. Negative Recovery Time

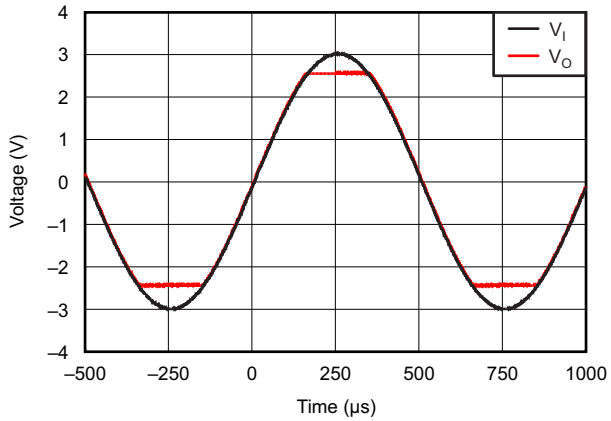
7.4 Device Functional Modes

7.4.1 Rail-to-Rail Input

The OPAx320-Q1 feature true rail-to-rail input operation, with supply voltages as low as ±0.9 V (1.8 V). The design of the OPAx320-Q1 amplifiers include an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6 V above the external supply (V+). This internal supply rail allows the single differential input pair to operate and remain very linear over a very wide input common-mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary input stage operational amplifiers. This topology allows the OPAx320-Q1 to provide superior common-mode performance (CMRR > 110 dB, typical) over the entire common-mode input range, which extends 100 mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear $V_{(CM)}$ range of the OPAx320-Q1 provides maximum linearity and lowest distortion.

7.4.2 Phase Reversal

The OPAx320-Q1 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, and thus provide further in-system stability and predictability. Figure 35 shows the input voltage exceeding the supply voltage without any phase reversal.



V_S = ±2.5 V

Figure 35. No Phase Reversal

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

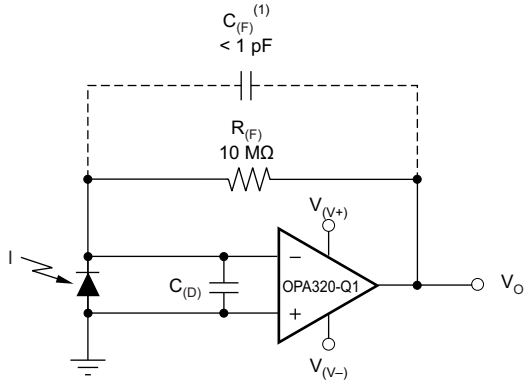
The OPAx320-Q1 can be used in a wide range of applications, such as transimpedance amplifiers, high-impedance sensors, active filters, and driving ADCs.

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx320-Q1 an excellent wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 36, are the expected diode capacitance ($C_{(D)}$), which should include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF); the desired transimpedance gain ($R_{(FB)}$); and the gain-bandwidth (GBW) for the OPAx320-Q1 (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) can be set to control the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 36. Dual-Supply Transimpedance Amplifier

8.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage $V_{(V+)}$	2.5 V
Supply voltage $V_{(V–)}$	–2.5 V

8.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole should be set to:

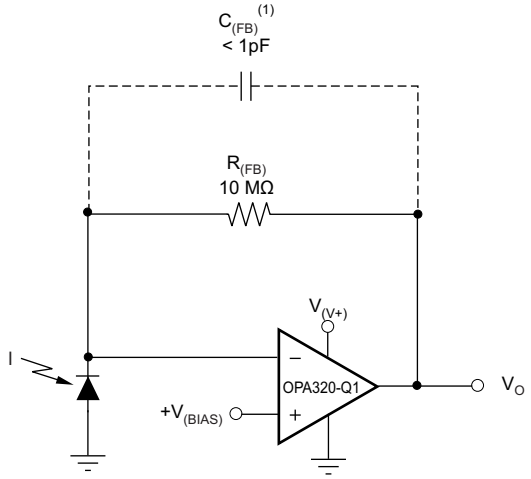
$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (2)$$

Use Equation 3 to calculate the bandwidth.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (3)$$

For even higher transimpedance bandwidth, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), and OPA656 or OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 37. This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 37. Single-Supply Transimpedance Amplifier

For additional information, refer to the *Compensate Transimpedance Amplifiers Intuitively Application Report*.

8.2.1.2.1 Optimizing The Transimpedance Circuit

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(FB)}$ increases with the square-root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if not required for stability.

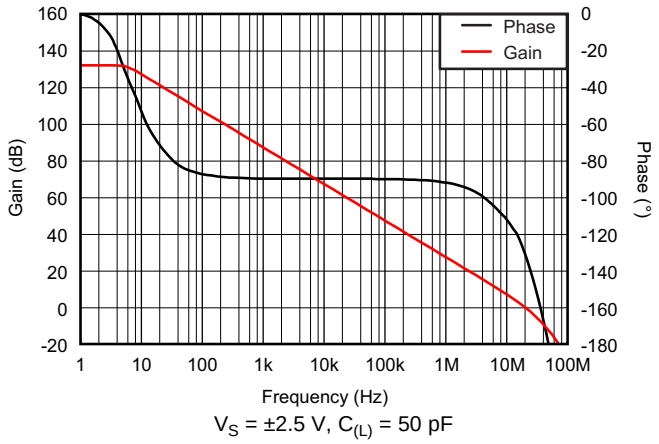
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the following documents:

- Texas Instruments, *Noise Analysis of FET Transimpedance Amplifiers Application Bulletin*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps Application Report*

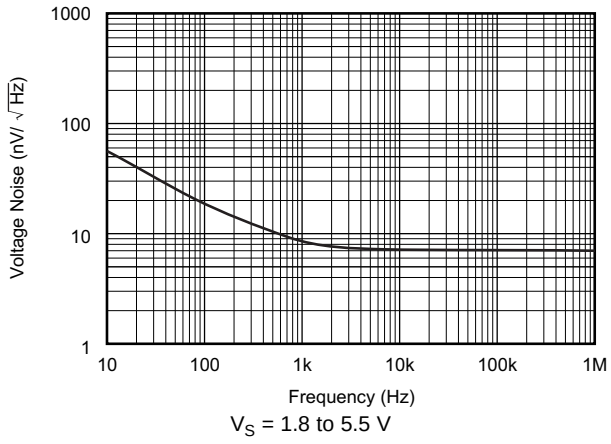
8.2.1.3 Application Curves

Wide gain bandwidth as shown in Figure 38 and low input voltage noise as shown in Figure 39 make the OPAx320-Q1 device an excellent wideband photodiode transimpedance amplifier.



V_S = ±2.5 V, $C_{(L)}$ = 50 pF

Figure 38. Open-Loop Gain and Phase vs Frequency



V_S = 1.8 to 5.5 V

Figure 39. Input Voltage Noise Spectral Density vs Frequency

8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 40, where ($V_{(+INx)} = V_S – I_{(BIAS)} \times R_{(S)}$). The last term, $I_{(BIAS)} \times R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} \times R_{(S)}$ less than the input voltage noise of the amplifier, so that it does not become the dominant noise factor. The OPAx320-Q1 series of op amps feature very low input bias current (typically 200 fA), and are therefore excellent choices for such applications.

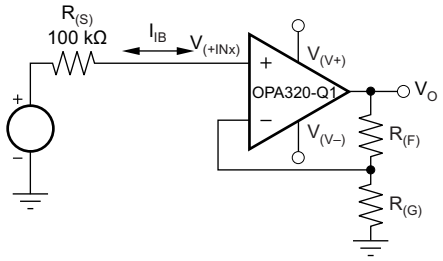


Figure 40. Noise as a Result of $I_{(BIAS)}$

8.2.3 Driving ADCs

The OPAx320-Q1 series op amps are an excellent choice for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPAx320-Q1 to drive ADCs without degradation of differential linearity and THD.

The OPAx320-Q1 can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 42 shows the OPAx320-Q1 configured to drive the ADS8326.

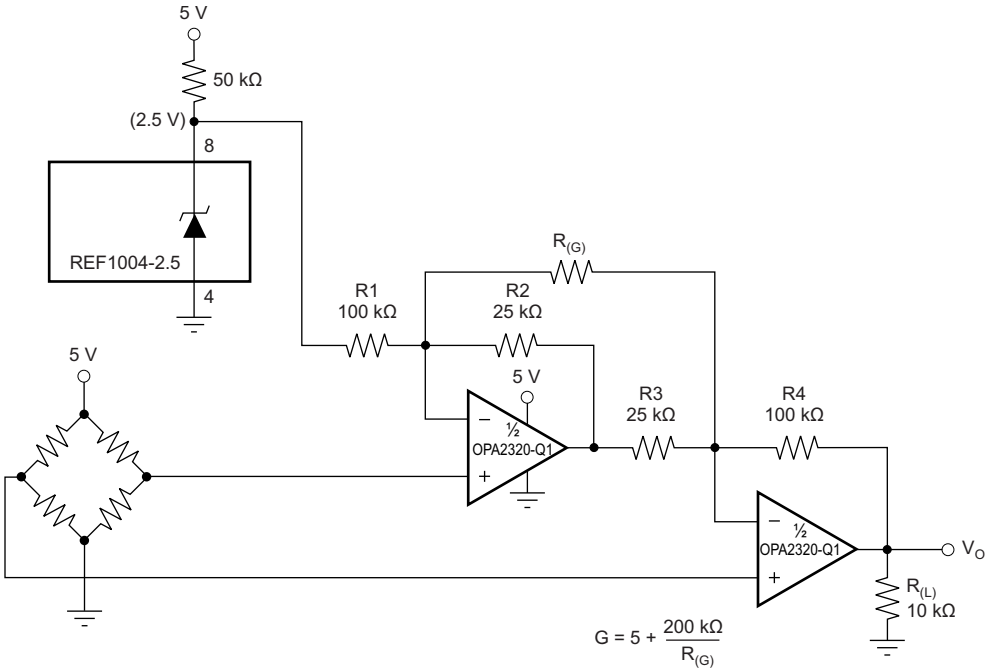
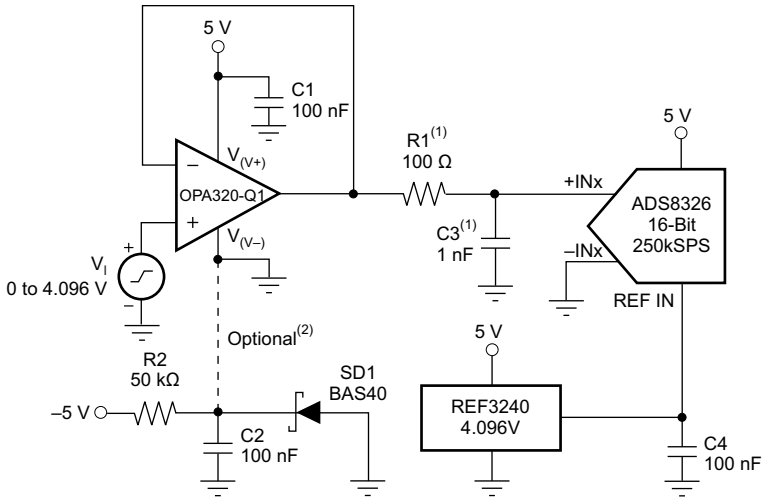


Figure 41. Two Op-Amp Instrumentation Amplifier With Improved High-Frequency Common-Mode Rejection



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

Figure 42. Driving the ADS8326

8.2.4 Active Filter

The OPAx320-Q1 is an excellent choice for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 43 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is excellent for applications requiring predictable gain characteristics, such as the antialiasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. adding an inverting amplifier
2. adding an additional second-order MFB stage
3. using a noninverting filter topology, such as the Sallen-Key

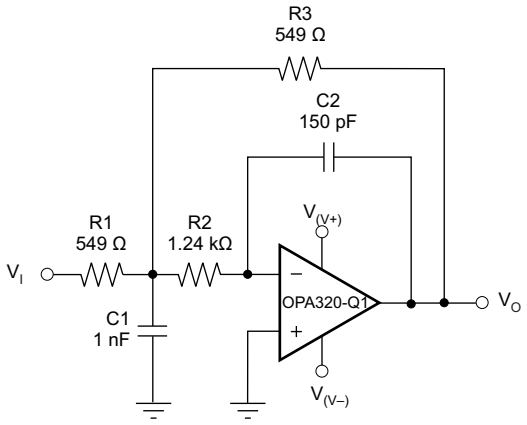


Figure 43. Second-Order Butterworth 500-kHz Low-Pass Filter

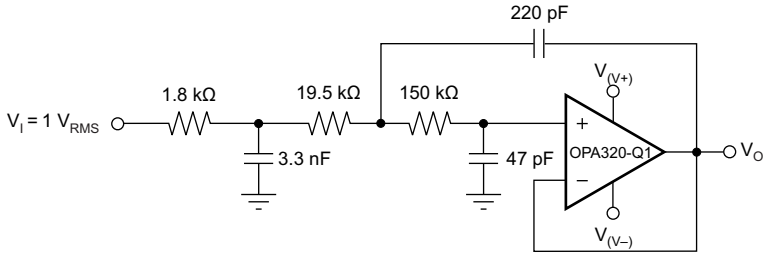


Figure 44. OPAx320-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9 Power Supply Recommendations

The OPAx320-Q1 are specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 6 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to the *Circuit Board Layout Techniques Application Report*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 45, keeping RF and RG close to the inverting input will minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

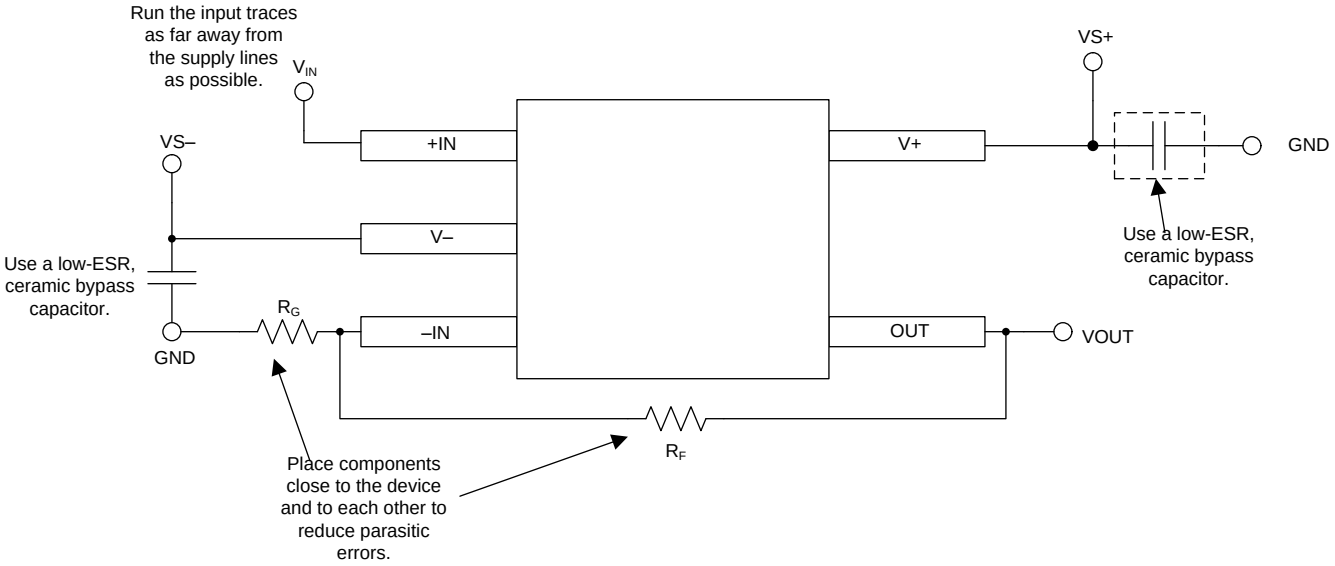


Figure 45. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

相关文档如下：

- 德州仪器 (TI)，《*ADS8326 16 位、2.7V 至 5.5V 高速微功耗采样模数转换器产品说明书*》
- 德州仪器 (TI)，《*用直观方式补偿跨阻放大器的应用报告*》
- 德州仪器 (TI)，《*FET 跨阻放大器噪声分析应用简报*》
- 德州仪器 (TI)，《*高速运算放大器噪声分析应用报告*》
- 德州仪器 (TI)，《*OPAx380 精密高速跨阻放大器产品说明书*》
- 德州仪器 (TI)，《*OPAx354 250MHz 轨至轨 I/O CMOS 运算放大器产品说明书*》
- 德州仪器 (TI)，《*具有关断功能的 OPAx355 200MHz CMOS 运算放大器产品说明书*》
- 德州仪器 (TI)，《*OPA656 宽带单位增益稳定 FET 输入运算放大器产品说明书*》

11.2 相关链接

表 1 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
OPA320-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2320-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2320AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZAEV
OPA2320AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZAEV
OPA320AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	15DD
OPA320AQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15DD
OPA320AQDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15DD
OPA320AQDBVRQ1G4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15DD
OPA320AQDBVTQ1	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	15DD
OPA320AQDBVTQ1.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15DD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2320-Q1, OPA320-Q1 :

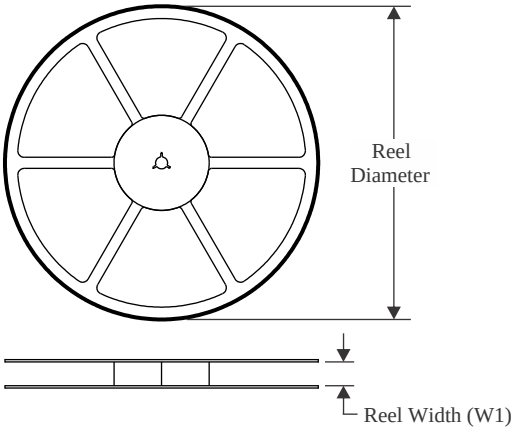
- Catalog : OPA2320, OPA320

NOTE: Qualified Version Definitions:

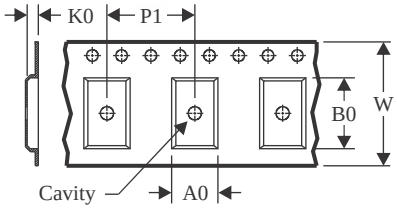
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

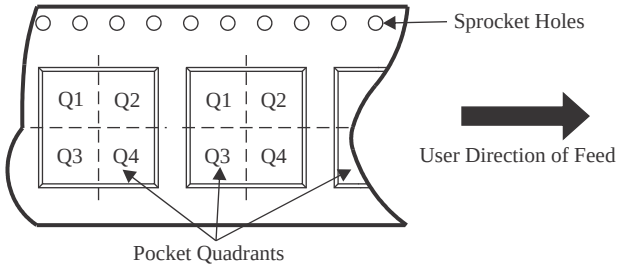


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

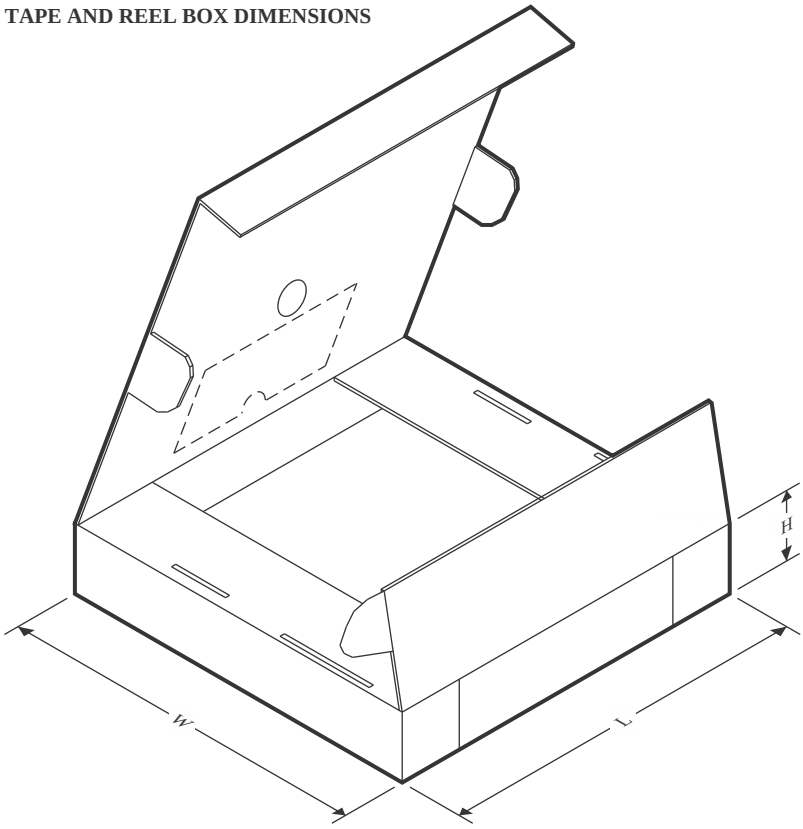
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2320AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA320AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA320AQDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA320AQDBVTQ1	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

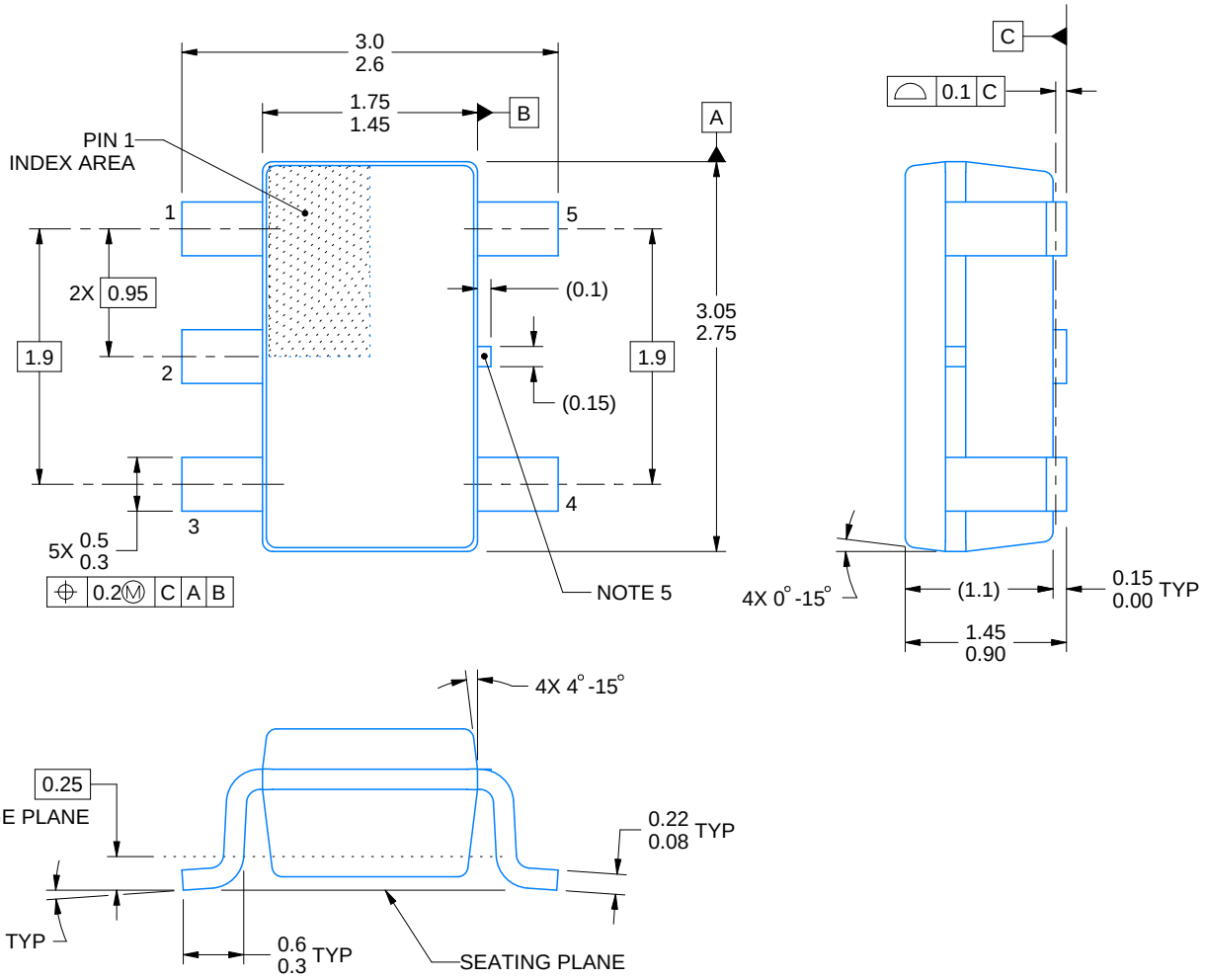
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2320AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA320AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA320AQDBVRQ1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA320AQDBVTQ1	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

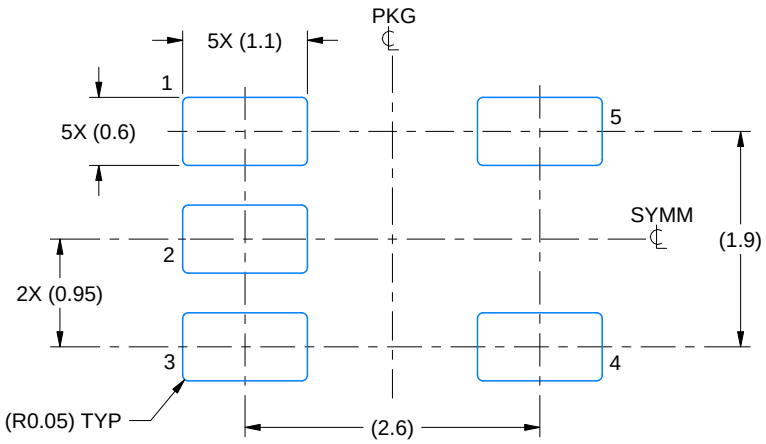
SMALL OUTLINE TRANSISTOR



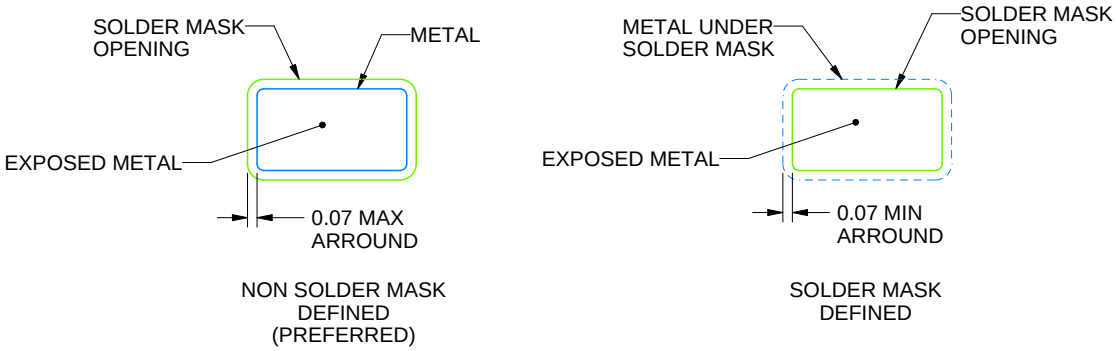
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

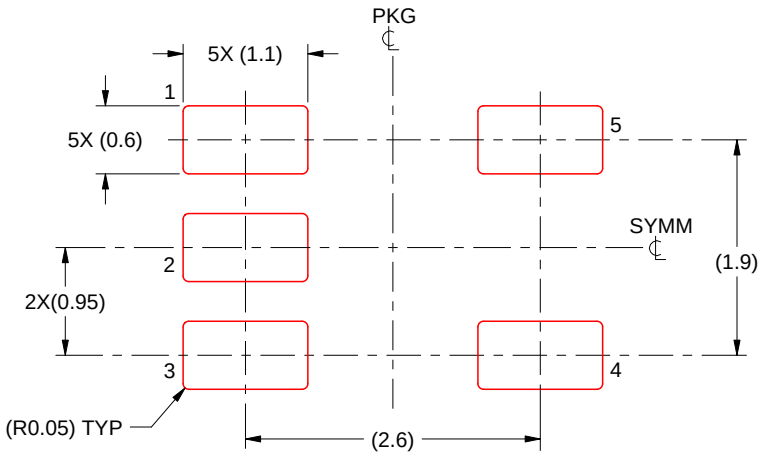


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

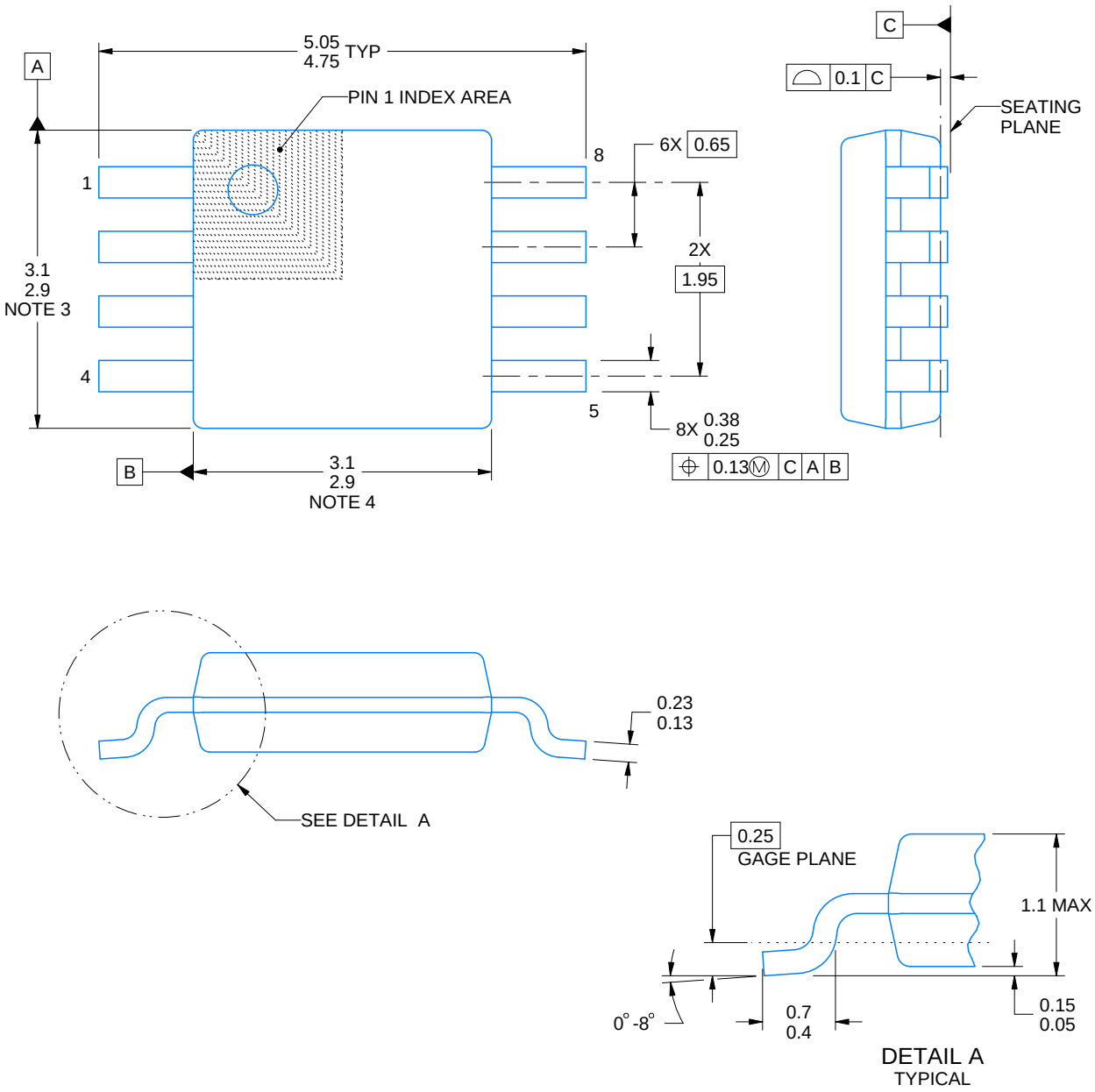
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

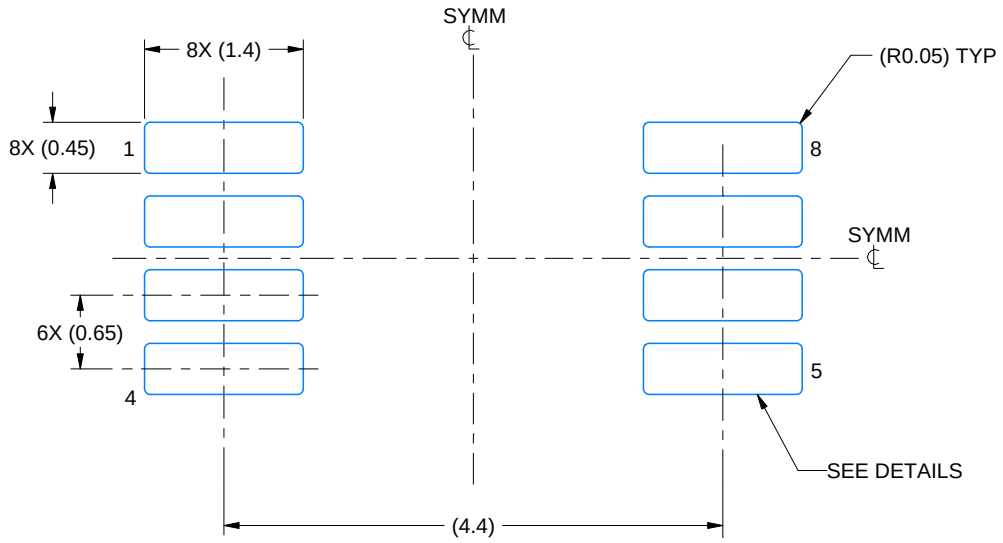
SMALL OUTLINE PACKAGE



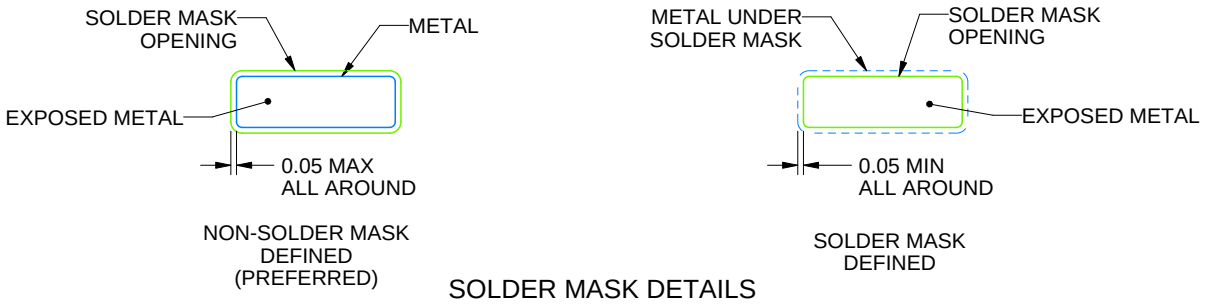
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

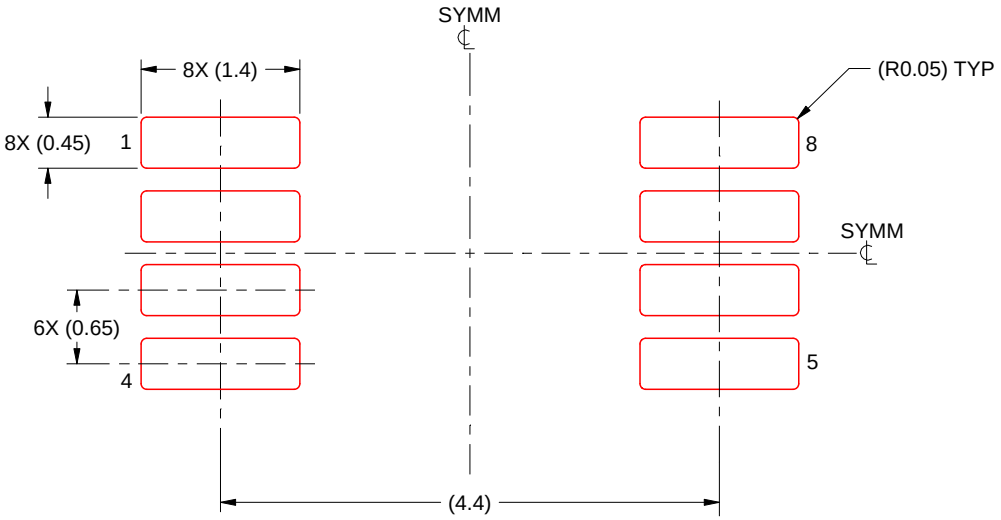


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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