3MHz，低功耗，低噪声，轨到轨输入输出 (RRI/O)，1.8V CMOS 运算放大器

查询样品: OPA2314-EP

特性

- 低 I_Q：**150μA/ch**（最大值）
- 宽电源电压：**1.8V** 至 **5.5V**
- 低噪声： **1kHz** 下为 **14nV/√Hz**
- 增益带宽：**3MHz**
- 低输入偏置电流：**0.2pA**
- 低偏移电压：**0.5mV**
- 单位增益稳定
- 内部射频 **(RF) /** 电磁干扰 **(EMI)** 滤波器

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装或测试场所
- 一个制造场所
- 支持扩展（**-40°C** 至 **150°C**）温度范围 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

应用范围

- 电池供电仪器：
  - 消费类应用、工业应用、医疗应用
  - 笔记本电脑、便携式媒体播放器
- 光电二极管放大器
- 有源滤波器
- 远程感测
- 无线仪表
- 手持测试设备

(1) 可提供额外温度范围-请与厂家联系

说明

OPA2314 是一款双通道运算放大器并且代表了新一代低功耗、通用 CMOS 放大器。 轨到轨输入和输出摆幅，低静态电流（在
V_S时为 5.0V 时的典型值为 150μA）与 3MHz 的宽带宽和极低噪声（1kHz 时为 14nV/√Hz）组合在一起使得这个系列对于要求在成本和性能间达到很好平衡的多种电池供电类应用具有很大的吸引力。 低输入偏置电流支持带有兆欧级源阻抗的应用。

OPA2314 器件的稳健耐用设计方便了电路设计人员的使用：负载电容高达 300pF 时单位增益稳定、一个集成的 RF/EMI 抑制滤波器、在过驱情况下无相位反转、以及高静电放电 (ESD) 保护（4kV 人体模型 (HBM)）。

这个器件针对低至 +1.8V (±0.9V) 和最高 +5.5V (±2.75V) 的低压运行进行了优化，并且其额定运行温度范围为 -40°C 至 +150°C 的完全扩展温度范围。

OPA2314（双通道）采用四方扁平无引线 （DFN)-8 封装。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-40°C to 150°C	DFN-8 – DRB	OPA2314ASDRBTEP	OUVS	V62/12626-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			UNIT
Supply voltage		7	V
Signal input terminals	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit(3)		Continuous	mA
Operating temperature, T_A		–40 to +150	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+170	°C
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V(1)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +150°C.**
At T_A = +25 °C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V_S+) – 1.3 V		0.5	2.5	mV
	Over temperature	**T_A = –40°C to +150°C**			**3.5**	**mV**
dV_{OS}/dT	**vs Temperature**			**1**		**µV/°C**
PSRR	vs Power supply	V_{CM} = (V_S+) – 1.3 V	78	92		dB
	V_S = 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	**T_A = –40°C to +150°C**	**72**			**dB**
	Channel separation, dc	At dc		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	**V_S = 1.8 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V, T_A = –40°C to +150°C**	**68**	**86**		**dB**
		V_S = 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V, T_A = –40°C to +150°C	**71**	**90**		**dB**
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V(2), T_A = –40°C to +150°C	**60**			
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±10	pA
	Over temperature	**T_A = –40°C to +150°C**			**±2**	**nA**
I_{OS}	Input offset current			±0.2	±10	pA
	Over temperature	**T_A = –40°C to +150°C**			**±2**	**nA**
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		5		μV_{PP}
e_n	Input voltage noise density	f = 10 kHz		13		$nV/\sqrt{Hz}$
		f = 1 kHz		14		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		5		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{IN}	Differential	V_S = 5.0 V		1		pF
	Common-mode	V_S = 5.0 V		5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-Loop Voltage Gain	V_S = 1.8 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	90	115		dB
		V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	100	128		dB
		V_S = 1.8 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ	90	100		dB
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ	94	110		dB
	Over temperature	**V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ**	**90**	**110**		**dB**
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ		**100**		**dB**
	Phase margin	V_S = 5.0 V, G = +1, R_L = 10 kΩ		65		deg

(1) Parameters with MIN and/or MAX specification limits are 100% production tested, unless otherwise noted.
(2) Limits are based on characterization and statistical analysis; not production tested.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V(1) (continued)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +150°C.**
At T_A = +25 °C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 1.8 V, R_L = 10 kΩ, C_L = 10 pF		2.7		MHz
		V_S = 5.0 V, R_L = 10 kΩ, C_L = 10 pF		3		MHz
SR	Slew rate(3)	V_S = 5.0 V, G = +1		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5.0 V, 2-V step , G = +1		2.3		µs
		To 0.01%, V_S = 5.0V, 2-V step , G = +1		3.1		µs
	Overload recovery time	V_S = 5.0 V, V_{IN} × Gain > V_S		5.2		µs
THD+N	Total harmonic distortion + noise(4)	V_S = 5.0 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ		0.001		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 10 kΩ		5	15	mV
		V_S = 5.5 V, R_L = 10 kΩ		5	20	mV
		V_S = 1.8 V, R_L = 2 kΩ		15	30	mV
		V_S = 5.5 V, R_L = 2 kΩ		22	40	mV
	Over temperature	**V_S = 5.5 V, R_L = 10 kΩ**			**30**	**mV**
		V_S = 5.5 V, R_L = 2 kΩ		**60**		**mV**
I_{SC}	Short-circuit current	V_S = 5.0 V		±20		mA
R_O	Open-loop output impedance	V_S = 5.5 V, f = 100 Hz		570		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	V_S = 1.8 V, I_O = 0 mA		130	180	µA
		V_S = 5.0 V, I_O = 0 mA		150	190	µA
	Over temperature	**V_S = 5.0 V, I_O = 0 mA**			**220**	**µA**
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		44		µs
TEMPERATURE						
	Specified range		–40		+150	°C
	Operating range		–40		+150	°C
	Storage range		–65		+150	°C

(3) Signifies the slower value of the positive or negative slew rate.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.

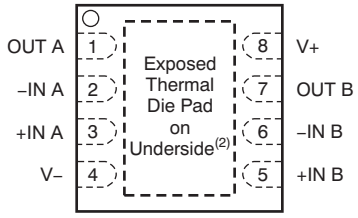
THERMAL INFORMATION

THERMAL METRIC(1)		OPA2314ASDRBTEP DRB (DFN) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	53.8	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	69.2	
θ_{JB}	Junction-to-board thermal resistance	20.1	
ψ_{JT}	Junction-to-top characterization parameter	3.8	
ψ_{JB}	Junction-to-board characterization parameter	20.0	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	11.6	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

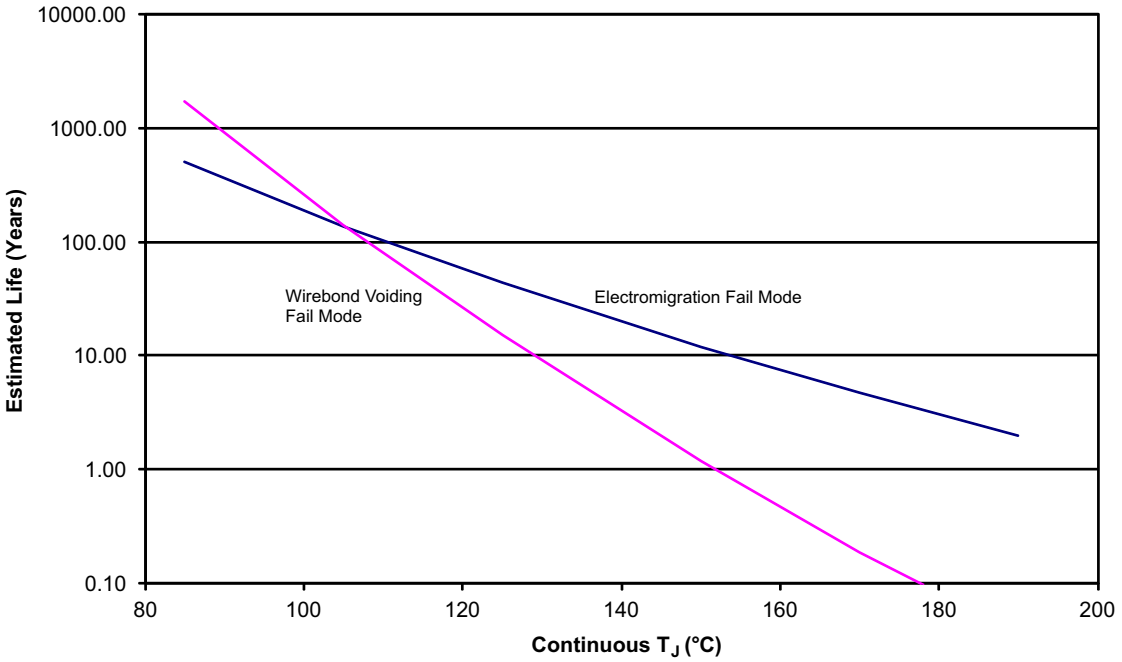
PIN CONFIGURATIONS

DRB PACKAGE(1)
DFN-8
(TOP VIEW)



(1) Pitch: 0,65mm.

(2) Connect thermal pad to V–. Pad size: 1,8mm × 1,5mm.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. OPA2314-EP Operating Life Derating Chart

TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

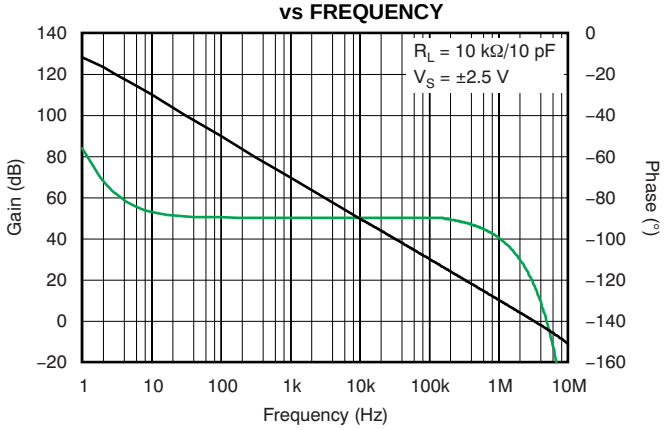


Figure 2.

OPEN-LOOP GAIN vs TEMPERATURE

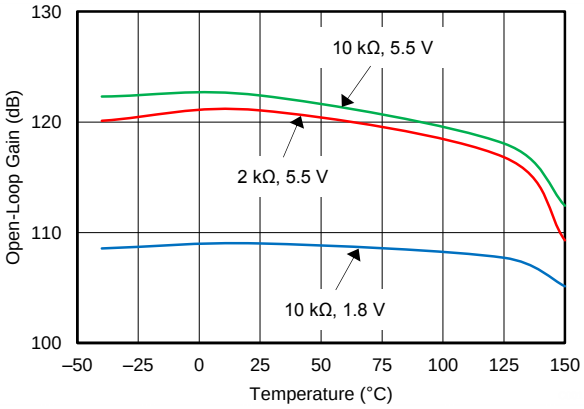


Figure 3.

QUIESCENT CURRENT vs SUPPLY

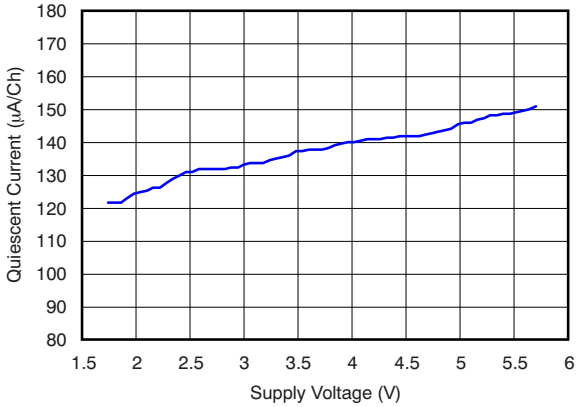


Figure 4.

QUIESCENT CURRENT vs TEMPERATURE

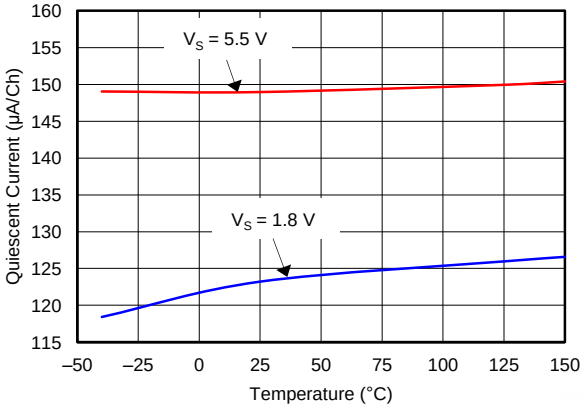


Figure 5.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

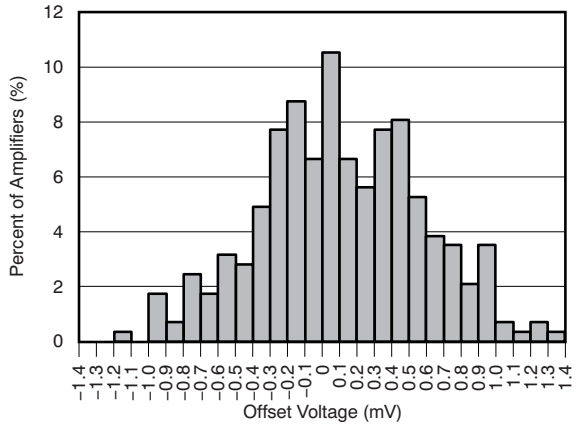


Figure 6.

OFFSET VOLTAGE DRIFT DISTRIBUTION

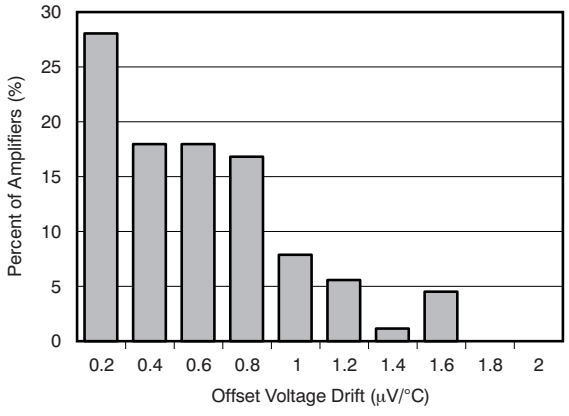


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

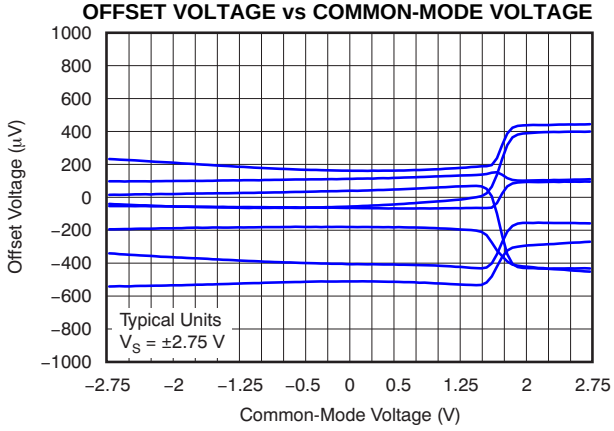


Figure 8.

OFFSET VOLTAGE vs TEMPERATURE

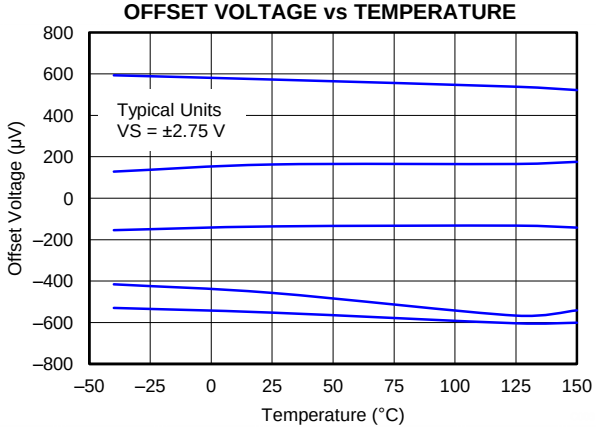


Figure 9.

CMRR AND PSRR vs FREQUENCY (Referred-to-Input)

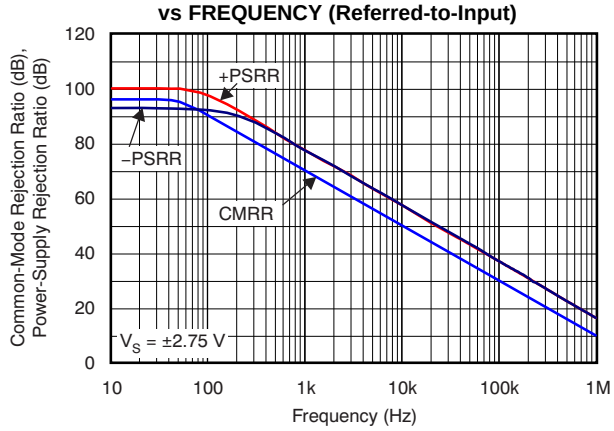


Figure 10.

CMRR AND PSRR vs TEMPERATURE

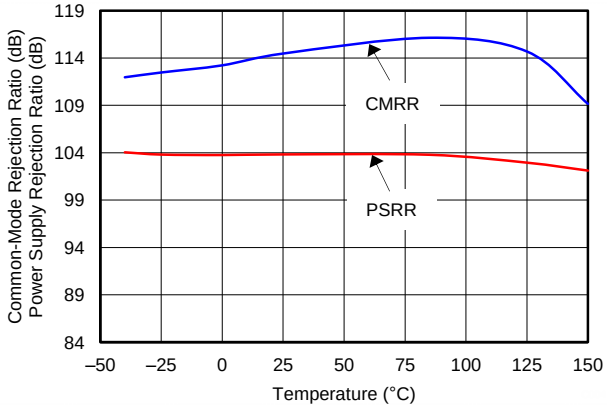


Figure 11.

0.1-Hz to 10-Hz INPUT VOLTAGE NOISE

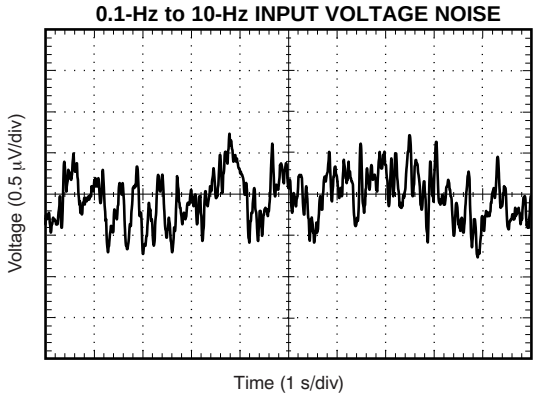


Figure 12.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

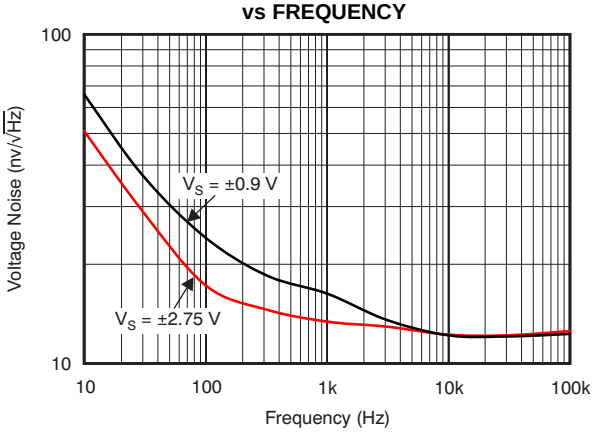


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

VOLTAGE NOISE vs COMMON-MODE VOLTAGE

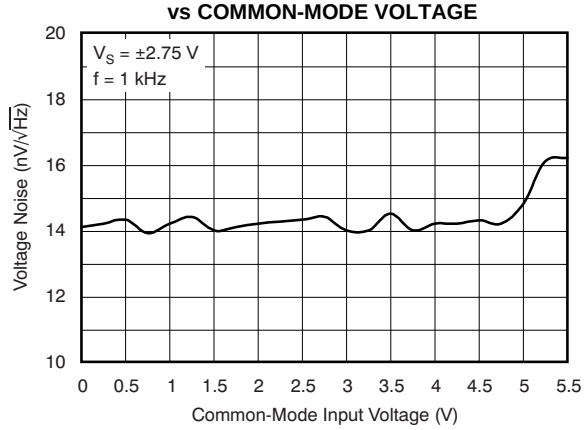


Figure 14.

INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

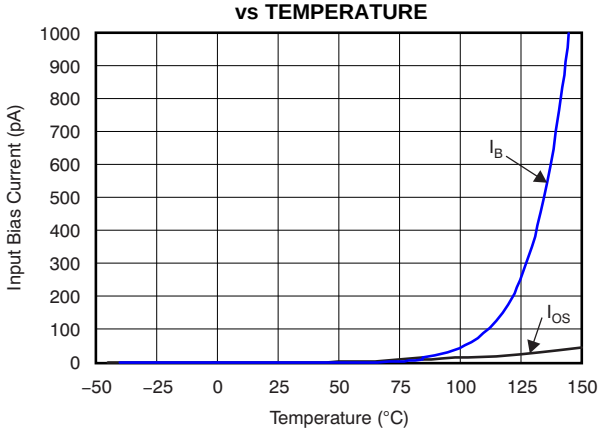


Figure 15.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

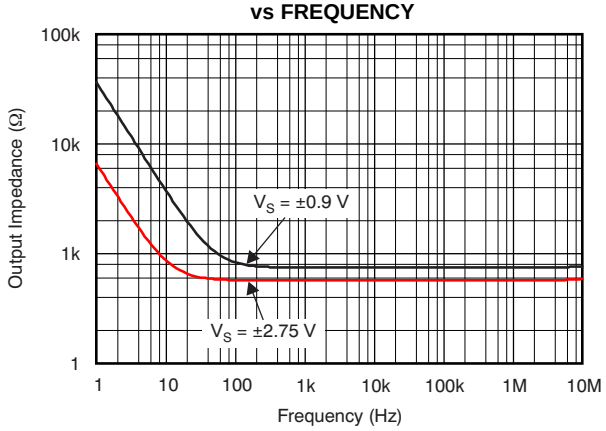


Figure 16.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY AND SUPPLY VOLTAGE

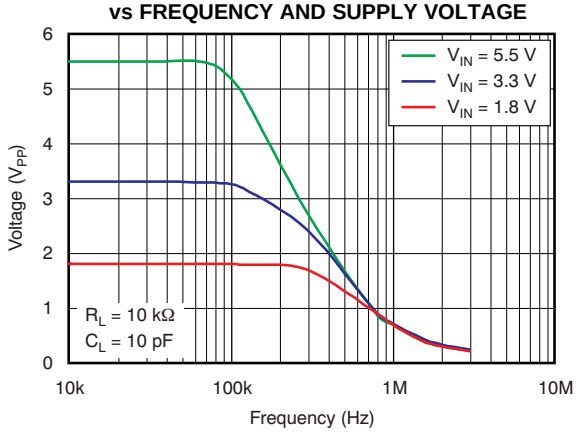


Figure 17.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (OVER TEMPERATURE)

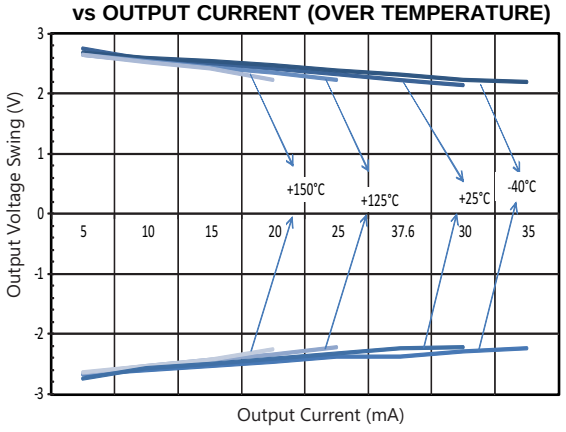


Figure 18.

CLOSED-LOOP GAIN vs FREQUENCY

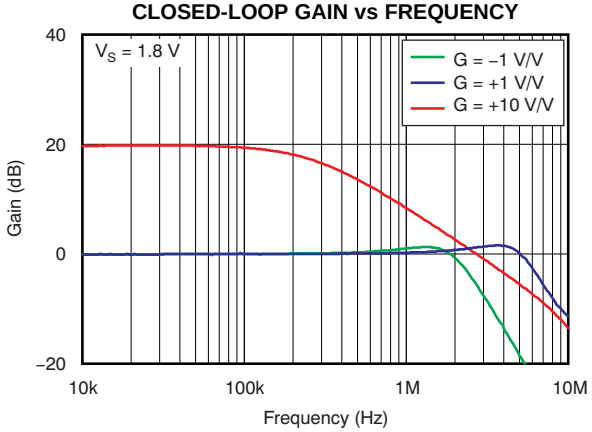


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

CLOSED-LOOP GAIN vs FREQUENCY

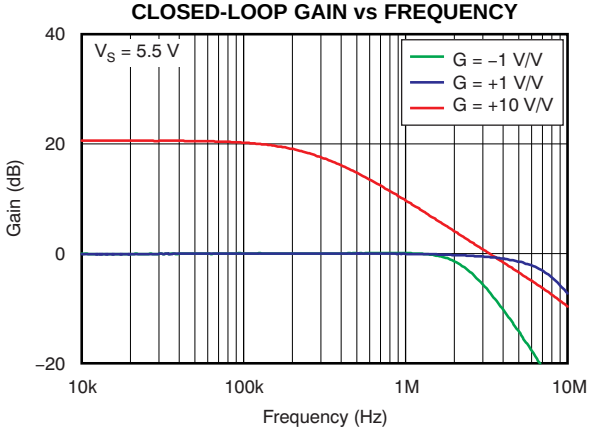


Figure 20.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

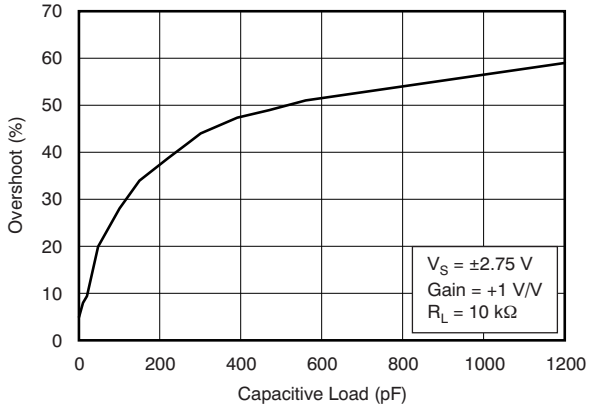


Figure 21.

SMALL-SIGNAL PULSE RESPONSE (NONINVERTING)

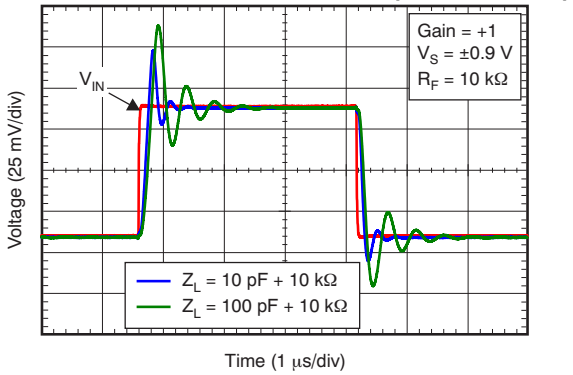


Figure 22.

SMALL-SIGNAL PULSE RESPONSE (INVERTING)

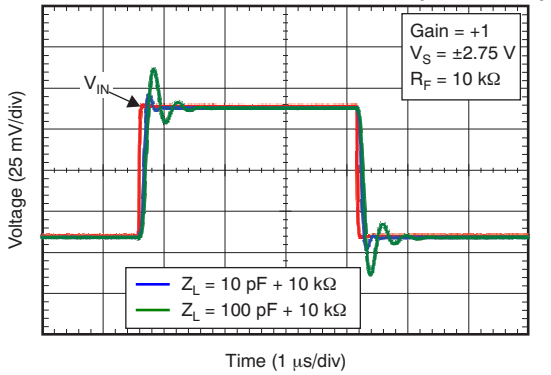


Figure 23.

LARGE-SIGNAL PULSE RESPONSE (NONINVERTING)

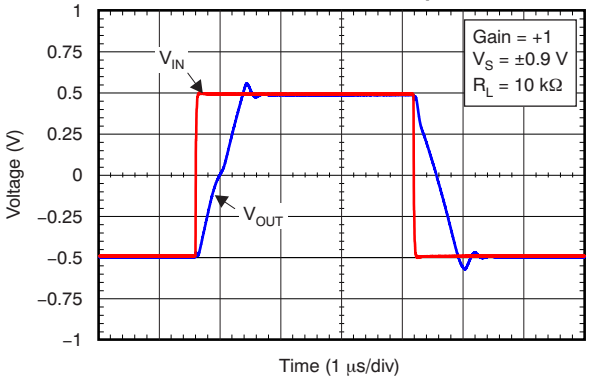


Figure 24.

LARGE-SIGNAL PULSE RESPONSE (INVERTING)

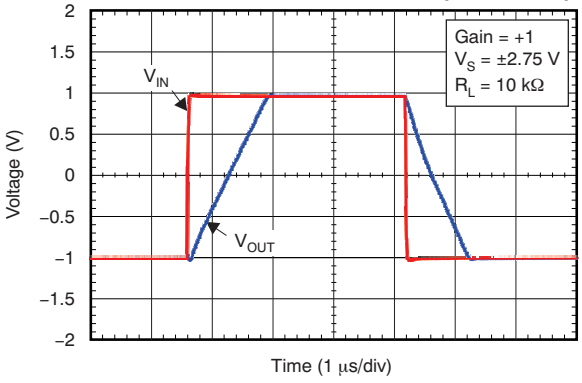


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

POSITIVE OVERLOAD RECOVERY

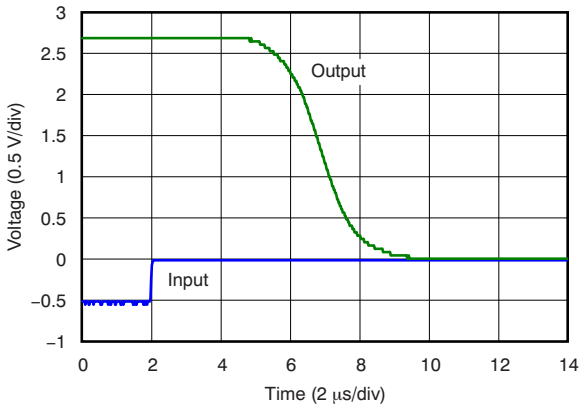


Figure 26.

NEGATIVE OVERLOAD RECOVERY

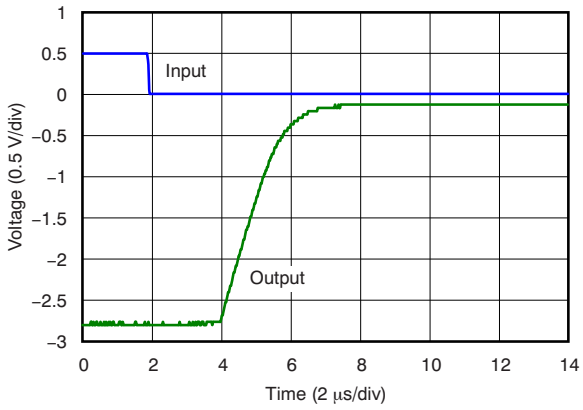


Figure 27.

NO PHASE REVERSAL

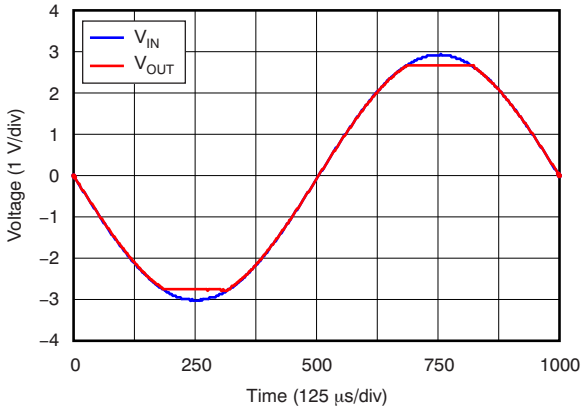


Figure 28.

CHANNEL SEPARATION vs FREQUENCY
OPA2314

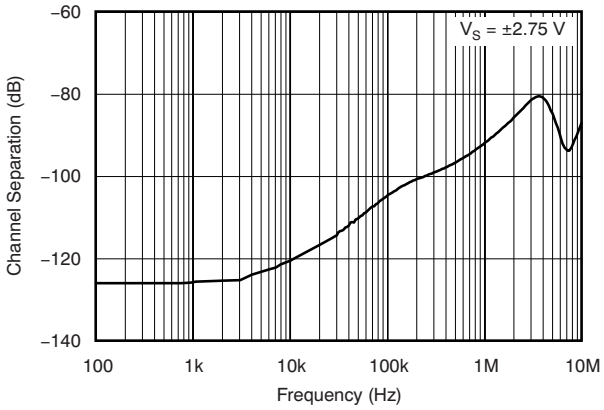


Figure 29.

THD+N vs OUTPUT AMPLITUDE
(G = +1 V/V)

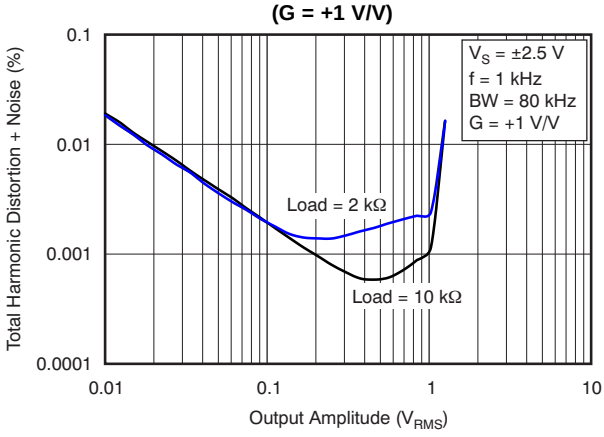


Figure 30.

THD+N vs OUTPUT AMPLITUDE
(G = –1 V/V)

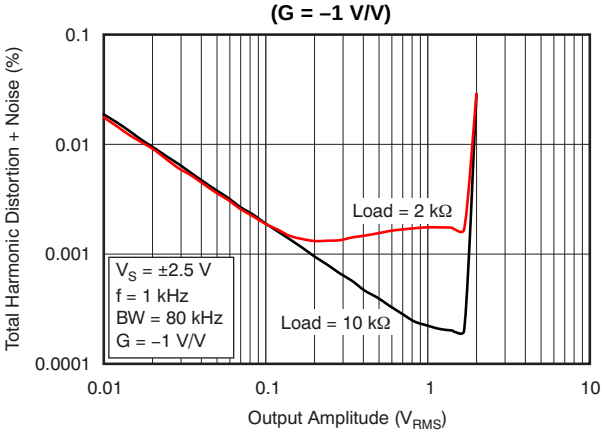


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

THD+N vs FREQUENCY

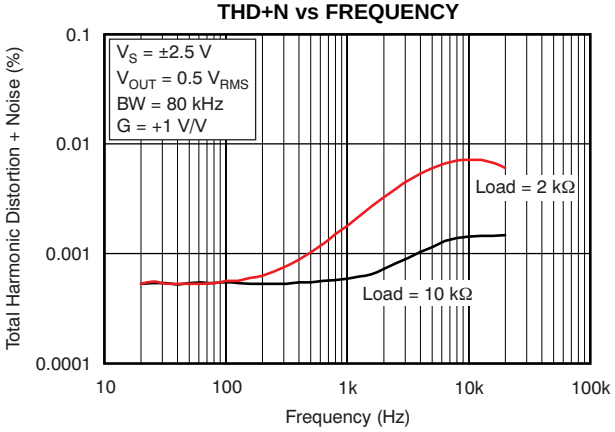


Figure 32.

ELECTROMAGNETIC INTERFERENCE REJECTION RATIO Referred to Noninverting Input (EMIRR IN+) vs FREQUENCY

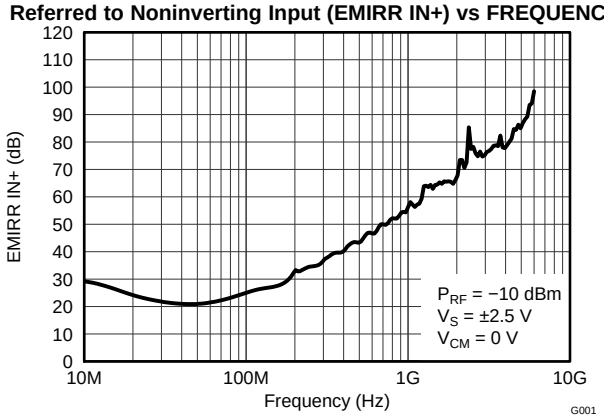


Figure 33.

APPLICATION INFORMATION

The OPA2314 is a low-power, rail-to-rail input/output operational amplifier specifically designed for portable applications. This device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2314 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The OPA2314 features 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good ac performance at very low power consumption. DC applications are also well served with a very low input noise voltage of 14 nV/√Hz at 1 kHz, low input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

Operating Voltage

The OPA2314 is fully specified and ensured for operation from +1.8 V to +5.5 V. In addition, many specifications apply from –40°C to +150°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics graphs. Power-supply pins should be bypassed with 0.01-μF ceramic capacitors.

Rail-to-Rail Input

The input common-mode voltage range of the OPA2314 extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 34. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

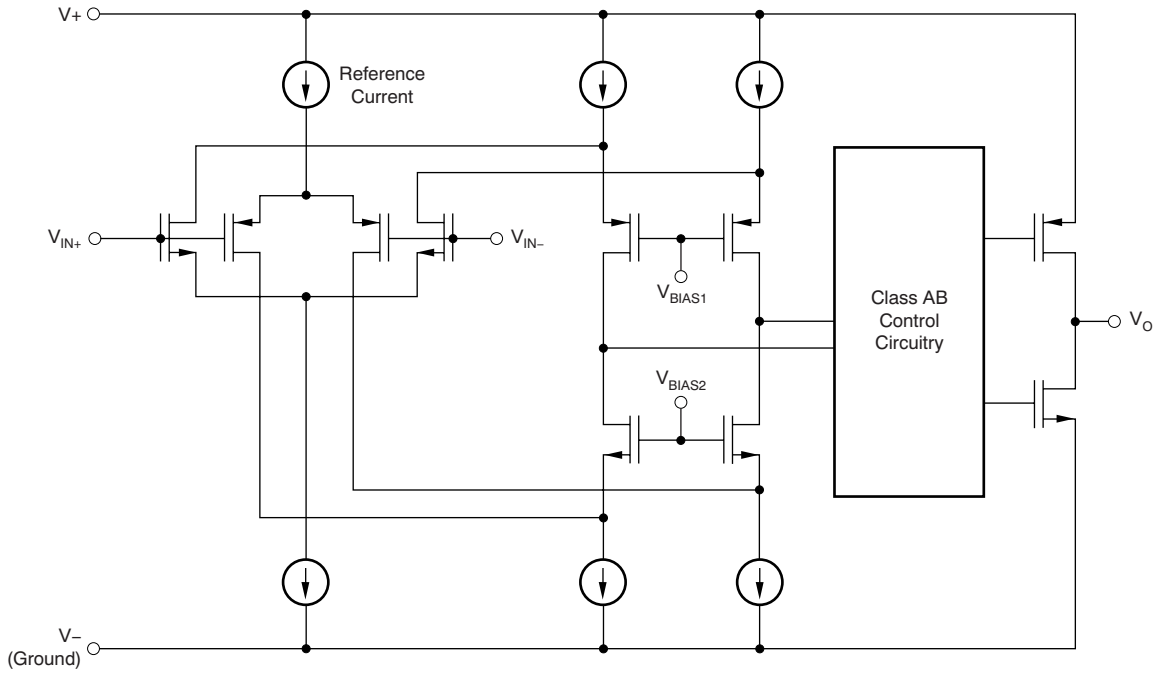


Figure 34. Simplified Schematic

Input and ESD Protection

The OPA2314 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 35 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

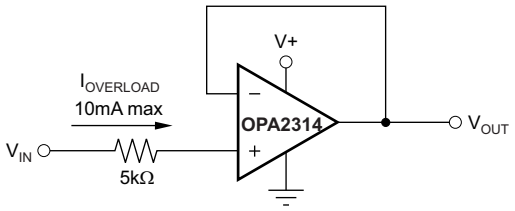


Figure 35. Input Current Protection

Common-Mode Rejection Ratio (CMRR)

CMRR for the OPA2314 is specified in several ways so the best match for a given application may be used; see the Electrical Characteristics. First, the CMRR of the device in the common-mode range below the transition region [VCM < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (VCM = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region (see Figure 8).

EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from its nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA2314 operational amplifier incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Figure 33 shows the results of this testing on the OPAx314. Detailed information can also be found in the application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from the TI website.

Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPA2314 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails, as can be seen in the typical characteristic graph, *Output Voltage Swing vs Output Current*.

Capacitive Load and Stability

The OPA2314 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA2314 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2314 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, *Small-Signal Overshoot vs. Capacitive Load*.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 36. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

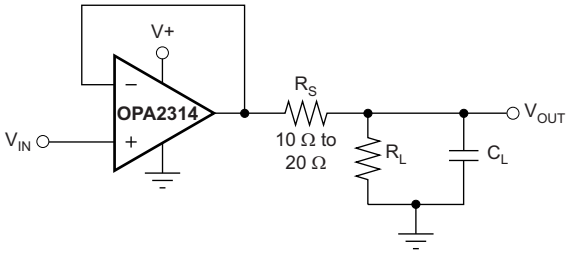


Figure 36. Improving Capacitive Load Drive

DFN Package

The OPA2314 (dual version) uses the DFN style package (also known as SON); this package is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes printed circuit board (PCB) space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low, 0.9-mm height. DFN packages are physically small, have a smaller routing area, improved thermal performance, reduced electrical parasitics, and use a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can easily be mounted using standard PCB assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download from the TI website at www.ti.com.

NOTE: The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V-).

APPLICATION EXAMPLES

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as Figure 37 illustrates.

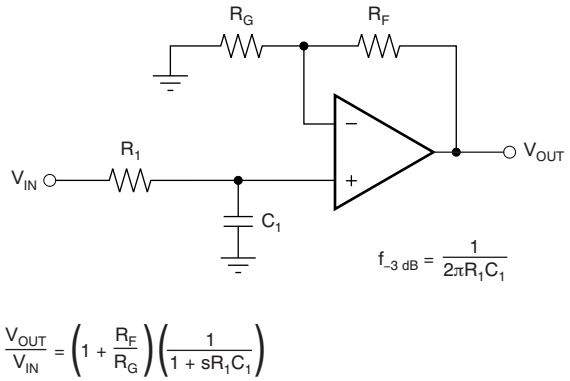


Figure 37. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as Figure 38 shows. For best results, the amplifier should have a bandwidth that is eight to 10 times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

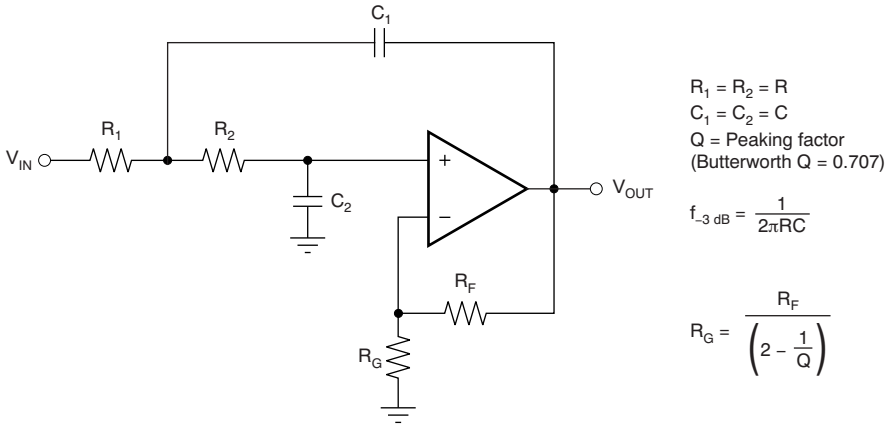


Figure 38. Two-Pole Low-Pass Sallen-Key Filter

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2314ASDRBTEP	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	OUVS
OPA2314ASDRBTEP.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	OUVS
OPA2314ASDRBTEP.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	OUVS
V62/12626-01XE	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	OUVS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA2314-EP :

- Catalog : OPA2314
- Automotive : OPA2314-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

GENERIC PACKAGE VIEW

DRB 8

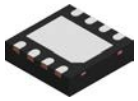
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

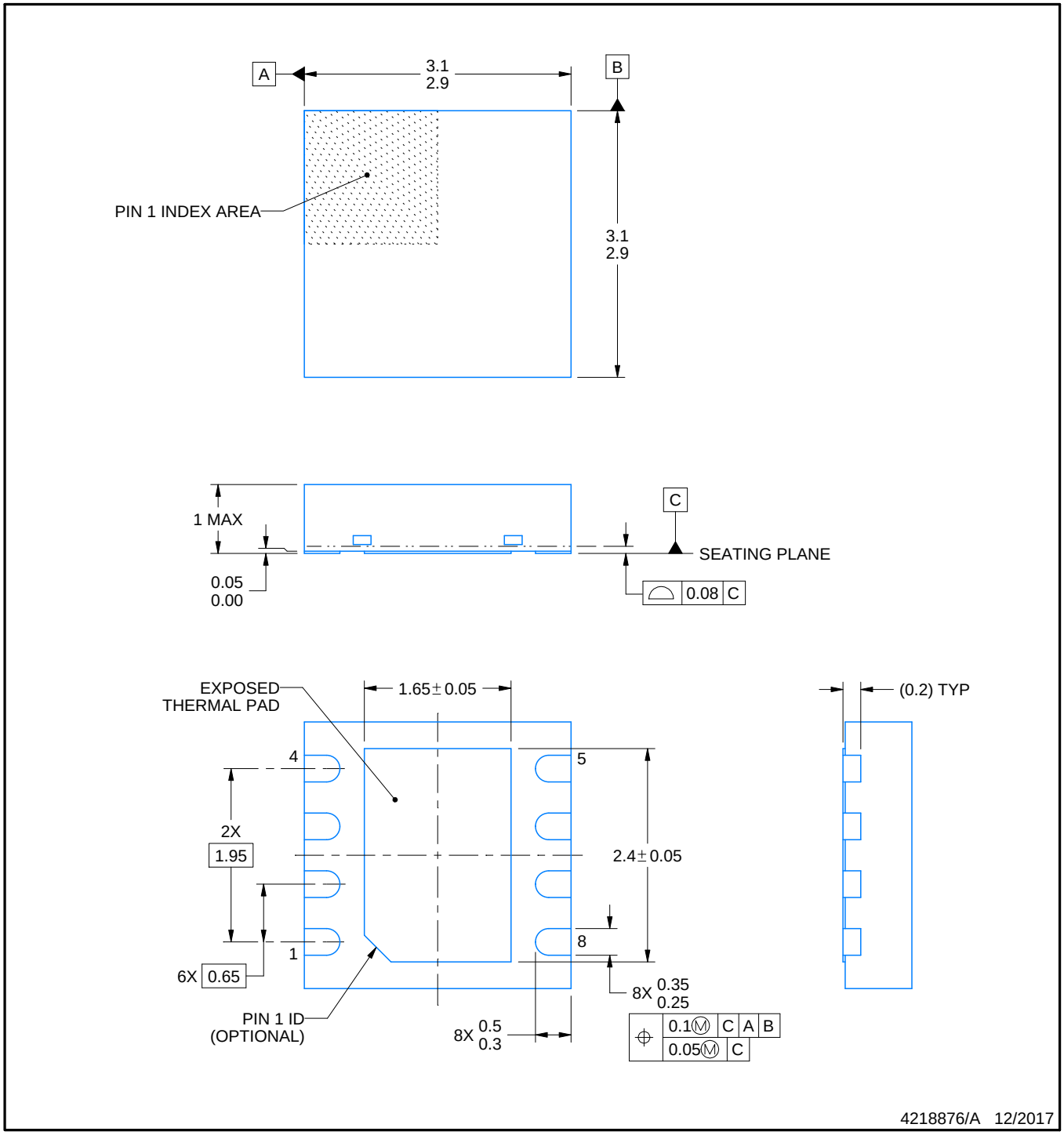
DRB0008B



PACKAGE OUTLINE

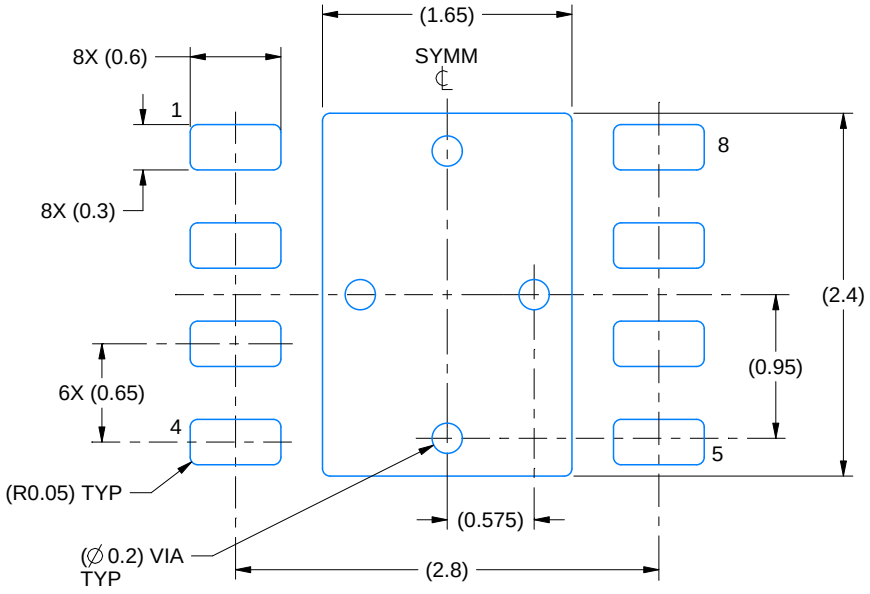
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

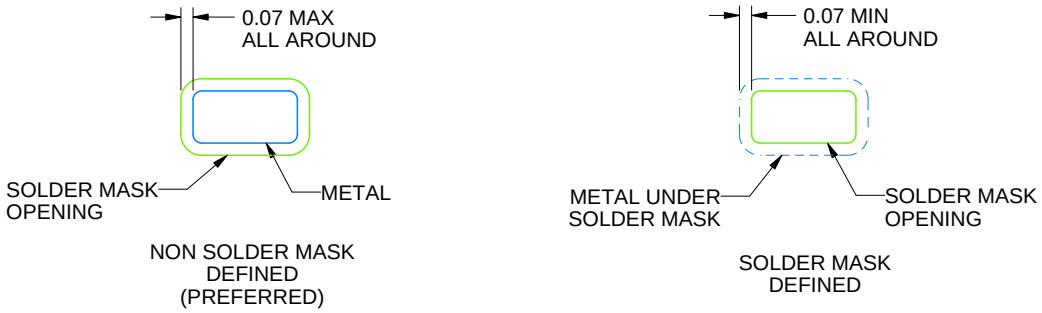


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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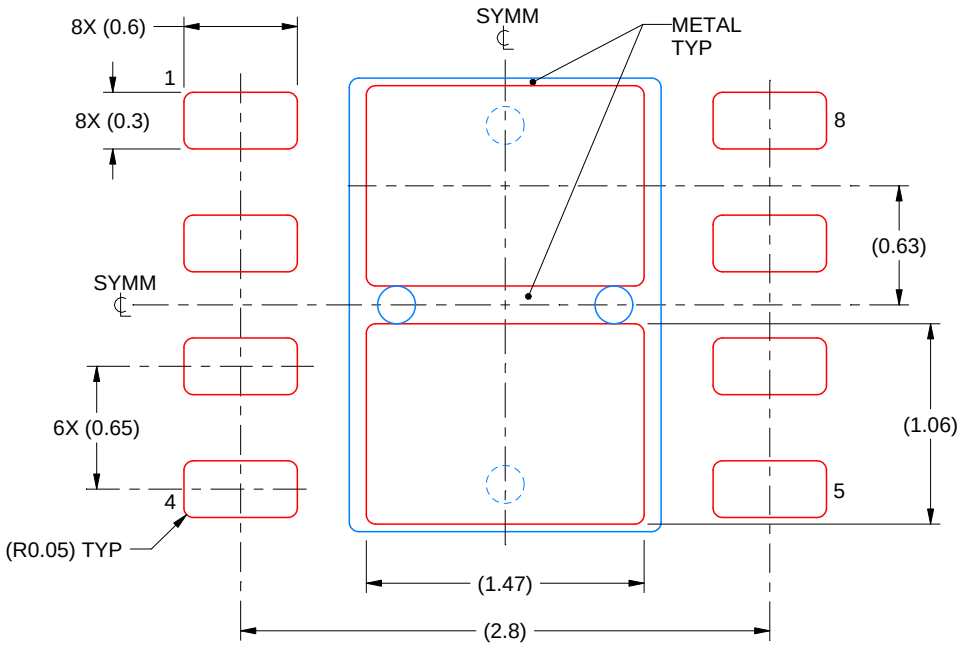
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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