OPA2277-EP 高精度、低噪声运算放大器

1 特性

- 超低偏移电压：10μV
- 高开环增益：134dB
- 高共模抑制比：140dB
- 高电源抑制比：130dB
- 低偏置电流：1nA（最大值）
- 宽电源电压范围：±2V 至 ±18V
- 低静态电流：800μA/放大器
- 支持国防、航天和医疗应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 支持军用（-55°C 至 125°C）温度范围 (1)
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

2 应用范围

- 换能器放大器
- 桥式放大器
- 温度测量
- 应变仪放大器
- 精密积分器
- 电池供电仪器
- 测试设备

(1) 欲了解其他可用温度范围，请与厂家联系

3 说明

OPA2277 高精度运算放大器取代了行业标准的 OP-177。 此器件改进了噪声性能，具有更宽的输出电压摆幅，并且在使静态电流减半的同时将速度提升了一倍。 其具有诸多特性，其中包括超低的偏移电压、超低漂移、低偏置电流、高共模抑制比及高电源抑制比。

OPA2277 由 ±2V 至 ±18V 电源供电运行，性能出色。 大多数运算放大器仅有一个指定的电源电压，而 OPA2277 有所不同，其电源电压取决于实际应用；唯一的限制条件是电源电压在 ±5V 至 ±15V 范围内。 当放大器输出摆幅达到指定限值时，可保持高性能。 由于初始偏移电压非常低（最高 ±20μV），因此通常无需用户调整。

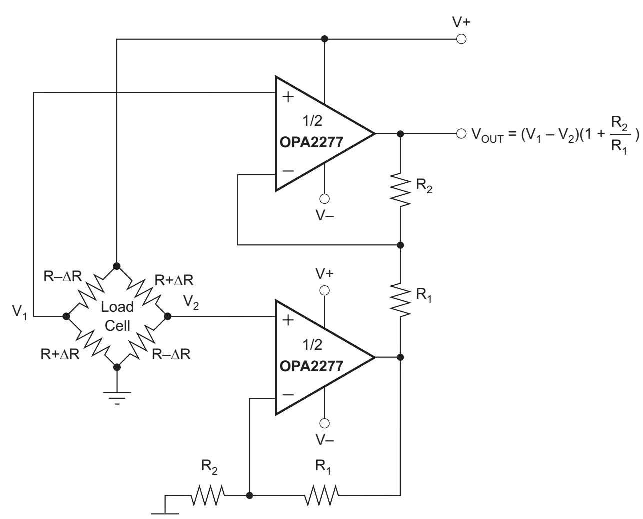
OPA2277 易于使用，而且不存在某些运算放大器中会出现的反相和过载问题。 其单位增益稳定，在宽范围负载条件下可保持出色的动态性能。 OPA2277 具有完全独立的电路，即便在过驱或过载时也可以实现最低串扰和零交互。 该器件提供 DIP-8 和 SO-8 两种封装。 OPA2277 的额定工作温度范围为 –55°C 至 125°C。

器件信息(1)

订货编号	封装	封装尺寸（标称值）
OPA2277MDTEP	SOIC (8)	3.91mm x 4.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 称重放大器原理图



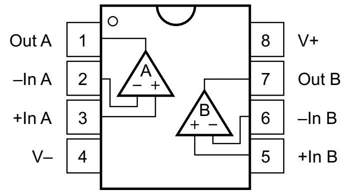
目录

5 修订历史记录

日期	修订版本	注释
2014年12月	*	最初发布。

6 Pin Configuration and Functions

D Package
8 Pins
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT A	1	O	Amplifier output A
–IN A	2	I	Inverting amplifier input A
+IN A	3	I	Non-inverting amplifier input A
V–	4	I	Negative amplifier power supply input
+IN B	5	I	Non-inverting amplifier input B
–IN B	6	I	Inverting amplifier input B
OUT B	7	O	Amplifier output B
V+	8	I	Positive amplifier power supply input

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltage		36	V
	Input voltage	(V–) – 0.7	(V+) + 0.7	V
	Output short-circuit (to ground)[2]	Continuous		
	Operating temperature	–55	125	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage temperature range	–55	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) One channel per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Specified voltage range	±5		±15	V
	Operating voltage range	±2		±18	V
T_J	Operating junction temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		OPA2277	UNIT
		D	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	
ψ_{JT}	Junction-to-top characterization parameter	3.9	
ψ_{JB}	Junction-to-board characterization parameter	39.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At T_A = 25°C, V_S = ±5 V to ±15 V, R_L = 2 kΩ (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±20	±65	µV
	vs temperature, T_J = –55°C to 125°C					±150	µV
	vs temperature (dV_{OS}/dT), T_J = –55°C to 125°C				±0.15		µV/°C
	vs power supply (PSRR)		V_S = ±2 V to ±18 V		±0.3	±1	µV/V
	T_J = –55°C to 125°C		V_S = ±2 V to ±18 V			±1	µV/V
	vs time				0.2		µV/mo
	Channel separation (dual)		dc		0.1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±2.8	nA
	T_J = –55°C to 125°C					±7	nA
I_{OS}	Input offset current				±0.5	±2.8	nA
	T_J = –55°C to 125°C					±7	nA
NOISE							
	Input voltage noise, f = 0.1 to 10 Hz				0.22		µVpp
					0.035		µVrms
e_n	Input voltage noise density	f = 10 Hz			12		nV/√Hz
		f = 100 Hz			8		nV/√Hz
		f = 1 Hz			8		nV/√Hz
		f = 10 Hz			8		nV/√Hz
i_n	Current noise density	f = 1 kHz			0.2		pA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection		V_{CM} = (V–) + 2 V to (V+) – 2 V	115	140		dB
	T_J = –55°C to 125°C		V_{CM} = (V–) + 2 V to (V+) – 2 V	115			dB
INPUT IMPEDANCE							
	Differential				100 || 3		MΩ || pF
	Common-mode		V_{CM} = (V–) + 2 V to (V+) – 2 V		250 || 3		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain T_J = –55°C to 125°C		V_O = (V–) + 0.5 V to (V+) – 1.2 V, R_L = 10 kΩ		140		dB
			V_O = (V–) + 1.5 V to (V+) – 1.5 V, R_L = 2 kΩ	126	134		dB
			V_O = (V–) + 1.5 V to (V+) – 1.5 V, R_L = 2 Ω	126			dB
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1		MHz
SR	Slew rate				0.8		V/µs
	Settling time	0.1%	V_S = ±15 V, G = 1, 10-V step		14		µs
		0.01%	V_S = ±15 V, G = 1, 10-V step		16		µs
	Overload recovery time		V_{IN} x G = V_S		3		µs
	Total harmonic distortion + noise (THD + N)		f = 1 kHz, G = 1, V_O = 3.5 Vrms		0.002%		

Electrical Characteristics (continued)

At T_A = 25°C, V_S = ±5 V to ±15 V, R_L = 2 kΩ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output	R_L = 10 kΩ	(V–) + 0.5		(V+) – 1.2	V
		R_L = 10 kΩ, T_J = –55°C to 125°C	(V–) + 0.5		(V+) – 1.2	V
		R_L = 2 kΩ	(V–) + 1.5		(V+) – 1.5	V
		R_L = 2 kΩ, T_J = –55°C to 125°C	(V–) + 1.5		(V+) – 1.5	V
I_{SC}	Short-circuit current			±35		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		
POWER SUPPLY						
V_S	Specified voltage range		±5		±15	V
	Operating voltage range		±2		±18	V
I_Q	Quiescent current (per amplifier)	I_O = 0 A		±790	±825	µA
	T_J = –55°C to 125°C	I_O = 0 A			±900	µA
TEMPERATURE RANGE						
	Specified temperature range		–55		125	°C
	Operating temperature range		–55		125	°C
T_{stg}	Storage temperature range		–55		125	°C

7.6 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

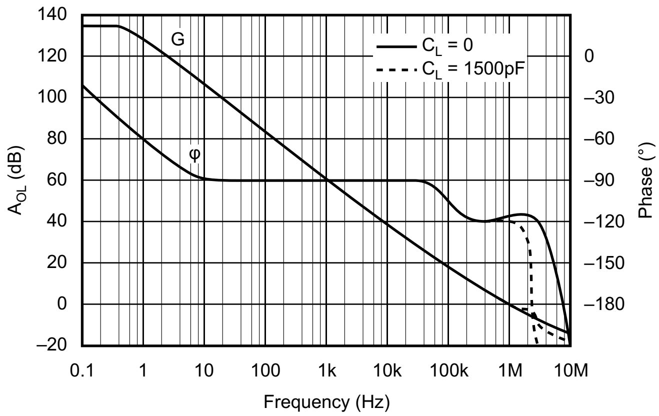


Figure 1. Open-Loop Gain/Phase vs Frequency

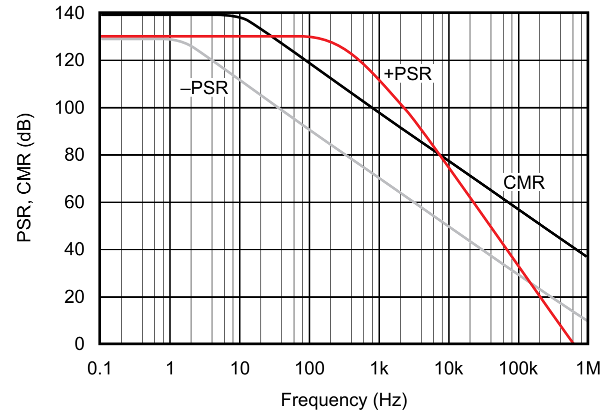


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

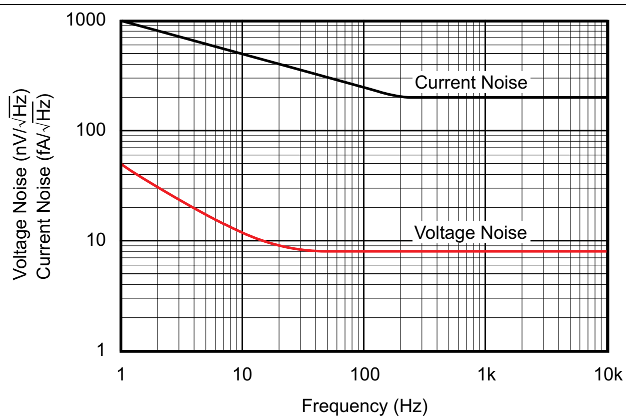


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency

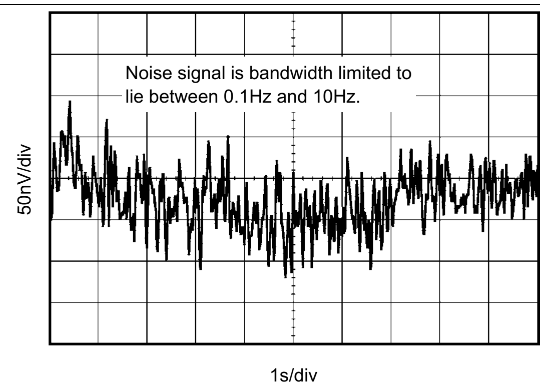


Figure 4. Input Noise Voltage vs Time

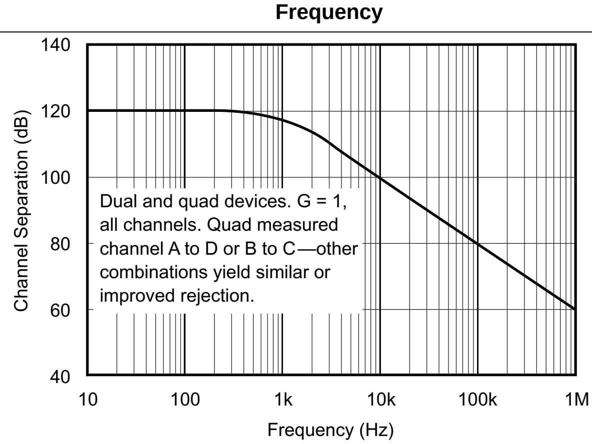
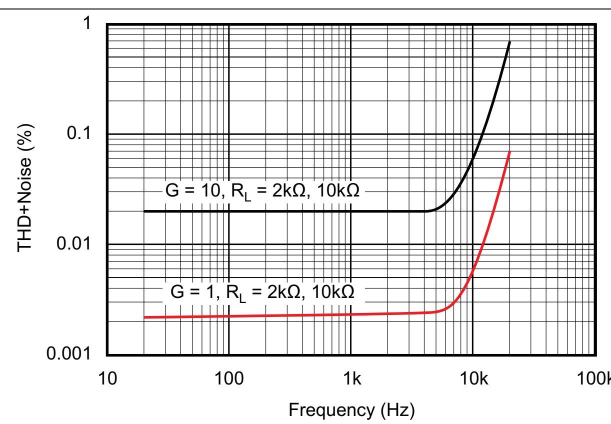


Figure 5. Channel Separation vs Frequency



V_{OUT} = 3.5 Vrms

Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

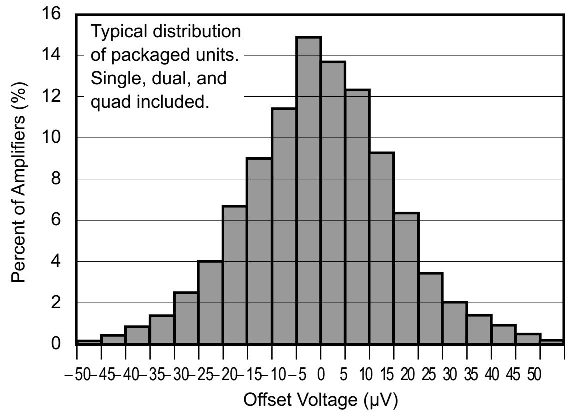


Figure 7. Offset Voltage Production Distribution

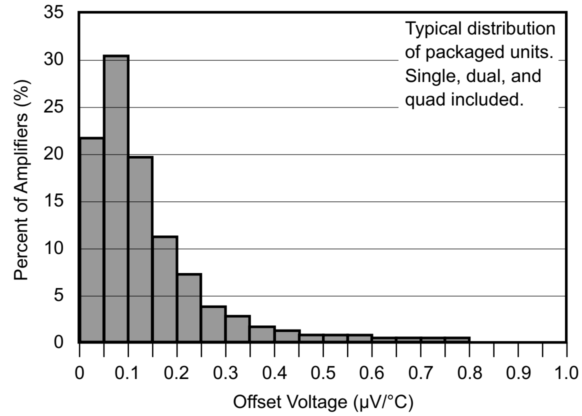


Figure 8. Offset Voltage Drift Production Distribution

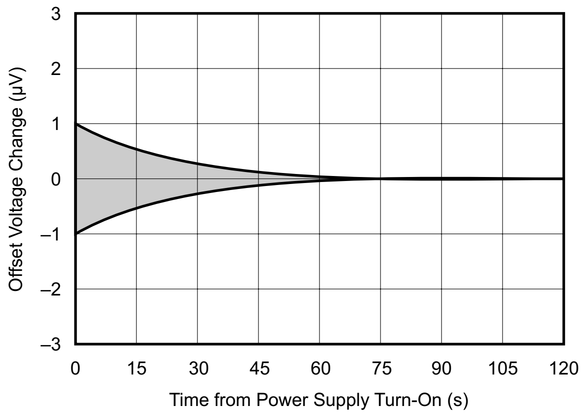


Figure 9. Warm-Up Offset Voltage Drift

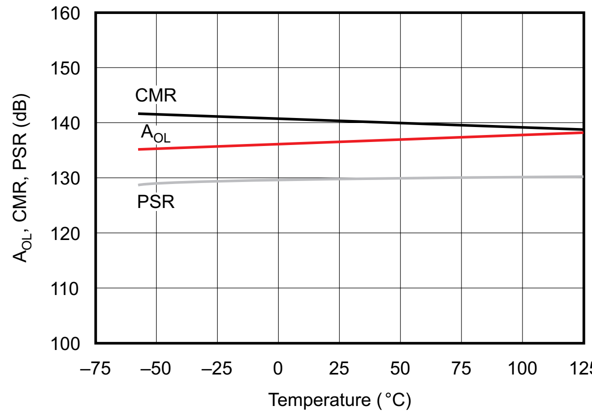


Figure 10. A_{OL}, CMR, PSR vs Temperature

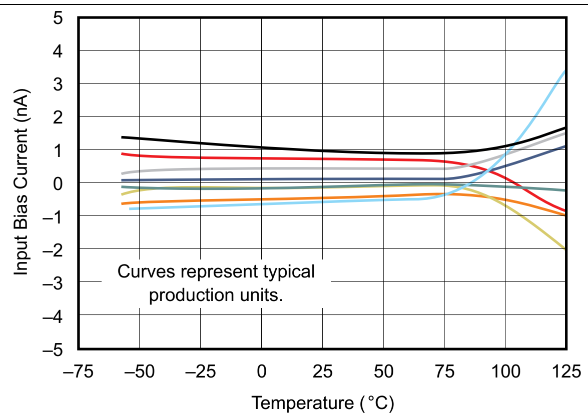


Figure 11. Input Bias Current vs Temperature

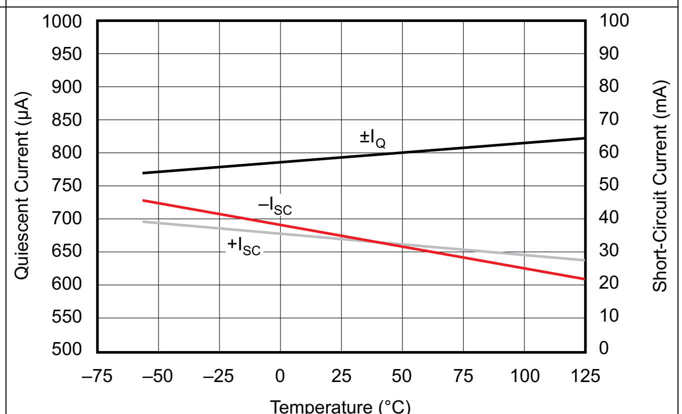


Figure 12. Quiescent Current and Short-Circuit Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

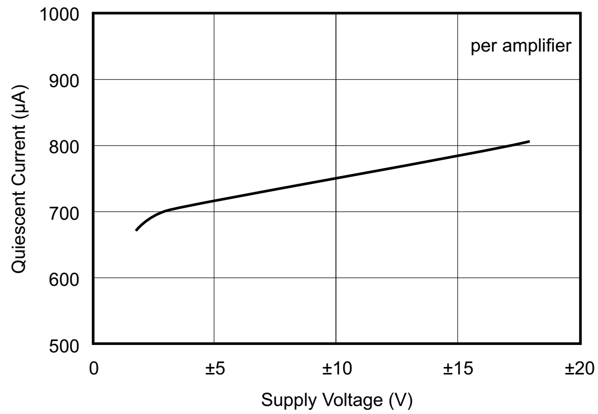


Figure 13. Quiescent Current vs Supply Voltage

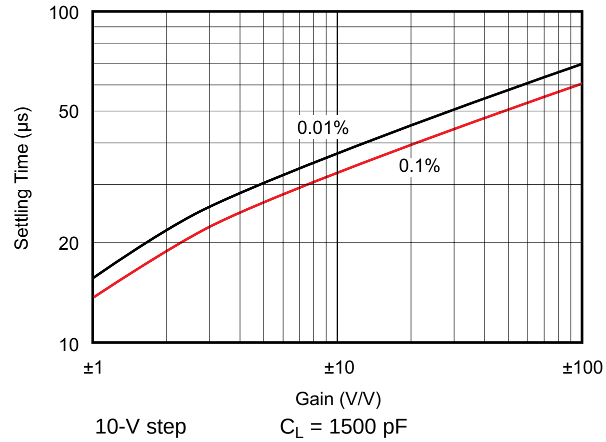


Figure 14. Settling Time vs Closed-Loop Gain

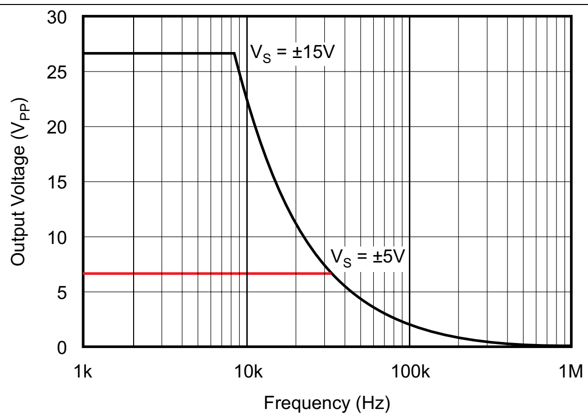


Figure 15. Maximum Output Voltage vs Frequency

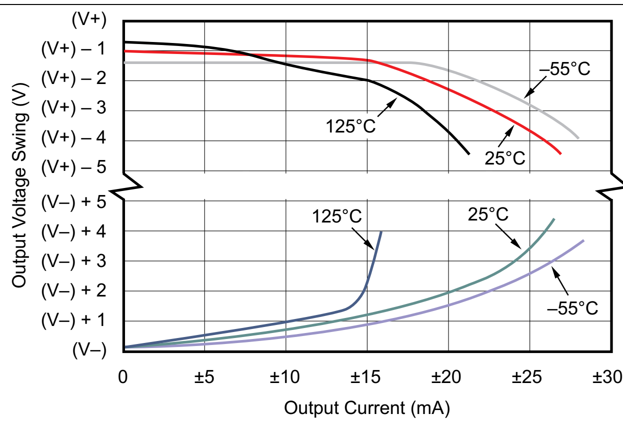


Figure 16. Output Voltage Swing vs Output Current

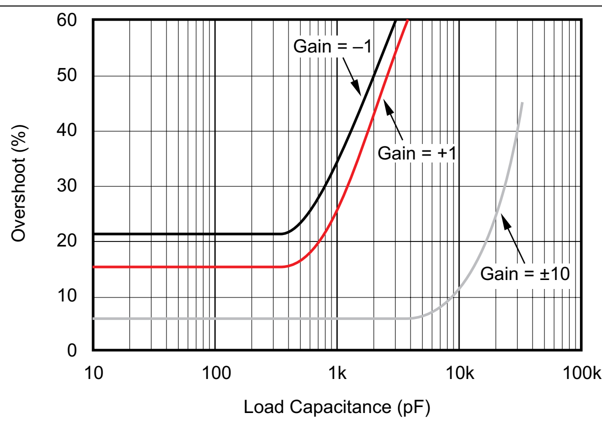


Figure 17. Small-Signal Overshoot vs Load Capacitance

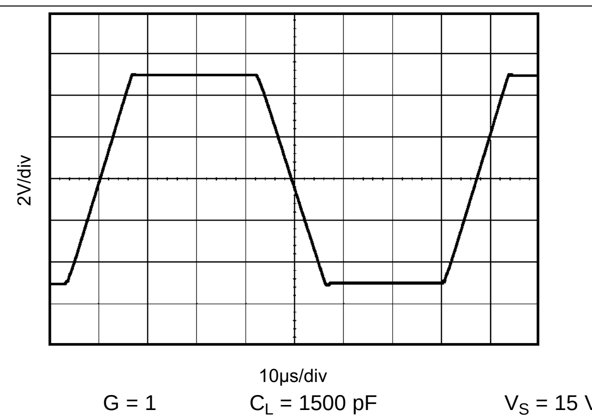
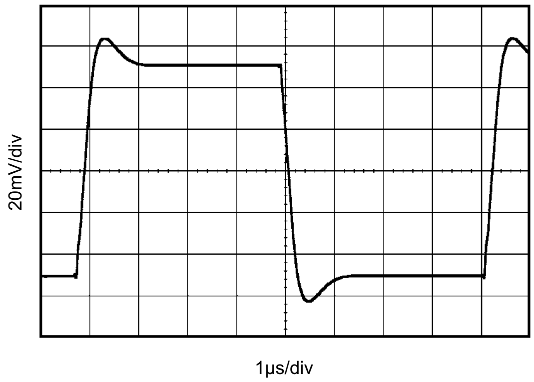


Figure 18. Large-Signal Step Response

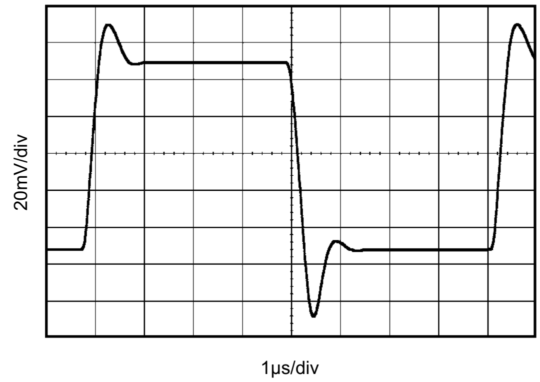
Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



G = 1 C_L = 0 pF V_S = 15 V

Figure 19. Small-Signal Step Response



G = 1 C_L = 1500 pF V_S = 15 V

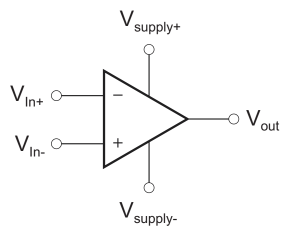
Figure 20. Small-Signal Step Response

8 Detailed Description

8.1 Overview

The OPA2277 is a unity-gain stable, high-precision, and low-noise operational amplifier. OPA2277 operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2277 is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. High performance is maintained as the amplifiers swing to their specified limit. Because the initial offset voltage (±50-μV max) is so low, user adjustment is usually not required.

8.2 Functional Block Diagram



8.3 Feature Description

The OPA2277 precision operational amplifier replaces the industry standard OP-177. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power-supply rejection.

OPA2277 is easy to use and free from phase inversion and overload problems found in some operational amplifiers. It is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. OPA2277 features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA2277 is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

9.2 Typical Application

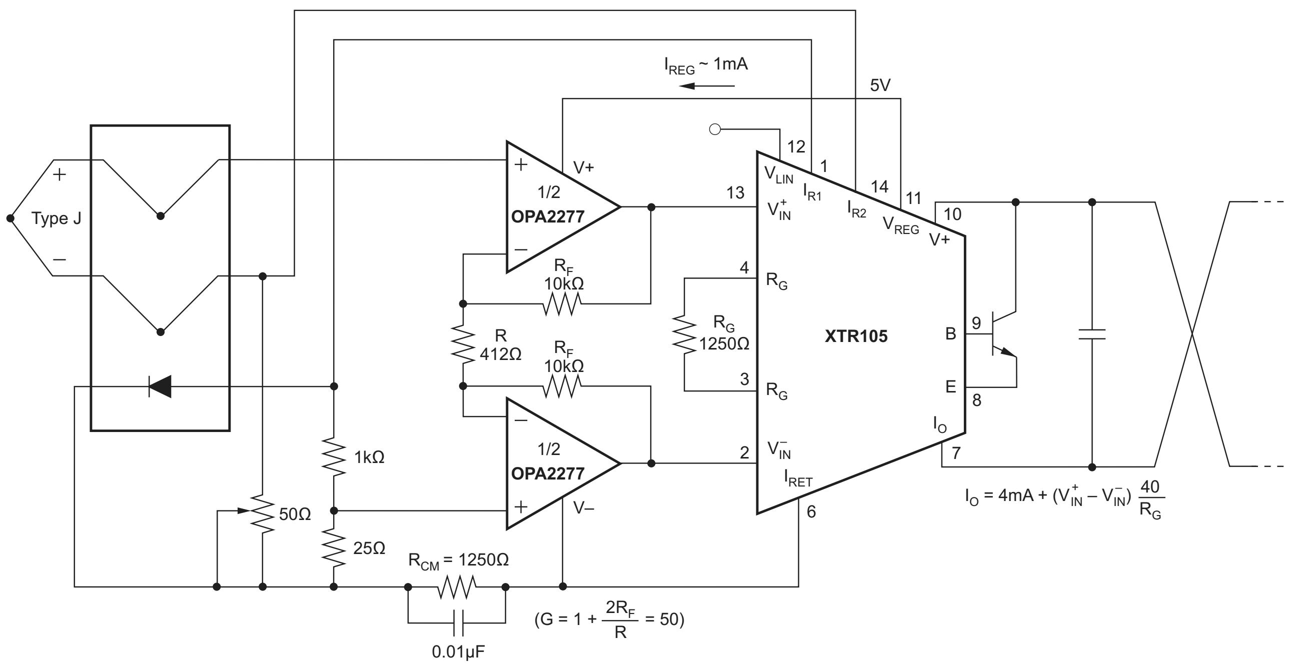


Figure 21. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

9.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation (see Figure 21), Table 1 lists the design parameters needed with gain = 50.

$$G = 1 + \frac{2R_F}{R} = 50 \tag{1}$$

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_F	10 kΩ
R	412 Ω

9.2.2 Detailed Design Procedure

9.2.2.1 Offset Voltage Adjustment

The OPA2277 is laser-trimmed for very-low offset voltage and drift so most circuits do not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 22. Only use this adjustment to null the offset of the operational amplifier. Do not use this adjustment to compensate for offsets created elsewhere in a system because this can introduce additional temperature drift.

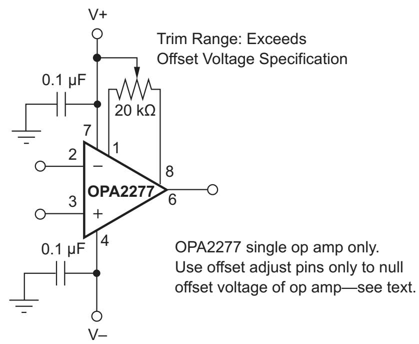


Figure 22. OPA2277 Offset Voltage Trim Circuit

9.2.2.2 Input Protection

The inputs of the OPA2277 are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but does not damage the operational amplifier.

9.2.2.3 Input Bias Current Cancellation

The input stage base current of the OPA2277 is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor as is often done with other operational amplifiers (see Figure 23). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

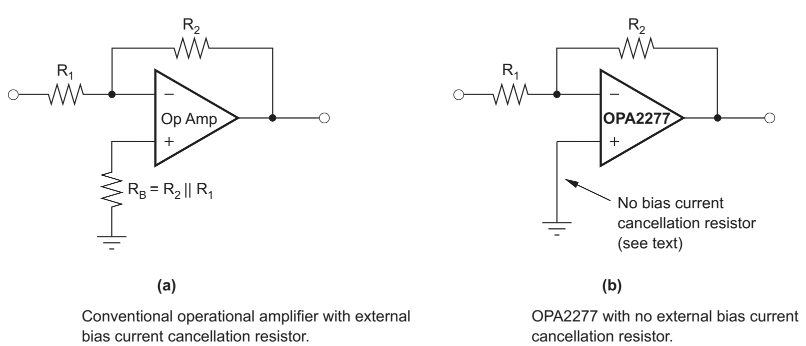
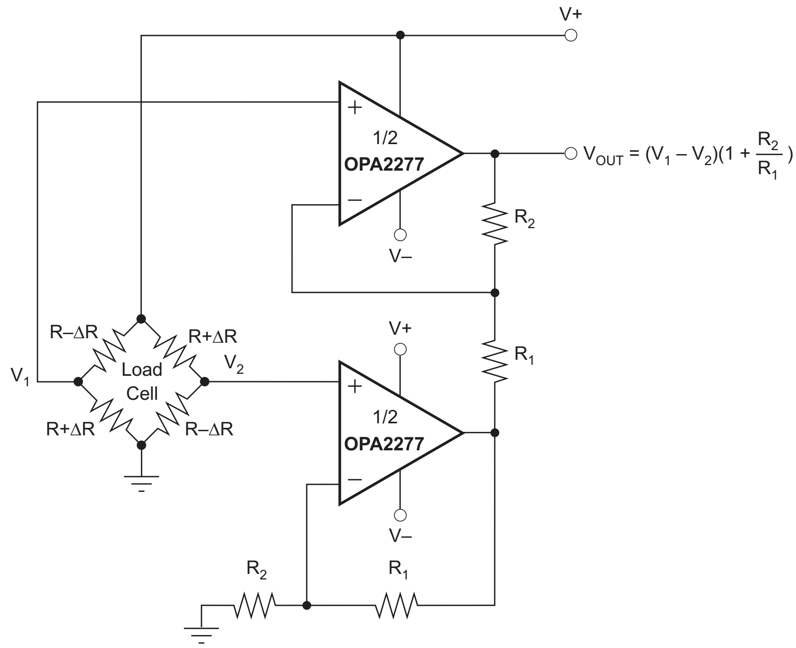


Figure 23. Input Bias Current Cancellation



A. For integrated solution see: INA126, INA2126 (dual), INA125 (on-board reference), or INA122 (single-supply).

Figure 24. Load Cell Amplifier

9.2.3 Application Curves

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ. Figure 25 shows Change in input bias current versus power supply voltage. Curve shows normalized change in bias current with respect to V_S = ±10 V (+20 V). Typical IB may range from –0.5 to 0.5 nA at V_S = ±10 V. Figure 26 shows change in input bias current versus common-mode voltage. Curve shows normalized change in bias current with respect to V_{CM} = 0 V. Typical IB may range from –0.5 to 0.5 nA at V_{CM} = 0 V.

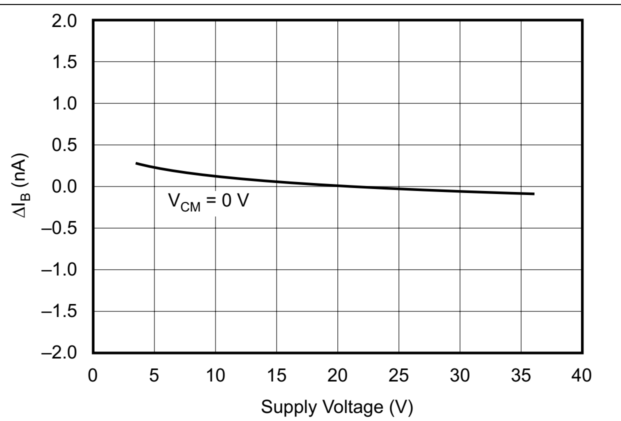


Figure 25. Change in Input Bias Current vs Power Supply Voltage

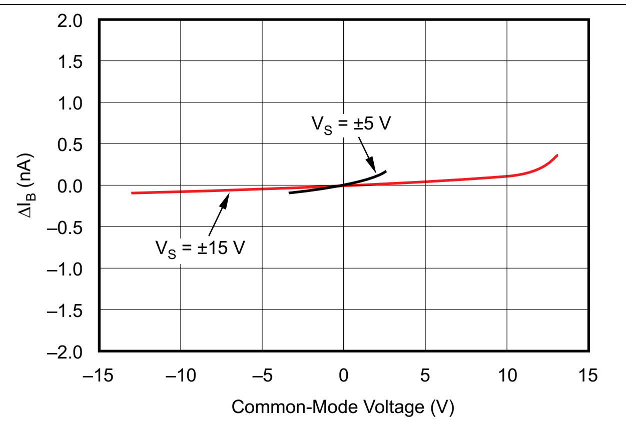


Figure 26. Change in Input Bias Current vs Common-Mode Voltage

10 Power Supply Recommendations

The OPA2277 operational amplifier operates from ±2.5- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2277 is specified for real-world applications. A single set of specifications applies over the ±5- to ±15-V supply range. Specifications are ensured for applications between ±5- and ±15-V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA2277 can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply could be set to 25 V with the negative supply at –5 V, or vice-versa. In addition, key parameters are ensured over the specified temperature range, –55°C to 125°C. The *Typical Characteristics* show parameters which vary significantly with operating voltage or temperature.

11 Layout

11.1 Layout Guidelines

Solder the lead-frame die pad to a thermal pad on the PCB. Mechanical drawings in *机械封装和可订购信息* show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA2277 has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential which can degrade the ultimate performance of the OPA2277. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

11.2 Layout Example

11.2.1 Board Layout

This demonstration fixture is a two-layer PCB. It uses a ground plane on the bottom, and signal and power traces on the top. The ground plane has been opened up around Op Amp pins sensitive to capacitive loading. Power-supply traces are laid out to keep current loop areas to a minimum. The SMA (or SMB) connectors may be mounted either vertically or horizontally.

The location and type of capacitors used for power-supply bypassing are crucial to high-frequency amplifiers. The tantalum capacitors, C_1 and C_2, do not need to be as close to pins 7 and 4 on your PCB, and may be shared with other amplifiers.

11.2.2 Measurement Tips

This demonstration fixture and the component values shown are designed to operate in a 50Ω environment. Most data sheet plots are obtained in this manner. Change the component values for different input and output impedance levels.

Do not use high-impedance probes; they represent a heavy capacitive load to the Op Amps, and will alter the amplifier response. Instead, use low impedance (≤ 500Ω) probes with adequate bandwidth. The probe input capacitance and resistance set an upper limit on the measurement bandwidth. If a high-impedance probe must be used, place a 100Ω resistor on the probe tip to isolate its capacitance from the circuit.

Layout Example (continued)

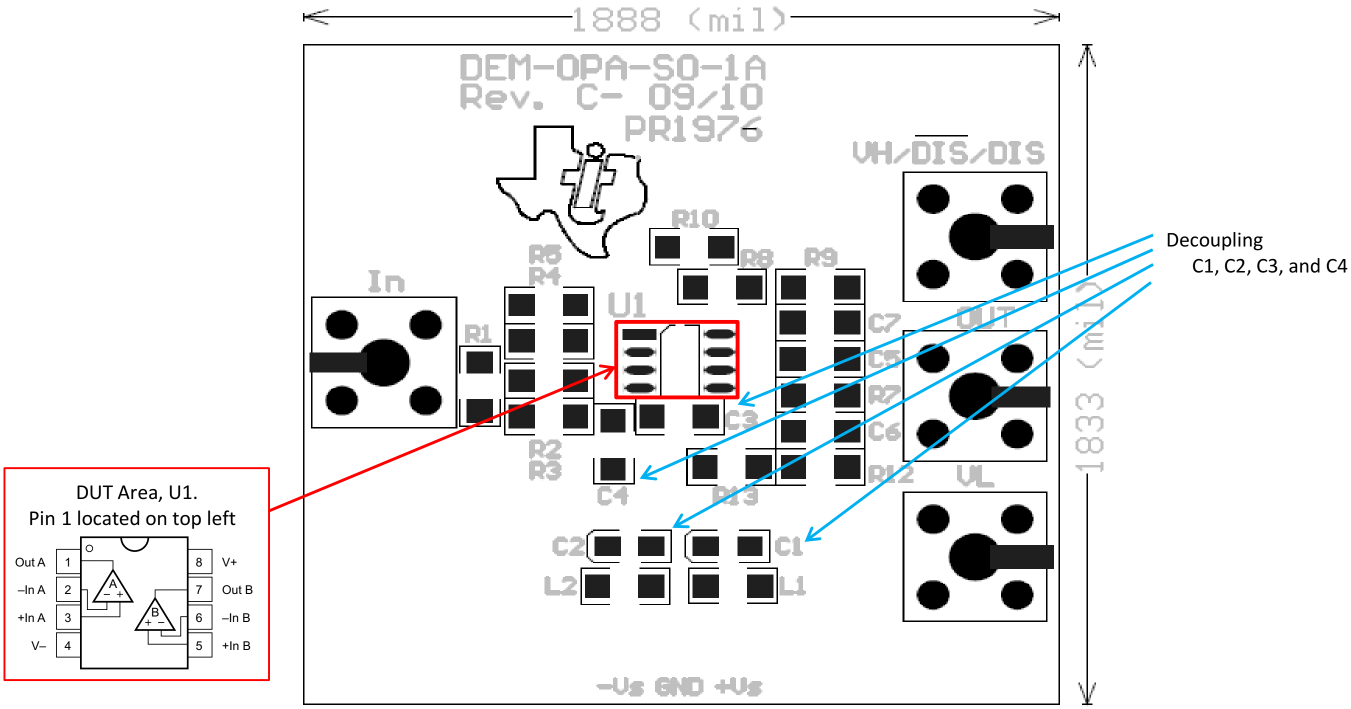


Figure 27. Decoupling Capacitors and DUT Area

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2277MDTEP	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 2277E
OPA2277MDTEP.A	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 2277E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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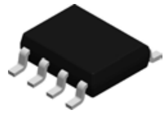
OTHER QUALIFIED VERSIONS OF OPA2277-EP :

- Catalog : OPA2277

NOTE: Qualified Version Definitions:

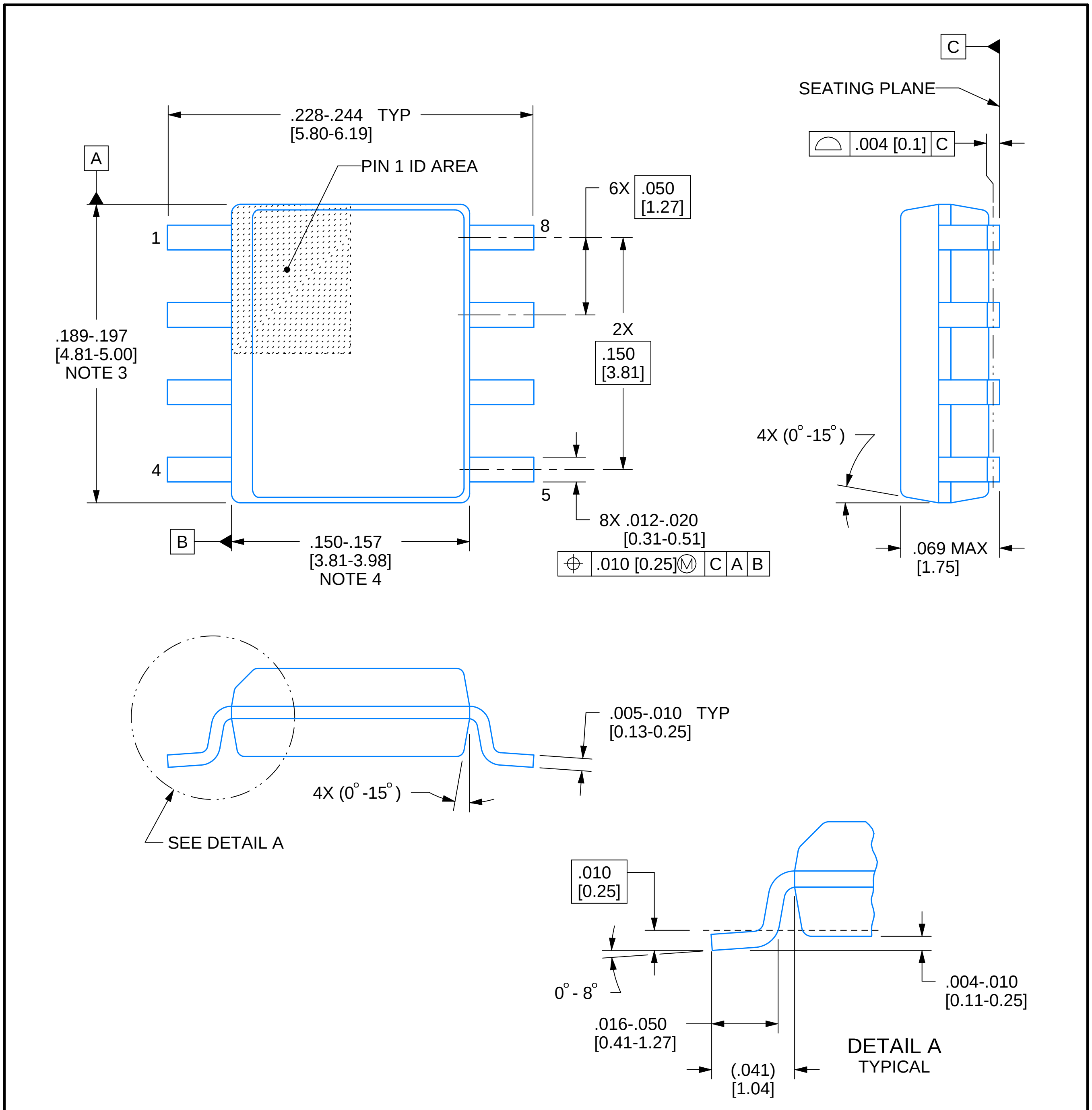
- Catalog - TI's standard catalog product



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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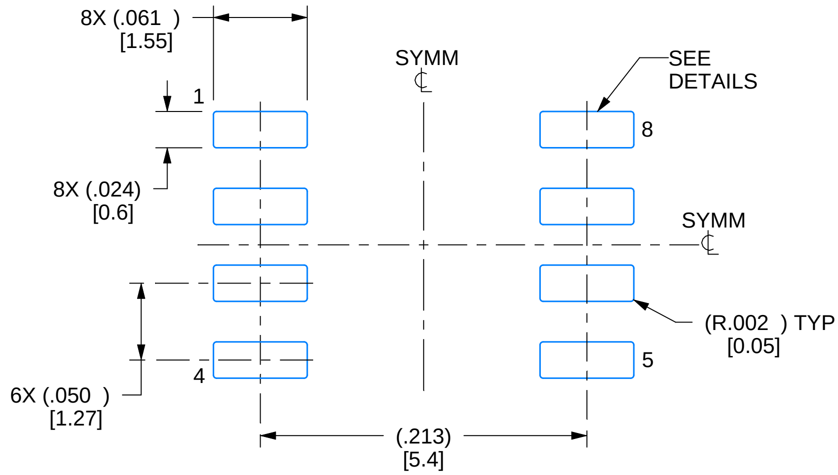
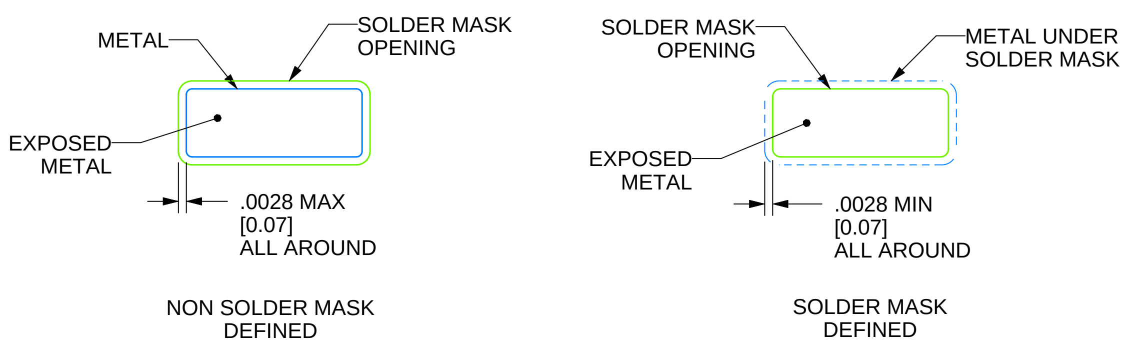
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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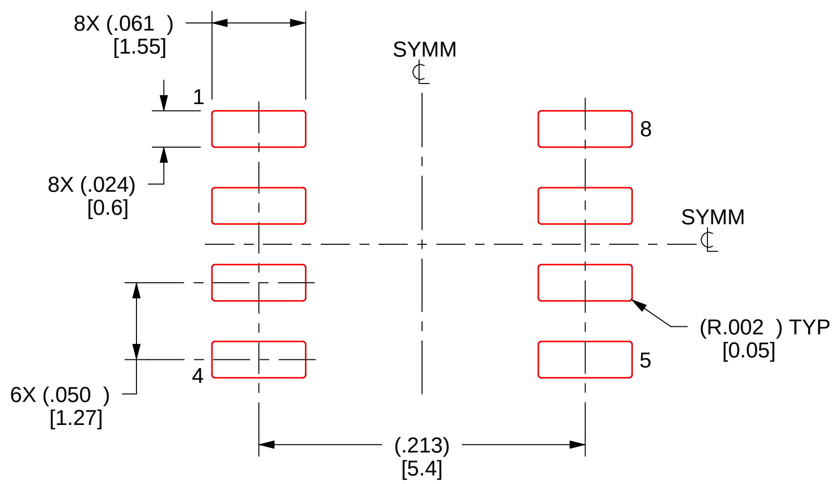
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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