

## 高精度、低噪声运算放大器

查询样品: [OPA2227-EP](#)

### 特性

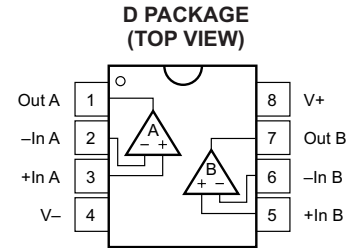
- 低噪声:  $3 \text{ nV}/\sqrt{\text{Hz}}$
- 宽带宽: **8 MHz**, **2.3 V/ $\mu\text{s}$**
- 稳定时间: **5  $\mu\text{s}$**
- 高共模抑制比 (CMRR): **138dB** (典型值)
- 高开环增益: **160dB** (典型值)
- 低输入偏置电流: **25°C** 时最大值 **10nA**
- 低偏移电压: **25°C** 时最大值 **100 $\mu\text{V}$**
- 宽电源电压:  **$\pm 2.5\text{V}$  至  $\pm 18\text{V}$**

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 可在军用温度范围内 ( **$-55^\circ\text{C}/125^\circ\text{C}$** )工作 <sup>(1)</sup>
- 拓展的产品使用寿命
- 拓展的产品变更通知
- 产品可追溯性

### 应用范围

- 数据采集
- 电信设备
- 地球物理学分析
- 振动分析
- 光谱分析
- 专业音频设备
- 有源滤波器
- 电源控制



(1) 可获得的额外温度范围 - 请与厂家联系

### 说明

OPA2227 运算放大器兼有低噪声和高精度宽带宽, 这使得此器件成为对交流 (ac) 和精密直流 (dc) 性能有严格要求的应用的理想选择。

OPA2227 单位增益稳定且特有高转换率 (2.3V/ $\mu\text{s}$ ) 和宽带宽 (8MHz)。

OPA2227 运算放大器是专业音频设备的理想选择。此外, 低静态电流和低成本使得它们非常适合于对高精度有严格要求的便携式应用。

OPA2227 运算放大器是行业标准 OP-27 的引脚到引脚的替代产品, 但此器件进行了全面重大改进。为了空间节省和降低每通道成本, 还提供双通道和四通道版本。

OPA2227 采用一个小外形尺寸集成电路 (SOIC)-8 封装。运行额定温度介于  $-55^\circ\text{C}$  至  $125^\circ\text{C}$  之间。



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: [SBOS594](#)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE	TOP-SIDE MARKING	ORDERABLE PART NUMBER	VID NUMBER	TRANSPORT MEDIA
–55°C to 125°C	SOIC-8 – D	2227EP	OPA2227MDREP	V62/12610-01XE	Tape and Reel, large
			OPA2227MDEP	V62/12610-01XE-T	Tube

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply voltage	±18	V
Signal input terminals	Voltage	(V–) – 0.7 to (V+) + 0.7
	Current	20
Output short-circuit (to ground) <sup>(2)</sup>	Continuous	
Operating temperature	–55 to 125	°C
Storage temperature	–65 to 150	°C
Junction temperature	150	°C
Lead temperature (soldering, 10 s)	300	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) One channel per package.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		OPA2227	UNITS
		D	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	91.9	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	39.9	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	40.6	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	3.9	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	39.6	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/SprA953).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

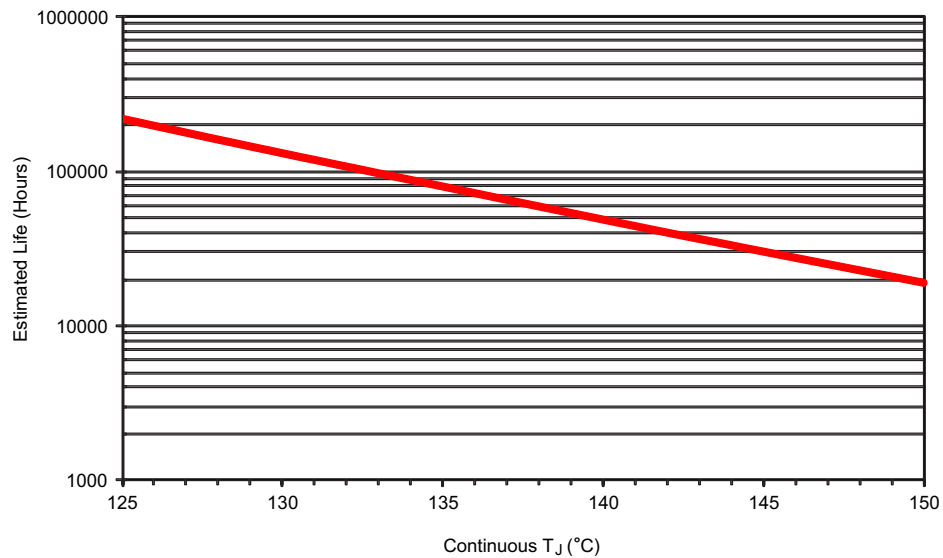
At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{ V}$  to  $\pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage ( $V_{OS}$ )	$V_S = \pm 2.5\text{ V}$ to $\pm 18\text{ V}$		$\pm 5$	$\pm 100$	$\mu\text{V}$
vs Temperature, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			$\pm 10$	$\pm 250$	$\mu\text{V}$
vs Temperature ( $dV_{OS}/dT$ ), $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			$\pm 0.1$		$\mu\text{V}/^\circ\text{C}$
vs Power supply (PSRR) $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			$\pm 0.5$	$\pm 2.1$	$\mu\text{V/V}$
vs Time			0.2		$\mu\text{V/mo}$
Channel separation (dual)	dc $f = 1\text{ kHz}$ , $R_L = 5\text{ k}\Omega$		0.2 110		$\mu\text{V/V}$ dB
INPUT BIAS CURRENT					
Input bias current ( $I_B$ )			$\pm 2.5$	$\pm 10$	nA
$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$		See Typical Characteristics			
Input offset current ( $I_{OS}$ )			$\pm 2.5$	$\pm 10$	nA
$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$		See Typical Characteristics			
NOISE					
Input voltage noise, $f = 0.1\text{ Hz}$ to $10\text{ Hz}$			90		nVp-p
			15		nVrms
Input voltage noise density ( $e_n$ ) $f = 10\text{ Hz}$			3.5		$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{ Hz}$			3		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{ kHz}$			3		$\text{nV}/\sqrt{\text{Hz}}$
Current noise density ( $i_n$ ), $f = 1\text{ kHz}$			0.4		$\text{pA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE					
Common-mode voltage range ( $V_{CM}$ ) $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	$V_{CM} = (V-) + 2\text{ V}$ to $(V+) - 2\text{ V}$	(V-) + 2		(V+) - 2	V
Common-mode rejection (CMRR)		120	138		dB
$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$		108	138		dB
INPUT IMPEDANCE					
Differential	Open-loop voltage gain ( $A_{OL}$ )		$10^7 \parallel 12$		$\Omega \parallel \text{pF}$
Common-mode	$V_{CM} = (V-) + 2\text{ V}$ to $(V+) - 2\text{ V}$		$10^9 \parallel 3$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN					
Open-loop voltage gain ( $A_{OL}$ ) $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	$V_O = (V-) + 2\text{ V}$ to $(V+) - 2\text{ V}$ , $R_L = 10\text{ k}\Omega$	132	160		dB
		112	160		
	$V_O = (V-) + 3.5\text{ V}$ to $(V+) - 3.5\text{ V}$ , $R_L = 600\text{ }\Omega$	132	160		
$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$		112	160		
FREQUENCY RESPONSE					
Gain bandwidth product (GBW)	$G = 1$ , 10-V Step, $C_L = 100\text{ pF}$ $G = 1$ , 10-V Step, $C_L = 100\text{ pF}$ $V_{IN} \times G = V_S$		8		MHz
Slew rate (SR)			2.3		V/ $\mu\text{s}$
Settling time: 0.1%			5		$\mu\text{s}$
0.01%			5.6		$\mu\text{s}$
Overload recovery time			1.3		$\mu\text{s}$
Total harmonic distortion + noise (THD+N)		$f = 1\text{ kHz}$ , $G = 1$ , $V_O = 3.5\text{ Vrms}$		0.00005	
OUTPUT					
Voltage output $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	$R_L = 10\text{ k}\Omega$ $R_L = 600\text{ }\Omega$	(V-) + 2 (V-) + 3.5		(V+) - 2 (V+) - 3.5	V
Short-circuit current ( $I_{SC}$ )			$\pm 45$		mA
Capacitive load drive ( $C_{LOAD}$ )		See Typical Characteristics			
POWER SUPPLY					
Specified voltage range ( $V_S$ )	$I_O = 0\text{ A}$	$\pm 5$		$\pm 15$	V
Operating voltage range		$\pm 2.5$		$\pm 18$	V
Quiescent current (per amplifier) ( $I_Q$ )			$\pm 3.7$	$\pm 3.95$	

## ELECTRICAL CHARACTERISTICS (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{ V}$  to  $\pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	$I_O = 0\text{ A}$			$\pm 4.30$	mA
<b>TEMPERATURE RANGE</b>					
Specified temperature range		-55		125	$^\circ\text{C}$
Operating temperature range		-55		125	$^\circ\text{C}$
Storage temperature range		-65		150	$^\circ\text{C}$

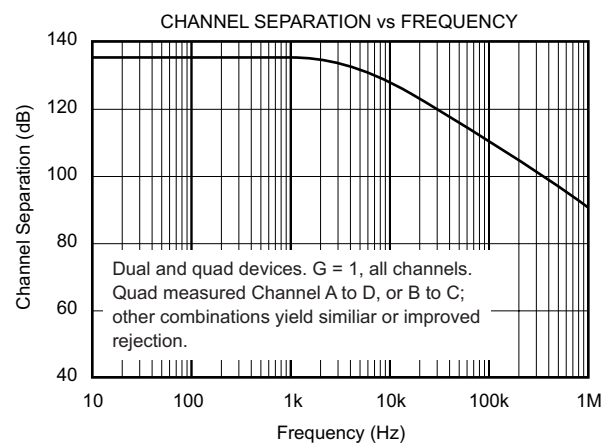
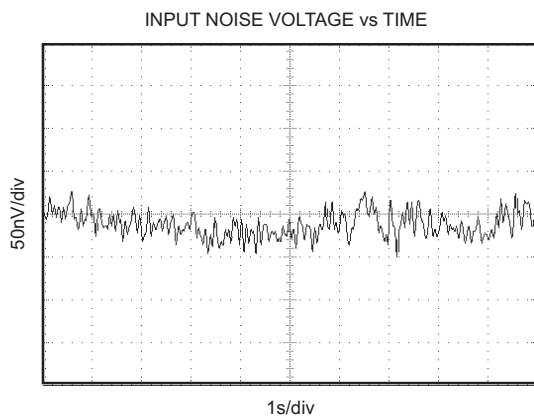
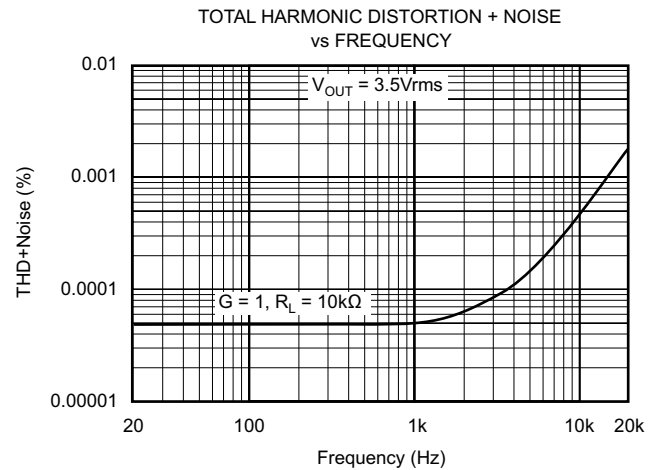
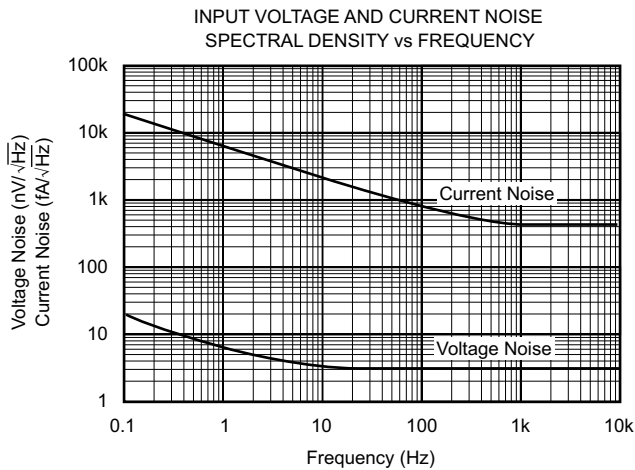
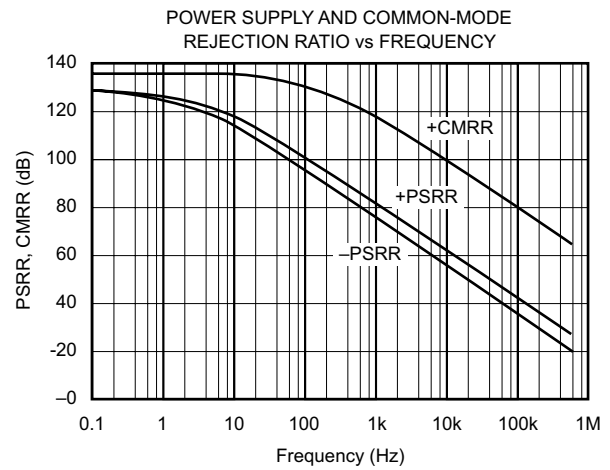
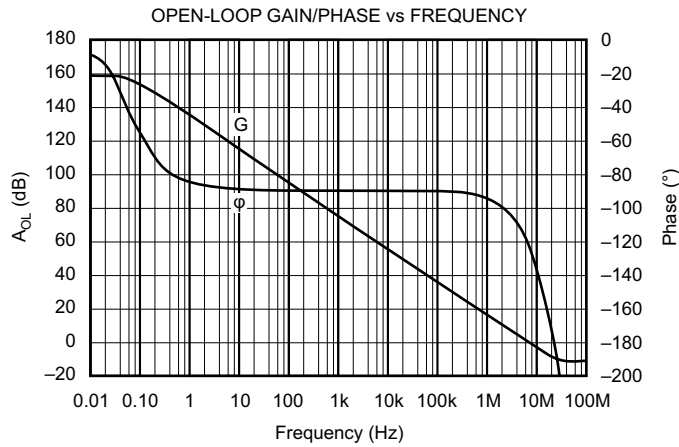


- See datasheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at  $105^\circ\text{C}$  junction temperature (does not include package interconnect life).

**Figure 1. OPA2227-EP Wirebond Life Derating Chart**

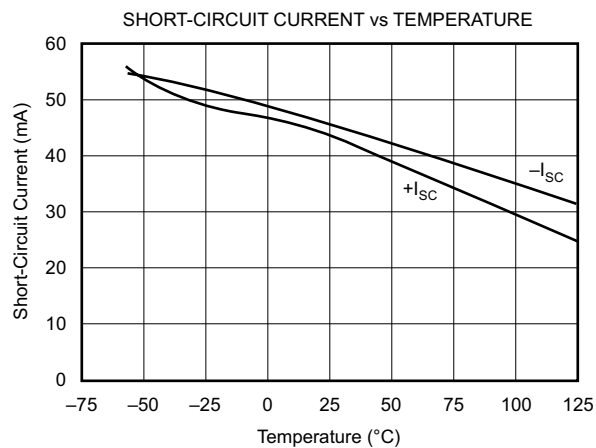
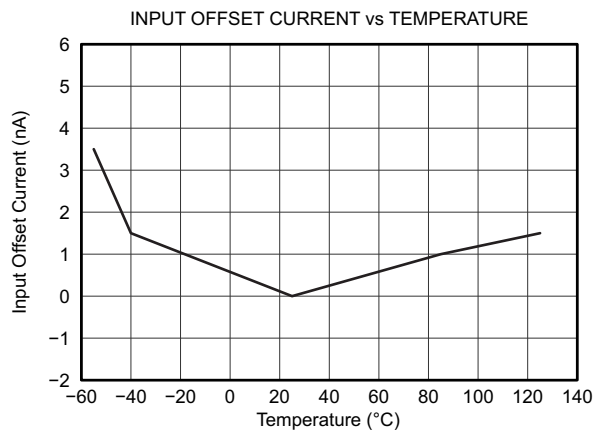
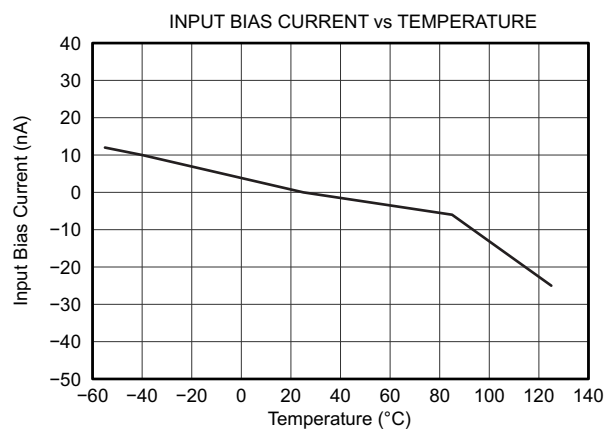
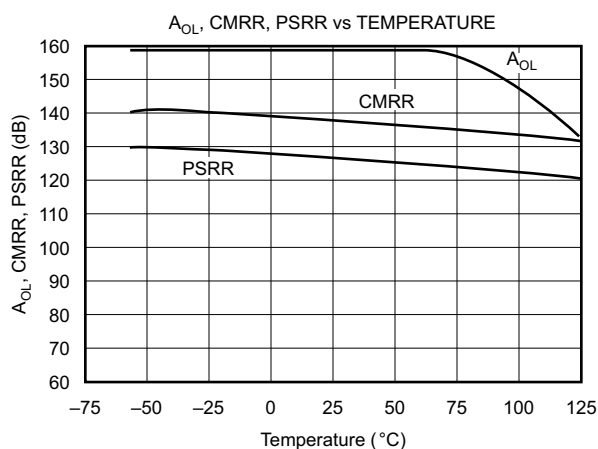
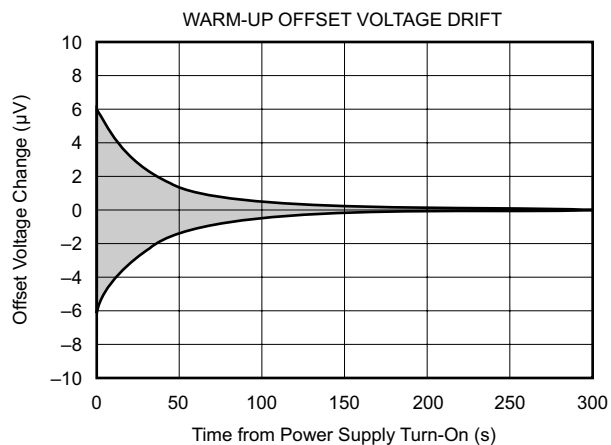
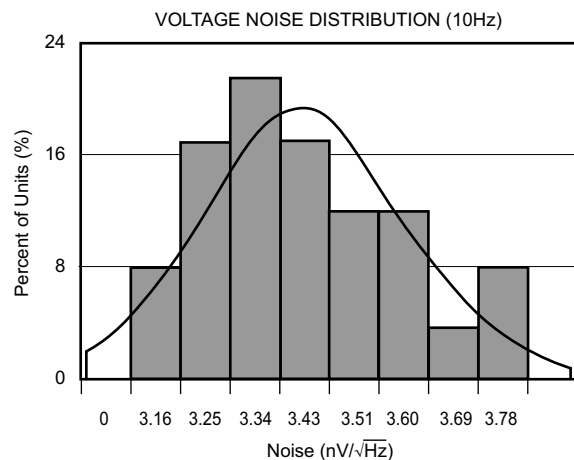
## TYPICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted).



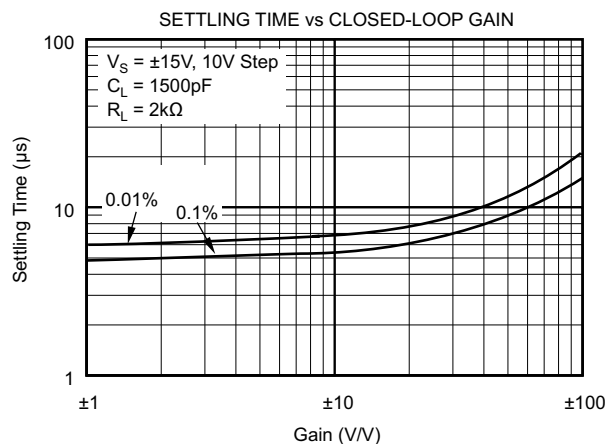
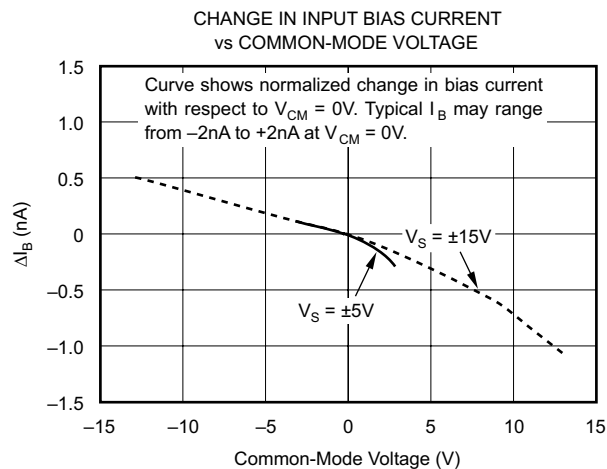
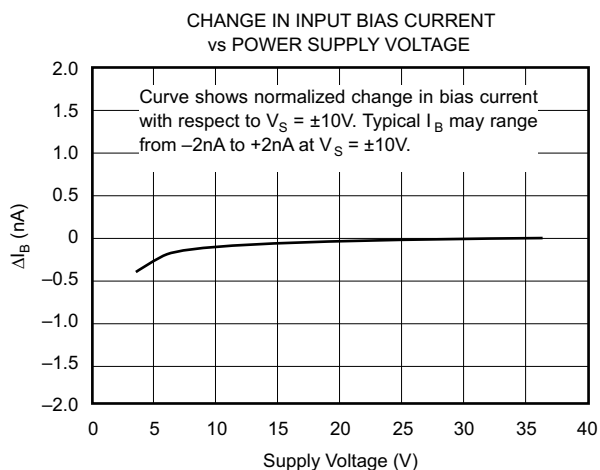
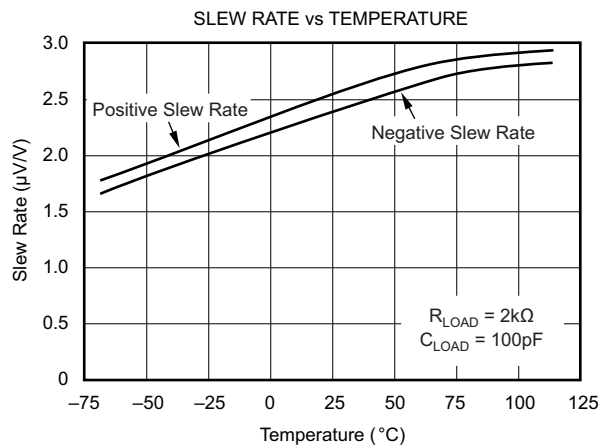
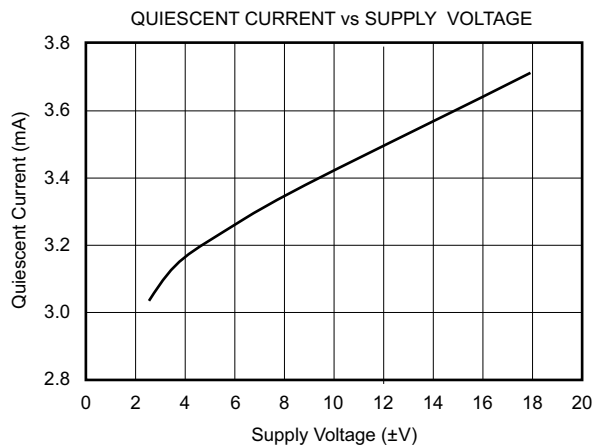
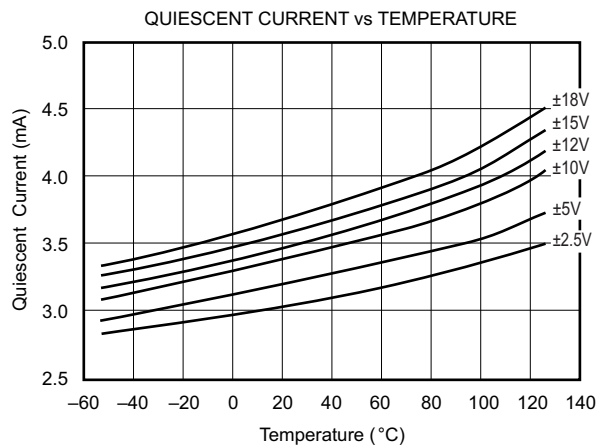
## TYPICAL CHARACTERISTICS (continued)

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted).



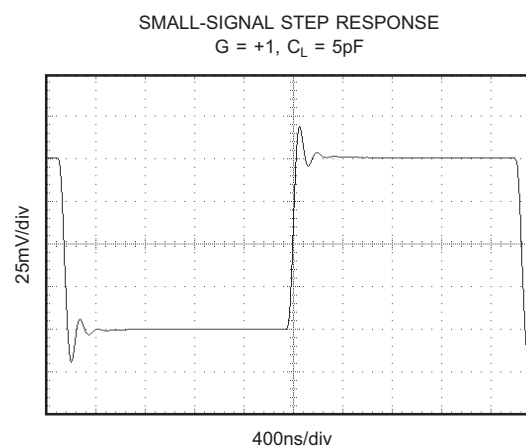
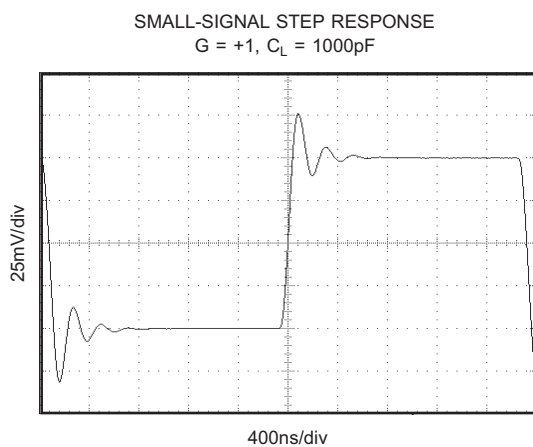
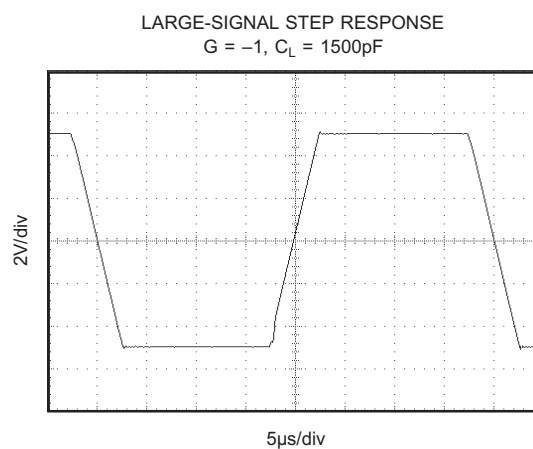
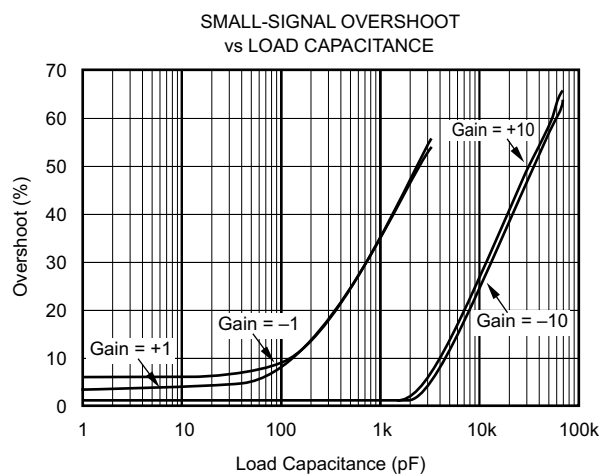
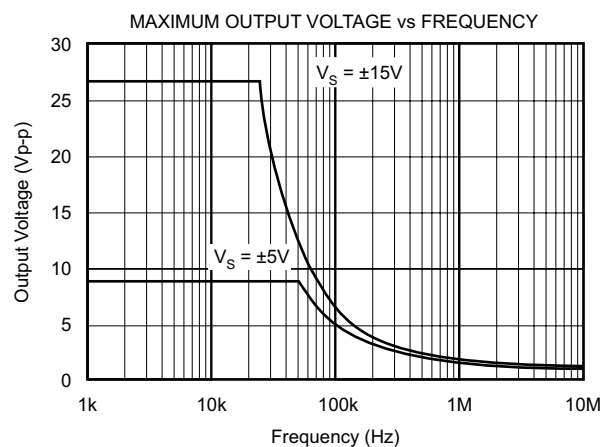
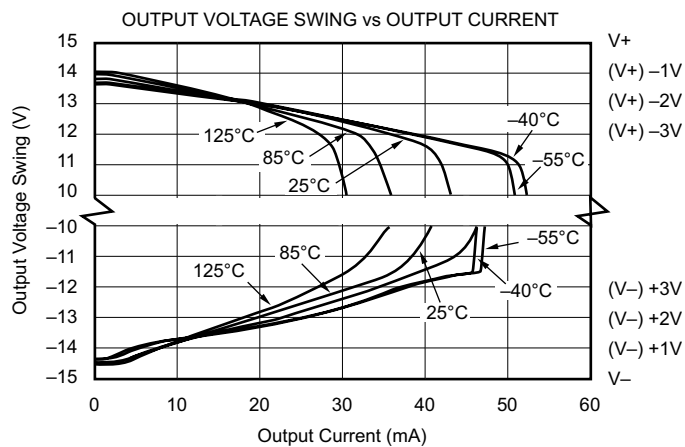
## TYPICAL CHARACTERISTICS (continued)

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted).



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted).





## APPLICATION INFORMATION

### Basic Connection

The OPA2227 is a precision operational amplifier with very low noise. It is unity-gain stable with a slew rate of 2.3 V/ $\mu$ s and 8-MHz bandwidth. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu$ F capacitors are adequate.

### Offset Voltage and Drift

The OPA2227 has very low offset voltage and drift. To achieve highest dc precision, circuit layout and mechanical conditions should be optimized. Connections of dissimilar metals can generate thermal potentials at the op amp inputs which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade its performance. The thermal potentials can be made to cancel by assuring that they are equal at both input terminals. In addition:

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as those created by cooling fans.

### Operating Voltage

OPA2227 operational amplifier operates from  $\pm 2.5$ -V to  $\pm 18$ -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2227 is specified for real-world applications; a single set of specifications applies over the  $\pm 5$ -V to  $\pm 15$ -V supply range. Specifications are assured for applications between  $\pm 5$ -V and  $\pm 15$ -V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA2227 can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply could be set to 25 V with the negative supply at  $-5$  V or vice-versa. In addition, key parameters are assured over the specified temperature range,  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Parameters which vary significantly with operating voltage or temperature are shown in the Typical Performance Curves.

### Offset Voltage Adjustment

The OPA2227 is laser-trimmed for very low offset and drift so most applications will not require external adjustment.

### Input Protection

Back-to-back diodes (see [Figure 2](#)) are used for input protection on the OPA2227. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes due to the amplifier's finite slew rate. Without external current-limiting resistors, the input devices can be destroyed. Sources of high input current can cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

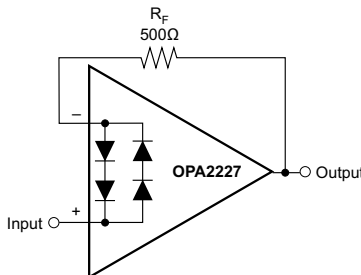


Figure 2. Pulsed Operation

When using the OPA2227 as a unity-gain buffer (follower), the input current should be limited to 20 mA. This can be accomplished by inserting a feedback resistor or a resistor in series with the source. Sufficient resistor size can be calculated:

$$R_X = V_S / 20 \text{ mA} - R_{\text{SOURCE}} \quad (1)$$

where  $R_x$  is either in series with the source or inserted in the feedback path. For example, for a 10-V pulse ( $V_S = 10\text{ V}$ ), total loop resistance must be  $500\ \Omega$ . If the source impedance is large enough to sufficiently limit the current on its own, no additional resistors are needed. The size of any external resistors must be carefully chosen since they will increase noise. See the Noise Performance section of this data sheet for further information on noise calculation. Figure 2 shows an example implementing a current limiting feedback resistor.

### Input Bias Current Cancellation

The input bias current of the OPA2227 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 3) may actually increase offset and noise and is therefore not recommended.

Conventional Op Amp Configuration

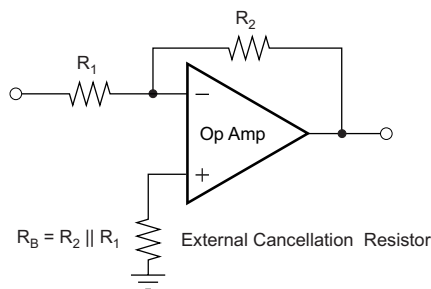


Figure 3. Input Bias Current Cancellation

### Noise Performance

Figure 4 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA2227 has very low voltage noise, making it ideal for low source impedances (less than  $20\text{ k}\Omega$ ). A similar precision operational amplifier, the OPA277, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance ( $10\text{ k}\Omega$  to  $100\text{ k}\Omega$ ). Above  $100\text{ k}\Omega$ , a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation is shown for the calculation of the total circuit noise. Note that  $e_n$  = voltage noise,  $i_n$  = current noise,  $R_S$  = source impedance,  $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}\text{ J/K}$  and  $T$  is temperature in K. For more details on calculating noise, see "Basic Noise Calculations."

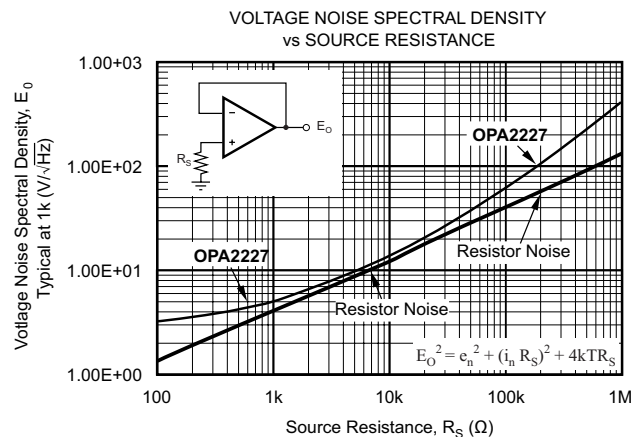


Figure 4. Noise Performance of the OPA2227 in Unity-Gain Buffer Configuration

## Basic Noise Calculations

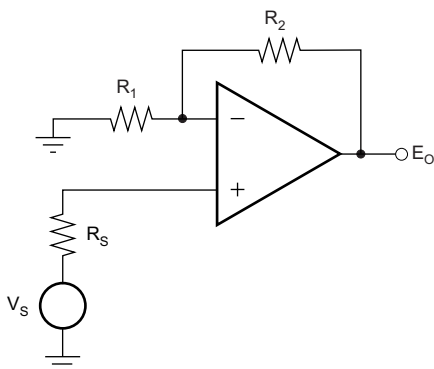
Design of low noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in [Figure 4](#). Since the source impedance is usually fixed, select the operational amplifier and the feedback resistors to minimize their contribution to the total noise.

[Figure 4](#) shows total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

[Figure 5](#) shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

## Noise in Noninverting Gain Configuration



Noise at the output:

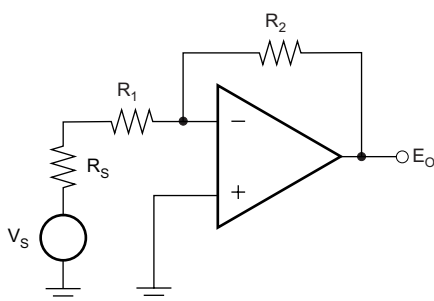
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_s^2 + (i_n R_s)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where  $e_s = \sqrt{4kTR_s} \cdot \left(1 + \frac{R_2}{R_1}\right)$  = thermal noise of  $R_s$

$$e_1 = \sqrt{4kTR_1} \cdot \left(\frac{R_2}{R_1}\right) = \text{thermal noise of } R_1$$

$$e_2 = \sqrt{4kTR_2} = \text{thermal noise of } R_2$$

## Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_s}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_s^2$$

Where  $e_s = \sqrt{4kTR_s} \cdot \left(\frac{R_2}{R_1 + R_s}\right)$  = thermal noise of  $R_s$

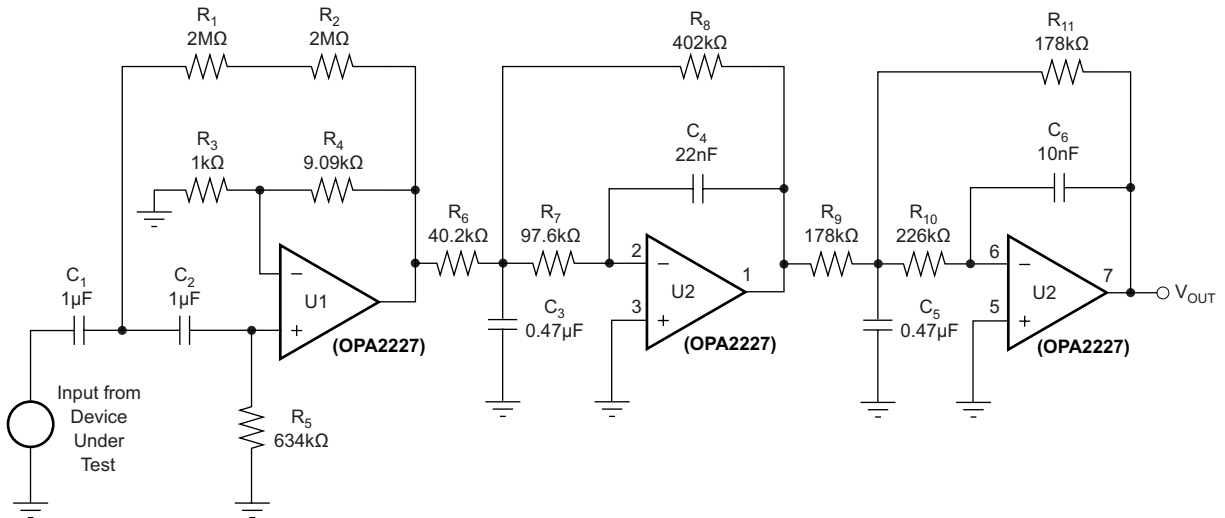
$$e_1 = \sqrt{4kTR_1} \cdot \left(\frac{R_2}{R_1 + R_s}\right) = \text{thermal noise of } R_1$$

$$e_2 = \sqrt{4kTR_2} = \text{thermal noise of } R_2$$

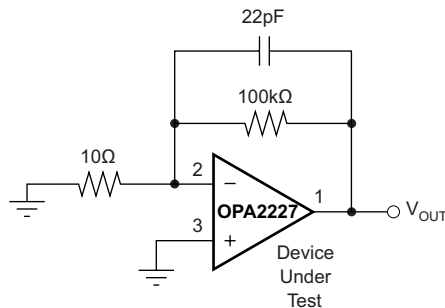
For op amps at 1kHz,  $e_n = 3\text{nV}/\sqrt{\text{Hz}}$  and  $i_n = 0.4\text{pA}/\sqrt{\text{Hz}}$ .

Figure 5. Noise Calculation in Gain Configurations

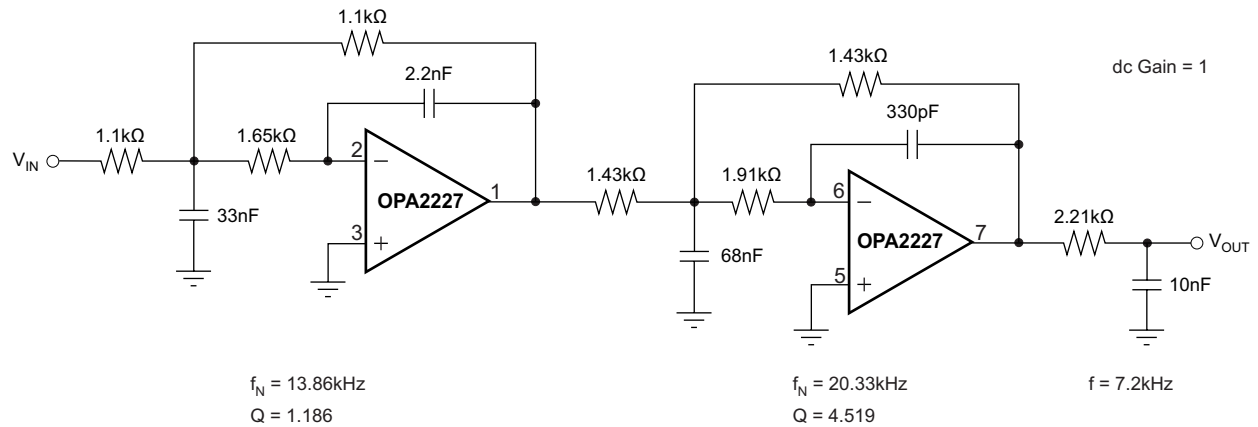
Figure 6 shows the 0.1-Hz to 10-Hz bandpass filter used to test the noise of the OPA2227. The filter circuit was designed using Texas Instruments' FilterPro software (available at [www.ti.com](http://www.ti.com)). Figure 7 shows the configuration of the OPA2227 for noise testing.



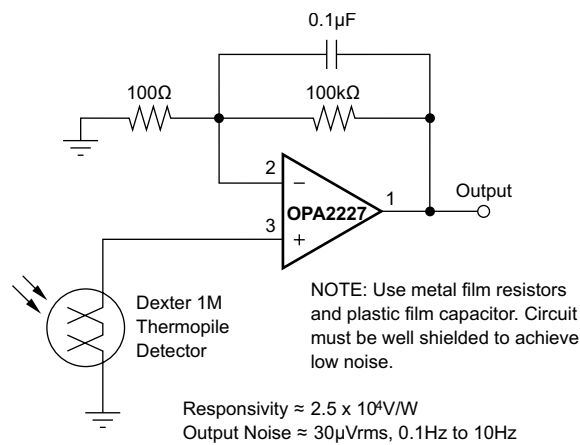
**Figure 6. 0.1-Hz to 10-Hz Bandpass Filter Used to Test Wideband Noise of the OPA2227**



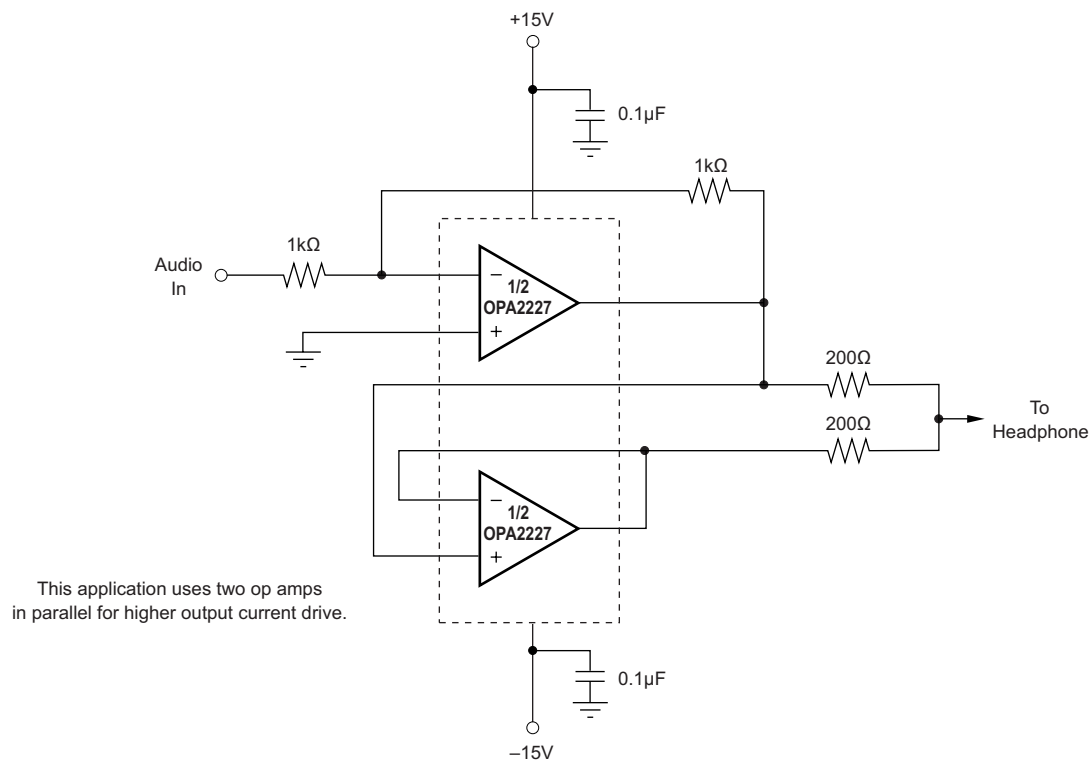
**Figure 7. Noise Test Circuit**



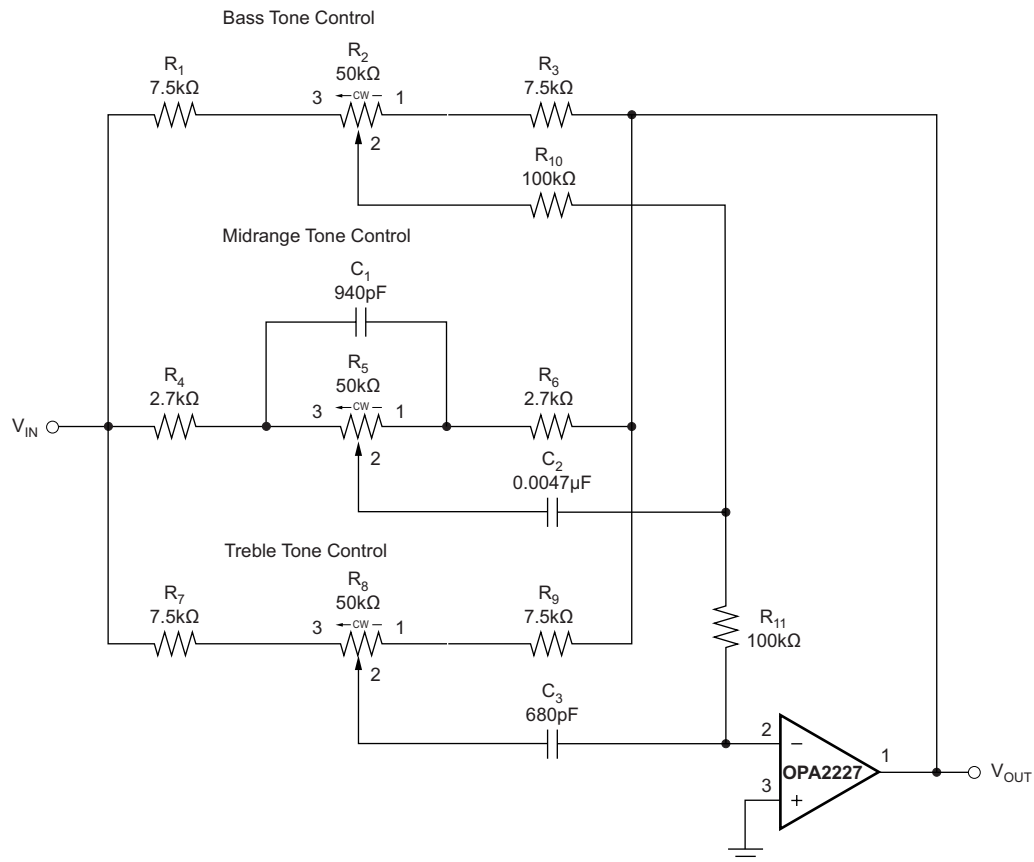
**Figure 8. Three-Pole, 20-kHz Low Pass, 0.5-dB Chebyshev Filter**



**Figure 9. Long-Wavelength Infrared Detector Amplifier**



**Figure 10. Headphone Amplifier**



**Figure 11. Three-Band ActiveTone Control (Bass, Midrange and Treble)**



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2227MDREP</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	2227EP
OPA2227MDREP.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	2227EP

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF OPA2227-EP :

- Catalog : [OPA2227](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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