OPAx130 低功耗、精密 FET 输入运算放大器

1 特性

- 低静态电流：530 μA/放大器
- 低失调电压：最大 1mV
- 高开环增益： 123dB (R_L = 10kΩ)
- 高 CMRR：90dB（最小值）
- FET 输入：I_B = 20pA（最大值）
- 出色的带宽：1MHz
- 宽电源电压范围：±2.25V 至 ±18V
- 单通道、双通道和四通道版本

2 应用

- 数据采集 (DAQ)
- 流量变送器
- 实验室和现场仪表
- 心电图 (ECG)

3 说明

OPA130、OPA2130 和 OPA4130 (OPAx130) 系列 FET 输入运算放大器将精密直流性能和低静态电流集于一身。单通道、双通道和四通道版本具有完全相同的规格，可大幅度提高设计灵活性。OPAx130 适用于通用、便携式和电池供电型应用，尤其是具有高源阻抗的应用。

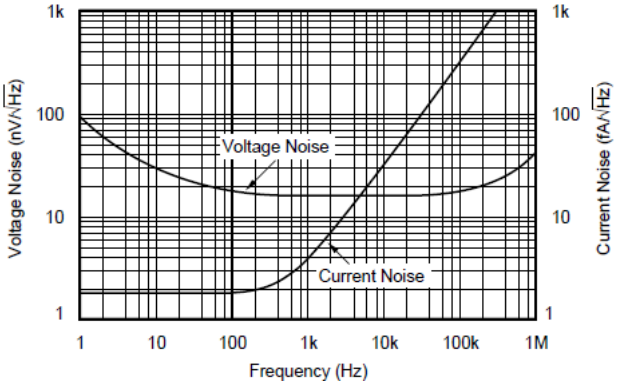
OPAx130 运算放大器易于使用，而且不存在常见 FET 输入运算放大器中会出现的相位反转和过载问题。输入共源共栅电路提供出色的共模抑制，并在放大器的宽输入电压范围内保持低输入偏置电流。OPAx130 系列运算放大器是单位增益稳定型放大器，且可在宽负载条件范围（包括高负载电容）内提供出色的动态行为。双通道和四通道设计有完全独立的电路，即使在过驱或过载时，也可尽可能减少串扰并消除相互干扰。

单通道和双通道版本采用 8 引脚 SOIC 表面贴装式封装。四通道版本采用 14 引脚 SOIC 表面贴装式封装。所有器件的额定工作温度范围为 –40°C 至 +85°C。

器件信息

器件型号	通道数	封装(1)
OPA130	单通道	D（SOIC，8）
OPA2130	双通道	D（SOIC，8）
OPA4130	四通道	D（SOIC，14）

(1) 有关更多信息，请参阅节 9。



输入电压和电流噪声频谱密度与频率间的关系

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4 Pin Configuration and Functions

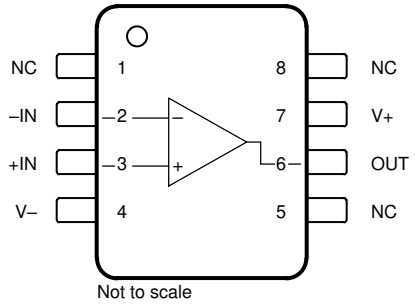


图 4-1. OPA130 D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions: OPA130

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input, channel A
– IN	2	Input	Inverting input, channel A
NC	1, 5	—	Do not connect these pins(1)
NC	8	—	No internal connection. Float this pin.
OUT	6	Output	Output
V+	7	Power	Positive (highest) power supply
V –	4	Power	Negative (lowest) power supply

(1) Existing layouts for the OPA130 D package before revision B of this data sheet do not need to be redesigned.

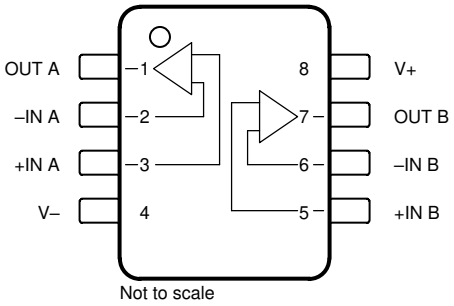


图 4-2. OPA2130 D Package, 8-Pin SOIC (Top View)

表 4-2. Pin Functions: OPA2130

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V –	4	Power	Negative (lowest) power supply

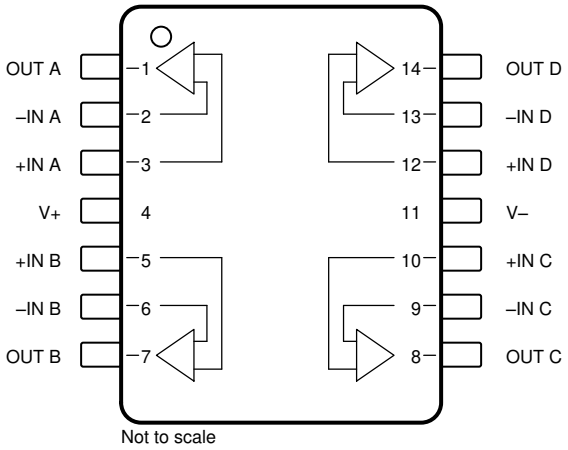


图 4-3. OPA4130 D Package, 14-Pin SOIC (Top View)

表 4-3. Pin Functions: OPA4130

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
– IN C	9	Input	Inverting input, channel C
– IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V –	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±18	V
		Single supply		36	
	Input voltage(2)		(V–) – 0.5	(V+) + 0.5	V
	Input current(2)			±10	mA
I_{SC}	Output short-circuit(3)		Continuous		
T_A	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–40	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.25	±15	±18	V
		Single supply	4.5	30	36	
T_A	Ambient temperature		–40	25	85	°C

5.3 Thermal Information - OPA130

THERMAL METRIC(1)		OPA130 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information - OPA2130

THERMAL METRIC(1)		OPA2130 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - OPA4130

THERMAL METRIC(1)		OPA4130 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2	±10	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25V to ±18V			±2	±20	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±20	pA
		T_A = –40°C to +85°C			See *Typical Characteristics*		
I_{OS}	Input offset current(1)				±2	±20	pA
NOISE							
e_n	Input voltage noise density	f = 10Hz			30		nV/√Hz
		f = 100Hz			18		
		f = 1kHz			16		
		f = 10kHz			16		
I_n	Input current noise density	f = 1kHz			4		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	–13V ≤ V_{CM} ≤ 11.5V		90	105		dB
INPUT IMPEDANCE							
	Differential				10^{13} || 5		Ω || pF
	Common-mode	–13V ≤ V_{CM} ≤ 11.5V			10^{13} || 4.3		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	–13.8V ≤ V_O ≤ 13V, R_L = 10kΩ		114	123		dB
		–13V ≤ V_O ≤ 12V, R_L = 2kΩ		104	110		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1		MHz
SR	Slew rate				2		V/µs
	Settling time	10V step, G = 1	0.1%		5.5		µs
			0.01%		7		
THD+N	Total harmonic distortion plus noise	f = 1kHz, G = 1, V_O = 3.5V_{rms}			0.0003%		
	Overload recovery time	G = 1, V_{IN} = ±15V			2		µs
OUTPUT							
V_O	Voltage output	R_L = 10kΩ	Positive	(V+) – 2	(V+) – 1.5		V
			Negative		(V–) + 1	(V–) + 1.2	
		R_L = 2kΩ	Positive	(V+) – 3	(V+) – 2.5		
			Negative		(V–) + 1.5	(V–) + 2	
I_{SC}	Short-circuit current				±18		mA
C_{LOAD}	Capacitive load drive	Stable operation			See *Typical Characteristics*		
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0mA			±530	±650	µA

(1) High-speed test at T_J = 25°C.

5.7 Typical Characteristics

at T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = midsupply (unless otherwise noted)

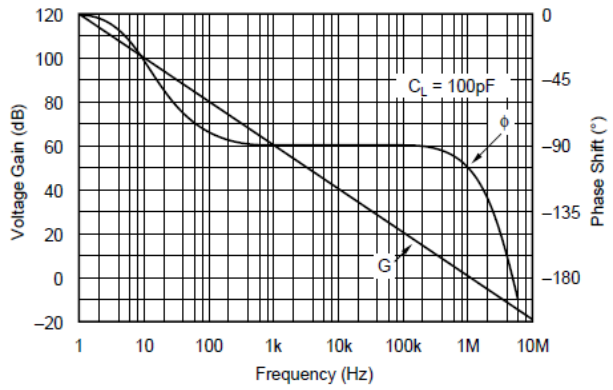


图 5-1. Open-Loop Gain and Phase vs Frequency

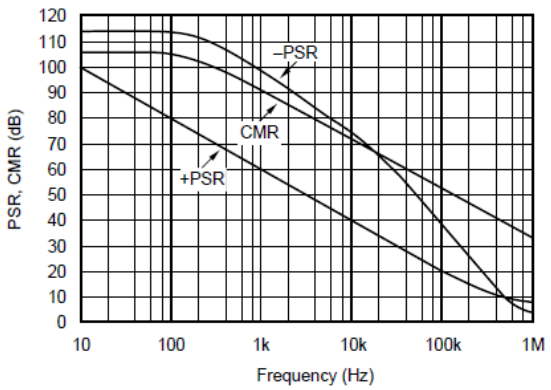


图 5-2. Power Supply and Common-Mode Rejection vs Frequency

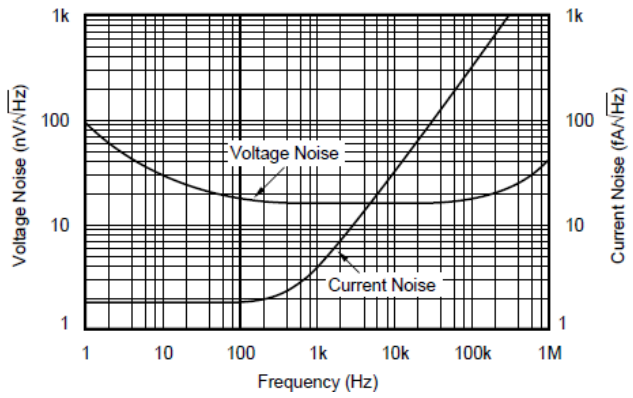


图 5-3. Input Voltage and Current Noise Spectral Density vs Frequency

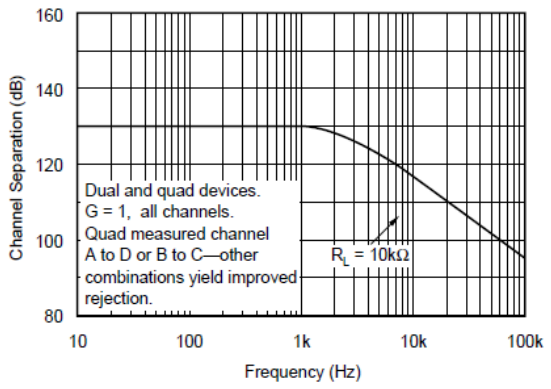


图 5-4. Channel Separation vs Frequency

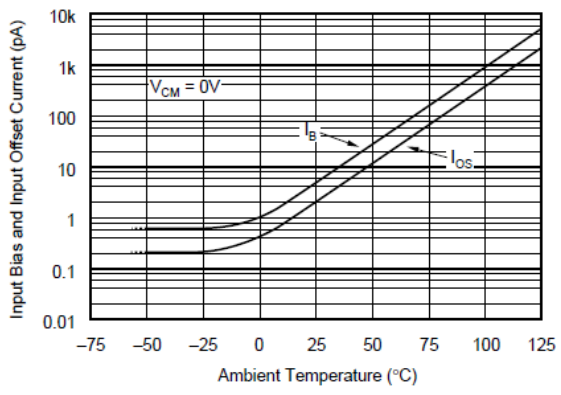


图 5-5. Input Bias and Input Offset Current vs Temperature

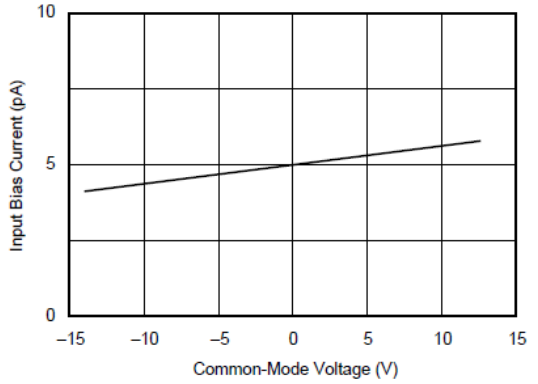


图 5-6. Input Bias Current vs Input Common-Mode Voltage

5.7 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = midsupply (unless otherwise noted)

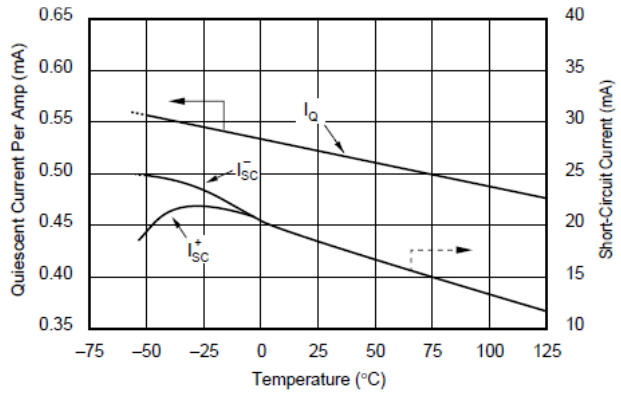


图 5-7. Quiescent Current and Short-Circuit Current vs Temperature

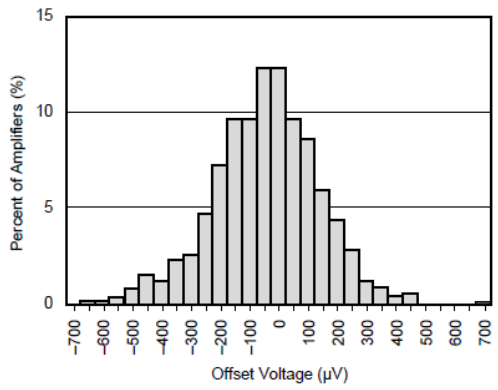


图 5-8. Offset Voltage Production Distribution

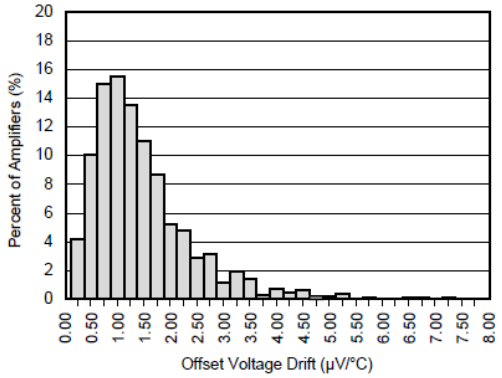


图 5-9. Offset Voltage Drift Production Distribution

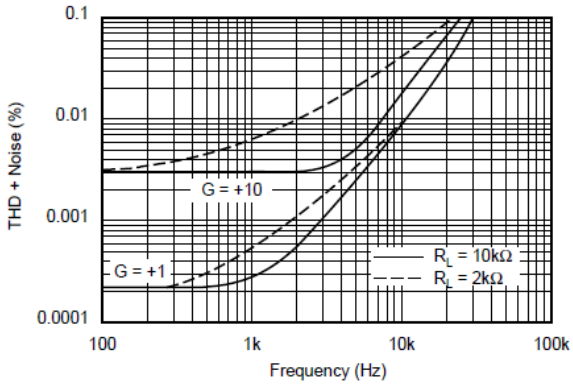


图 5-10. Total Harmonic Distortion + Noise vs Frequency

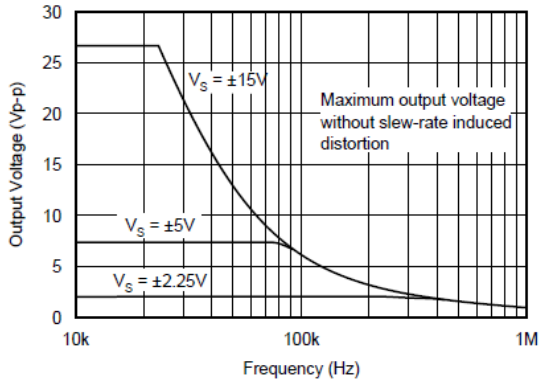
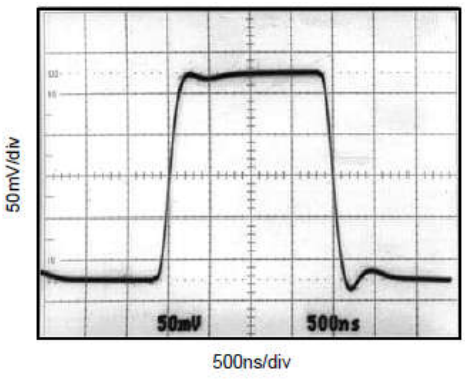


图 5-11. Maximum Output Voltage vs Frequency

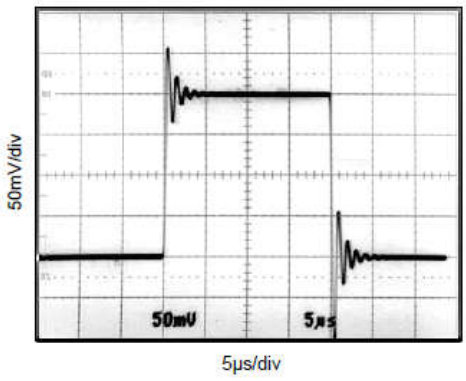


G = 1, C_L = 100pF

图 5-12. Small-Signal Step Response

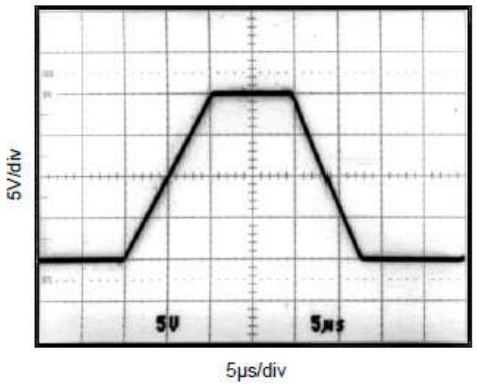
5.7 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = midsupply (unless otherwise noted)



G = 1, C_L = 1000pF

图 5-13. Small-Signal Step Response



G = 1, C_L = 100pF

图 5-14. Large-Signal Step Response

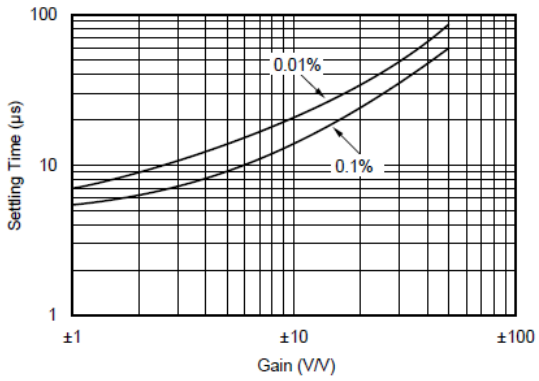


图 5-15. Settling Time vs Gain

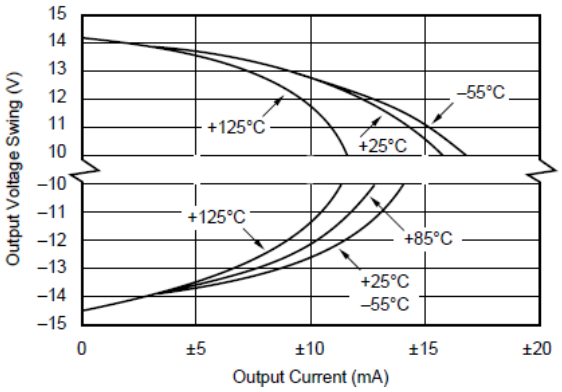


图 5-16. Output Voltage Swing vs Output Current

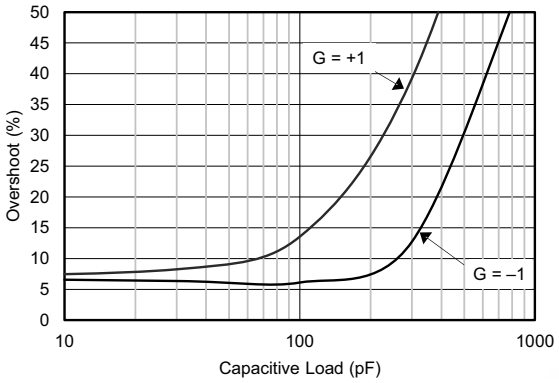


图 5-17. Small-Signal Overshoot vs Load Capacitance

6 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The OPAx130 series of op amps are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass power supply pins with 10nF ceramic capacitors or larger.

The OPAx130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. The OPAx130 series of op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, and normal behavior can be expected when one amplifier in a package is overdriven or short-circuited.

6.1.1 Operating Voltage

The OPAx130 op amps operate with power supplies from ±2.25V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. See 节 5.7 for parameters that vary significantly with operating voltage.

6.1.2 Offset Voltage Trim

The offset voltage of the OPAx130 amplifiers is laser trimmed and usually requires no user adjustment. The OPAx130 provide less than ±1mV of input offset voltage and less than 10µV/°C of input offset voltage drift over the operating temperature range.

6.1.3 Input Bias Current

图 5-5 shows that the input bias current of the OPAx130 is approximately 5pA at room temperature and increases with temperature.

Input stage cascode circuitry allows the input bias current to remain virtually unchanged throughout the full input common-mode range of the OPAx130. See also 图 5-6.

6.2 Typical Application

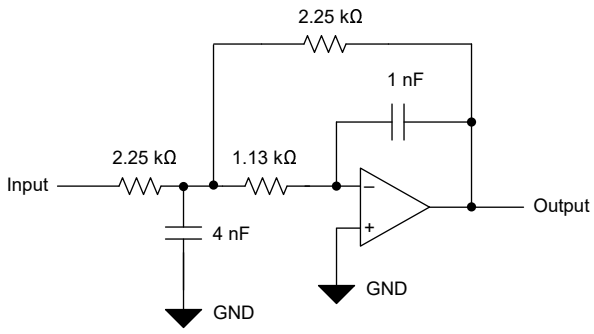


图 6-1. Second-Order Low-Pass Filter

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (March 2006) to Revision B (May 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 删除了数据表中的 DIP 封装	1
• 更新了开环增益，以匹配*特性* 中的*电气特性*	1
• 添加了*应用*	1
• Updated pin diagrams, added pin function tables, and moved all to new *Pin Configuration and Functions*	3
• Updated input voltage in *Absolute Maximum Ratings*	5
• Added input current and related footnote to *Absolute Maximum Ratings*	5
• Added *Recommended Operating Conditions* and *Thermal Information*	5
• Changed format of *Electrical Characteristics* to latest standard	7
• Updated nominal conditions in the header of *Electrical Characteristics*	7
• Deleted channel separation specification	7
• Updated common-mode voltage	7
• Updated common-mode rejection ratio and common-mode input impedance test conditions	7
• Changed differential input impedance from $10^{13}\Omega$ || 1pF to $10^{13}\Omega$ || 5pF	7
• Changed common-mode input impedance from $10^{13}\Omega$ || 3pF to $10^{13}\Omega$ || 4.3pF	7
• Updated open loop voltage gain MIN and TYP values for R_L = 10kΩ and R_L = 2kΩ	7
• Updated settling time test condition	7
• Moved voltage output negative MIN values to MAX values	7

- Changed capacitive load drive specification from 10nF to See *Typical Characteristics* 7
- Deleted note 1 from *Electrical Characteristics* 7
- Deleted Figure 5-7, A_{OL}, *CMR, PSR vs Temperature* 8
- Updated Figure 5-17, *Small-Signal Overshoot vs Load Capacitance* 8
- Updated text in *Offset Voltage Trim* 11
- Changed Figure 1, *OPA130 Offset Voltage Trim Circuit*, to Figure 6-1, *Second-Order Low-Pass Filter* 11

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA130UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA
OPA130UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA
OPA130UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA
OPA130UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA
OPA130UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA
OPA2130UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(2130UA, OPA)
OPA2130UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(2130UA, OPA)
OPA2130UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(2130UA, OPA)
OPA2130UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	(2130UA, OPA)
OPA4130UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4130UA
OPA4130UA.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4130UA
OPA4130UA.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4130UA
OPA4130UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4130UA
OPA4130UA/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	OPA4130UA
OPA4130UA/2K5.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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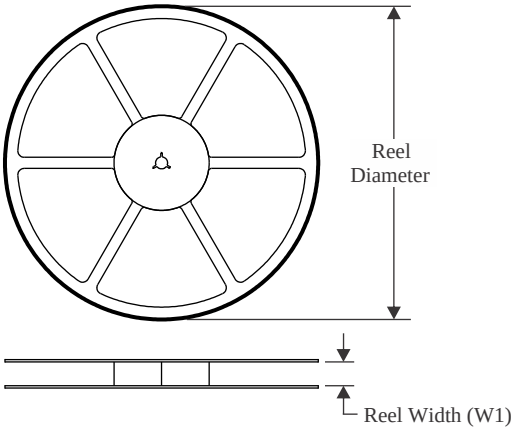
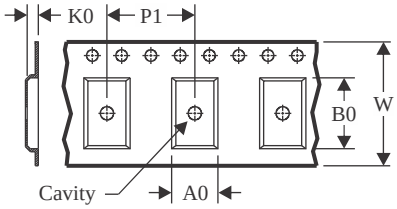
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

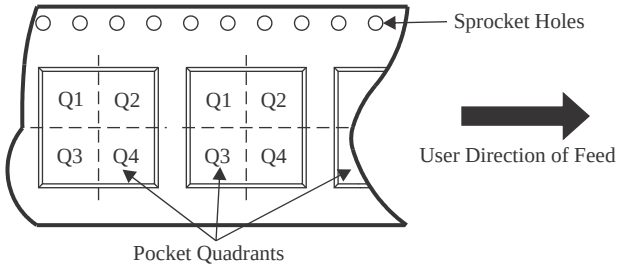


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

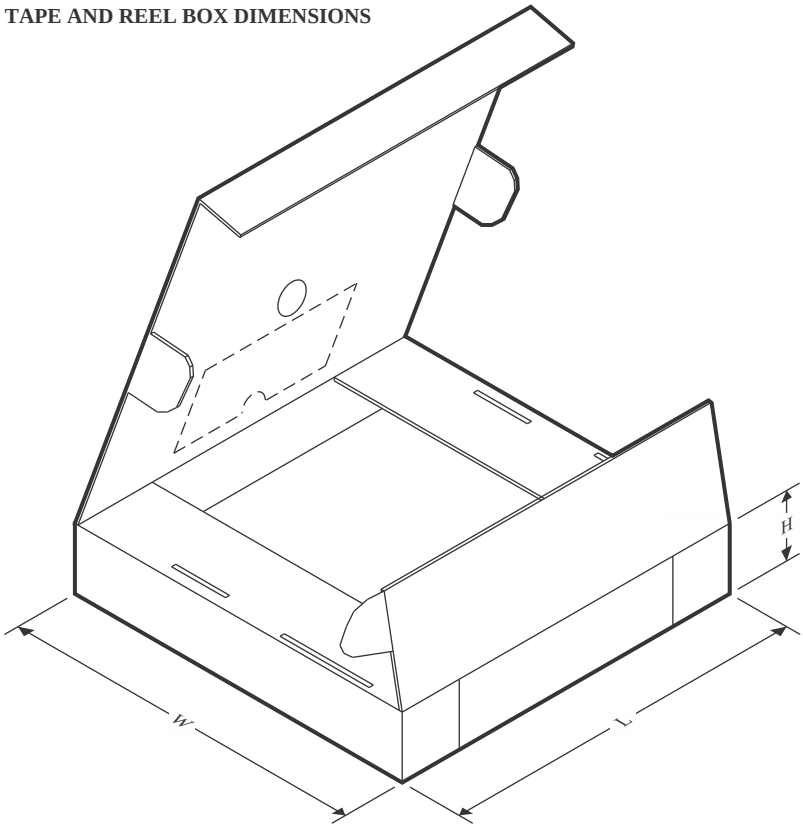
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4130UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

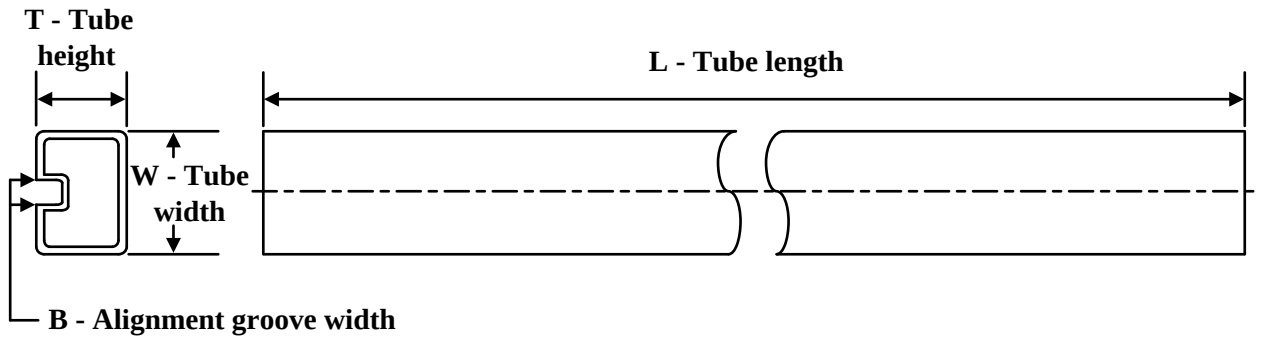
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

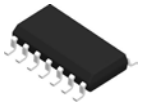
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA130UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2130UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4130UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA130UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA130UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2130UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2130UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4130UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4130UA.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA4130UA.B	D	SOIC	14	50	506.6	8	3940	4.32

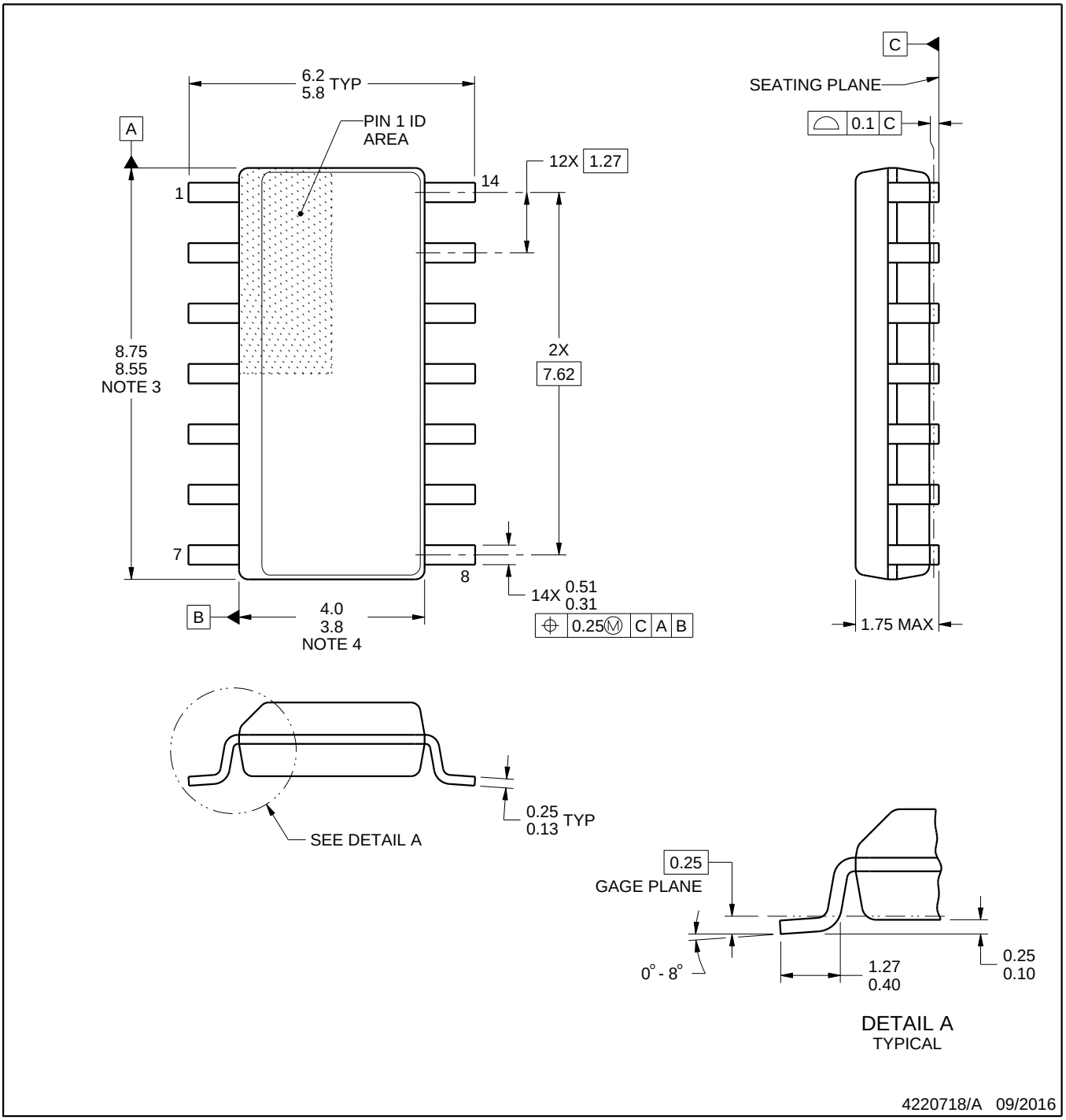


PACKAGE OUTLINE

D0014A

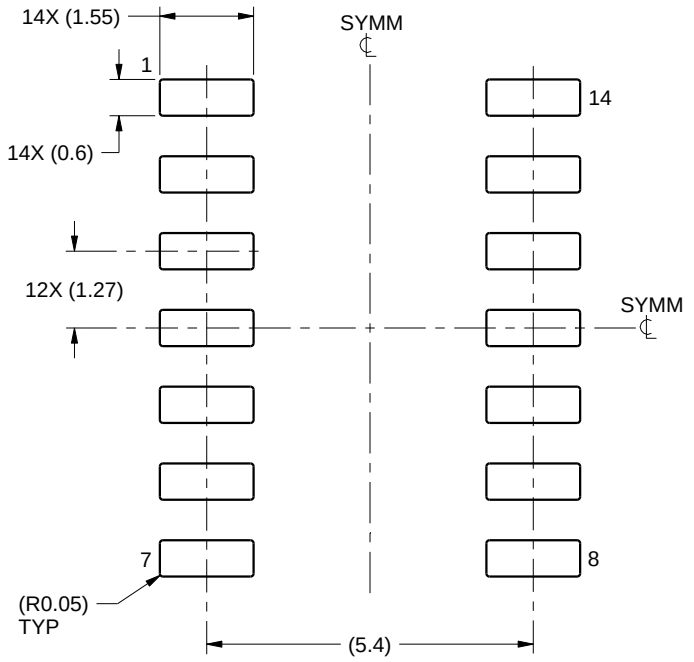
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

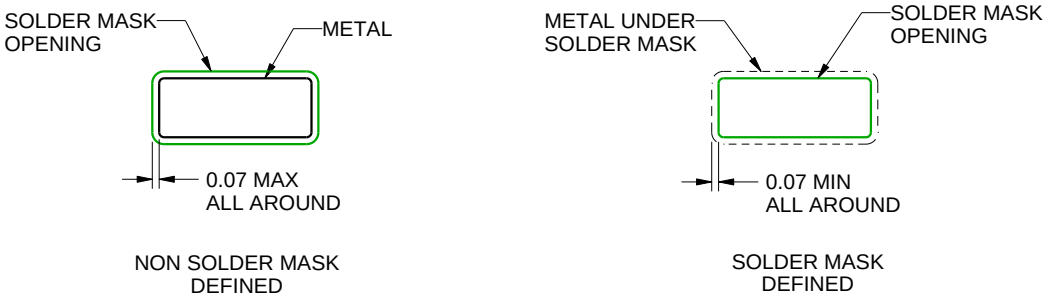


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

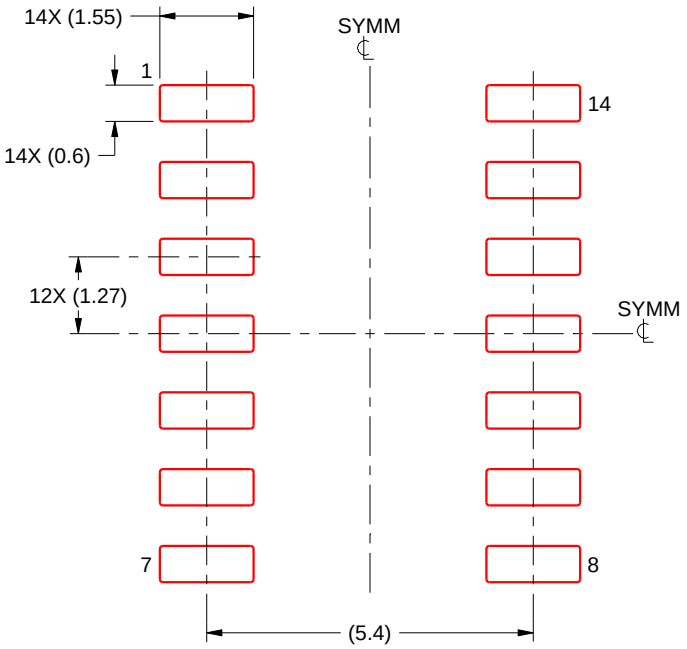
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

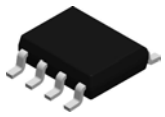


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

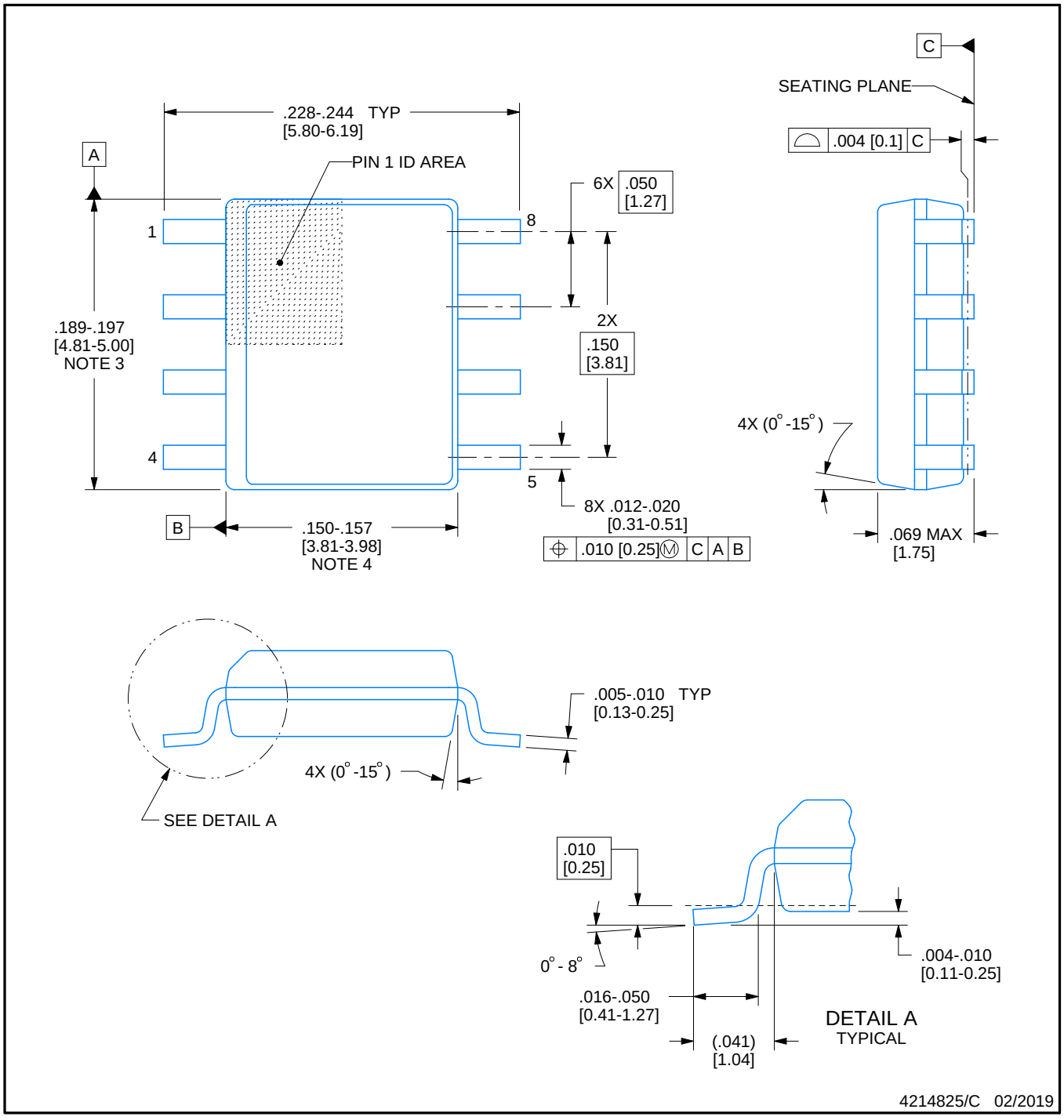


PACKAGE OUTLINE

D0008A

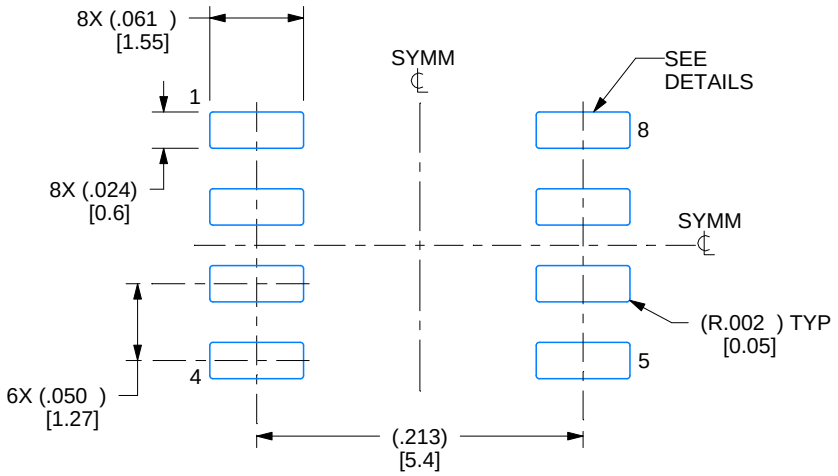
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

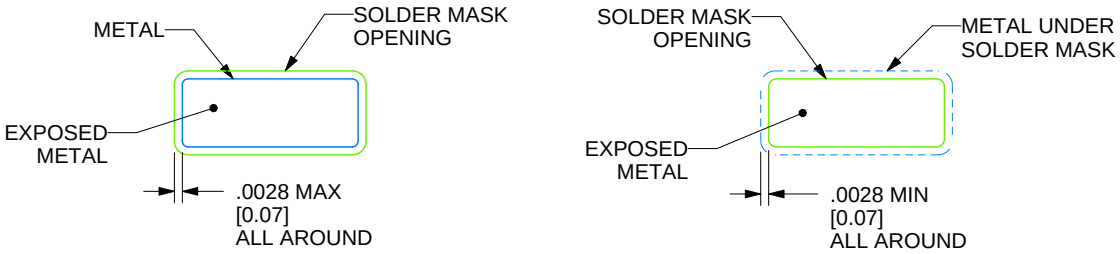


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

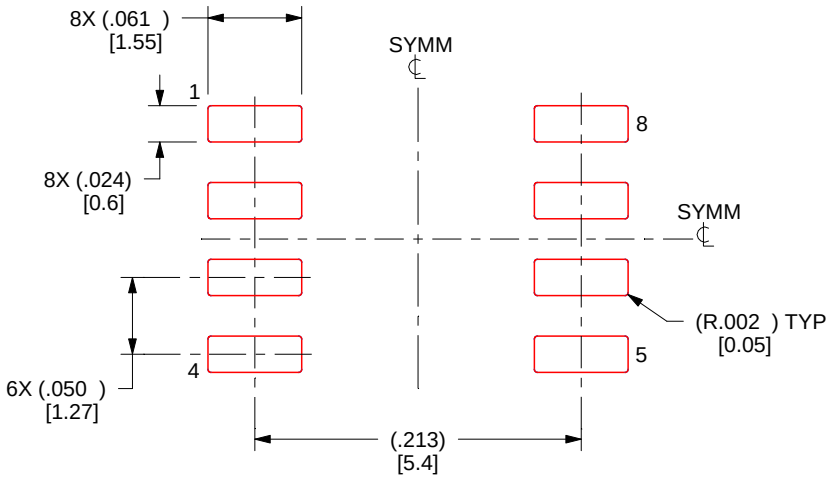
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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