

## 混合信号微控制器

### 特性

- 低电源电压范围: **1.8V 至 3.6V**
- 超低功耗
  - 激活模式: **220 $\mu$ A** (在 **1MHz** 频率和 **2.2V** 电压条件下)
  - 待机模式: **0.5 $\mu$ A**
  - 关闭模式 (RAM 保持): **0.1 $\mu$ A**
- **5** 种节能模式
- 可在不到 **1 $\mu$ s** 的时间里超快速地从待机模式唤醒
- **16** 位精简指令集 (RISC) 架构, **62.5ns** 指令周期时间
- 基本时钟模块配置
  - 带有四个已校准频率的高达 **16MHz** 的内部频率
  - 内部超低功耗低频 (LF) 振荡器
  - **32kHz** 晶振
  - 外部数字时钟源
- 一个具有 **3** 个捕获/比较寄存器的 **16** 位 **Timer\_A**
- 多达 **16** 个触感使能输入输出 (I/O) 引脚
- 支持 **SPI** 和 **I2C** 的通用串行接口 (USI)
- 欠压检测器
- 串行板上编程, 无需外部编程电压,

利用安全熔丝实现可编程代码保护

- 具有两线制 (**Spy-Bi-Wire**) 接口的片上仿真逻辑电路
- 系列产品汇总于 **Table 1**
- 封装选项
  - 薄型小外形尺寸封装 (TSSOP): **14** 引脚
- 如需了解完整的模块说明, 请查阅 **《MSP430x2xx 系列产品用户指南》 (SLAU144)**

### 支持国防、航空航天、和医疗应用

- 受控基线
- 同一组装和测试场所
- 同一制造场所
- 在扩展 (**-40°C 至 85°C**) 温度范围内可用 <sup>(1)</sup>
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

(1) 可定制工作温度范围

### 说明

德州仪器 (TI) 的 MSP430™ 系列超低功率微控制器包含几个器件, 这些器件特有针对多种应用的不同外设集。这种架构与 5 种低功耗模式相组合, 专为在便携式测量应用中延长电池的使用寿命而进行了优化。该器件具有一个强大的 **16** 位 RISC CPU, **16** 位寄存器和有助于大大提高编码效率的常数发生器。数控振荡器可在少于 **1  $\mu$ s** 内将器件从低功耗模式唤醒至激活模式。

MSP430G2302 系列微控制器是超低功耗混合信号微控制器, 此微控制器带有内置的**16** 位定时器, 和多达 **16** 个 I/O 触感使能引脚以及使用通用串行通信接口实现的内置通信功能。

配置详细信息, 请参见 **Table 1**。典型应用包括低成本传感器系统, 此类系统负责捕获模拟信号、将之转换为数字值、随后对数据进行处理以进行显示或传送至主机系统。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MSP430 is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012, Texas Instruments Incorporated  
English Data Sheet: **SLAS868**

**Table 1. Available Options<sup>(1)</sup>**

| Device             | EEM | Flash (kB) | RAM (B) | Timer_A | ADC10 Channel | USI | CLOCK        | I/O | Package Type |
|--------------------|-----|------------|---------|---------|---------------|-----|--------------|-----|--------------|
| MSP430G2302IPW1REP | 1   | 4          | 256     | 1x TA3  | -             | 1   | LF, DCO, VLO | 10  | 14-TSSOP     |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**Table 2. ORDERING INFORMATION<sup>(1)</sup>**

| T <sub>A</sub> | PACKAGE    | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER     |
|----------------|------------|-----------------------|------------------|----------------|
| -40°C to 85°C  | TSSOP - PW | MSP430G2302IPW1EP     | G2302EP          | V62/12623-01XE |
|                |            | MSP430G2302IPW1REP    |                  |                |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DEVICE PINOUTS

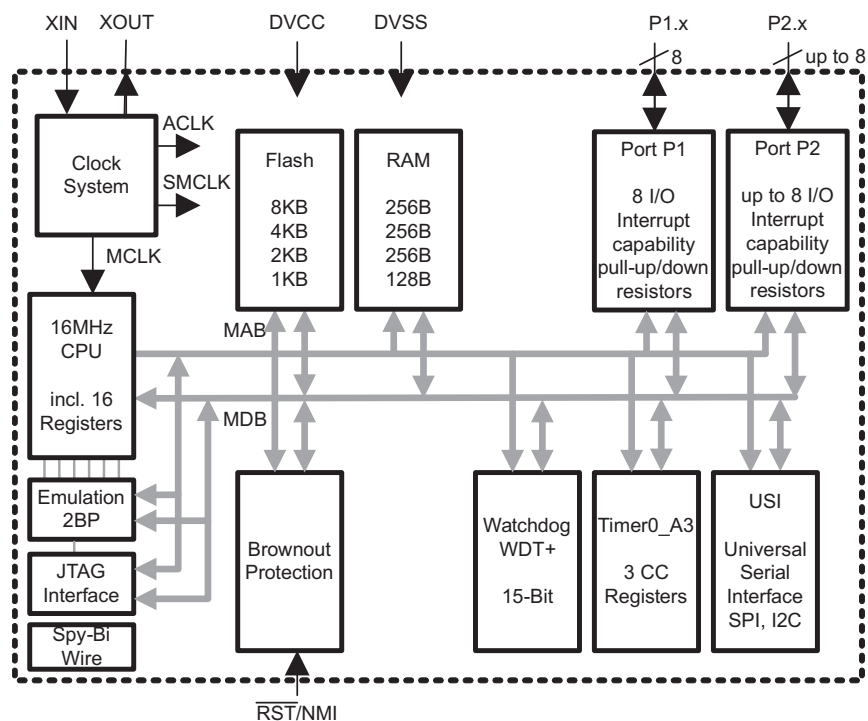
### PW PACKAGE (TOP VIEW)

|                                      |   |    |                                |
|--------------------------------------|---|----|--------------------------------|
| DVCC                                 | 1 | 14 | DVSS                           |
| P1.0/TA0CLK/ACLK/A0                  | 2 | 13 | XIN/P2.6/TA0.1                 |
| P1.1/TA0.0/A1                        | 3 | 12 | XOUT/P2.7                      |
| P1.2/TA0.1/A2                        | 4 | 11 | TEST/SBWTCK                    |
| P1.3/ADC10CLK/A3/VREF-/VEREF-        | 5 | 10 | RST/NMI/SBWTDIO                |
| P1.4/TA0.2/SMCLK/A4/VREF+/VEREF+/TCK | 6 | 9  | P1.7/SDI/SDA/A7/TDO/TDI        |
| P1.5/TA0.0/SCLK/A5/TMS               | 7 | 8  | P1.6/TA0.1/SDO/SCL/A6/TDI/TCLK |

NOTE: The pulldown resistors of port pins P2.0, P2.1, P2.2, P2.3, P2.4, and P2.5 should be enabled by setting P2REN.x = 1.

## FUNCTIONAL BLOCK DIAGRAMS

Functional Block Diagram, MSP430G2302



NOTE: Port P2: Two pins are available on the 14-pin package option. Eight pins are available on the 20-pin package option.

## TERMINAL FUNCTIONS

**Table 3. Terminal Functions**

| TERMINAL   |             | I/O | DESCRIPTION  |
|--|-------------|-----|--|
| NAME   | NO.<br>PW14 |     |  |
| P1.0/<br>TA0CLK/<br>ACLK/<br>A0                          | 2           | I/O | General-purpose digital I/O pin<br>Timer0_A, clock signal TACLK input<br>ACLK signal output<br>ADC10 analog input A0   |
| P1.1/<br>TA0.0/<br>A1                                    | 3           | I/O | General-purpose digital I/O pin<br>Timer0_A, capture: CCI0A input, compare: Out0 output<br>ADC10 analog input A1   |
| P1.2/<br>TA0.1/<br>A2                                    | 4           | I/O | General-purpose digital I/O pin<br>Timer0_A, capture: CCI1A input, compare: Out1 output<br>ADC10 analog input A2   |
| P1.3/<br>ADC10CLK/<br>A3/<br>VREF-/VEREF                 | 5           | I/O | General-purpose digital I/O pin<br>ADC10, conversion clock output<br>ADC10 analog input A3<br>ADC10 negative reference voltage   |
| P1.4/<br>TA0.2/<br>SMCLK/<br>A4/<br>VREF+/VEREF+/<br>TCK | 6           | I/O | General-purpose digital I/O pin<br>Timer0_A, capture: CCI2A input, compare: Out2 output<br>SMCLK signal output<br>ADC10 analog input A4<br>ADC10 positive reference voltage<br>JTAG test clock, input terminal for device programming and test |
| P1.5/<br>TA0.0/<br>A5/<br>SCLK/<br>TMS                   | 7           | I/O | General-purpose digital I/O pin<br>Timer0_A, compare: Out0 output<br>ADC10 analog input A5<br>USI: clk input in I2C mode; clk in/output in SPI mode<br>JTAG test mode select, input terminal for device programming and test                   |
| P1.6/<br>TA0.1/<br>A6/<br>SDO/<br>SCL/<br>TDI/<br>TCLK   | 8           | I/O | General-purpose digital I/O pin<br>Timer0_A, compare: Out1 output<br>ADC10 analog input A6<br>USI: Data output in SPI mode<br>USI: I2C clock in I2C mode<br>JTAG test data input or test clock input during programming and test               |
| P1.7/<br>A7/<br>SDI/<br>SDA/<br>TDO/TDI <sup>(1)</sup>   | 9           | I/O | General-purpose digital I/O pin<br>ADC10 analog input A7<br>USI: Data input in SPI mode<br>USI: I2C data in I2C mode<br>JTAG test data output terminal or test data input during programming and test  |
| XIN/<br>P2.6/<br>TA0.1                                   | 13          | I/O | Input terminal of crystal oscillator<br>General-purpose digital I/O pin<br>Timer0_A, compare: Out1 output  |

(1) TDO or TDI is selected via JTAG instruction.

**Table 3. Terminal Functions (continued)**

| TERMINAL                 |             | I/O | DESCRIPTION   |
|--------------------------|-------------|-----|---|
| NAME                     | NO.<br>PW14 |     |   |
| XOUT/<br>P2.7            | 12          | I/O | Output terminal of crystal oscillator <sup>(2)</sup><br>General-purpose digital I/O pin   |
| RST/<br>NMI/<br>SBWTDIO/ | 10          | I   | Reset<br>Nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output during programming and test  |
| TEST/<br>SBWTCK          | 11          | I   | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST.<br>Spy-Bi-Wire test clock input during programming and test |
| DVCC                     | 1           | NA  | Supply voltage  |
| AVCC                     | NA          | NA  | Supply voltage  |
| DVSS                     | 14          | NA  | Ground reference  |
| AVSS                     | NA          | NA  | Ground reference  |
| NC                       | -           | NA  | Not connected   |
| QFN Pad                  | -           | NA  | QFN package pad connection to VSS recommended.  |

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

## SHORT-FORM DESCRIPTION

### CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

### Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 4](#) shows examples of the three types of instruction formats; [Table 5](#) shows the address modes.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 4. Instruction Word Formats**

| FORMAT                            | EXAMPLE   | OPERATION                                 |
|-----------------------------------|-----------|---|
| Dual operands, source-destination | ADD R4,R5 | $R4 + R5 \rightarrow R5$                  |
| Single operands, destination only | CALL R8   | $PC \rightarrow (TOS), R8 \rightarrow PC$ |
| Relative jump, un/conditional     | JNE       | Jump-on-equal bit = 0                     |

**Table 5. Address Mode Descriptions<sup>(1)</sup>**

| ADDRESS MODE           | S | D | SYNTAX          | EXAMPLE          | OPERATION   |
|------------------------|---|---|-----------------|------------------|---|
| Register               | ✓ | ✓ | MOV Rs,Rd       | MOV R10,R11      | $R10 \rightarrow R11$                                 |
| Indexed                | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | $M(2+R5) \rightarrow M(6+R6)$                         |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI    |                  | $M(EDE) \rightarrow M(TONI)$                          |
| Absolute               | ✓ | ✓ | MOV &MEM,&TCDAT |                  | $M(MEM) \rightarrow M(TCDAT)$                         |
| Indirect               | ✓ |   | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | $M(R10) \rightarrow M(Tab+R6)$                        |
| Indirect autoincrement | ✓ |   | MOV @Rn+,Rm     | MOV @R10+,R11    | $M(R10) \rightarrow R11$<br>$R10 + 2 \rightarrow R10$ |
| Immediate              | ✓ |   | MOV #X,TONI     | MOV #45,TONI     | $\#45 \rightarrow M(TONI)$                            |

(1) S = source, D = destination

## Operating Modes

The MSP430 devices have one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped



## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed) the CPU goes into LPM4 immediately after power-up.

**Table 6. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE   | INTERRUPT FLAG                                    | SYSTEM INTERRUPT                                   | WORD ADDRESS     | PRIORITY        |
|--|---|--|------------------|-----------------|
| Power-Up<br>External Reset<br>Watchdog Timer+<br>Flash key violation<br>PC out-of-range <sup>(1)</sup> | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV <sup>(2)</sup> | Reset  | 0FFFEh           | 31, highest     |
| NMI<br>Oscillator fault<br>Flash memory access violation   | NMIIFG<br>OFIFG<br>ACCVIFG <sup>(2)(3)</sup>      | (non)-maskable<br>(non)-maskable<br>(non)-maskable | 0FFFCCh          | 30              |
|  |   |  | 0FFFAh           | 29              |
|  |   |  | 0FFF8h           | 28              |
|  |   |  | 0FFF6h           | 27              |
| Watchdog Timer+  | WDTIFG  | maskable   | 0FFF4h           | 26              |
| Timer0_A3  | TACCR0 CCIFG <sup>(4)</sup>                       | maskable   | 0FFF2h           | 25              |
| Timer0_A3  | TACCR2 TACCR1 CCIFG.<br>TAIFG <sup>(4)</sup>      | maskable   | 0FFF0h           | 24              |
|  |   |  | 0FFEEh           | 23              |
|  |   |  | 0FFECCh          | 22              |
| USI  | USIIFG, USISTTIFG <sup>(2)(4)</sup>               | maskable   | 0FFE8h           | 20              |
| I/O Port P2 (up to eight flags)  | P2IFG.0 to P2IFG.7 <sup>(2)(4)</sup>              | maskable   | 0FFE6h           | 19              |
| I/O Port P1 (up to eight flags)  | P1IFG.0 to P1IFG.7 <sup>(2)(4)</sup>              | maskable   | 0FFE4h           | 18              |
|  |   |  | 0FFE2h           | 17              |
|  |   |  | 0FFE0h           | 16              |
| See <sup>(5)</sup>   |   |  | 0FFDEh to 0FFC0h | 15 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags


(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.





(5) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

## Special Function Registers (SFRs)









Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

|               |   |   |
|---------------|---|---|
| <b>Legend</b> | <b>rw:</b>  | Bit can be read and written.                            |
|               | <b>rw-0,1:</b>  | Bit can be read and written. It is reset or set by PUC. |
|               | <b>rw-(0,1):</b>  | Bit can be read and written. It is reset or set by POR. |
|               |  | SFR bit is not present in device.                       |




**Table 7. Interrupt Enable Register 1 and 2**

| Address | 7   | 6   | 5      | 4     | 3  | 2   | 1    | 0     |
|---------|---|---|--------|-------|--|---|------|-------|
| 00h     |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
|         |   |   | rw-0   | rw-0  |  |   | rw-0 | rw-0  |









**WDTIE** Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.  
**OFIE** Oscillator fault interrupt enable  
**NMIIE** (Non)maskable interrupt enable  
**ACCVIE** Flash access violation interrupt enable

| Address | 7   | 6   | 5   | 4   | 3  | 2   | 1   | 0   |
|---------|---|---|---|---|--|---|---|---|
| 01h     |  |  |  |  |  |  |  |  |

**Table 8. Interrupt Flag Register 1 and 2**

| Address | 7   | 6   | 5   | 4      | 3      | 2      | 1     | 0      |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h     |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
|         |   |   |   | rw-0   | rw-(0) | rw-(1) | rw-1  | rw-(0) |

**WDTIFG** Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V<sub>CC</sub> power-on or a reset condition at the RST/NMI pin in reset mode.  
**OFIFG** Flag set on oscillator fault.  
**PORIFG** Power-On Reset interrupt flag. Set on V<sub>CC</sub> power-up.  
**RSTIFG** External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on V<sub>CC</sub> power-up.  
**NMIIFG** Set via RST/NMI pin

| Address | 7   | 6   | 5   | 4   | 3  | 2   | 1   | 0   |
|---------|---|---|---|---|--|---|---|---|
| 03h     |  |  |  |  |  |  |  |  |

## Memory Organization

**Table 9. Memory Organization**

|                        |           | <b>MSP430G2302</b> |
|------------------------|-----------|--------------------|
| Memory                 | Size      | 4kB                |
| Main: interrupt vector | Flash     | 0xFFFF to 0xFFC0   |
| Main: code memory      | Flash     | 0xFFFF to 0xF000   |
| Information memory     | Size      | 256 Byte           |
|                        | Flash     | 010FFh to 01000h   |
| RAM                    | Size      | 256 B              |
|                        |           | 0x02FF to 0x0200   |
| Peripherals            | 16-bit    | 01FFh to 0100h     |
|                        | 8-bit     | 0FFh to 010h       |
|                        | 8-bit SFR | 0Fh to 00h         |

## Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

## Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

## Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1  $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

## Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

**Table 10. Tags Used by the ADC Calibration Tags**

| NAME        | ADDRESS | VALUE | DESCRIPTION   |
|-------------|---------|-------|---|
| TAG_DCO_30  | 0x10F6  | 0x01  | DCO frequency calibration at $V_{CC} = 3$ V and $T_A = 30^\circ\text{C}$ at calibration |
| TAG_ADC10_1 | 0x10DA  | 0x10  | ADC10_1 calibration tag   |
| TAG_EMPTY   | -       | 0xFE  | Identifier for empty memory areas   |

**Table 11. Labels Used by the ADC Calibration Tags**

| LABEL                 | CONDITION AT CALIBRATION / DESCRIPTION                        | SIZE | ADDRESS OFFSET |
|-----------------------|---|------|----------------|
| CAL_ADC_25T85         | INCHx = 0x1010, REF2_5 = 1, $T_A = 85^\circ\text{C}$          | word | 0x0010         |
| CAL_ADC_25T30         | INCHx = 0x1010, REF2_5 = 1, $T_A = 30^\circ\text{C}$          | word | 0x000E         |
| CAL_ADC_25VREF_FACTOR | REF2_5 = 1, $T_A = 30^\circ\text{C}$ , $I_{(VREF+)} = 1$ mA   | word | 0x000C         |
| CAL_ADC_15T85         | INCHx = 0x1010, REF2_5 = 0, $T_A = 85^\circ\text{C}$          | word | 0x000A         |
| CAL_ADC_15T30         | INCHx = 0x1010, REF2_5 = 0, $T_A = 30^\circ\text{C}$          | word | 0x0008         |
| CAL_ADC_15VREF_FACTOR | REF2_5 = 0, $T_A = 30^\circ\text{C}$ , $I_{(VREF+)} = 0.5$ mA | word | 0x0006         |
| CAL_ADC_OFFSET        | External VREF = 1.5 V, $f_{(ADC10CLK)} = 5$ MHz               | word | 0x0004         |
| CAL_ADC_GAIN_FACTOR   | External VREF = 1.5 V, $f_{(ADC10CLK)} = 5$ MHz               | word | 0x0002         |
| CAL_BC1_1MHz          | -   | byte | 0x0009         |
| CAL_DCO_1MHz          | -   | byte | 0x00008        |
| CAL_BC1_8MHz          | -   | byte | 0x0007         |
| CAL_DCO_8MHz          | -   | byte | 0x0006         |
| CAL_BC1_12MHz         | -   | byte | 0x0005         |
| CAL_DCO_12MHz         | -   | byte | 0x0004         |
| CAL_BC1_16MHz         | -   | byte | 0x0003         |
| CAL_DCO_16MHz         | -   | byte | 0x0002         |

### Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter  $S_{DCO}$ .
- Modulation control bits MODx select how often  $f_{DCO(RSEL,DCO+1)}$  is used within the period of 32 DCOCLK cycles. The frequency  $f_{DCO(RSEL,DCO)}$  is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

### Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

### Digital I/O

There are two 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition(port P1 and port P2 only) is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and port P2, if available.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.
- Each I/O has an individually programmable pin-oscillator enable bit to enable low-cost touch sensing.

### WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

## Timer0\_A3

Timer0\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 12. Timer0\_A3 Signal Connections<sup>(1)</sup>**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| PW14             |                     |                   |              |                      | PW14              |
| P1.0-2           | TACLK               | TACLK             | Timer        | NA                   |                   |
|                  | ACLK                | ACLK              |              |                      |                   |
|                  | SMCLK               | SMCLK             |              |                      |                   |
| PinOsc           |                     | INCLK             |              |                      |                   |
| P1.1-3           | TA0.0               | CCI0A             | CCR0         | TA0                  | P1.1-3            |
|                  | ACLK                | CCI0B             |              |                      | P1.5-7            |
|                  | V <sub>SS</sub>     | GND               |              |                      |                   |
|                  | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |
| P1.2-4           | TA0.1               | CCI1A             | CCR1         | TA1                  | P1.2-4            |
|                  | CAOUT               | CCI1B             |              |                      | P1.6-8            |
|                  | V <sub>SS</sub>     | GND               |              |                      | P2.6-13           |
|                  | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |
| P1.4-6           | TA0.2               | CCI2A             | CCR2         | TA2                  | P1.4-6            |
| PinOsc           | TA0.2               | CCI2B             |              |                      |                   |
|                  | V <sub>SS</sub>     | GND               |              |                      |                   |
|                  | V <sub>CC</sub>     | V <sub>CC</sub>   |              |                      |                   |

(1) Only one pin-oscillator must be enabled at a time.

## USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

**Peripheral File Map**
**Table 13. Peripherals With Word Access**

| MODULE                 | REGISTER DESCRIPTION     | REGISTER NAME | OFFSET |
|------------------------|--------------------------|---------------|--------|
| <b>Timer0_A3</b>       | Capture/compare register | TACCR2        | 0176h  |
|                        | Capture/compare register | TACCR1        | 0174h  |
|                        | Capture/compare register | TACCR0        | 0172h  |
|                        | Timer_A register         | TAR           | 0170h  |
|                        | Capture/compare control  | TACCTL2       | 0166h  |
|                        | Capture/compare control  | TACCTL1       | 0164h  |
|                        | Capture/compare control  | TACCTL0       | 0162h  |
|                        | Timer_A control          | TACTL         | 0160h  |
|                        | Timer_A interrupt vector | TAIV          | 012Eh  |
| <b>Flash Memory</b>    | Flash control 3          | FCTL3         | 012Ch  |
|                        | Flash control 2          | FCTL2         | 012Ah  |
|                        | Flash control 1          | FCTL1         | 0128h  |
| <b>Watchdog Timer+</b> | Watchdog/timer control   | WDTCTL        | 0120h  |

**Table 14. Peripherals With Byte Access**

| MODULE                     | REGISTER DESCRIPTION          | REGISTER NAME | OFFSET |
|----------------------------|-------------------------------|---------------|--------|
| <b>USI</b>                 | USI control 0                 | USICTL0       | 078h   |
|                            | USI control 1                 | USICTL1       | 079h   |
|                            | USI clock control             | USICKCTL      | 07Ah   |
|                            | USI bit counter               | USICNT        | 07Bh   |
|                            | USI shift register            | USISR         | 07Ch   |
| <b>Basic Clock System+</b> | Basic clock system control 3  | BCSCTL3       | 053h   |
|                            | Basic clock system control 2  | BCSCTL2       | 058h   |
|                            | Basic clock system control 1  | BCSCTL1       | 057h   |
|                            | DCO clock frequency control   | DCOCTL        | 056h   |
| <b>Port P2</b>             | Port P2 selection 2           | P2SEL2        | 042h   |
|                            | Port P2 resistor enable       | P2REN         | 02Fh   |
|                            | Port P2 selection             | P2SEL         | 02Eh   |
|                            | Port P2 interrupt enable      | P2IE          | 02Dh   |
|                            | Port P2 interrupt edge select | P2IES         | 02Ch   |
|                            | Port P2 interrupt flag        | P2IFG         | 02Bh   |
|                            | Port P2 direction             | P2DIR         | 02Ah   |
|                            | Port P2 output                | P2OUT         | 029h   |
|                            | Port P2 input                 | P2IN          | 028h   |
| <b>Port P1</b>             | Port P1 selection 2           | P1SEL2        | 041h   |
|                            | Port P1 resistor enable       | P1REN         | 027h   |
|                            | Port P1 selection             | P1SEL         | 026h   |
|                            | Port P1 interrupt enable      | P1IE          | 025h   |
|                            | Port P1 interrupt edge select | P1IES         | 024h   |
|                            | Port P1 interrupt flag        | P1IFG         | 023h   |
|                            | Port P1 direction             | P1DIR         | 022h   |
|                            | Port P1 output                | P1OUT         | 021h   |
|                            | Port P1 input                 | P1IN          | 020h   |
| <b>Special Function</b>    | SFR interrupt flag 2          | IFG2          | 003h   |
|                            | SFR interrupt flag 1          | IFG1          | 002h   |
|                            | SFR interrupt enable 2        | IE2           | 001h   |
|                            | SFR interrupt enable 1        | IE1           | 000h   |



## Absolute Maximum Ratings<sup>(1)</sup>

|   |                     |                            |
|---|---------------------|----------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$             |                     | –0.3 V to 4.1 V            |
| Voltage applied to any pin <sup>(2)</sup>           |                     | –0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device pin                     |                     | ±2 mA                      |
| Storage temperature range, $T_{stg}$ <sup>(3)</sup> | Unprogrammed device | –55°C to 150°C             |
|   | Programmed device   | –55°C to 150°C             |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## Thermal Information

| THERMAL METRIC    |   | MSP430G2302 | UNITS |
|-------------------|---|-------------|-------|
|                   |   | PW          |       |
|                   |   | 14 PINS     |       |
| $\theta_{JA}$     | Junction-to-ambient thermal resistance <sup>(1)</sup>       | 98.7        | °C/W  |
| $\theta_{JCTop}$  | Junction-to-case (top) thermal resistance <sup>(2)</sup>    | 26.8        |       |
| $\theta_{JB}$     | Junction-to-board thermal resistance <sup>(3)</sup>         | 41.2        |       |
| $\psi_{JT}$       | Junction-to-top characterization parameter <sup>(4)</sup>   | 1.1         |       |
| $\psi_{JB}$       | Junction-to-board characterization parameter <sup>(5)</sup> | 40.5        |       |
| $\theta_{JCbott}$ | Junction-to-case (bottom) thermal resistance <sup>(6)</sup> | N/A         |       |

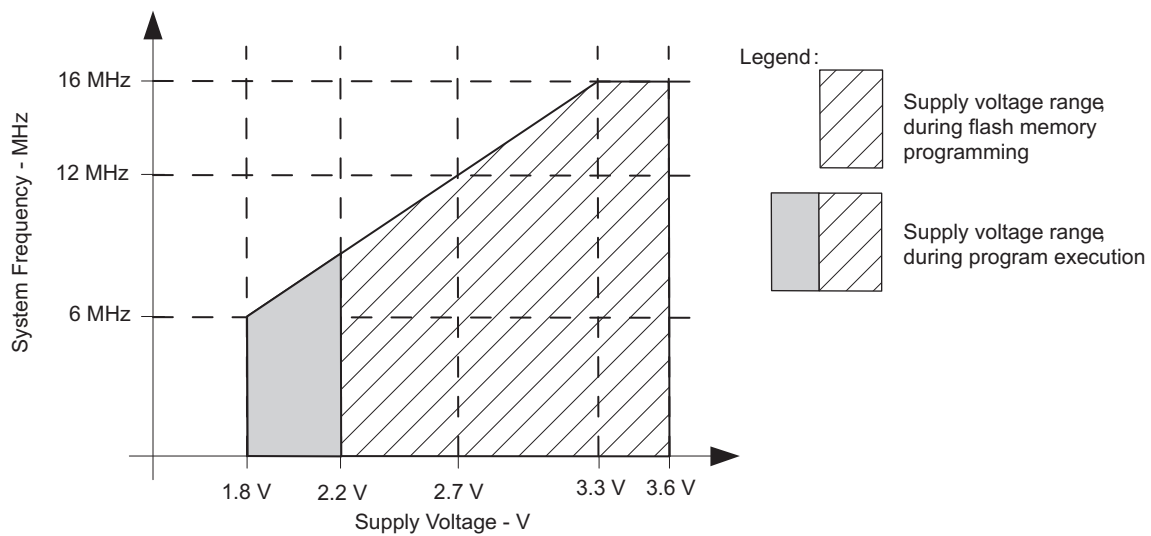
- (1) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
- (2) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
- (3) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
- (4) 结至顶部特征参数， $\psi_{JT}$ ，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得  $\theta_{JA}$ 。
- (5) 结至电路板特征参数， $\psi_{JB}$ ，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得  $\theta_{JA}$ 。
- (6) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。

## Recommended Operating Conditions

|              |   |   | MIN | NOM | MAX | UNIT |
|--------------|---|---|-----|-----|-----|------|
| $V_{CC}$     | Supply voltage  | During program execution                                | 1.8 |     | 3.6 | V    |
|              |   | During flash programming/erase                          | 2.2 |     | 3.6 |      |
| $V_{SS}$     | Supply voltage  |   |     | 0   |     | V    |
| $T_A$        | Operating free-air temperature  |   | -40 |     | 85  | °C   |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency using the USART module) <sup>(1)(2)</sup> | $V_{CC} = 1.8\text{ V}$ ,<br>Duty cycle = 50% $\pm$ 10% | dc  |     | 6   | MHz  |
|              |   | $V_{CC} = 2.7\text{ V}$ ,<br>Duty cycle = 50% $\pm$ 10% | dc  |     | 12  |      |
|              |   | $V_{CC} = 3.3\text{ V}$ ,<br>Duty cycle = 50% $\pm$ 10% | dc  |     | 16  |      |

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.

(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.2 V.

**Figure 1. Safe Operating Area**

## Electrical Characteristics

### Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                      | TEST CONDITIONS   | $V_{CC}$ | MIN | TYP | MAX | UNIT          |
|--|---|----------|-----|-----|-----|---------------|
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1\text{ MHz}$ ,<br>$f_{ACLK} = 32768\text{ Hz}$ ,<br>Program executes in flash,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 | 2.2 V    |     | 220 |     | $\mu\text{A}$ |
|  |   | 3 V      |     | 320 | 400 |               |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

### Typical Characteristics – Active Mode Supply Current (Into $V_{CC}$ )

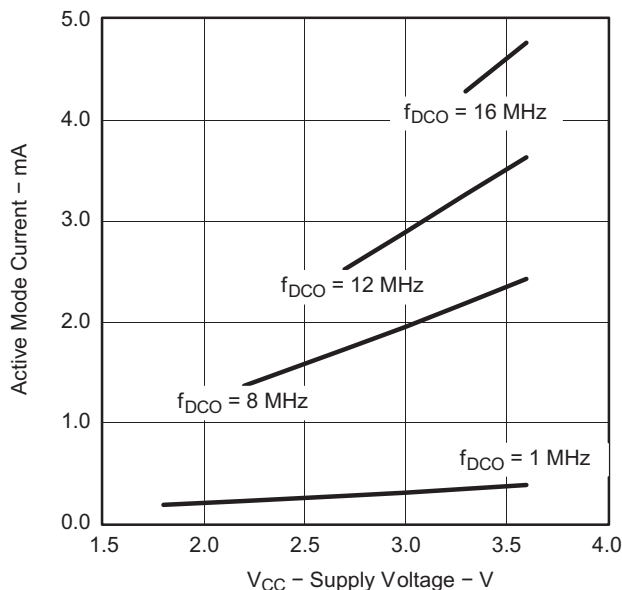


Figure 2. Active Mode Current vs  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$

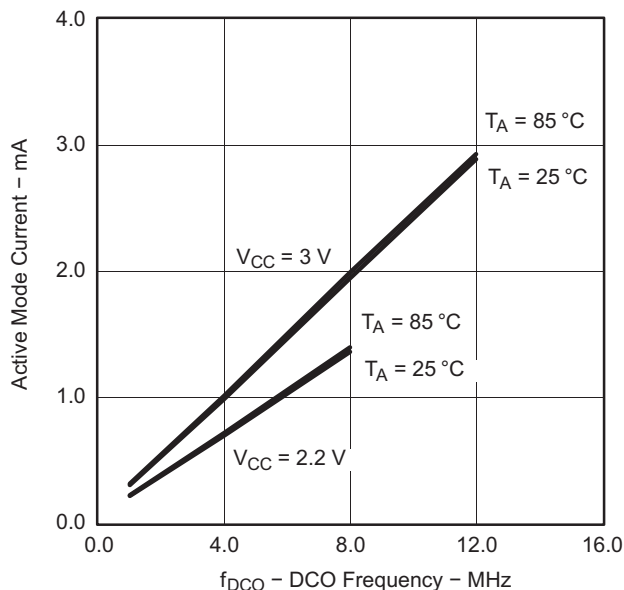


Figure 3. Active Mode Current vs DCO Frequency

## Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER  | TEST CONDITIONS   | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT    |
|--|---|-------|----------|-----|-----|-----|---------|
| $I_{LPM0,1MHz}$ Low-power mode 0 (LPM0) current <sup>(3)</sup> | $f_{MCLK} = 0$ MHz,<br>$f_{SMCLK} = f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 | 25°C  | 2.2 V    |     | 55  |     | $\mu A$ |
| $I_{LPM2}$ Low-power mode 2 (LPM2) current <sup>(4)</sup>      | $f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1,<br>OSCOFF = 0 | 25°C  | 2.2 V    |     | 22  |     | $\mu A$ |
| $I_{LPM3,LFX1}$ Low-power mode 3 (LPM3) current <sup>(4)</sup> | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0  | 25°C  | 2.2 V    |     | 0.7 | 1.0 | $\mu A$ |
| $I_{LPM3,VLO}$ Low-power mode 3 current, (LPM3) <sup>(4)</sup> | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK}$ from internal LF oscillator (VLO),<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0   | 25°C  | 2.2 V    |     | 0.5 | 0.7 | $\mu A$ |
| $I_{LPM4}$ Low-power mode 4 (LPM4) current <sup>(5)</sup>      | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 0$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 1  | 25°C  | 2.2 V    |     | 0.1 | 0.5 | $\mu A$ |
|  |   | 85°C  | 2.2 V    |     | 0.8 | 1.5 | $\mu A$ |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.

(3) Current for brownout and WDT clocked by SMCLK included.

(4) Current for brownout and WDT clocked by ACLK included.

(5) Current for brownout included.

## Typical Characteristics Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

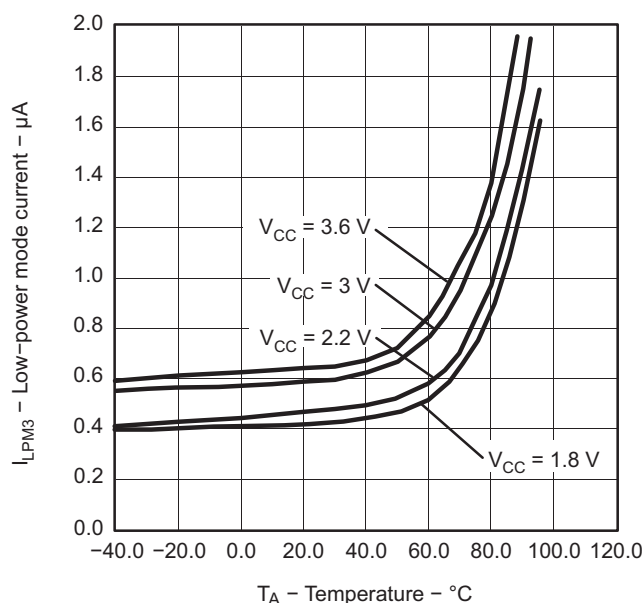


Figure 4. LPM3 Current vs Temperature

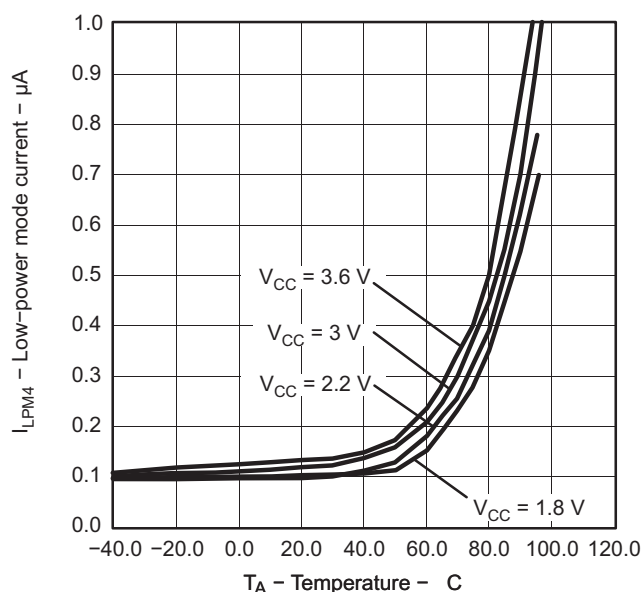


Figure 5. LPM4 Current vs Temperature

## Schmitt-Trigger Inputs – Ports Px<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS  | V <sub>CC</sub> | MIN                  | TYP | MAX                  | UNIT |
|--|--|-----------------|----------------------|-----|----------------------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          |  |                 | 0.45 V <sub>CC</sub> |     | 0.75 V <sub>CC</sub> | V    |
|  |  | 3 V             | 1.35                 |     | 2.25                 |      |
| V <sub>IT–</sub> Negative-going input threshold voltage                          |  |                 | 0.25 V <sub>CC</sub> |     | 0.55 V <sub>CC</sub> | V    |
|  |  | 3 V             | 0.75                 |     | 1.65                 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |  | 3 V             | 0.3                  |     | 1                    | V    |
| R <sub>Pull</sub> Pullup/pulldown resistor                                       | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> | 3 V             | 20                   | 35  | 50                   | kΩ   |
| C <sub>I</sub> Input capacitance   | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>   |                 |                      | 5   |                      | pF   |

- (1) An external signal sets the interrupt flag every time the minimum interrupt pulse width  $t_{(int)}$  is met. It may be set even with trigger signals shorter than  $t_{(int)}$ .

## Leakage Current – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                       | V <sub>CC</sub> | MIN | MAX | UNIT |
|--|---------------------------------------|-----------------|-----|-----|------|
| I <sub>lkg</sub> (Px.x) High-impedance leakage current | See <sup>(1)</sup> and <sup>(2)</sup> | 3 V             |     | ±50 | nA   |

- (1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.  
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input, and the pullup/pulldown resistor is disabled.

## Outputs – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                             | V <sub>CC</sub> | MIN | TYP                   | MAX | UNIT |
|---|---|-----------------|-----|-----------------------|-----|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = –6 mA <sup>(1)</sup> | 3 V             |     | V <sub>CC</sub> – 0.3 |     | V    |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 6 mA <sup>(1)</sup>  | 3 V             |     | V <sub>SS</sub> + 0.3 |     | V    |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

## Output Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----|-----|-----|------|
| f <sub>Px,y</sub> Port output frequency (with load) | Px.y, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ <sup>(1)</sup> <sup>(2)</sup> | 3 V             |     | 12  |     | MHz  |
| f <sub>Port_CLK</sub> Clock output frequency        | Px.y, C <sub>L</sub> = 20 pF <sup>(2)</sup>                                       | 3 V             |     | 16  |     | MHz  |

- (1) A resistive divider with two 0.5-kΩ resistors between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.  
(2) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

## Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT  
vs  
LOW-LEVEL OUTPUT VOLTAGE

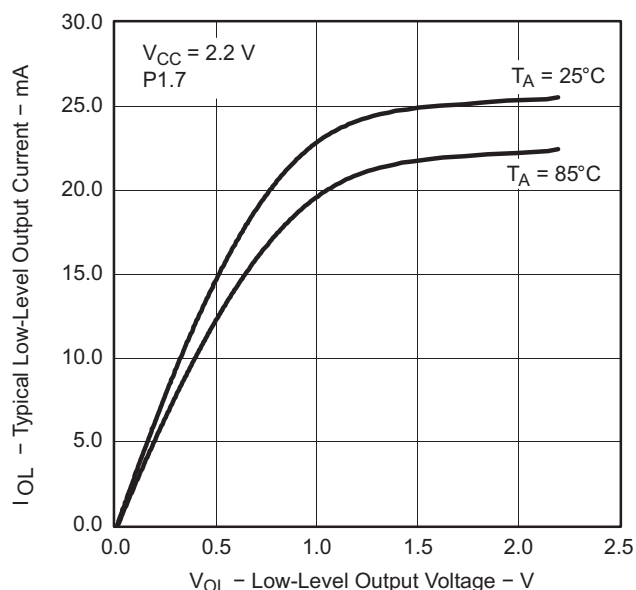


Figure 6.

TYPICAL LOW-LEVEL OUTPUT CURRENT  
vs  
LOW-LEVEL OUTPUT VOLTAGE

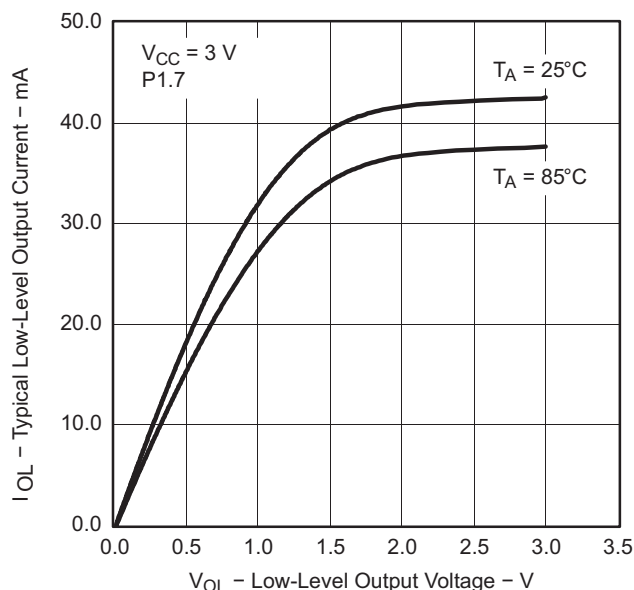


Figure 7.

TYPICAL HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

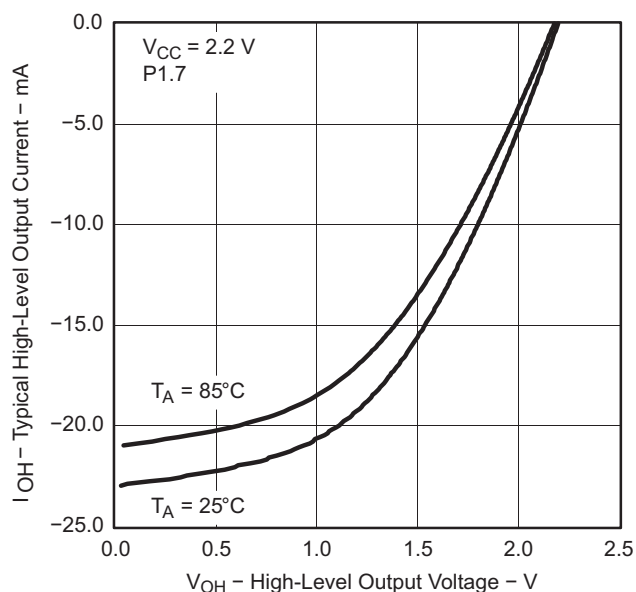


Figure 8.

TYPICAL HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

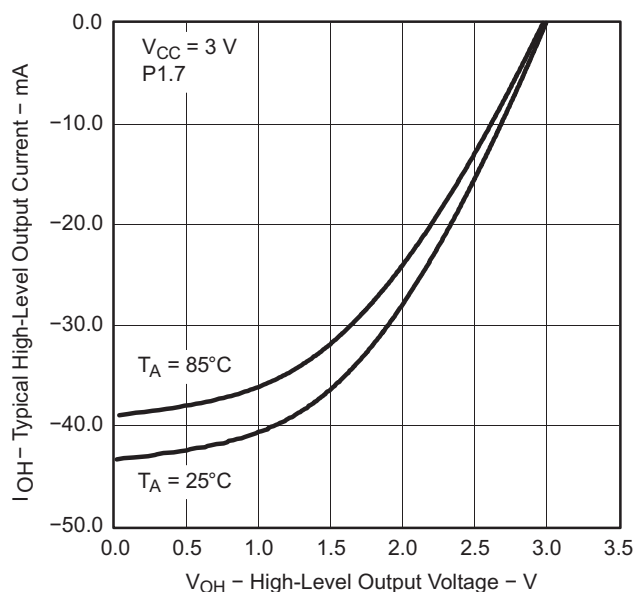


Figure 9.

## Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                                   | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|-----------|-----------------------------------|--|-----------------|------|-----|-----|------|
| foP1.x    | Port output oscillation frequency | P1.y, C <sub>L</sub> = 10 pF, R <sub>L</sub> = 100 kΩ <sup>(1)(2)</sup>          | 3 V             | 1400 |     |     | kHz  |
|           |                                   | P1.y, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 100 kΩ <sup>(1)(2)</sup>          |                 | 900  |     |     |      |
| foP2.x    | Port output oscillation frequency | P2.0 to P2.5, C <sub>L</sub> = 10 pF, R <sub>L</sub> = 100 kΩ <sup>(1)(2)</sup>  | 3 V             | 1800 |     |     | kHz  |
|           |                                   | P2.0 to P2.5, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 100 kΩ <sup>(1)(2)</sup>  |                 | 1000 |     |     |      |
| foP2.6/7  | Port output oscillation frequency | P2.6 and P2.7, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 100 kΩ <sup>(1)(2)</sup> | 3 V             | 700  |     |     | kHz  |

- (1) A resistive divider with two 100-kΩ resistors between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage oscillates with a typical amplitude of 700 mV at the specified toggle frequency.

## Typical Characteristics – Pin-Oscillator Frequency

TYPICAL OSCILLATING FREQUENCY  
vs  
LOAD CAPACITANCE

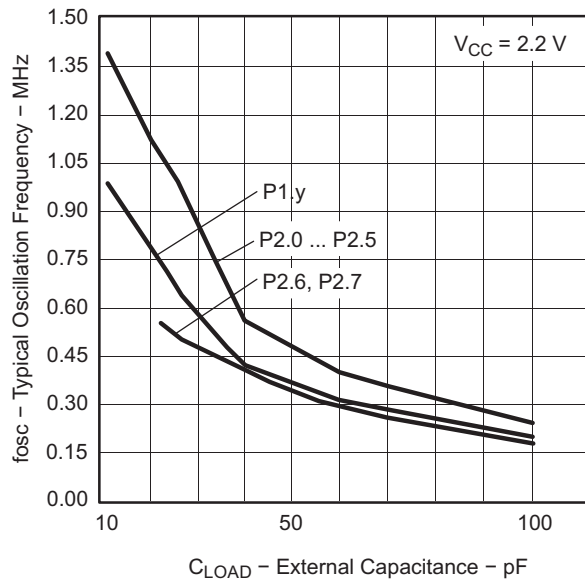


Figure 10.

TYPICAL OSCILLATING FREQUENCY  
vs  
LOAD CAPACITANCE

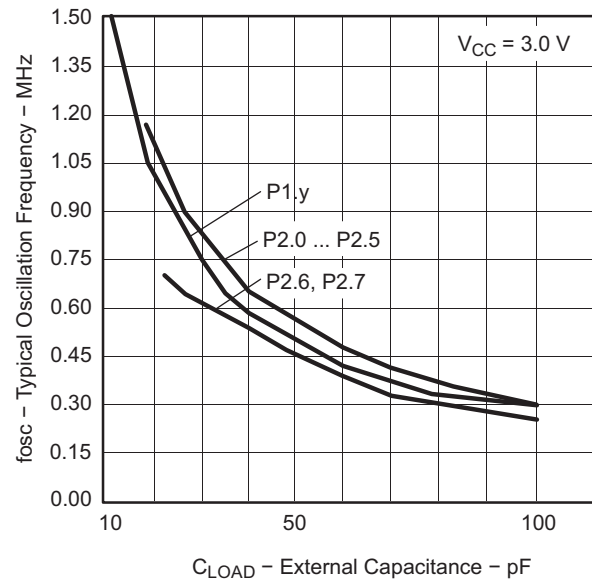


Figure 11.

## POR/Brownout Reset (BOR)<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS  | V <sub>CC</sub>              | MIN | TYP                        | MAX  | UNIT |
|-------------------------|--|------------------------------|-----|----------------------------|------|------|
| V <sub>CC(start)</sub>  | See Figure 12  | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 0.7 × V <sub>(B_IT-)</sub> |      | V    |
| V <sub>(B_IT-)</sub>    | See Figure 12 through Figure 14  | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 1.40                       |      | V    |
| V <sub>hys(B_IT-)</sub> | See Figure 12  | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 140                        |      | mV   |
| t <sub>d(BOR)</sub>     | See Figure 12  |                              |     |                            | 2000 | μs   |
| t <sub>(reset)</sub>    | Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally | 2.2 V                        | 2   |                            |      | μs   |

- (1) The current consumption of the brownout module is already included in the I<sub>CC</sub> current consumption data. The voltage level V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub> is ≤ 1.8 V.

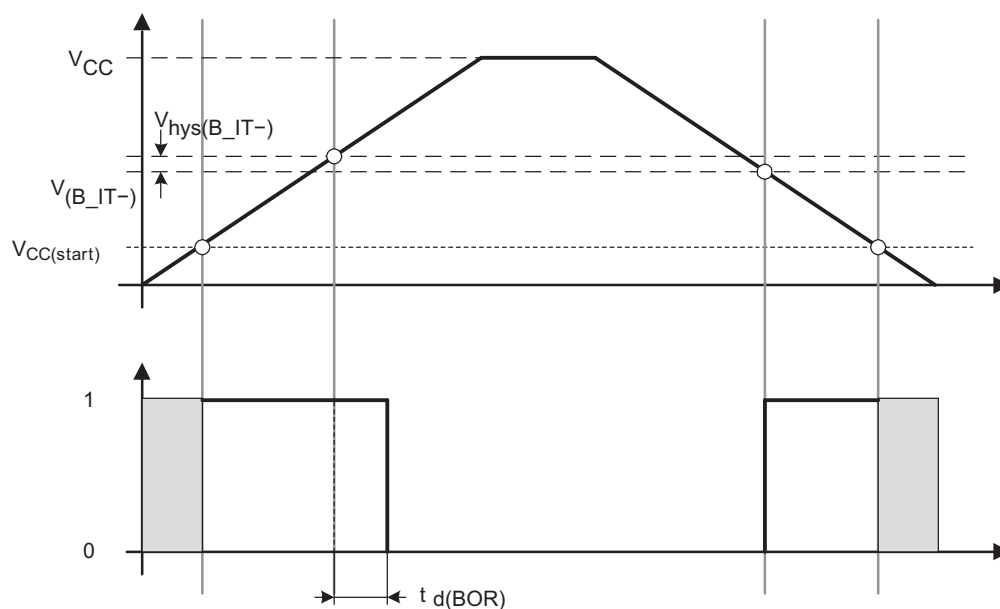
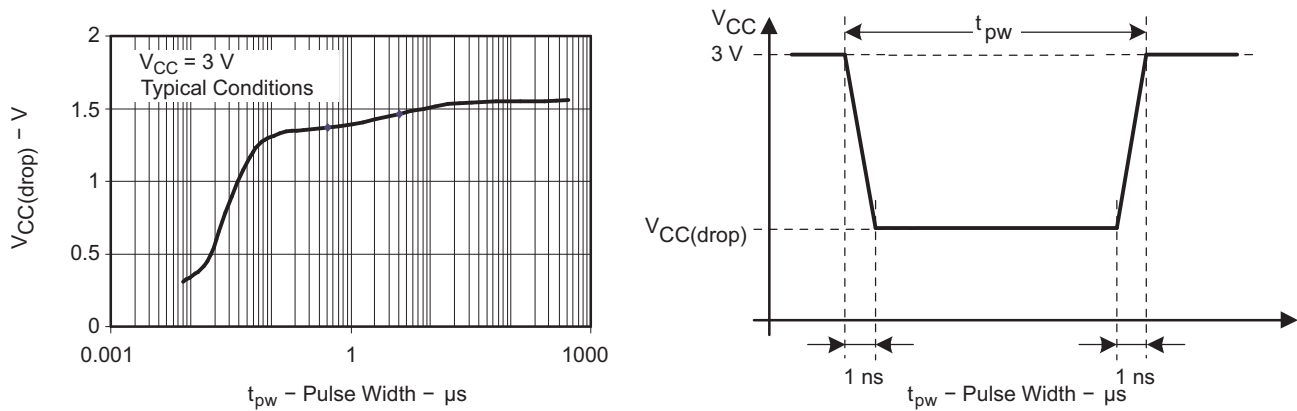


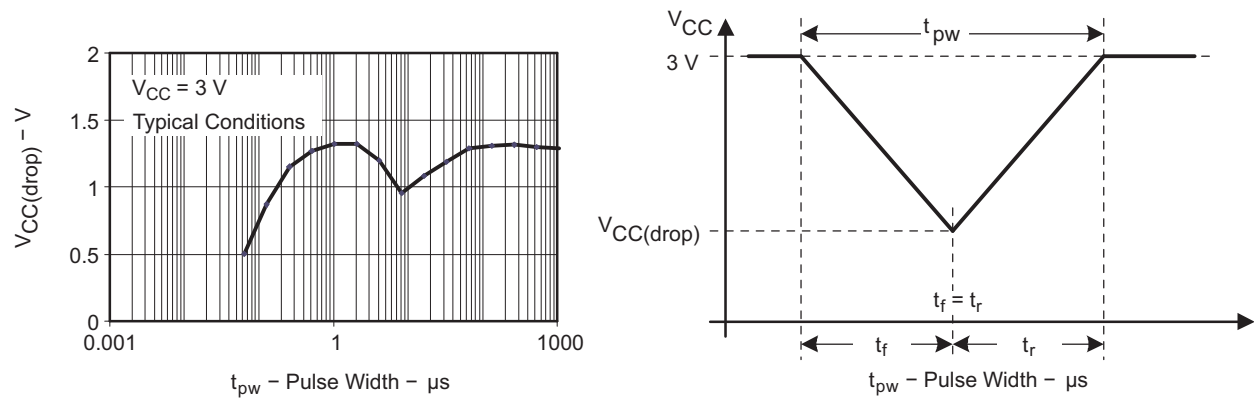
Figure 12. POR/Brownout Reset (BOR) vs Supply Voltage



## Typical Characteristics – POR/Brownout Reset (BOR)



**Figure 13.  $V_{CC(drop)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal**



**Figure 14.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**

## DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |  | TEST CONDITIONS                                      | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT  |
|------------------------|--|--|-----------------|------|------|------|-------|
| V <sub>CC</sub>        | Supply voltage                               | RSELx < 14   |                 | 1.8  |      | 3.6  | V     |
|                        |  | RSELx = 14   |                 | 2.2  |      | 3.6  | V     |
|                        |  | RSELx = 15   |                 | 3    |      | 3.6  | V     |
| f <sub>DCO(0,0)</sub>  | DCO frequency (0, 0)                         | RSELx = 0, DCOx = 0, MODx = 0                        | 3 V             | 0.06 |      | 0.14 | MHz   |
| f <sub>DCO(0,3)</sub>  | DCO frequency (0, 3)                         | RSELx = 0, DCOx = 3, MODx = 0                        | 3 V             | 0.07 |      | 0.17 | MHz   |
| f <sub>DCO(1,3)</sub>  | DCO frequency (1, 3)                         | RSELx = 1, DCOx = 3, MODx = 0                        | 3 V             |      | 0.15 |      | MHz   |
| f <sub>DCO(2,3)</sub>  | DCO frequency (2, 3)                         | RSELx = 2, DCOx = 3, MODx = 0                        | 3 V             |      | 0.21 |      | MHz   |
| f <sub>DCO(3,3)</sub>  | DCO frequency (3, 3)                         | RSELx = 3, DCOx = 3, MODx = 0                        | 3 V             |      | 0.30 |      | MHz   |
| f <sub>DCO(4,3)</sub>  | DCO frequency (4, 3)                         | RSELx = 4, DCOx = 3, MODx = 0                        | 3 V             |      | 0.41 |      | MHz   |
| f <sub>DCO(5,3)</sub>  | DCO frequency (5, 3)                         | RSELx = 5, DCOx = 3, MODx = 0                        | 3 V             |      | 0.58 |      | MHz   |
| f <sub>DCO(6,3)</sub>  | DCO frequency (6, 3)                         | RSELx = 6, DCOx = 3, MODx = 0                        | 3 V             | 0.54 |      | 1.06 | MHz   |
| f <sub>DCO(7,3)</sub>  | DCO frequency (7, 3)                         | RSELx = 7, DCOx = 3, MODx = 0                        | 3 V             | 0.80 |      | 1.50 | MHz   |
| f <sub>DCO(8,3)</sub>  | DCO frequency (8, 3)                         | RSELx = 8, DCOx = 3, MODx = 0                        | 3 V             |      | 1.6  |      | MHz   |
| f <sub>DCO(9,3)</sub>  | DCO frequency (9, 3)                         | RSELx = 9, DCOx = 3, MODx = 0                        | 3 V             |      | 2.3  |      | MHz   |
| f <sub>DCO(10,3)</sub> | DCO frequency (10, 3)                        | RSELx = 10, DCOx = 3, MODx = 0                       | 3 V             |      | 3.4  |      | MHz   |
| f <sub>DCO(11,3)</sub> | DCO frequency (11, 3)                        | RSELx = 11, DCOx = 3, MODx = 0                       | 3 V             |      | 4.25 |      | MHz   |
| f <sub>DCO(12,3)</sub> | DCO frequency (12, 3)                        | RSELx = 12, DCOx = 3, MODx = 0                       | 3 V             | 4.30 |      | 7.30 | MHz   |
| f <sub>DCO(13,3)</sub> | DCO frequency (13, 3)                        | RSELx = 13, DCOx = 3, MODx = 0                       | 3 V             | 6.00 |      | 9.60 | MHz   |
| f <sub>DCO(14,3)</sub> | DCO frequency (14, 3)                        | RSELx = 14, DCOx = 3, MODx = 0                       | 3 V             | 8.60 |      | 13.9 | MHz   |
| f <sub>DCO(15,3)</sub> | DCO frequency (15, 3)                        | RSELx = 15, DCOx = 3, MODx = 0                       | 3 V             | 12.0 |      | 18.5 | MHz   |
| f <sub>DCO(15,7)</sub> | DCO frequency (15, 7)                        | RSELx = 15, DCOx = 7, MODx = 0                       | 3 V             | 16.0 |      | 26.0 | MHz   |
| S <sub>RSEL</sub>      | Frequency step between range RSEL and RSEL+1 | $S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$ | 3 V             |      | 1.35 |      | ratio |
| S <sub>DCO</sub>       | Frequency step between tap DCO and DCO+1     | $S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$  | 3 V             |      | 1.08 |      | ratio |
| Duty cycle             |  | Measured at SMCLK output                             | 3 V             |      | 50   |      | %     |

## Calibrated DCO Frequencies – Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS  | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|--|--|----------------|-----------------|-----|------|-----|------|
| 1-MHz tolerance over temperature <sup>(1)</sup>  | BCSCTL1= CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>calibrated at 30°C and 3 V   | 0°C to 85°C    | 3 V             | -3  | ±0.5 | +3  | %    |
| 1-MHz tolerance over V <sub>CC</sub>             | BCSCTL1= CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>calibrated at 30°C and 3 V   | 30°C           | 1.8 V to 3.6 V  | -3  | ±2   | +3  | %    |
| 1-MHz tolerance overall                          | BCSCTL1= CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>calibrated at 30°C and 3 V   | -40°C to 85°C  | 1.8 V to 3.6 V  | -6  | ±3   | +6  | %    |
| 8-MHz tolerance over temperature <sup>(1)</sup>  | BCSCTL1= CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>calibrated at 30°C and 3 V   | 0°C to 85°C    | 3 V             | -3  | ±0.5 | +3  | %    |
| 8-MHz tolerance over V <sub>CC</sub>             | BCSCTL1= CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>calibrated at 30°C and 3 V   | 30°C           | 2.2 V to 3.6 V  | -3  | ±2   | +3  | %    |
| 8-MHz tolerance overall                          | BCSCTL1= CALBC1_8MHZ,<br>DCOCTL = CALDCO_8MHZ,<br>calibrated at 30°C and 3 V   | -40°C to 85°C  | 2.2 V to 3.6 V  | -6  | ±3   | +6  | %    |
| 12-MHz tolerance over temperature <sup>(1)</sup> | BCSCTL1= CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>calibrated at 30°C and 3 V | 0°C to 85°C    | 3 V             | -3  | ±0.5 | +3  | %    |
| 12-MHz tolerance over V <sub>CC</sub>            | BCSCTL1= CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>calibrated at 30°C and 3 V | 30°C           | 2.7 V to 3.6 V  | -3  | ±2   | +3  | %    |
| 12-MHz tolerance overall                         | BCSCTL1= CALBC1_12MHZ,<br>DCOCTL = CALDCO_12MHZ,<br>calibrated at 30°C and 3 V | -40°C to 85°C  | 2.7 V to 3.6 V  | -6  | ±3   | +6  | %    |
| 16-MHz tolerance over temperature <sup>(1)</sup> | BCSCTL1= CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>calibrated at 30°C and 3 V | 0°C to 85°C    | 3.3 V           | -3  | ±0.5 | +3  | %    |
| 16-MHz tolerance over V <sub>CC</sub>            | BCSCTL1= CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>calibrated at 30°C and 3 V | 30°C           | 3.3 V to 3.6 V  | -3  | ±2   | +3  | %    |
| 16-MHz tolerance overall                         | BCSCTL1= CALBC1_16MHZ,<br>DCOCTL = CALDCO_16MHZ,<br>calibrated at 30°C and 3 V | -40°C to 85°C  | 3.3 V to 3.6 V  | -6  | ±3   | +6  | %    |

(1) This is the frequency change from the measured frequency at 30°C over temperature.

## Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                   | V <sub>CC</sub>                                | MIN | TYP  | MAX | UNIT |
|-------------------------|---|--|-----|--|-----|------|
| t <sub>DCO,LPM3/4</sub> | DCO clock wake-up time from LPM3/4 <sup>(1)</sup> | BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ | 3 V | 1.5  |     | μs   |
| t <sub>CPU,LPM3/4</sub> | CPU wake-up time from LPM3/4 <sup>(2)</sup>       |  |     | 1/f <sub>MCLK</sub> +<br>t <sub>Clock,LPM3/4</sub> |     |      |

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).

(2) Parameter applicable only if DCOCLK is used for MCLK.

### Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

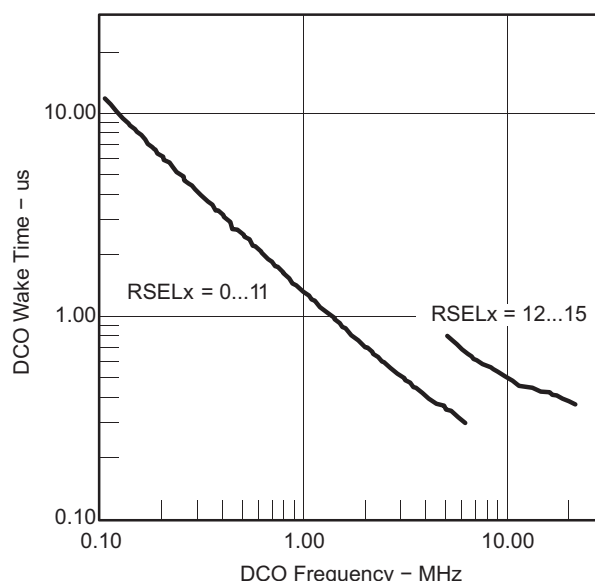


Figure 15. DCO Wake-Up Time From LPM3 vs DCO Frequency

## Crystal Oscillator, XT1, Low-Frequency Mode<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT |
|-----------------------------|---|--|-----------------|-------|-------|-------|------|
| f <sub>LFXT1,LF</sub>       | LFXT1 oscillator crystal frequency, LF mode 0, 1                  | XTS = 0, LFXT1Sx = 0 or 1  | 1.8 V to 3.6 V  | 32768 |       |       | Hz   |
| f <sub>LFXT1,LF,logic</sub> | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, XCAPx = 0, LFXT1Sx = 3  | 1.8 V to 3.6 V  | 10000 | 32768 | 50000 | Hz   |
| OA <sub>LF</sub>            | Oscillation allowance for LF crystals                             | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF  |                 | 500   |       |       | kΩ   |
|                             |   | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF |                 | 200   |       |       |      |
| C <sub>L,eff</sub>          | Integrated effective load capacitance, LF mode <sup>(2)</sup>     | XTS = 0, XCAPx = 0   |                 | 1     |       |       | pF   |
|                             |   | XTS = 0, XCAPx = 1   |                 | 5.5   |       |       |      |
|                             |   | XTS = 0, XCAPx = 2   |                 | 8.5   |       |       |      |
|                             |   | XTS = 0, XCAPx = 3   |                 | 11    |       |       |      |
| Duty cycle                  | LF mode   | XTS = 0, Measured at P2.0/ACLK, f <sub>LFXT1,LF</sub> = 32768 Hz                   | 2.2 V           | 30    | 50    | 70    | %    |
| f <sub>Fault,LF</sub>       | Oscillator fault frequency, LF mode <sup>(3)</sup>                | XTS = 0, XCAPx = 0, LFXT1Sx = 3 <sup>(4)</sup>                                     | 2.2 V           | 10    | 10000 |       | Hz   |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - (a) Keep the trace between the device and the crystal as short as possible.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

## Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|----------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub>                    | VLO frequency <sup>(1)</sup>       | -40°C to 85°C  | 3 V             | 4   | 12  | 20  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | -40°C to 85°C  | 3 V             |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | 25°C           | 1.8 V to 3.6 V  |     | 4   |     | %/V  |

- (1) Ensured by design on specified temperature.

## Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS               | V <sub>CC</sub>                 | MIN | TYP                 | MAX | UNIT |
|---------------------|-------------------------------|---------------------------------|-----|---------------------|-----|------|
| f <sub>TA</sub>     | Timer_A input clock frequency | SMCLK<br>Duty cycle = 50% ± 10% |     | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>TA,cap</sub> | Timer_A capture timing        | TA0, TA1                        | 3 V | 20                  |     | ns   |

## USI, Universal Serial Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                         | V <sub>CC</sub>  | MIN             | TYP                 | MAX                   | UNIT |
|---------------------|---|--|-----------------|---------------------|-----------------------|------|
| f <sub>USI</sub>    | USI module clock frequency              | External: SCLK,<br>Duty cycle = 50% ± 10%                |                 | f <sub>SYSTEM</sub> |                       | MHz  |
| f <sub>(SCLK)</sub> | Serial clock frequency, slave mode      | SPI slave mode   |                 |                     | 6                     | MHz  |
| V <sub>OL,I2C</sub> | Low-level output voltage on SDA and SCL | USI module in I2C mode,<br>I <sub>OL(max)</sub> = 1.5 mA | V <sub>SS</sub> |                     | V <sub>SS</sub> + 0.4 | V    |

### Typical Characteristics – USI Low-Level Output Voltage on SDA and SCL

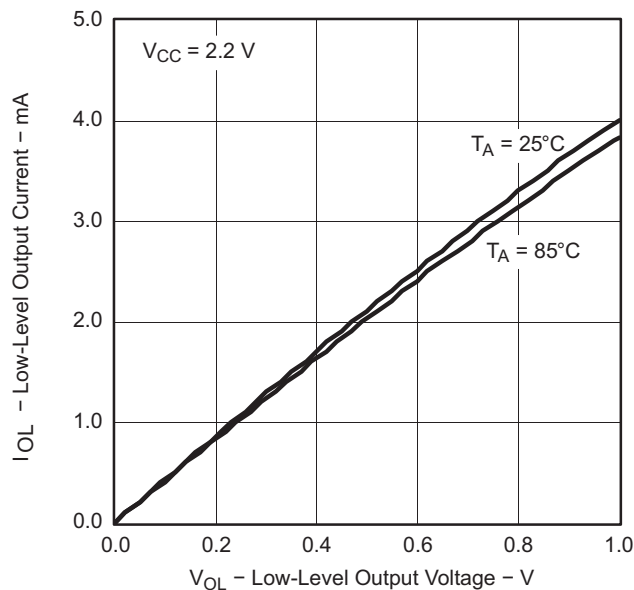


Figure 16. USI Low-Level Output Voltage vs Output Current

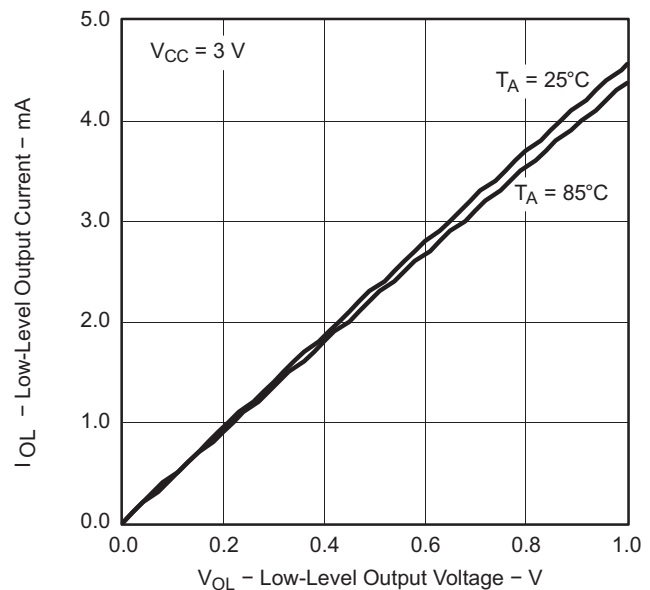


Figure 17. USI Low-Level Output Voltage vs Output Current

## Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                  | TEST CONDITIONS                                     | V <sub>CC</sub>       | MIN             | TYP             | MAX | UNIT             |
|----------------------------|---|-----------------------|-----------------|-----------------|-----|------------------|
| V <sub>CC(PGM/ERASE)</sub> | Program and erase supply voltage                    |                       | 2.2             |                 | 3.6 | V                |
| f <sub>FTG</sub>           | Flash timing generator frequency                    |                       | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub>           | Supply current from V <sub>CC</sub> during program  | 2.2 V, 3.6 V          |                 | 1               | 5   | mA               |
| I <sub>ERASE</sub>         | Supply current from V <sub>CC</sub> during erase    | 2.2 V, 3.6 V          |                 | 1               | 7   | mA               |
| t <sub>CPT</sub>           | Cumulative program time <sup>(1)</sup>              | 2.2 V, 3.6 V          |                 |                 | 10  | ms               |
| t <sub>CMErase</sub>       | Cumulative mass erase time                          | 2.2 V, 3.6 V          | 20              |                 |     | ms               |
|                            | Program and erase endurance                         |                       | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub>     | Data retention duration                             | T <sub>J</sub> = 25°C | 100             |                 |     | years            |
| t <sub>Word</sub>          | Word or byte program time                           | See <sup>(2)</sup>    |                 | 30              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub>      | Block program time for first byte or word           | See <sup>(2)</sup>    |                 | 25              |     | t <sub>FTG</sub> |
| t <sub>Block, 1-63</sub>   | Block program time for each additional byte or word | See <sup>(2)</sup>    |                 | 18              |     | t <sub>FTG</sub> |
| t <sub>Block, End</sub>    | Block program end-sequence wait time                | See <sup>(2)</sup>    |                 | 6               |     | t <sub>FTG</sub> |
| t <sub>Mass Erase</sub>    | Mass erase time                                     | See <sup>(2)</sup>    |                 | 10593           |     | t <sub>FTG</sub> |

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write mode and block write mode.

(2) These values are hardwired into the flash controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).

## Flash Memory (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                    | TEST CONDITIONS    | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT             |
|------------------------|--------------------|--------------------|-----------------|-----|------|-----|------------------|
| t <sub>Seg Erase</sub> | Segment erase time | See <sup>(2)</sup> |                 |     | 4819 |     | t <sub>FTG</sub> |

## RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS | MIN | MAX | UNIT |
|--|-----------------|-----|-----|------|
| $V_{(RAMh)}$ RAM retention supply voltage <sup>(1)</sup> | CPU halted      | 1.6 |     | V    |

- (1) This parameter defines the minimum supply voltage  $V_{CC}$  when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

## JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS | $V_{CC}$ | MIN   | TYP | MAX | UNIT       |
|--|-----------------|----------|-------|-----|-----|------------|
| $f_{SBW}$ Spy-Bi-Wire input frequency  |                 | 2.2 V    | 0     |     | 20  | MHz        |
| $t_{SBW,Low}$ Spy-Bi-Wire low clock pulse length   |                 | 2.2 V    | 0.025 |     | 15  | $\mu s$    |
| $t_{SBW,En}$ Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge <sup>(1)</sup> ) |                 | 2.2 V    |       |     | 1   | $\mu s$    |
| $t_{SBW,Ret}$ Spy-Bi-Wire return to normal operation time  |                 | 2.2 V    | 15    |     | 100 | $\mu s$    |
| $f_{TCK}$ TCK input frequency <sup>(2)</sup>   |                 | 2.2 V    | 0     |     | 5   | MHz        |
| $R_{Internal}$ Internal pulldown resistance on TEST  |                 | 2.2 V    | 25    | 60  | 90  | k $\Omega$ |

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum  $t_{SBW,En}$  time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
- (2)  $f_{TCK}$  may be restricted to meet the timing requirements of the module selected.

## JTAG Fuse <sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

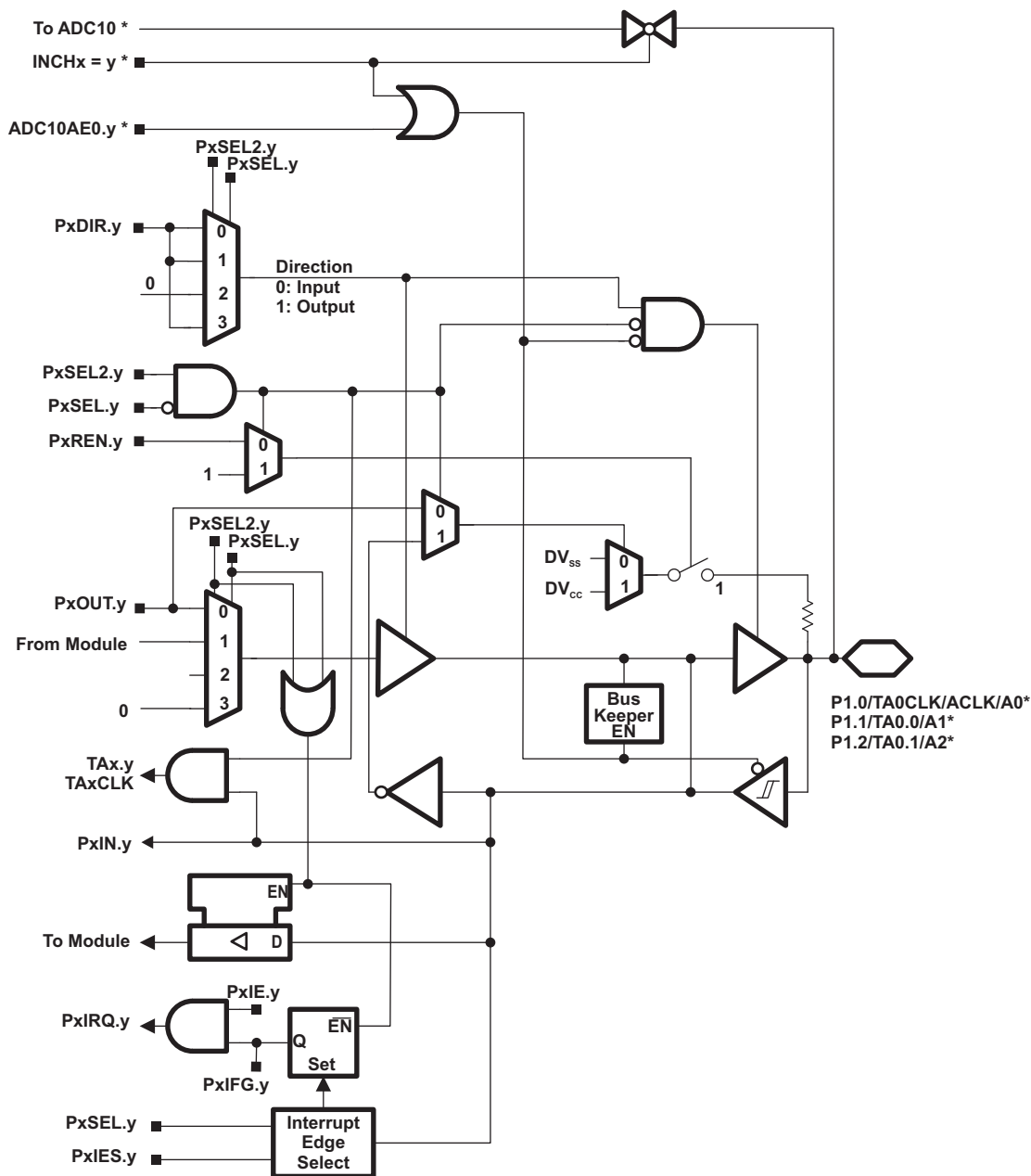
| PARAMETER  | TEST CONDITIONS    | MIN | MAX | UNIT |
|--|--------------------|-----|-----|------|
| $V_{CC(FB)}$ Supply voltage during fuse-blow condition | $T_A = 25^\circ C$ | 2.5 |     | V    |
| $V_{FB}$ Voltage level on TEST for fuse blow           |                    | 6   | 7   | V    |
| $I_{FB}$ Supply current into TEST during fuse blow     |                    |     | 100 | mA   |
| $t_{FB}$ Time to blow fuse                             |                    |     | 1   | ms   |

- (1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.



## PIN SCHEMATICS

### Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger



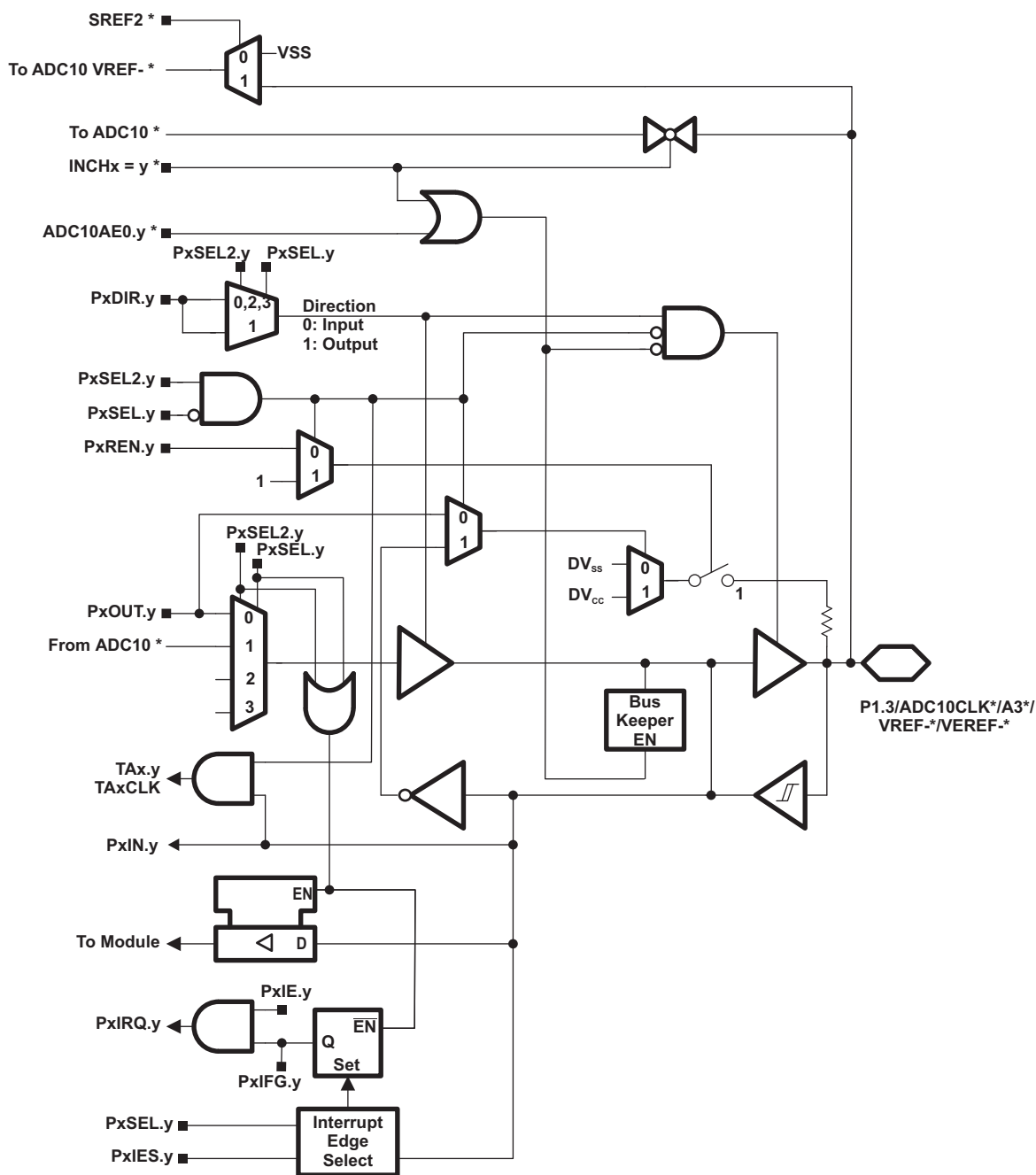
\* Note: MSP430G2x32 devices only. MSP430G2x02 devices have no ADC10.

**Table 15. Port P1 (P1.0 to P1.2) Pin Functions**

| PIN NAME (P1.x)                      | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |         |          |
|--------------------------------------|---|--------------------|---------------------------------------|---------|----------|
|                                      |   |                    | P1DIR.x                               | P1SEL.x | P1SEL2.x |
| P1.0/<br>TA0CLK/<br>ACLK/<br>Pin Osc | 0 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        |
|                                      |   | TA0.TACLK          | 0                                     | 1       | 0        |
|                                      |   | ACLK               | 1                                     | 1       | 0        |
|                                      |   | Capacitive sensing | x                                     | 0       | 1        |
| P1.1/<br>TA0.0/<br>Pin Osc           | 1 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        |
|                                      |   | TA0.0              | 1                                     | 1       | 0        |
|                                      |   | TA0.CCI0A          | 0                                     | 1       | 0        |
|                                      |   | Capacitive sensing | X                                     | 0       | 1        |
| P1.2/<br>TA0.1/<br>Pin Osc           | 2 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        |
|                                      |   | TA0.1              | 1                                     | 1       | 0        |
|                                      |   | TA0.CCI1A          | 0                                     | 1       | 0        |
|                                      |   | Capacitive sensing | X                                     | 0       | 1        |

(1) X = don't care

## Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger



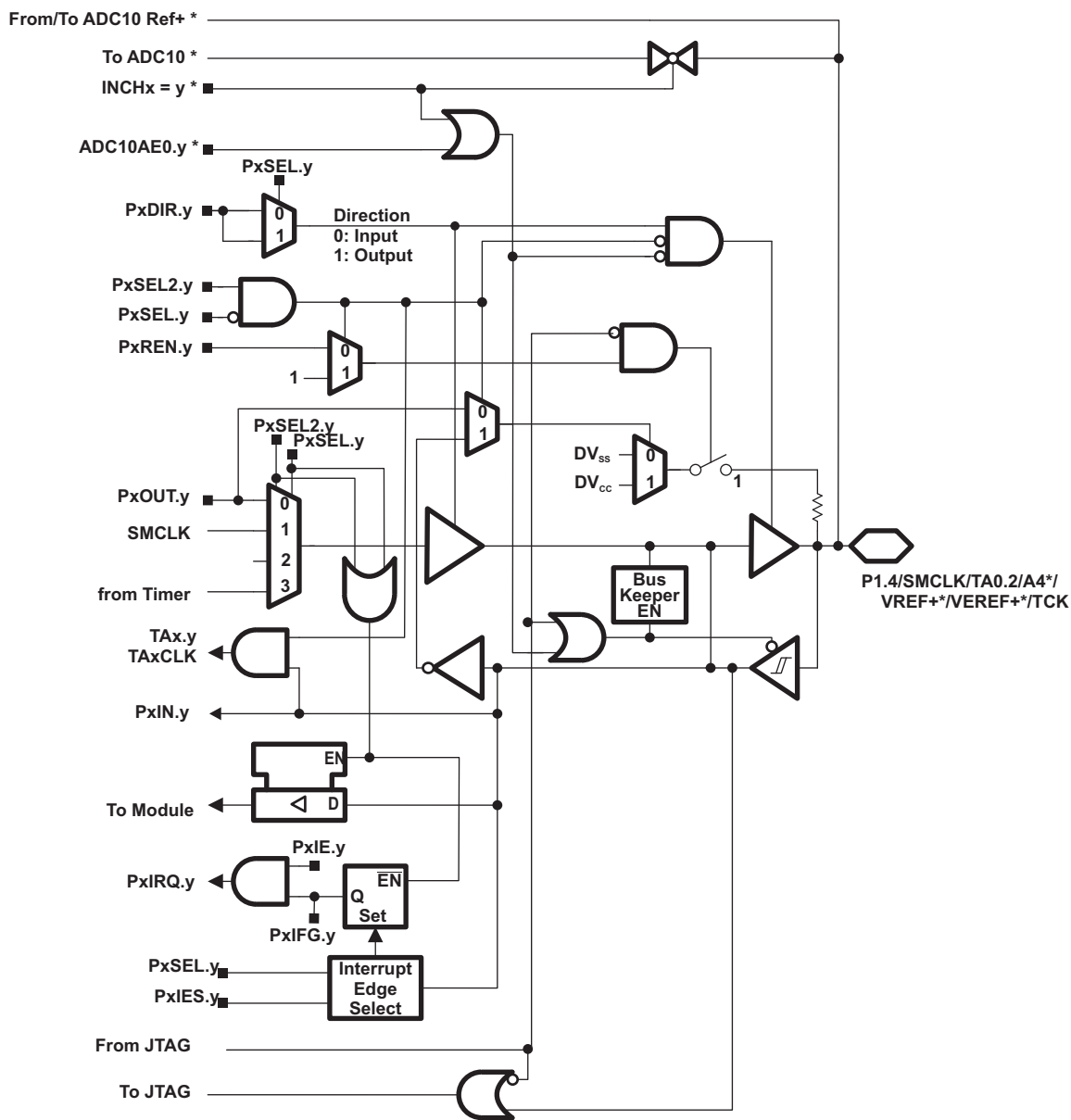
\* Note: MSP430G2x32 devices only. MSP430G2x02 devices have no ADC10.

**Table 16. Port P1 (P1.3) Pin Functions**

| PIN NAME<br>(P1.x)  | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |         |          |                         |
|---|---|--------------------|---------------------------------------|---------|----------|-------------------------|
|   |   |                    | P1DIR.x                               | P1SEL.x | P1SEL2.x | ADC10AE.x<br>(INCH.x=1) |
| P1.3/<br>ADC10CLK/<br>A3/<br>VREF-/<br>VEREF-/<br>Pin Osc | 3 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        | 0                       |
|   |   | ADC10CLK           | 1                                     | 1       | 0        | 0                       |
|   |   | A3                 | X                                     | X       | X        | 1 (y = 3)               |
|   |   | VREF-              | X                                     | X       | X        | 1                       |
|   |   | VEREF-             | X                                     | X       | X        | 1                       |
|   |   | Capacitive sensing | X                                     | 0       | 1        | 0                       |

(1) X = don't care

## Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger



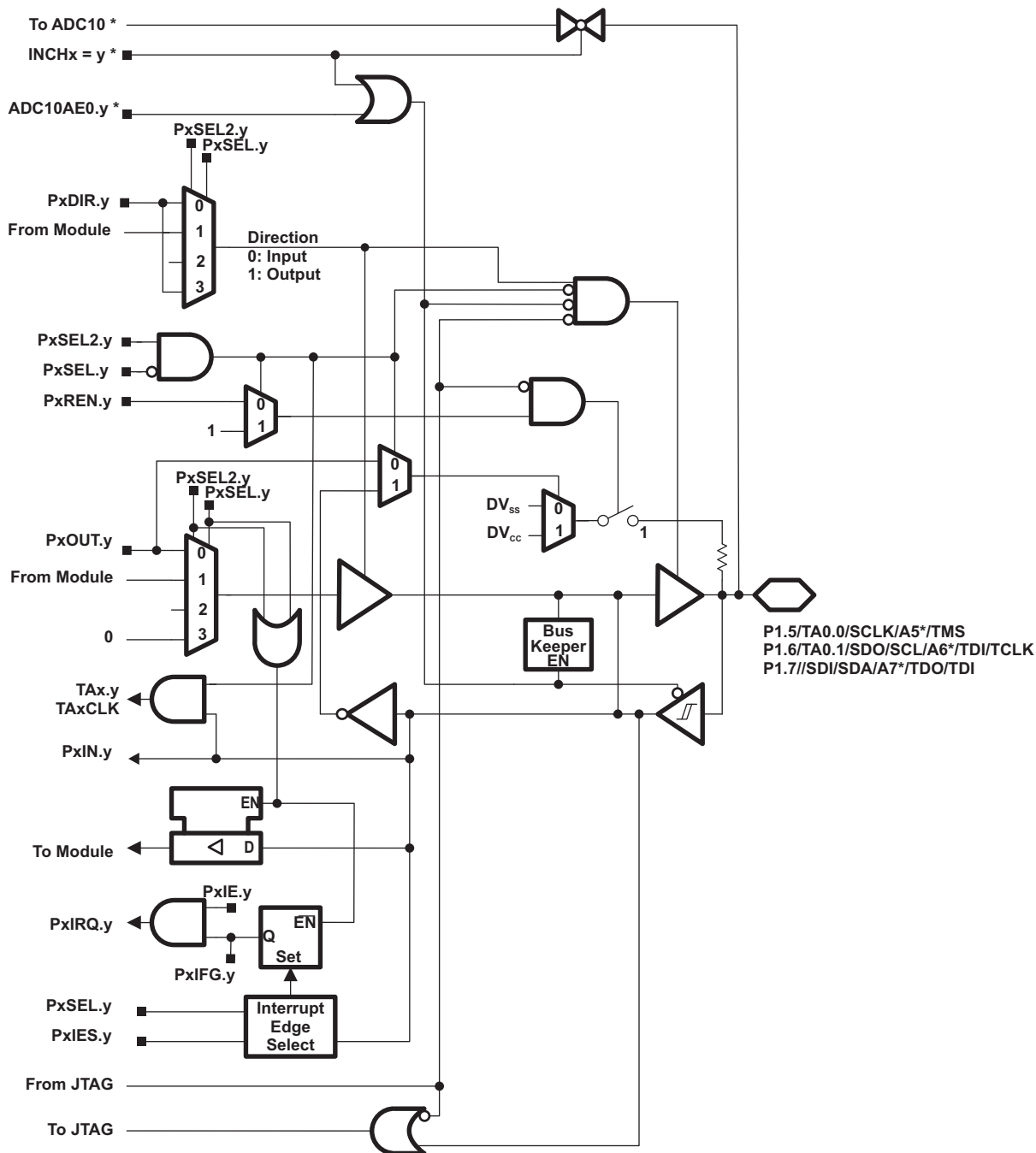
\* Note: MSP430G2x32 devices only. MSP430G2x02 devices have no ADC10.

**Table 17. Port P1 (P1.4) Pin Functions**

| PIN NAME (P1.x)                             | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |         |          |                         |           |
|---|---|--------------------|---------------------------------------|---------|----------|-------------------------|-----------|
|   |   |                    | P1DIR.x                               | P1SEL.x | P1SEL2.x | ADC10AE.x<br>(INCH.x=1) | JTAG Mode |
| P1.4/<br>SMCLK/<br>TA0.2/                   | 4 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        | 0                       | 0         |
|   |   | SMCLK              | 1                                     | 1       | 0        | 0                       | 0         |
|   |   | TA0.2              | 1                                     | 1       | 1        | 0                       | 0         |
|   |   | TA0.CCI2A          | 0                                     | 1       | 1        | 0                       | 0         |
| VREF+/<br>VEREF+/<br>A4/<br>TCK/<br>Pin Osc |   | VREF+              | X                                     | X       | X        | 1                       | 0         |
|   |   | VEREF+             | X                                     | X       | X        | 1                       | 0         |
|   |   | A4                 | X                                     | X       | X        | 1 (y = 4)               | 0         |
|   |   | TCK                | X                                     | X       | X        | 0                       | 1         |
|   |   | Capacitive sensing | X                                     | 0       | 1        | 0                       | 0         |

(1) X = don't care

## Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger



\* Note: MSP430G2x32 devices only. MSP430G2x02 devices have no ADC10.

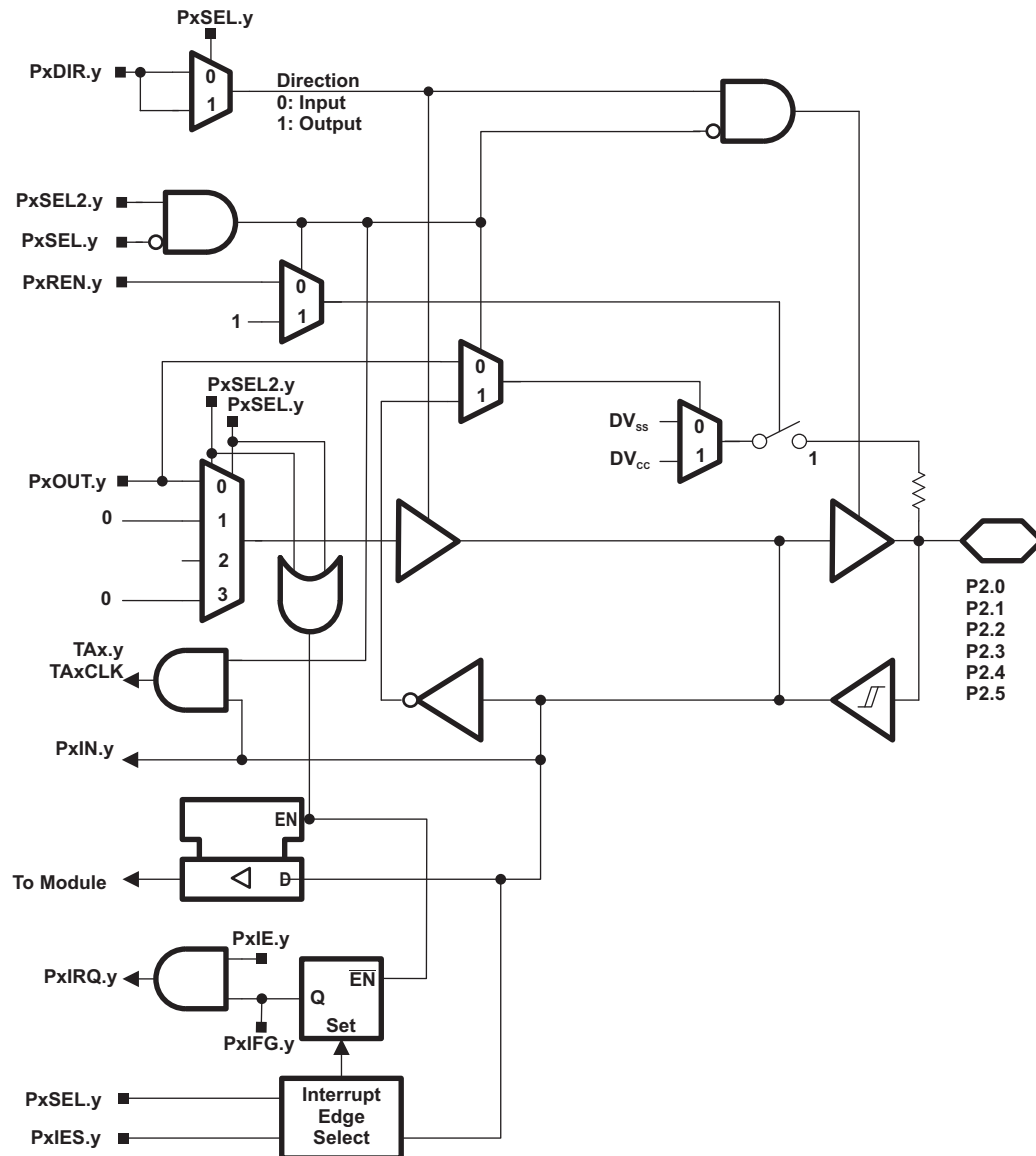
**Table 18. Port P1 (P1.5 to P1.7) Pin Functions**

| PIN NAME<br>(P1.x)   | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |         |          |        |           |                         |
|--|---|--------------------|---------------------------------------|---------|----------|--------|-----------|-------------------------|
|  |   |                    | P1DIR.x                               | P1SEL.x | P1SEL2.x | USIP.x | JTAG Mode | ADC10AE.x<br>(INCH.x=1) |
| P1.5/<br>TA0.0/<br>SCLK/<br>A5/<br>TMS/<br>Pin Osc             | 5 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        | 0      | 0         | 0                       |
|  |   | TA0.0              | 1                                     | 1       | 0        | 0      | 0         | 0                       |
|  |   | SPI mode           | from USI                              | 1       | 0        | 1      | 0         | 0                       |
|  |   | A5                 | X                                     | X       | X        | 0      | 0         | 1 (y = 5)               |
|  |   | TMS                | X                                     | X       | X        | 0      | 1         | 0                       |
|  |   | Capacitive sensing | X                                     | 0       | 1        | 0      | 0         | 0                       |
| P1.6/<br>TA0.1/<br>SDO/<br>SCL/<br>A6/<br>TDI/TCLK/<br>Pin Osc | 6 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        | 0      | 0         | 0                       |
|  |   | TA0.1              | 1                                     | 1       | 0        | 0      | 0         | 0                       |
|  |   | SPI mode           | from USI                              | 1       | 0        | !      | 0         | 0                       |
|  |   | I2C mode           | from USI                              | 1       | 0        | !      | 0         | 0                       |
|  |   | A6                 | X                                     | X       | X        | 0      | 0         | 1 (y = 6)               |
|  |   | TDI/TCLK           | X                                     | X       | X        | 0      | 1         | 0                       |
|  |   | Capacitive sensing | X                                     | 0       | 1        | 0      | 0         | 0                       |
| P1.7/<br>SDI/<br>SDA/<br>A7/<br>TDO/TDI/<br>Pin Osc            | 7 | P1.x (I/O)         | I: 0; O: 1                            | 0       | 0        | 0      | 0         | 0                       |
|  |   | SPI mode           | from USI                              | 1       | 0        | 1      | 0         | 0                       |
|  |   | SPI mode           | from USI                              | 1       | 0        | 1      | 0         | 0                       |
|  |   | A7                 | X                                     | X       | X        | 0      | 0         | 1 (y = 7)               |
|  |   | TDO/TDI            | X                                     | X       | X        | 0      | 1         | 0                       |
|  |   | Capacitive sensing | X                                     | 0       | 1        | 0      | 0         | 0                       |

(1) X = don't care



### Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger



**Table 19. Port P2 (P2.0 to P2.5) Pin Functions**

| PIN NAME<br>(P2.x) | x | FUNCTION                         | CONTROL BITS / SIGNALS <sup>(1)</sup> |         |          |
|--------------------|---|----------------------------------|---------------------------------------|---------|----------|
|                    |   |                                  | P2DIR.x                               | P2SEL.x | P2SEL2.x |
| P2.0/<br>Pin Osc   | 0 | P2.x (I/O)<br>Capacitive sensing | I: 0; O: 1<br>X                       | 0<br>0  | 0<br>1   |
| P2.1/<br>Pin Osc   | 1 | P2.x (I/O)<br>Capacitive sensing | I: 0; O: 1<br>X                       | 0<br>0  | 0<br>1   |
| P2.2/<br>Pin Osc   | 2 | P2.x (I/O)<br>Capacitive sensing | I: 0; O: 1<br>X                       | 0<br>0  | 0<br>1   |
| P2.3/<br>Pin Osc   | 3 | P2.x (I/O)<br>Capacitive sensing | I: 0; O: 1<br>X                       | 0<br>0  | 0<br>1   |
| P2.4/<br>Pin Osc   | 4 | P2.x (I/O)<br>Capacitive sensing | I: 0; O: 1<br>X                       | 0<br>0  | 0<br>1   |
| P2.5/<br>Pin Osc   | 5 | P2.x (I/O)<br>Capacitive sensing | I: 0; O: 1<br>X                       | 0<br>0  | 0<br>1   |

(1) X = don't care

## Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

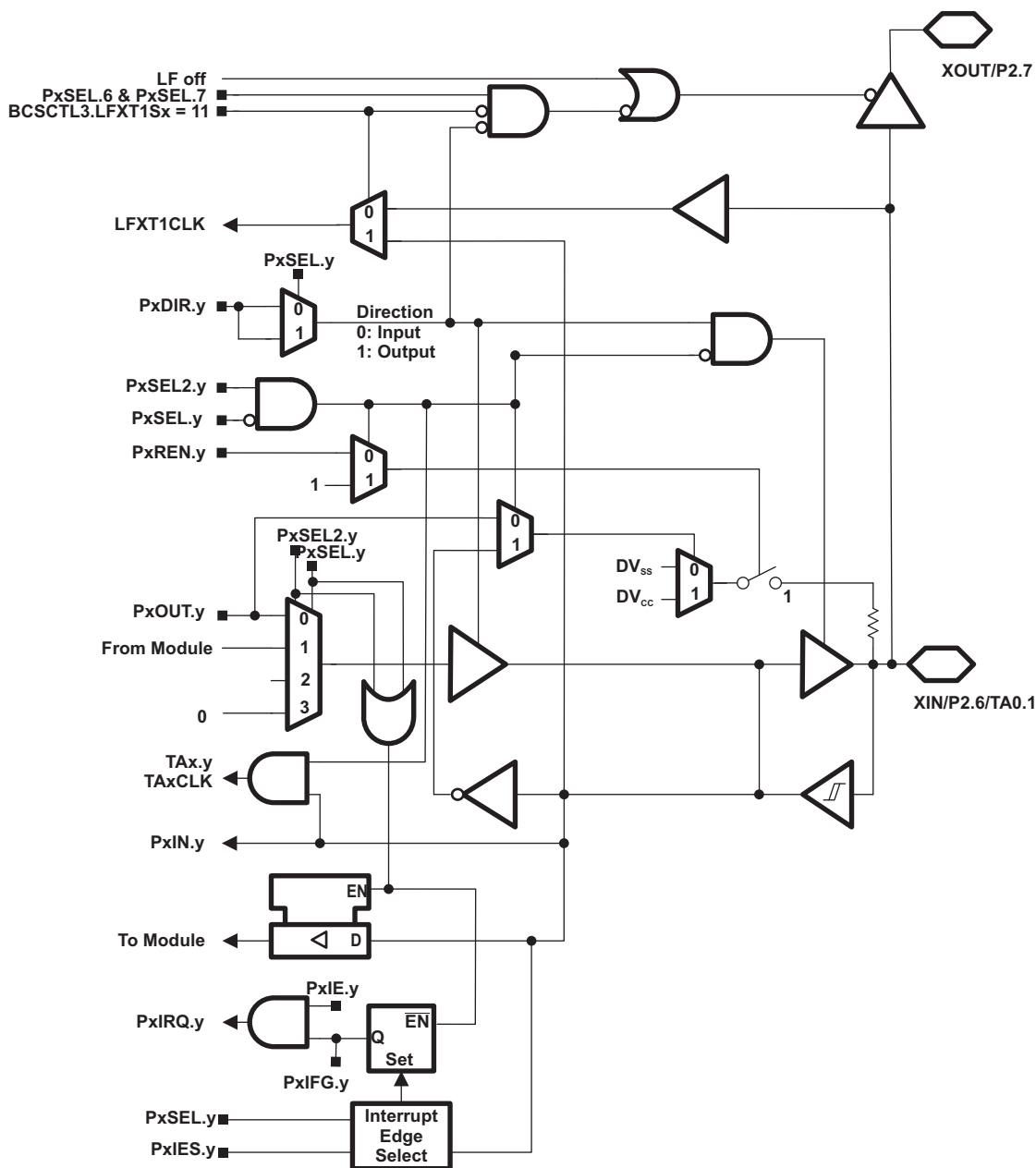
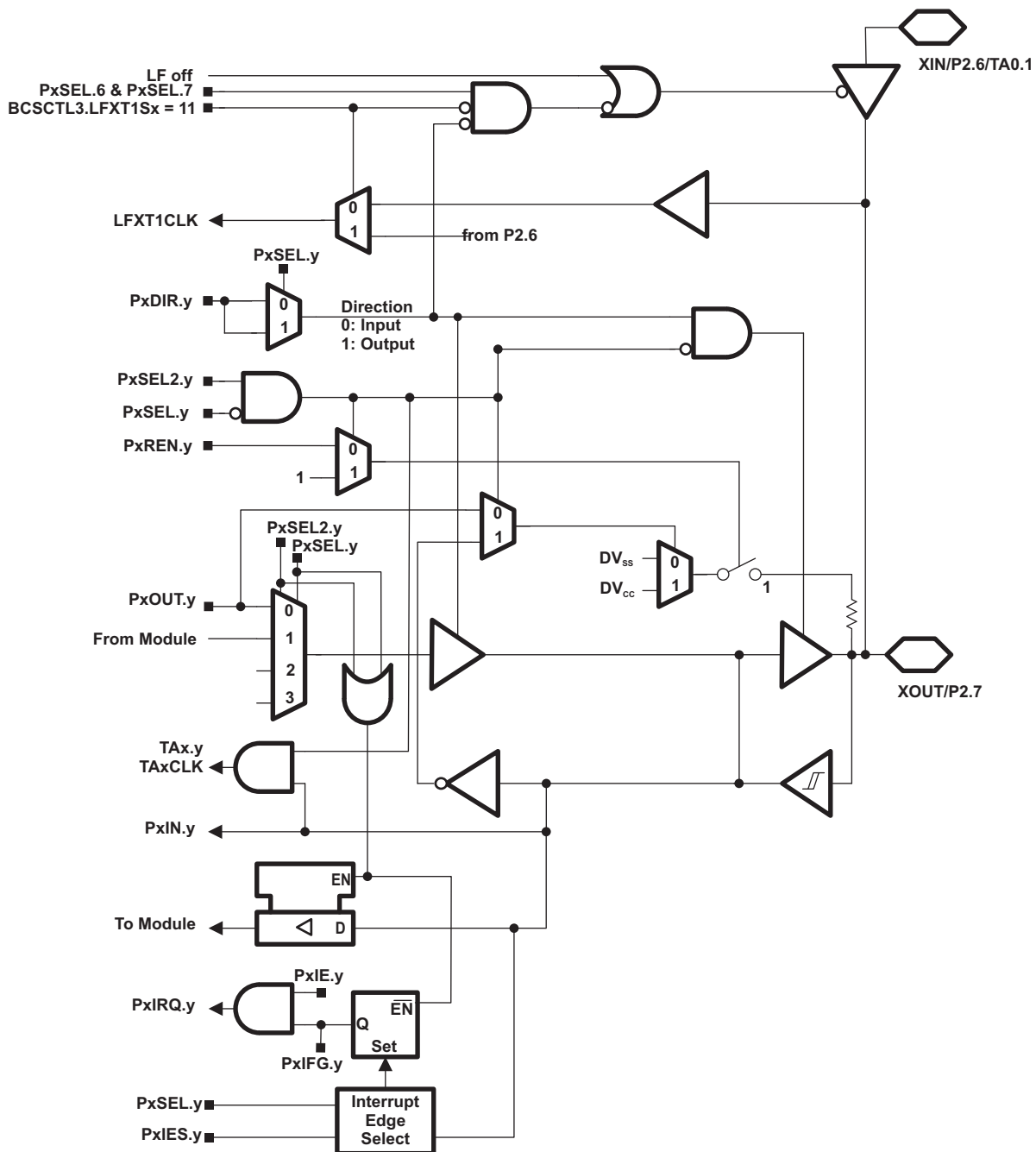


Table 20. Port P2 (P2.6) Pin Functions

| PIN NAME<br>(P2.x) | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |                    |                      |
|--------------------|---|--------------------|---------------------------------------|--------------------|----------------------|
|                    |   |                    | P2DIR.x                               | P2SEL.6<br>P2SEL.7 | P2SEL2.6<br>P2SEL2.7 |
| XIN/               | 6 | XIN                | 0                                     | 1<br>1             | 0<br>0               |
| P2.6/              |   | P2.x (I/O)         | I: 0; O: 1                            | 0<br>X             | 0<br>0               |
| TA0.1/             |   | Timer0_A3.TA1      | 1                                     | 1<br>0             | 0<br>0               |
| Pin Osc            |   | Capacitive sensing | X                                     | 0<br>X             | 1<br>X               |

(1) X = don't care

## Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger



**Table 21. Port P2 (P2.7) Pin Functions**

| PIN NAME<br>(P2.x) | x | FUNCTION           | CONTROL BITS / SIGNALS <sup>(1)</sup> |                    |                      |
|--------------------|---|--------------------|---------------------------------------|--------------------|----------------------|
|                    |   |                    | P2DIR.x                               | P2SEL.6<br>P2SEL.7 | P2SEL2.6<br>P2SEL2.7 |
| XOUT/              |   | XOUT               | X                                     | 1<br>1             | 0<br>0               |
| P2.7/              | 7 | P2.x (I/O)         | I: 0; O: 1                            | X<br>0             | 0<br>0               |
| Pin Osc            |   | Capacitive sensing | X                                     | X<br>0             | X<br>1               |

(1) X = don't care

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430G2302IPW1EP</a>  | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2302EP             |
| MSP430G2302IPW1EP.A                | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2302EP             |
| <a href="#">MSP430G2302IPW1REP</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2302EP             |
| MSP430G2302IPW1REP.A               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2302EP             |
| <a href="#">V62/12623-01XE</a>     | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2302EP             |
| <a href="#">V62/12623-01XE-T</a>   | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2302EP             |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF MSP430G2302-EP :**

- Catalog : [MSP430G2302](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430G2302IPW1REP | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430G2302IPW1REP | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |



## TUBE



\*All dimensions are nominal

| Device              | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MSP430G2302IPW1EP   | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| MSP430G2302IPW1EP.A | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| V62/12623-01XE-T    | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |



4220202/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

**PW0014A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月