# MSP430FR5739-EP 混合信号微控制器

## 1 器件概述

### 1.1 特性

- 嵌入式微控制器
  - 时钟频率高达 24MHz 的 16 位精简指令集 (RISC) 架构
  - 宽电源电压范围（2V 至 3.6V）
  - 工作温度范围 -55°C 至 85°C
- 经优化超低功率模式
  - 激活模式：81.4µA/MHz（典型值）
  - 待机（具有 VLO 的 LPM3）：6.3µA（典型值）
  - 实时时钟（具有晶振的 LPM3.5）：1.5µA（典型值）
  - 关断 (LPM4.5)：0.32µA（典型值）
- 超低功率铁电 RAM (FRAM)
  - 高达 16KB 的非易失性存储器
  - 超低功率写入
  - 125ns 每个字的快速写入（1ms 内写入 16KB）
  - 内置纠错编码 (ECC) 和存储器保护单元 (MPU)
  - 通用内存 = 程序 + 数据 + 存储
  - $10^{15}$ 写入周期持耐久性
  - 抗辐射和非磁性
- 智能数字外设
  - 32 位硬件乘法器 (MPY)
  - 3 通道内部直接存储器访问 (DMA)
  - 具有日历和报警功能的实时时钟 (RTC)
  - 5 个具有多达 3 个捕捉/比较寄存器的 16 位定时器
  - 16 位循环冗余校验器 (CRC)
- 高性能模拟
  - 支持电压基准和可编程滞后的 16 通道模拟比较器
  - 具有内部基准、采样与保持功能的 14 通道、10 位模数转换器
    - 在流耗为 100µA 时为 200ksps
- 增强型串行通信
  - eUSCI_A0 和 eUSCI_A1 支持：
    - 支持自动波特率侦测的通用异步收发器 (UART)
    - IrDA 编码和解码
    - 速率高达 10Mbps 的串行外设接口 (SPI)
  - eUSCI_B0 支持：
    - 支持多个从器件寻址的 $I^2C$
    - 速率高达 10Mbps 的串行外设接口 (SPI)
  - 硬件通用异步收发器 (UART) 引导加载程序 (BSL)
- 电源管理系统
  - 完全集成的低压降稳压器 (LDO)
  - 具有复位功能的内核与电源电压监控器
  - 常开模式的零功率欠压检测
  - 无需外部电压的串行板上程序设计
- 灵活的时钟系统
  - 具有 6 个可选出厂校准频率的固定频率数控振荡器 (DCO)（视器件而定）
  - 低功率低频内部时钟源 (VLO)
  - 32kHz 晶振 (LFXT)
  - 高频晶振 (HFXT)
- 开发工具和软件
  - 免费专业开发环境 ( Code Composer Studio ™ IDE)
  - 低成本全功能套件 ()
  - 完全开发套件(MSP-FET430U40A)
  - 目标板 (MSP-TS430RHA40A)
- 系列产品成员
  - 在 中汇总的变量和可用封装
  - 如需了解完整的模块说明, 请查阅 *《MSP430FR57xx 系列用户指南》* (SLAU272)
- 支持国防、航天和医疗应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 支持扩展温度范围（-55°C 至 85°C）（一些注释的参数仅支持 –40°C 至 85°C）
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

## 1.2 应用范围

- 家庭自动化
- 安全性
- 传感器管理
- 数据采集

**注意事项** 这些产品采用 FRAM 非易失性存储器技术。 FRAM 保持对于极端温度环境敏感，例如那些回流焊接或者手工焊接时产生的温度。 更多信息，请参见 *最大绝对额定值*。

**注意事项** 必须采用与器件级 ESD 规范兼容的系统级 ESD 保护以防止电气过载或者数据或代码内存的干扰。 要获得更多信息，请参阅应用报告 《*MSP430™ 系统级 ESD 注意事项*》 (SLAA530)

## 1.3 说明

德州仪器 (TI) 573MSP430FRx 系列超低功率微控制器包含多个器件，该系列器件具有嵌入式 FRAM 非易失性存储器，超低功率 16 位 MSP430™ CPU，以及针对多种应用的不同外设。 此架构，FRAM，和外设，与 7 种低功率模式组合在一起，针对在便携式和无线感测应用中实现延长电池寿命进行了优化。 FRAM 是一款全新的非易失性存储器，此存储器将 SRAM 的速度，灵活性，和耐久性与闪存的稳定性和可靠性结合在一起，总体能耗更低。 其外设包括：1 个 10 位模数转换器 (ADC)、1 个具有基准电压生成和滞后功能的 16 通道比较器、3 个支持 $I^2C$、SPI 或 UART 协议的增强型串行通道、1 个内部直接存储器访问 (DMA)、1 个硬件乘法器、1 个实时时钟 (RTC)、5 个 16 位定时器和数字 I/O。

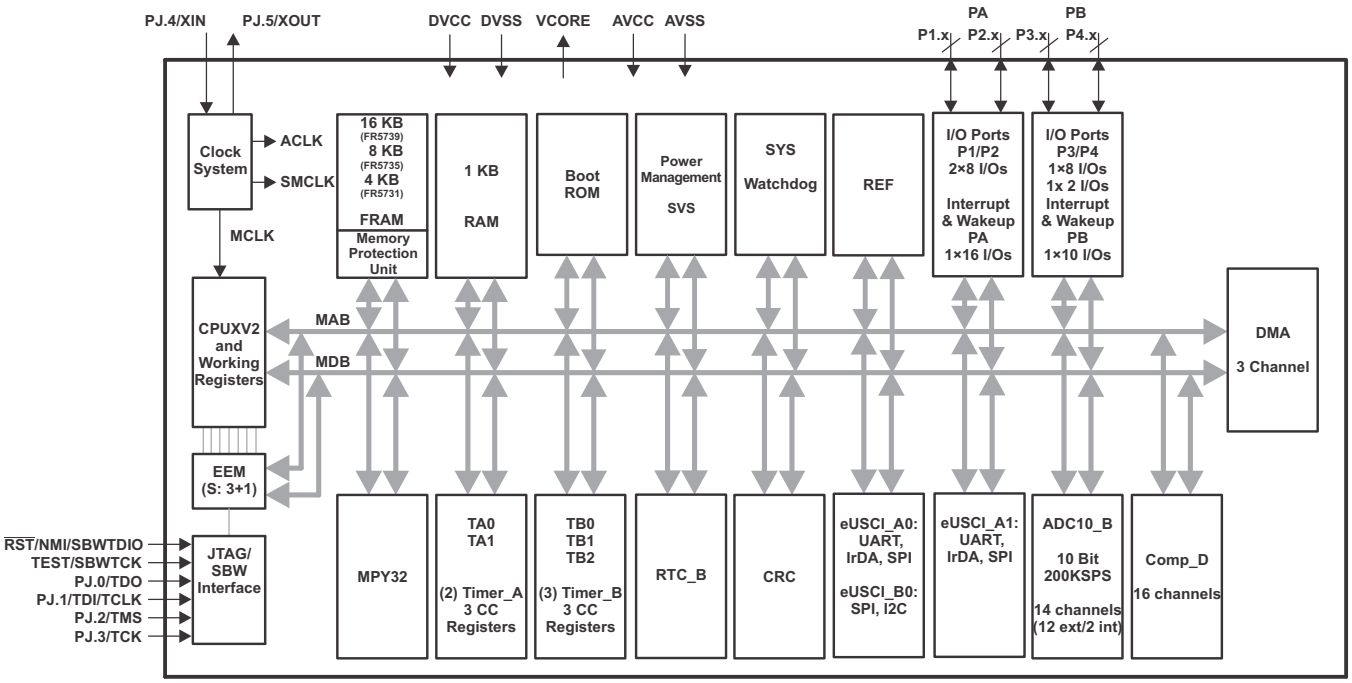
器件信息(1)

| 器件型号 | 封装 | 封装尺寸(2) |
|---|---|---|
| MSP430FR5739-EP | VQFN (40) | 6.00mm x 6.00mm |

(1) 要获得最新的产品、封装和订购信息，请参见 节 9 中的封装选项附录，或者浏览 TI 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。 要获得包含容差值的封装尺寸，请参见 节 9中的机械数据。

## 1.4 功能框图

本节给出了 MSP430FR5739 器件采用 RHA 封装时的功能框图。



# 内容

## 2 修订历史记录

| Changes from Original (November 2014) to Revision A | Page |
|---|---|
| • 器件状态更新为生产数据 | 1 |

# 3 Pin Configuration and Functions

## 3.1 Pin Diagram

Figure 3-1 shows the pin diagram for the MSP430FR5739-EP device in the 40-pin RHA package.

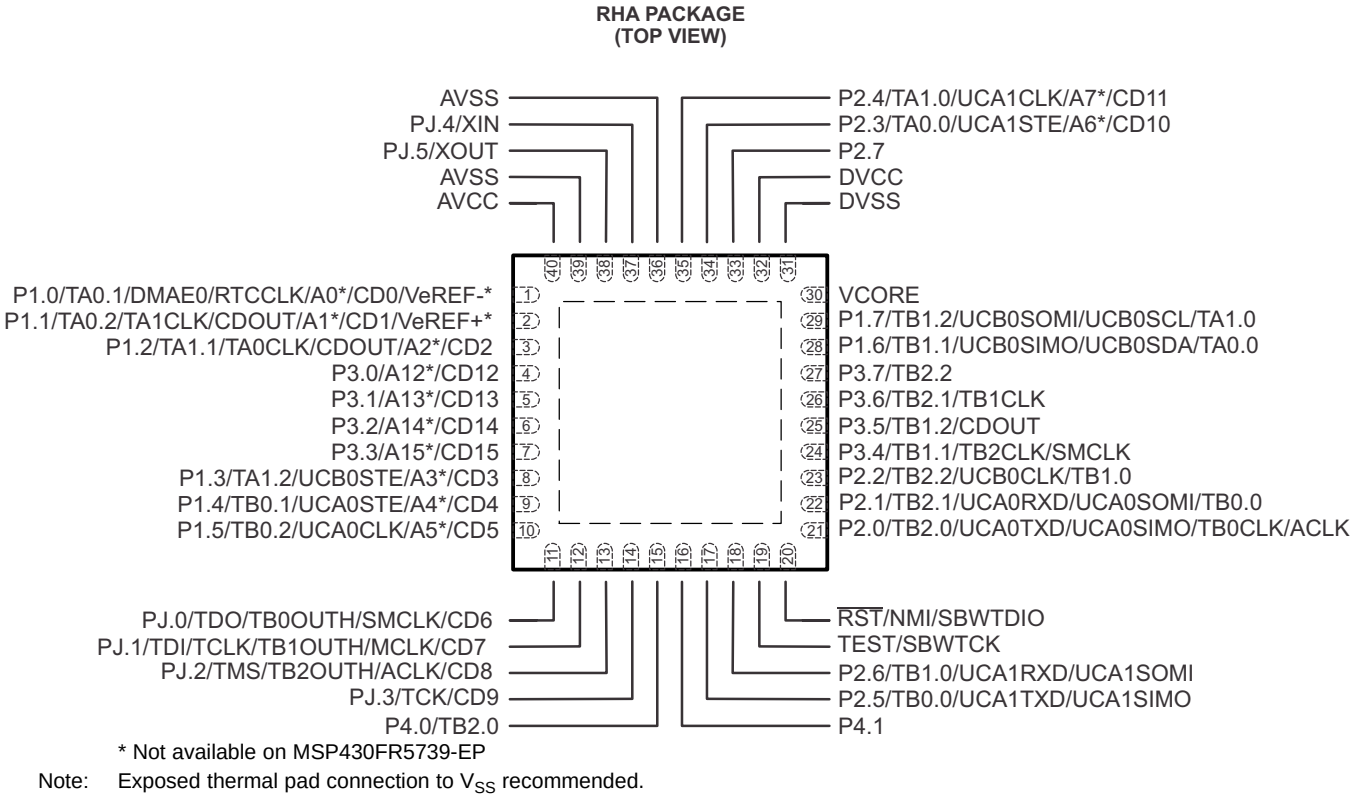



**Figure 3-1. 40-Pin RHA Package (Top View)**

## 3.2 Signal Descriptions

Table 3-1 describes the signals.

**Table 3-1. Signal Descriptions**

| PIN | | I/O (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P1.0/TA0.1/DMAE0/ RTCCLK/A0/CD0/VeREF- | 1 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA0 CCR1 capture: CCI1A input, compare: Out1<br>External DMA trigger<br>RTC clock calibration output<br>Analog input A0 – ADC (not available on devices without ADC)<br>Comparator_D input CD0<br>External applied reference voltage (not available on devices without ADC) |
| P1.1/TA0.2/TA1CLK/ CDOUT/A1/CD1/VeREF+ | 2 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA0 CCR2 capture: CCI2A input, compare: Out2<br>TA1 input clock<br>Comparator_D output<br>Analog input A1 – ADC (not available on devices without ADC)<br>Comparator_D input CD1<br>Input for an external reference voltage to the ADC (not available on devices without ADC) |
| P1.2/TA1.1/TA0CLK/ CDOUT/A2/CD2 | 3 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA1 CCR1 capture: CCI1A input, compare: Out1<br>TA0 input clock<br>Comparator_D output<br>Analog input A2 – ADC (not available on devices without ADC)<br>Comparator_D input CD2 |
| P3.0/A12/CD12 | 4 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>Analog input A12 – ADC (not available on devices without ADC)<br>Comparator_D input CD12 |
| P3.1/A13/CD13 | 5 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>Analog input A13 – ADC<br>Comparator_D input CD13 |
| P3.2/A14/CD14 | 6 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>Analog input A14 – ADC (not available on devices without ADC)<br>Comparator_D input CD14 |
| P3.3/A15/CD15 | 7 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>Analog input A15 – ADC (not available on devices without ADC)<br>Comparator_D input CD15 |
| P1.3/TA1.2/UCB0STE/ A3/CD3 | 8 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA1 CCR2 capture: CCI2A input, compare: Out2<br>Slave transmit enable – eUSCI_B0 SPI mode<br>Analog input A3 – ADC (not available on devices without ADC)<br>Comparator_D input CD3 |

(1) I = input, O = output, N/A = not available

**Table 3-1. Signal Descriptions (continued)**

| PIN | | I/O (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P1.4/TB0.1/UCA0STE/ A4/CD4 | 9 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB0 CCR1 capture: CCI1A input, compare: Out1<br>Slave transmit enable – eUSCI_A0 SPI mode<br>Analog input A4 – ADC (not available on devices without ADC)<br>Comparator_D input CD4 |
| P1.5/TB0.2/UCA0CLK/ A5/CD5 | 10 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB0 CCR2 capture: CCI2A input, compare: Out2<br>Clock signal input – eUSCI_A0 SPI slave mode, Clock signal output – eUSCI_A0 SPI master mode<br>Analog input A5 – ADC (not available on devices without ADC)<br>Comparator_D input CD5 |
| PJ.0/TDO/TB0OUTH/ SMCLK/CD6 (2) | 11 | I/O | General-purpose digital I/O<br>Test data output port<br>Switch all PWM outputs high impedance input – TB0<br>SMCLK output<br>Comparator_D input CD6 |
| PJ.1/TDI/TCLK/TB1OUTH/ MCLK/CD7 (2) | 12 | I/O | General-purpose digital I/O<br>Test data input or test clock input<br>Switch all PWM outputs high impedance input – TB1 (not available on devices without TB1)<br>MCLK output<br>Comparator_D input CD7 |
| PJ.2/TMS/TB2OUTH/ ACLK/CD8 (2) | 13 | I/O | General-purpose digital I/O<br>Test mode select<br>Switch all PWM outputs high impedance input – TB2 (not available on devices without TB2)<br>ACLK output<br>Comparator_D input CD8 |
| PJ.3/TCK/CD9 (2) | 14 | I/O | General-purpose digital I/O<br>Test clock<br>Comparator_D input CD9 |
| P4.0/TB2.0 | 15 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR0 capture: CCI0B input, compare: Out0 (not available on devices without TB2) |
| P4.1 | 16 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| P2.5/TB0.0/UCA1TXD/ UCA1SIMO | 17 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB0 CCR0 capture: CCI0A input, compare: Out0<br>Transmit data – eUSCI_A1 UART mode, Slave in, master out – eUSCI_A1 SPI mode (not available on devices without UCSI_A1) |
| P2.6/TB1.0/UCA1RXD/ UCA1SOMI | 18 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1)<br>Receive data – eUSCI_A1 UART mode, Slave out, master in – eUSCI_A1 SPI mode (not available on devices without UCSI_A1) |

(2) See Section 5.7 for use with JTAG function.

**Table 3-1. Signal Descriptions (continued)**

| PIN | | I/O (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| TEST/SBWTCK (2) (3) | 19 | I | Test mode pin – enable JTAG pins<br>Spy-Bi-Wire input clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO (2) (3) | 20 | I/O | Reset input active low<br>Non-maskable interrupt input<br>Spy-Bi-Wire data input/output |
| P2.0/TB2.0/UCA0TXD/ UCA0SIMO/TB0CLK/ACLK (3) | 21 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB2)<br>Transmit data – eUSCI_A0 UART mode<br>Slave in, master out – eUSCI_A0 SPI mode<br>TB0 clock input<br>ACLK output |
| P2.1/TB2.1/UCA0RXD/ UCA0SOMI/TB0.0 (3) | 22 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB2)<br>Receive data – eUSCI_A0 UART mode<br>Slave out, master in – eUSCI_A0 SPI mode<br>TB0 CCR0 capture: CCI0A input, compare: Out0 |
| P2.2/TB2.2/UCB0CLK/ TB1.0 | 23 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB2)<br>Clock signal input – eUSCI_B0 SPI slave mode, Clock signal output – eUSCI_B0 SPI master mode<br>TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1) |
| P3.4/TB1.1/TB2CLK/ SMCLK | 24 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB1)<br>TB2 clock input (not available on devices without TB2)<br>SMCLK output |
| P3.5/TB1.2/CDOUT | 25 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB1)<br>Comparator_D output |
| P3.6/TB2.1/TB1CLK | 26 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>TB2 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB2)<br>TB1 clock input (not available on devices without TB1) |
| P3.7/TB2.2 | 27 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB2) |
| P1.6/TB1.1/UCB0SIMO/ UCB0SDA/TA0.0 | 28 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB1)<br>Slave in, master out – eUSCI_B0 SPI mode<br>I2C data – eUSCI_B0 I2C mode<br>TA0 CCR0 capture: CCI0A input, compare: Out0 |

(3) See Section 5.6 and Section 5.7 for use with BSL and JTAG functions.

**Table 3-1. Signal Descriptions (continued)**

| PIN | | I/O (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P1.7/TB1.2/UCB0SOMI/ UCB0SCL/TA1.0 | 29 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB1)<br>Slave out, master in – eUSCI_B0 SPI mode<br>I2C clock – eUSCI_B0 I2C mode<br>TA1 CCR0 capture: CCI0A input, compare: Out0 |
| VCORE (4) | 30 | | Regulated core power supply (internal use only, no external current loading) |
| DVSS | 31 | | Digital ground supply |
| DVCC | 32 | | Digital power supply |
| P2.7 | 33 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 |
| P2.3/TA0.0/UCA1STE/ A6/CD10 | 34 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA0 CCR0 capture: CCI0B input, compare: Out0<br>Slave transmit enable – eUSCI_A1 SPI mode (not available on devices without eUSCI_A1)<br>Analog input A6 – ADC (not available on devices without ADC)<br>Comparator_D input CD10 |
| P2.4/TA1.0/UCA1CLK/ A7/CD11 | 35 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA1 CCR0 capture: CCI0B input, compare: Out0<br>Clock signal input – eUSCI_A1 SPI slave mode, Clock signal output – eUSCI_A1 SPI master mode (not available on devices without eUSCI_A1)<br>Analog input A7 – ADC (not available on devices without ADC)<br>Comparator_D input CD11 |
| AVSS | 36 | | Analog ground supply |
| PJ.4/XIN | 37 | I/O | General-purpose digital I/O<br>Input terminal for crystal oscillator XT1 |
| PJ.5/XOUT | 38 | I/O | General-purpose digital I/O<br>Output terminal of crystal oscillator XT1 |
| AVSS | 39 | | Analog ground supply |
| AVCC | 40 | | Analog power supply |
| QFN Pad | Pad | | QFN package pad. Connection to VSS recommended. |

(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.

# 4 Specifications

## 4.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage applied at $V_{CC}$ to $V_{SS}$ | | –0.3 | 4.1 | V |
| Voltage applied to any pin (excluding VCORE) (2) | | –0.3 | $V_{CC}$ + 0.3 V | V |
| Diode current at any device pin | | | ±2 | mA |
| $T_J$ | Maximum junction temperature | | 95 | °C |
| $T_{stg}$ | Storage temperature range(3) (4) (5) | –55 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$. $V_{CORE}$ is for internal device use only. No external DC loading or voltage should be applied.
(3) Data retention on FRAM memory cannot be ensured when exceeding the specified maximum storage temperature, $T_{stg}$.
(4) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(5) Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.

## 4.2 Recommended Operating Conditions

Typical values are specified at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during program execution and FRAM programming (AVCC = DVCC) (1) | | 2.0 | | 3.6 | V |
| $V_{SS}$ | Supply voltage (AVSS = DVSS) | | | 0 | | V |
| $T_A$ | Operating free-air temperature | | –55 | | 85 | °C |
| $T_J$ | Operating junction temperature | | –55 | | 85 | °C |
| $C_{VCORE}$ | Required capacitor at VCORE(2) | | | 470 | | nF |
| $C_{VCC}$/ $C_{VCORE}$ | Capacitor ratio of VCC to VCORE | | 10 | | | |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(3) | No FRAM wait states(4), 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 8.0 | MHz |
| | | With FRAM wait states(4), NACCESS = {2}, NPRECHG = {1}, 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 24.0 | |

(1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) A capacitor tolerance of ±20% or better is required.
(3) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(4) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* (SLAU272) for recommended settings for common system frequencies.

## 4.3 Thermal Information

| THERMAL METRIC(1) | | MSP430FR5739-EP VQFN 40 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 37.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 27.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 12.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 12.6 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 4.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | Frequency ($f_{MCLK} = f_{SMCLK}$)(4) | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 MHz | | 4 MHz | | 8 MHz | | 16 MHz | | 20 MHz | | 24 MHz | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM,\ FRAM\_UNI}$(5) | FRAM | 3 V | 0.27 | | 0.58 | | 1.0 | | 1.53 | | 1.9 | | 2.2 | | mA |
| $I_{AM,0\%}$(6) | FRAM 0% cache hit ratio | 3 V | 0.42 | 0.75 | 1.2 | 1.7 | 2.2 | 2.9 | 2.3 | 3.0 | 2.8 | 3.7 | 3.45 | 4.3 | mA |
| $I_{AM,50\%}$(6) (7) | FRAM 50% cache hit ratio | 3 V | 0.31 | | 0.73 | | 1.3 | | 1.75 | | 2.1 | | 2.5 | | |
| $I_{AM,66\%}$(6) (7) | FRAM 66% cache hit ratio | 3 V | 0.27 | | 0.58 | | 1.0 | | 1.55 | | 1.9 | | 2.2 | | |
| $I_{AM,75\%}$(6) (7) | FRAM 75% cache hit ratio | 3 V | 0.25 | | 0.5 | | 0.82 | | 1.3 | | 1.6 | | 1.8 | | |
| $I_{AM,100\%}$(6) (7) | FRAM 100% cache hit ratio | 3 V | 0.2 | 0.44 | 0.3 | 0.56 | 0.42 | 0.81 | 0.73 | 1.17 | 0.88 | 1.32 | 1.0 | 1.53 | |
| $I_{AM,\ RAM}$(7) (8) | RAM | 3 V | 0.2 | 0.41 | 0.35 | 0.56 | 0.55 | 0.77 | 1.0 | 1.27 | 1.20 | 1.47 | 1.45 | 1.8 | mA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Characterized with program executing typical data processing.
(4) At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency, $f_{MCLK,eff}$, decreases. The effective MCLK frequency is also dependent on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio. The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff,MHZ} = f_{MCLK,MHZ}$ x 1 / [# of wait states x ((1 - cache hit ratio percent/100)) + 1]
(5) Program and data reside entirely in FRAM. No wait states enabled. DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz). MCLK = SMCLK.
(6) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 25% ratio implies one of every four accesses is from cache, the remaining are FRAM accesses.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz). MCLK = SMCLK. No wait states enabled.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 ($f_{DCO}$ = 16 MHz). MCLK = SMCLK. One wait state enabled.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 ($f_{DCO}$ = 20 MHz). MCLK = SMCLK. Three wait states enabled.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 ($f_{DCO}$ = 24 MHz). MCLK = SMCLK. Three wait states enabled.
(7) See Figure 4-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Section 4.4.
$f_{ACLK}$ = 32786 Hz, $f_{MCLK} = f_{SMCLK}$ at specified frequency. No peripherals active.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.
(8) All execution is from RAM.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz). MCLK = SMCLK.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 ($f_{DCO}$ = 16 MHz). MCLK = SMCLK.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 ($f_{DCO}$ = 20 MHz). MCLK = SMCLK.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 ($f_{DCO}$ = 24 MHz). MCLK = SMCLK.

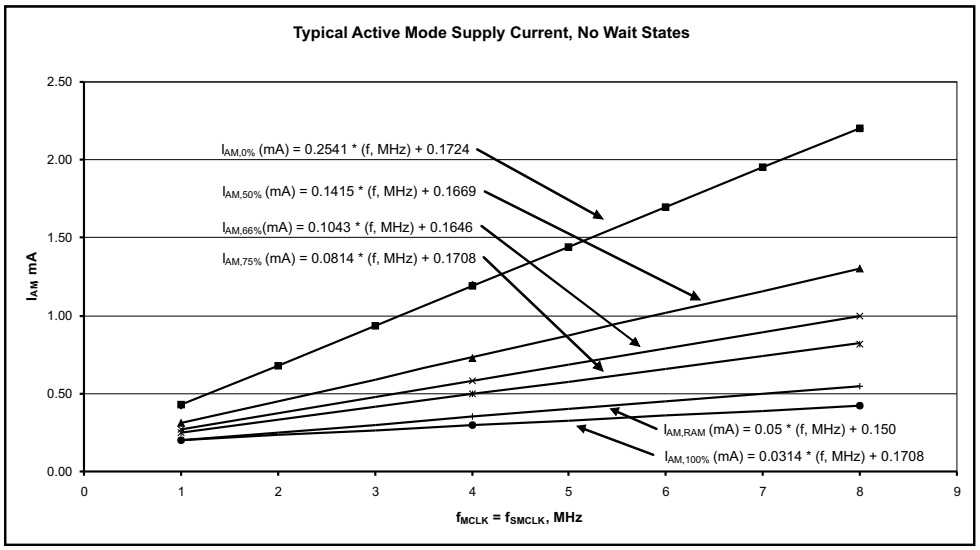



**Figure 4-1. Typical Active Mode Supply Currents, No Wait States**

## 4.5 Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (2)

| PARAMETER | | $V_{CC}$ | –55°C | | 25°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ | Low-power mode 0 (3) (4) | 2 V, 3 V | 166 | | 175 | | 225 | | µA |
| $_{LPM0,8MHz}$ | Low-power mode 0 (5) (4) | 2 V, 3 V | 170 | | 177 | 244 | 225 | 360 | µA |
| $_{LPM0,24MHz}$ | Low-power mode 0 (6) (4) | 2 V, 3 V | 274 | | 285 | 340 | 340 | 455 | µA |
| $I_{LPM2}$ | Low-power mode 2 (7) (8) | 2 V, 3 V | 56 | | 61 | 80 | 110 | 210 | µA |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode (9) (8) | 2 V, 3 V | 3.4 | | 6.4 | 15 | 48 | 150 | µA |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO mode (10) (8) | 2 V, 3 V | 3.3 | | 6.3 | 15 | 48 | 150 | µA |
| $I_{LPM4}$ | Low-power mode 4 (11) (8) | 2 V, 3 V | 2.9 | | 5.9 | 15 | 48 | 150 | µA |
| $I_{LPM3.5}$ | Low-power mode 3.5 (12) | 2 V, 3 V | 1.3 | | 1.5 | 2.2 | 2.8 | 5.0 | µA |
| $I_{LPM4.5}$ | Low-power mode 4.5 (13) | 2 V, 3 V | 0.3 | | 0.32 | 0.66 | 0.57 | 2.55 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = 1 MHz. DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz)
(4) Current for brownout, high-side supervisor ($SVS_H$) and low-side supervisor ($SVS_L$) included.
(5) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = 8 MHz. DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz)
(6) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = 24 MHz. DCORSEL = 1, DCOFSELx = 3 ($f_{DCO}$ = 24 MHz)
(7) Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz, DCORSEL = 0, DCOFSELx = 3, DCO bias generator enabled.
(8) Current for brownout, high-side supervisor ($SVS_H$) included. Low-side supervisor disabled ($SVS_L$).
(9) Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(10) Current for watchdog timer (clocked by ACLK) included. ACLK = VLO.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = $f_{VLO}$, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(11) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(12) Internal regulator disabled. No data retention. RTC active clocked by XT1 LF mode.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM3.5), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(13) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz

## 4.6 Schmitt-Trigger Inputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 2 V | 0.7 | | 1.7 | V |
| | | | 3 V | 1.45 | | 2.12 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 2 V | 0.41 | | 1.101 | V |
| | | | 3 V | 0.72 | | 1.68 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 2 V | 0.24 | | 0.855 | V |
| | | | 3 V | 0.27 | | 1.02 | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 19 | 35 | 51 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

## 4.7 Inputs – Ports P1 and P2 (1) (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing (2) | External trigger pulse duration to set interrupt flag | 2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

## 4.8 Leakage Current – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.x)}$ | High-impedance leakage current | (1) (2) | 2 V, 3 V | –65 | 65 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## 4.9 Outputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA (1) | 2 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA (2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA (1) | 3 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA (2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA (1) | 2 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA (2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA (1) | 3 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA (2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

## 4.10 Output Frequency – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

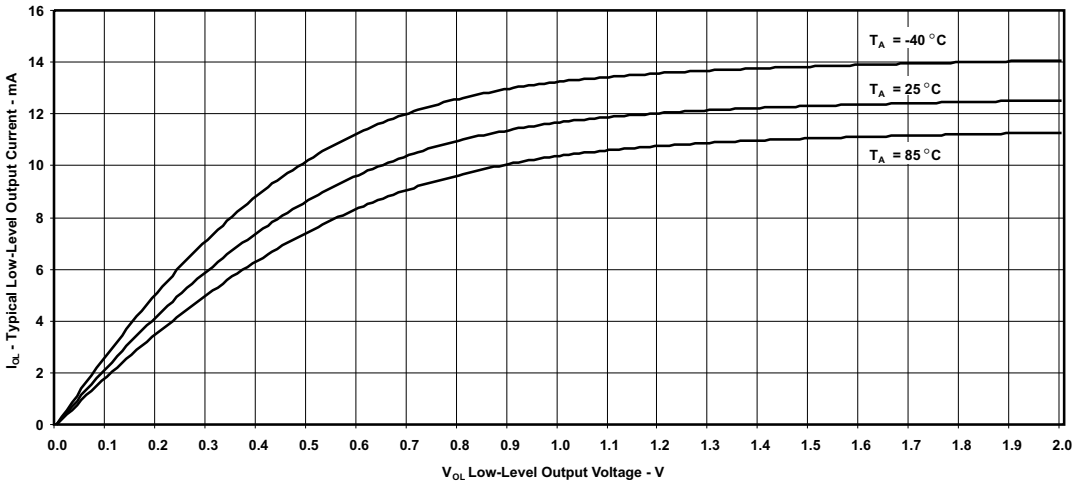
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | Px.y (1) (2) | 2 V | | 16 | MHz |
| | | | 3 V | | 24 | |
| $f_{Port\_CLK}$ | Clock output frequency | ACLK, SMCLK, or MCLK at configured output port, $C_L$ = 20 pF, no DC loading (2) | 2 V | | 16 | MHz |
| | | | 3 V | | 24 | |

(1) A resistive divider with 2 × 1.6 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider. $C_L$ = 20 pF is connected from the output to $V_{SS}$.
(2) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

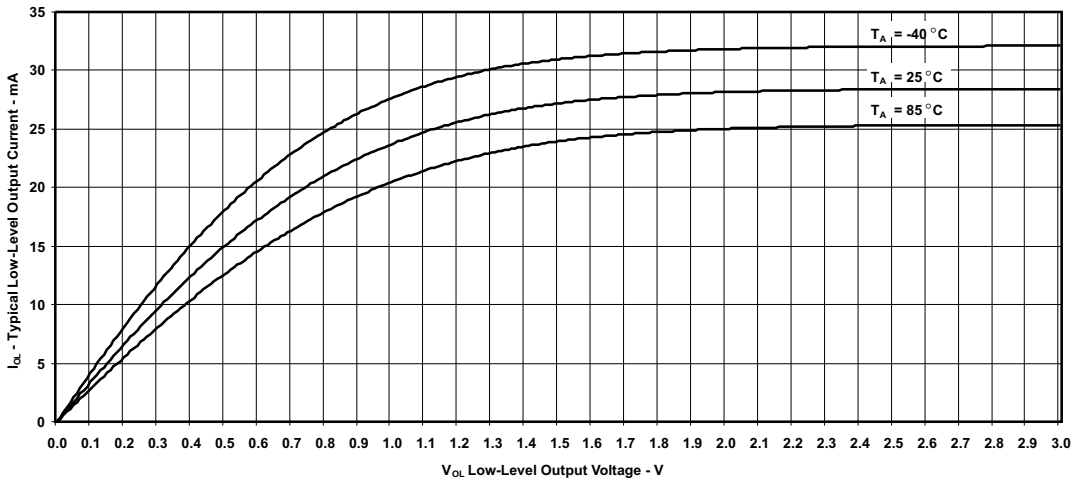
## 4.11 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



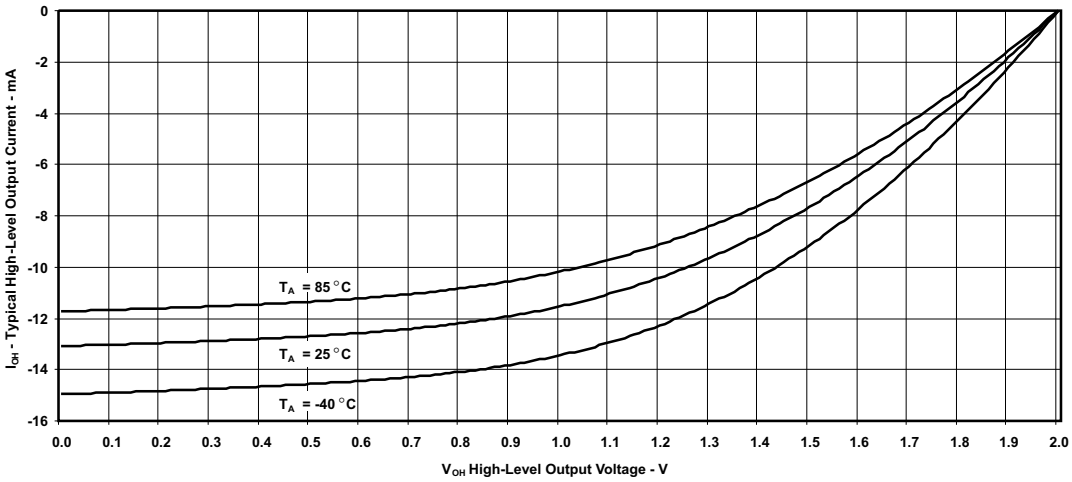

$V_{CC}$ = 2.0 V Measured at Px.y

**Figure 4-2. Typical Low-Level Output Current vs Low-Level Output Voltage**



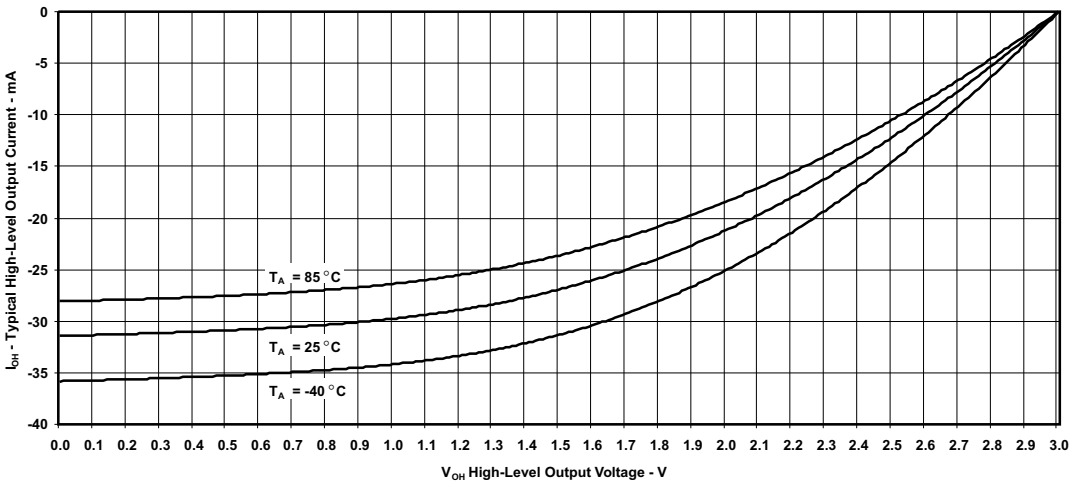

$V_{CC}$ = 3.0 V Measured at Px.y

**Figure 4-3. Typical Low-Level Output Current vs Low-Level Output Voltage**




$V_{CC}$ = 2.0 V Measured at Px.y

**Figure 4-4. Typical High-Level Output Current vs High-Level Output Voltage**




$V_{CC}$ = 3.0 V Measured at Px.y

**Figure 4-5. Typical High-Level Output Current vs High-Level Output Voltage**

## 4.12 Crystal Oscillator, XT1, Low-Frequency (LF) Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta I_{VCC.LF}$ | Additional current consumption XT1 LF mode from lowest drive setting | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $C_{L,eff}$ = 9 pF, $T_A$ = 25°C, | 3 V | | 60 | | nA |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {2}, $T_A$ = 25°C, $C_{L,eff}$ = 9 pF | 3 V | | 90 | | |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | 3 V | | 140 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1 (3) (4) | | 10 | 32.768 | 50 | kHz |
| $OA_{LF}$ | Oscillation allowance for LF crystals (5) | XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 210 | | kΩ |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 300 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz | | 30 | | 70 | % |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode (6) | XTS = 0 (7) | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Startup time, LF mode (8) | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 6 pF | 3 V | | 1000 | | ms |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | | | 1000 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode (9) (10) | XTS = 0 | | | 1 | | pF |

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) –40°C to 85°C

(3) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(4) Maximum frequency of operation of the entire device cannot be exceeded.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVE = {0}, $C_{L,eff} \le 6$ pF.
- For XT1DRIVE = {1}, 6 pF $\le C_{L,eff} \le$ 9 pF.
- For XT1DRIVE = {2}, 6 pF $\le C_{L,eff} \le$ 10 pF.
- For XT1DRIVE = {3}, 6 pF $\le C_{L,eff} \le$ 12 pF.

(6) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(7) Measured with logic-level input frequency but also applies to operation with crystals.

(8) Includes startup counter of 4096 clock cycles.

(9) Requires external capacitors at both terminals.

(10) Values are specified by crystal manufacturers. Include parasitic bond and package capacitance (approximately 2 pF per pin). Recommended values supported are 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF.

## 4.13 Crystal Oscillator, XT1, High-Frequency (HF) Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{VCC,HF}$ | XT1 oscillator crystal current HF mode | $f_{OSC}$ = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | 3 V | | 175 | | µA |
| | | $f_{OSC}$ = 8 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 300 | | |
| | | $f_{OSC}$ = 16 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {2}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 350 | | |
| | | $f_{OSC}$ = 24 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 550 | | |
| $f_{XT1,HF0}$ | XT1 oscillator crystal frequency, HF mode 0 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0} (3) | | 4 | | 6 | MHz |
| $f_{XT1,HF1}$ | XT1 oscillator crystal frequency, HF mode 1 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1} (3) | | 6 | | 10 | MHz |
| $f_{XT1,HF2}$ | XT1 oscillator crystal frequency, HF mode 2 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2} (3) | | 10 | | 16 | MHz |
| $f_{XT1,HF3}$ | XT1 oscillator crystal frequency, HF mode 3 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3} (3) | | 16 | | 24 | MHz |
| $f_{XT1,HF,SW}$ | XT1 oscillator logic-level square-wave input frequency, HF mode | XTS = 1, XT1BYPASS = 1 (4) (3) | | 1 | | 24 | MHz |
| $OA_{HF}$ | Oscillation allowance for HF crystals (5) | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF | | | 450 | | Ω |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1}, $f_{XT1,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF | | | 320 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2}, $f_{XT1,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF | | | 200 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF | | | 200 | | |
| $t_{START,HF}$ | Startup time, HF mode (6) | $f_{OSC}$ = 4 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | 3 V | | 8 | | ms |
| | | $f_{OSC}$ = 24 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 2 | | |

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) –40°C to 85°C
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes startup counter of 4096 clock cycles.

## Crystal Oscillator, XT1, High-Frequency (HF) Mode[1] *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[2]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{L,eff}$ | Integrated effective load capacitance (7) (8) | XTS = 1 | | | 1 | | pF |
| | Duty cycle, HF mode | XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 24 MHz | | 40 | 50 | 60 | % |
| $f_{Fault,HF}$ | Oscillator fault frequency, HF mode (9) | XTS = 1 (10) | | 145 | | 900 | kHz |

(7) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(8) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
(9) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

## 4.14 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 2 V to 3.6 V | 4.3 | 8.3 | 13.3 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK (1) | 2 V to 3.6 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_C$ | VLO frequency supply voltage drift | Measured at ACLK (2) | 2 V to 3.6 V | | 4 | | %/V |
| $f_{VLO,DC}$ | Duty cycle | Measured at ACLK | 2 V to 3.6 V | 35% | 50% | 65% | |

(1) Calculated using the box method: (MAX(–55 to 85°C) – MIN(–55 to 85°C)) / MIN(–55 to 85°C) / (85°C – (–55°C))
(2) Calculated using the box method: (MAX(2.0 to 3.6 V) – MIN(2.0 to 3.6 V)) / MIN(2.0 to 3.6 V) / (3.6 V – 2 V)

## 4.15 DCO Frequencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$<br>$T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{DCO,LO}$ | DCO frequency low, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V<br>–55°C to 85°C | | 5.37 | ±5% | MHz |
| | | Measured at ACLK, DCORSEL = 1 | 2 V to 3.6 V<br>–55°C to 85°C | | 16.2 | ±5% | MHz |
| $f_{DCO,MID}$ | DCO frequency mid, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V<br>–55°C to 85°C | | 6.67 | ±5% | MHz |
| | | Measured at ACLK, DCORSEL = 1 | 2 V to 3.6 V<br>–55°C to 85°C | | 20 | ±5% | MHz |
| $f_{DCO,HI}$ | DCO frequency high, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V<br>–55°C to 85°C | | 8 | ±5% | MHz |
| | | Measured at ACLK, DCORSEL = 1 | 2 V to 3.6 V<br>–55°C to 85°C | | 23.8 | ±5% | MHz |
| $f_{DCO,DC}$ | Duty cycle | Measured at ACLK, divide by 1, No external divide, all DCO settings | 2 V to 3.6 V<br>–55°C to 85°C | 35% | 50% | 65% | |

## 4.16 MODOSC

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{MODOSC}$ | Current consumption | Enabled | 2 V to 3.6 V | | 44 | | µA |
| $f_{MODOSC}$ | MODOSC frequency | | 2 V to 3.6 V | 4.2 | 5.0 | 5.7 | MHz |
| $f_{MODOSC,DC}$ | Duty cycle | Measured at ACLK, divide by 1 | 2 V to 3.6 V | 35% | 50% | 65% | |

## 4.17 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CORE}$(AM) | Core voltage, active mode | 2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.5 | | V |
| $V_{CORE}$(LPM) | Core voltage, low-current mode | 2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.5 | | V |

## 4.18 PMM, SVS, BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SVSH,AM}$ | $SVS_H$ current consumption, active mode | $V_{CC}$ = 3.6 V | | 5 | | µA |
| $I_{SVSH,LPM}$ | $SVS_H$ current consumption, low power modes | $V_{CC}$ = 3.6 V | | 0.8 | | µA |
| $V_{SVSH-}$ | $SVS_H$ on voltage level, falling supply voltage | | 1.81 | 1.88 | 1.95 | V |
| $V_{SVSH+}$ | $SVS_H$ off voltage level, rising supply voltage | | 1.85 | 1.93 | 2 | V |
| $t_{PD,SVSH,\ AM}$ | $SVS_H$ propagation delay, active mode | $dV_{CC}/dt$ = 10 mV/µs | | 10 | | µs |
| $t_{PD,SVSH,\ LPM}$ | $SVS_H$ propagation delay, low power modes | $dV_{CC}/dt$ = 1 mV/µs | | 30 | | µs |
| $I_{SVSL}$ | $SVS_L$ current consumption | | | 0.3 | | µA |
| $V_{SVSL–}$ | $SVS_L$ on voltage level | | | 1.42 | | V |
| $V_{SVSL+}$ | $SVS_L$ off voltage level | | | 1.47 | | V |

## 4.19 Wake-Up from Low Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP\ LPM0}$ | Wake-up time from LPM0 to active mode (1) | | 2 V, 3 V –55°C to 85°C | | 0.58 | 1.1 | µs |
| $t_{WAKE-UP\ LPM12}$ | Wake-up time from LPM1, LPM2 to active mode (1) | | 2 V, 3 V –55°C to 85°C | | 12 | 25 | µs |
| $t_{WAKE-UP\ LPM34}$ | Wake-up time from LPM3 or LPM4 to active mode (1) | | 2 V, 3 V –55°C to 85°C | | 78 | 165 | µs |
| $t_{WAKE-UP\ LPMx.5}$ | Wake-up time from LPM3.5 or LPM4.5 to active mode (1) | | 2 V, 3 V 0°C to 85°C | | 310 | 575 | µs |
| | | | 2 V, 3 V –55°C to 85°C | | 310 | 1100 | µs |
| $t_{WAKE-UP\ RESET}$ | Wake-up time from $\overline{RST}$ to active mode (2) | $V_{CC}$ stable | 2 V, 3 V –55°C to 85°C | | 230 | | µs |
| $t_{WAKE-UP\ BOR}$ | Wake-up time from BOR or power-up to active mode | $dV_{CC}/dt$ = 2400 V/s | 2 V, 3 V –55°C to 85°C | | 1.6 | | ms |
| $t_{RESET}$ | Pulse duration required at $\overline{RST}$/NMI terminal to accept a reset event (3) | | 2 V, 3 V –55°C to 85°C | 4 | | | ns |

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.
(2) The wake-up time is measured from the rising edge of the $\overline{RST}$ signal until the first instruction of the user program is executed.
(3) Meeting or exceeding this time makes sures a reset event occurs. Pulses shorter than this minimum time may or may not cause a reset event to occur.

## 4.20 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK, ACLK<br>External: TACLK<br>Duty cycle = 50% ± 10% | 2 V, 3 V | | | 24 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

## 4.21 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B input clock frequency | Internal: SMCLK, ACLK<br>External: TBCLK<br>Duty cycle = 50% ± 10% | 2 V, 3 V | | | 24 | MHz |
| $t_{TB,cap}$ | Timer_B capture timing | All capture inputs, Minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

## 4.22 eUSCI (UART Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in MBaud) | | | | | 5 | MHz |

## 4.23 eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time[1] | UCGLITx = 0 | 2 V, 3 V | 5 | 15 | 20 | ns |
| | | UCGLITx = 1 | | 20 | 45 | 60 | |
| | | UCGLITx = 2 | | 35 | 80 | 120 | |
| | | UCGLITx = 3 | | 50 | 110 | 180 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

## 4.24 eUSCI (SPI Master Mode) Recommended Operating Conditions

| PARAMETER | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ eUSCI input clock frequency | Internal: SMCLK, ACLK<br>Duty cycle = 50% ± 10% | | | | $f_{SYSTEM}$ | MHz |

## 4.25 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | |
| $t_{STE,ACC}$ | STE access time, STE active to SIMO data out | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 55 | ns |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 35 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 40 | ns |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 30 | |
| $t_{SU,MI}$ | SOMI input data setup time | | 2 V | 35 | | | ns |
| | | | 3 V | 35 | | | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| $t_{VALID,MO}$ | SIMO output data valid time (2) | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF | 2 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| $t_{HD,MO}$ | SIMO output data hold time (3) | $C_L$ = 20 pF | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 4-6 and Figure 4-7.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 4-6 and Figure 4-7.

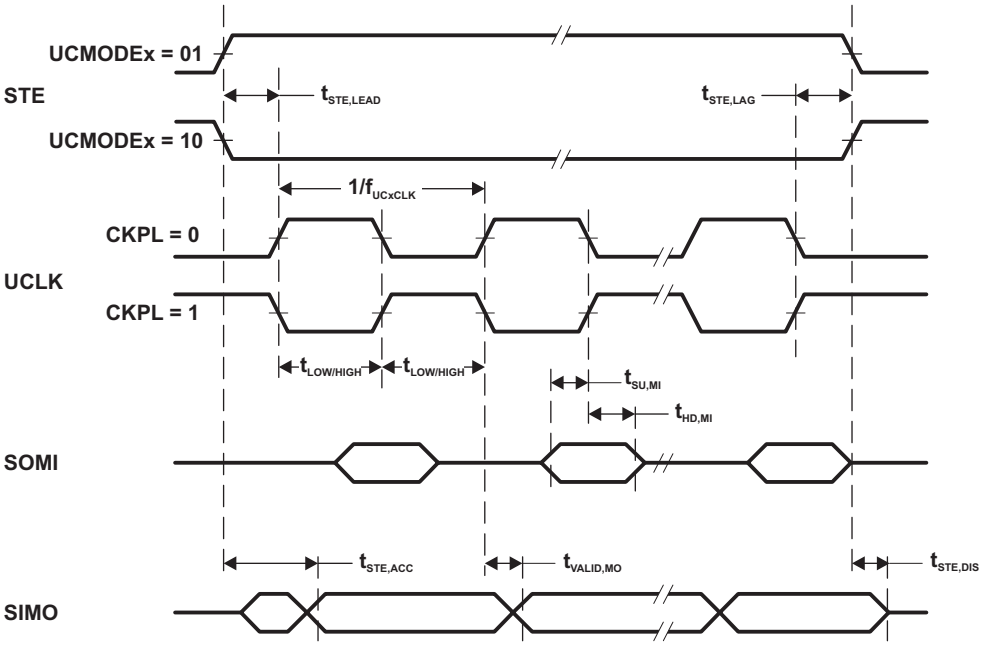



**Figure 4-6. SPI Master Mode, CKPH = 0**

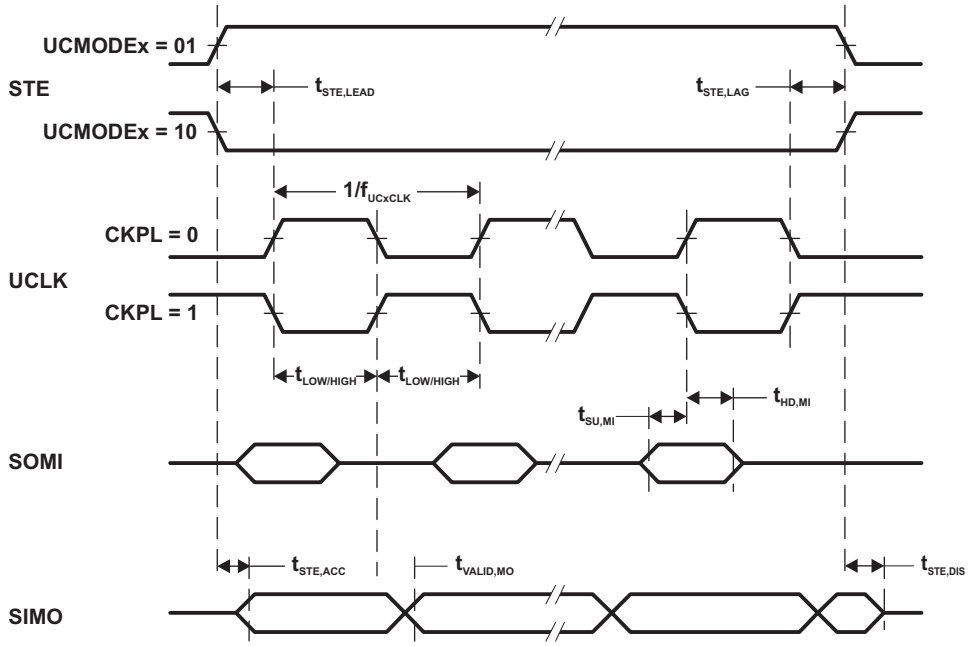



**Figure 4-7. SPI Master Mode, CKPH = 1**

## 4.26 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | 2 V | 7 | | | ns |
| | | | 3 V | 7 | | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | 2 V | | | 65 | ns |
| | | | 3 V | | | 40 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | 2 V | | | 40 | ns |
| | | | 3 V | | | 35 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 2 V | 2 | | | ns |
| | | | 3 V | 2 | | | |
| $t_{HD,SI}$ | SIMO input data hold time | | 2 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| $t_{VALID,SO}$ | SOMI output data valid time (2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 2 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| $t_{HD,SO}$ | SOMI output data hold time (3) | $C_L$ = 20 pF | 2 V | 4 | | | ns |
| | | | 3 V | 4 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 4-8 and Figure 4-9.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 4-8 and Figure 4-9.

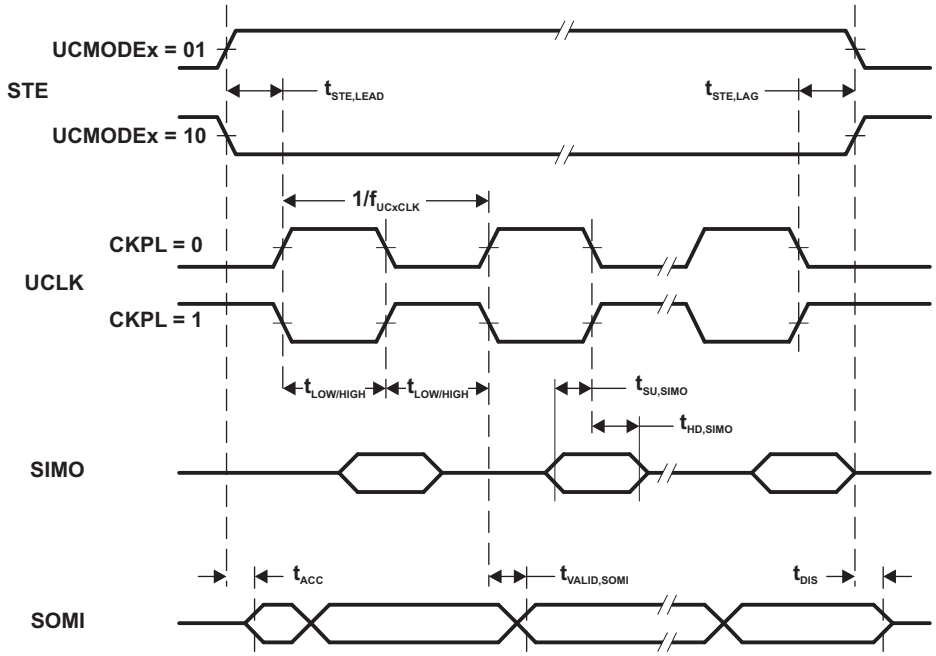



**Figure 4-8. SPI Slave Mode, CKPH = 0**

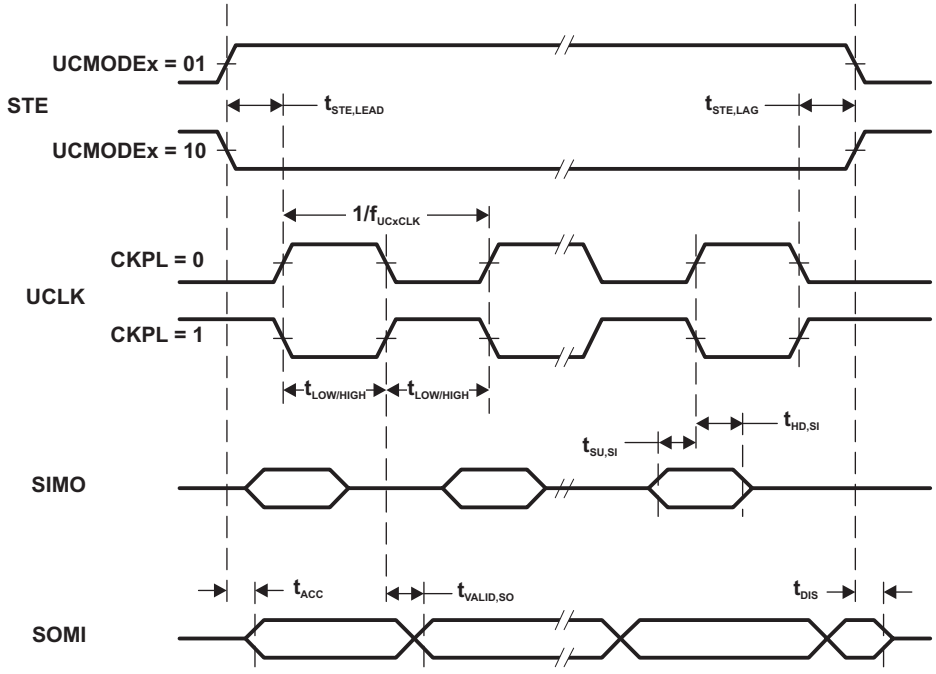



**Figure 4-9. SPI Slave Mode, CKPH = 1**

## 4.27 eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4-10)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ±10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2 V, 3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.7 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2 V, 3 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2 V, 3 V | 250 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2 V, 3 V | 50 | | 600 | ns |
| | | UCGLITx = 1 | | 25 | | 300 | ns |
| | | UCGLITx = 2 | | 12.5 | | 150 | ns |
| | | UCGLITx = 3 | | 6.25 | | 75 | ns |
| $t_{TIMEOUT}$ | Clock low timeout | UCCLTOx = 1 | 2 V, 3 V | | 27 | | ms |
| | | UCCLTOx = 2 | | | 30 | | ms |
| | | UCCLTOx = 3 | | | 33 | | ms |

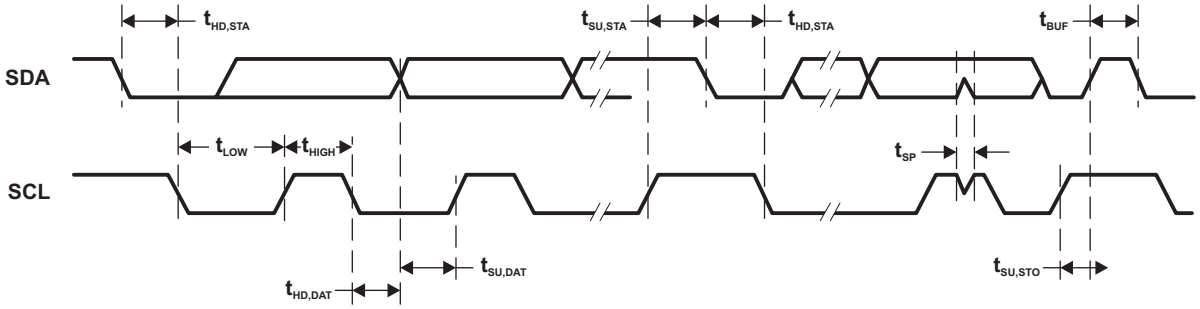



**Figure 4-10. I²C Mode Timing**

## 4.28 10-Bit ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC}$ and $DV_{CC}$ are connected together, $AV_{SS}$ and $DV_{SS}$ are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V | | 2.0 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range | All ADC10 pins | | 0 | | $AV_{CC}$ | V |
| $I_{ADC10\_A}$ | Operating supply current into AVCC terminal, reference current not included | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0 | 2 V | | 90 | 150 | µA |
| | | | 3 V | | 100 | 170 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad | 2.2 V | | 6 | | pF |
| $R_I$ | Input MUX ON resistance | $AV_{CC} \geq 2$ V, $0 V \leq V_{Ax} \leq AV_{CC}$ | | | | 36 | kΩ |

## 4.29 10-Bit ADC, Timing Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC10CLK}$ | | For specified performance of ADC10 linearity parameters | 2 V to 3.6 V | 0.45 | 5 | 5.5 | MHz |
| $f_{ADC10OSC}$ | Internal ADC10 oscillator (MODOSC) | ADC10DIV = 0, $f_{ADC10CLK} = f_{ADC10OSC}$ | 2 V to 3.6 V | 4.2 | 4.5 | 5.7 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4.5 MHz to 5.5 MHz | 2 V to 3.6 V | 2.18 | | 2.67 | µs |
| | | External $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0 | 2 V to 3.6 V | | (1) | | |
| $t_{ADC10ON}$ | Turn on settling time of the ADC | The error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB, Reference and input signal already settled | | | | 100 | ns |
| $t_{Sample}$ | Sampling time | $R_S$ = 1000 Ω, $R_I$ = 36000 Ω, $C_I$ = 3.5 pF, Approximately eight Tau (τ) are required to get an error of less than ±0.5 LSB | 2 V | 1.5 | | | µs |
| | | | 3 V | 2.0 | | | |

(1) $12 \times ADC10DIV \times 1/f_{ADC10CLK}$

## 4.30 10-Bit ADC, Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error | $1.4 V \leq (V_{eREF+} - V_{REF-}/V_{eREF-})min \leq 1.6$ V | 3.6 V | –1.4 | | 1.4 | LSB |
| | | $1.6 V < (V_{eREF+} - V_{REF-}/V_{eREF-})min \leq V_{AVCC}$ | | –1.3 | | 1.3 | |
| $E_D$ | Differential linearity error | $(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$ | 3.6 V | –1.2 | | 1.2 | LSB |
| $E_O$ | Offset error | $(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$ | 3.6 V | | ±2.5 | | mV |
| $E_G$ | Gain error, external reference | $(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$ | 3.6 V | –1.4 | | 1.4 | LSB |
| | Gain error, internal reference (1) | | | | ±4 | | |
| $E_T$ | Total unadjusted error, external reference | $(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$ | 3.6 V | | ±2.3 | | LSB |
| | Total unadjusted error, internal reference (1) | | | | ±4 | | |

(1) Error is dominated by the internal reference.

## 4.31 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input | $V_{eREF+} > V_{eREF-}$ (2) | | 1.4 | | $AV_{CC}$ | V |
| $V_{eREF-}$ | Negative external reference voltage input | $V_{eREF+} > V_{eREF-}$ (3) | | 0 | | 1.2 | V |
| ($V_{eREF+} – V_{REF-}/V_{eREF-}$) | Differential external reference voltage input | $V_{eREF+} > V_{eREF-}$ (4) | | 1.4 | | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VeREF-}$ | Static input current | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 1h, Conversion rate 200 ksps | 2.2 V, 3 V | | ±6 | | µA |
| | | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 8h, Conversion rate 20 ksps | 2.2 V, 3 V | | ±1 | | µA |
| $C_{VREF+}$, $C_{VREF-}$ | Capacitance at VREF+ or VREF- terminal (5) | | | | 10 | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_i$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_B. Also see the *MSP430FR57xx Family User's Guide* (SLAU272).

## 4.32 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.39 | 2.5 | 2.61 | V |
| | | REFVSEL = {1} for 2 V, REFON = 1 | 3 V | 1.91 | 2.0 | 2.09 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 3 V | 1.43 | 1.5 | 1.57 | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 2.0 | | | V |
| | | REFVSEL = {1} for 2 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal (1) | $f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0 | 3 V | | 33 | | µA |
| $T_{REF+}$ | Temperature coefficient of built-in reference | REFVSEL = (0, 1, 2}, REFON = 1 | | | ±35 | | ppm/°C |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, $T_A$ = 25°C, REFON = 1, REFVSEL = {0} for 1.5 V | | | 1600 | | µV/V |
| | | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, $T_A$ = 25°C, REFON = 1, REFVSEL = {1} for 2 V | | | 1900 | | |
| | | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, $T_A$ = 25°C, REFON = 1, REFVSEL = {2} for 2.5 V | | | 3600 | | |
| $t_{SETTLE}$ | Settling time of reference voltage (2) | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | 30 | | µs |

(1) The internal reference current is supplied by terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(2) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB.

## 4.33 REF, Temperature Sensor and Built-In $V_{MID}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | See (1) | ADC10ON = 1, INCH = 0Ah, $T_A$ = 0°C | 2 V, 3 V | | 790 | | mV |
| $TC_{SENSOR}$ | | ADC10ON = 1, INCH = 0Ah | 2 V, 3 V | | 2.55 | | mV/°C |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected (2) | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2 V | 30 | | | µs |
| | | | 3 V | 30 | | | |
| $V_{MID}$ | $AV_{CC}$ divider at channel 11 | ADC10ON = 1, INCH = 0Bh, $V_{MID}$ is ~0.5 × $V_{AVCC}$ | 2 V | 0.96 | 1.0 | 1.04 | V |
| | | | 3 V | 1.43 | 1.5 | 1.57 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected (3) | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2 V, 3 V | 1000 | | | ns |

(1) The temperature sensor offset can vary significantly. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(2) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(3) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

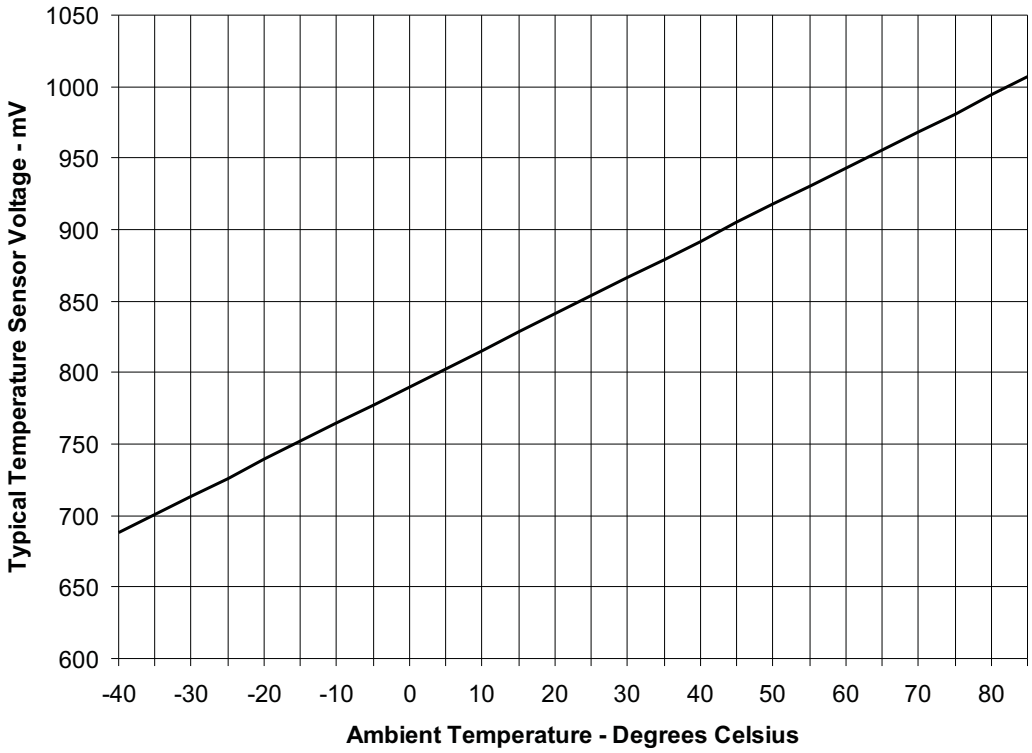



**Figure 4-11. Typical Temperature Sensor Voltage**

## 4.34 Comparator_D

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay, AVCC = 2 V to 3.6 V | Overdrive = 10 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 10 mV) | 49 | 100 | 202 | ns |
| | | Overdrive = 100 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 100 mV) | | 80 | | ns |
| | | Overdrive = 250 mV, (VIN+ – 400 mV) to (VIN+ + 250 mV) | | 50 | | ns |
| $t_{filter}$ | Filter timer added to the propagation delay of the comparator | CDF = 1, CDFDLY = 00 | 0.28 | 0.5 | 1.1 | µs |
| | | CDF = 1, CDFDLY = 01 | 0.49 | 0.9 | 1.8 | µs |
| | | CDF = 1, CDFDLY = 10 | 0.85 | 1.6 | 3.31 | µs |
| | | CDF = 1, CDFDLY = 11 | 1.59 | 3.0 | 6.5 | µs |
| $V_{offset}$ | Input offset | AVCC = 2 V to 3.6 V | –26 | | 26 | mV |
| $V_{ic}$ | Common mode input range | AVCC = 2 V to 3.6 V | 0 | | AVCC – 1 | V |
| $I_{comp(AVCC)}$ | Comparator only | CDON = 1, AVCC = 2 V to 3.6 V | | 28 | | µA |
| $I_{ref(AVCC)}$ | Reference buffer and R-ladder | CDREFLx = 01, AVCC = 2 V to 3.6 V | | 20 | | µA |
| $t_{enable,comp}$ | Comparator enable time | CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V | | 1.1 | 2.3 | µs |
| $t_{enable,rladder}$ | Resistor ladder enable time | CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V | | 1.1 | 2.3 | µs |
| $V_{CB\_REF}$ | Reference voltage for a tap | VIN = voltage input to the R-ladder, n = 0 to 31 | VIN × (n + 0.49) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.51) / 32 | V |

## 4.35 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DV_{CC(WRITE)}$ | Write supply voltage | | 2.0 | | 3.6 | V |
| $t_{WRITE}$ | Word or byte write time | | | | 120 | ns |
| $t_{ACCESS}$ | Read access time (1) | | | | 60 | ns |
| $t_{PRECHARGE}$ | Precharge time (1) | | | | 60 | ns |
| $t_{CYCLE}$ | Cycle time, read or write operation (1) | | 120 | | | ns |
| | Read and write endurance | | $10^{15}$ | | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | 100 | | | years |
| | | $T_J$ = 70°C | 40 | | | |
| | | $T_J$ = 85°C | 10 | | | |

(1) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* (SLAU272) for recommended settings for common system frequencies.

## 4.36 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

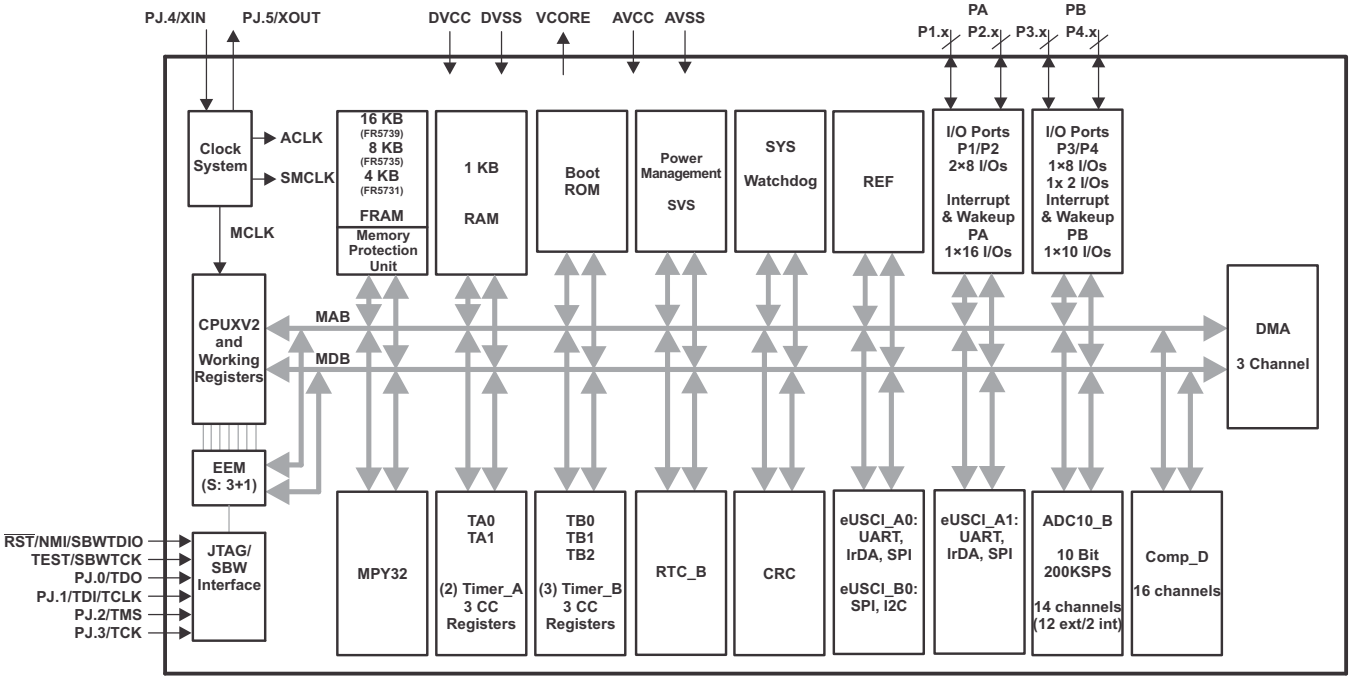
| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2 V, 3 V | 0.025 | | 15 | µs |
| $t_{SBW,\ En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1) | 2 V, 3 V | | | 1 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 18 | | 37 | µs |
| $f_{TCK}$ | TCK input frequency, 4-wire JTAG (2) | 2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2 V, 3 V | 19 | 35 | 51.5 | kΩ |

(1) Tools accessing the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

# 5 Detailed Description

## 5.1 Functional Block Diagram

This section shows the functional block diagram for the MSP430FR5739-EP in the RHA package.




## 5.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

## 5.3 Operating Modes

The MSP430 has one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

The following eight operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK active
  - MCLK disabled
  - SMCLK optionally active
  - Complete data retention
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK active
  - MCLK disabled
  - SMCLK optionally active
  - DCO disabled
  - Complete data retention
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - ACLK active
  - MCLK disabled
  - SMCLK optionally active
  - DCO disabled
  - Complete data retention
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - ACLK active
  - MCLK and SMCLK disabled
  - DCO disabled
  - Complete data retention
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK, MCLK, SMCLK disabled
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - RTC operation
  - Internal regulator disabled
  - No data retention
  - I/O pad state retention
  - Wakeup from $\overline{\text{RST}}$, general-purpose I/O, RTC events
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - I/O pad state retention
  - Wakeup from $\overline{\text{RST}}$ and general-purpose I/O

## 5.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 5-1. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power-Up, Brownout, Supply Supervisors<br>External Reset RST<br>Watchdog Timeout (Watchdog mode)<br>WDT, FRCTL MPU, CS, PMM Password Violation<br>FRAM double bit error detection<br>MPU segment violation<br>Software POR, BOR | SVSLIFG, SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW<br>DBDIFG<br>MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG<br>PMMPORIFG, PMMBORIFG<br>(SYSRSTIV) (1) (2) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>Vacant Memory Access<br>JTAG Mailbox<br>FRAM access time error<br>FRAM single, double bit error detection | VMAIFG<br>JMBNIFG, JMBOUTIFG<br>ACCTIMIFG<br>SBDIFG, DBDIFG<br>(SYSSNIV) (1) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>External NMI<br>Oscillator Fault | NMIIFG, OFIFG<br>(SYSUNIV) (1) (2) | (Non)maskable | 0FFFAh | 61 |
| Comparator_D | Comparator_D interrupt flags<br>(CBIV) (1) (3) | Maskable | 0FFF8h | 60 |
| TB0 | TB0CCR0 CCIFG0 (3) | Maskable | 0FFF6h | 59 |
| TB0 | TB0CCR1 CCIFG1 to TB0CCR2 CCIFG2, TB0IFG<br>(TB0IV) (1) (3) | Maskable | 0FFF4h | 58 |
| Watchdog Timer (Interval Timer Mode) | WDTIFG | Maskable | 0FFF2h | 57 |
| eUSCI_A0 Receive and Transmit | UCA0RXIFG, UCA0TXIFG (SPI mode)<br>UCA0STTIFG, UCA0TXCPTIFG, UCA0RXIFG, UXA0TXIFG (UART mode)<br>(UCA0IV) (1) (3) | Maskable | 0FFF0h | 56 |
| eUSCI_B0 Receive and Transmit | UCB0STTIFG, UCB0TXCPTIFG, UCB0RXIFG, UCB0TXIFG (SPI mode)<br>UCB0ALIFG, UCB0NACKIFG, UCB0STTIFG, UCB0STPIFG, UCB0RXIFG0, UCB0TXIFG0, UCB0RXIFG1, UCB0TXIFG1, UCB0RXIFG2, UCB0TXIFG2, UCB0RXIFG3, UCB0TXIFG3, UCB0CNTIFG, UCB0BIT9IFG (I2C mode)<br>(UCB0IV) (1) (3) | Maskable | 0FFEEh | 55 |
| ADC10_B | ADC10OVIFG, ADC10TOVIFG, ADC10HIIFG, ADC10LOIFG<br>ADC10INIFG, ADC10IFG0<br>(ADC10IV) (1) (3) (4) | Maskable | 0FFECh | 54 |
| TA0 | TA0CCR0 CCIFG0 (3) | Maskable | 0FFEAh | 53 |
| TA0 | TA0CCR1 CCIFG1 to TA0CCR2 CCIFG2, TA0IFG<br>(TA0IV) (1) (3) | Maskable | 0FFE8h | 52 |

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Only on devices with ADC, otherwise reserved.

**Table 5-1. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| eUSCI_A1 Receive and Transmit | UCA1RXIFG, UCA1TXIFG (SPI mode) UCA1STTIFG, UCA1TXCPTIFG, UCA1RXIFG, UXA1TXIFG (UART mode) (UCA1IV) (1) (3) | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) (1) (3) | Maskable | 0FFE4h | 50 |
| TA1 | TA1CCR0 CCIFG0 (3) | Maskable | 0FFE2h | 49 |
| TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) (1) (3) | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) (1) (3) | Maskable | 0FFDEh | 47 |
| TB1 | TB1CCR0 CCIFG0 (3) | Maskable | 0FFDCh | 46 |
| TB1 | TB1CCR1 CCIFG1 to TB1CCR2 CCIFG2, TB1IFG (TB1IV) (1) (3) | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) (1) (3) | Maskable | 0FFD8h | 44 |
| TB2 | TB2CCR0 CCIFG0 (3) | Maskable | 0FFD6h | 43 |
| TB2 | TB2CCR1 CCIFG1 to TB2CCR2 CCIFG2, TB2IFG (TB2IV) (1) (3) | Maskable | 0FFD4h | 42 |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV) (1) (3) | Maskable | 0FFD2h | 41 |
| I/O Port P4 | P4IFG.0 to P4IFG.2 (P4IV) (1) (3) | Maskable | 0FFD0h | 40 |
| RTC_B | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) (1) (3) | Maskable | 0FFCEh | 39 |
| Reserved | Reserved (5) | | 0FFCCh<br>⋮<br>0FF80h | 38<br>⋮<br>0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

## 5.5 Memory Organization

Table 5-2 describes the memory organization.

**Table 5-2. Memory Organization(1)(2)**

| | | MSP430FR5739-EP |
|---|---|---|
| Memory (FRAM)<br>Main: interrupt vectors<br>Main: code memory | Total Size | 15.5 KB<br>00FFFFh–00FF80h<br>00FF7Fh–00C200h |
| RAM | | 1 KB<br>001FFFh–001C00h |
| Device Descriptor Info (TLV) (FRAM) | | 128 B<br>001A7Fh–001A00h |
| Information memory (FRAM) | N/A | 0019FFh–001980h<br>Address space mirrored to Info A |
| | N/A | 00197Fh–001900h<br>Address space mirrored to Info B |
| | Info A | 128 B<br>0018FFh–001880h |
| | Info B | 128 B<br>00187Fh–001800h |
| Bootstrap loader (BSL) memory (ROM) | BSL 3 | 512 B<br>0017FFh–001600h |
| | BSL 2 | 512 B<br>0015FFh–001400h |
| | BSL 1 | 512 B<br>0013FFh–001200h |
| | BSL 0 | 512 B<br>0011FFh–001000h |
| Peripherals | Size | 4 KB<br>000FFFh–0h |

(1) N/A = Not available
(2) All address space not listed in this table is considered vacant memory.

## 5.6 Bootstrap Loader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface. Access to the device memory by the BSL is protected by an user-defined password. Use of the BSL requires four pins (see Table 5-3). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

**Table 5-3. BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P2.0 | Data transmit |
| P2.1 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

## 5.7 JTAG Operation

### 5.7.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are summarized in Table 5-4. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

**Table 5-4. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

### 5.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are summarized in Table 5-5. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

**Table 5-5. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| VCC | | Power supply |
| VSS | | Ground supply |

## 5.8 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Low-power ultra-fast write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait state generation
- Error Correction Coding (ECC) with single bit detection and correction, double bit detection

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see the application report *MSP430™ FRAM Technology – How To and Best Practices* (SLAA628).

## 5.9 Memory Protection Unit (MPU)

The FRAM can be protected from inadvertent CPU execution or write access by the MPU. Features of the MPU include:

- Main memory partitioning programmable up to three segments
- Each segment's (main and information memory) access rights can be individually selected
- Access violation flags with interrupt capability for easy servicing of access violations

## 5.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430FR57xx Family User's Guide* (SLAU272).

### 5.10.1 Digital I/O

There are up to four 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all ports.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

### 5.10.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF mode), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT1 (HF mode). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1 LF mode), a high-frequency crystal (XT1 HF mode), the internal VLO, or the internal DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by the same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by the same sources made available to ACLK.

### 5.10.3 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary and core supplies.

### 5.10.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 5.10.5 Real-Time Clock (RTC_B)

The RTC_B module contains an integrated real-time clock (RTC) (calendar mode). Calendar mode integrates an internal calendar which compensates for months with fewer than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 mode to minimize power consumption.

### 5.10.6 Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### 5.10.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.

**Table 5-6. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| **SYSRSTIV, System Reset** | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG $\overline{\text{RST}}$/NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wake up (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSLIFG SVSL event (BOR) | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog timeout (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | DBDIFG FRAM double bit error (PUC) | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | MPUPW MPU password violation (PUC) | 22h | |
| | | CSPW CS password violation (PUC) | 24h | |
| | | MPUSEGIIFG information memory segment violation (PUC) | 26h | |
| | | MPUSEG1IFG segment 1 memory violation (PUC) | 28h | |
| | | MPUSEG2IFG segment 2 memory violation (PUC) | 2Ah | |
| | | MPUSEG3IFG segment 3 memory violation (PUC) | 2Ch | |
| | | Reserved | 2Eh | |
| | | Reserved | 30h to 3Eh | Lowest |
| **SYSSNIV, System NMI** | 019Ch | No interrupt pending | 00h | |
| | | DBDIFG FRAM double bit error | 02h | Highest |
| | | ACCTIMIFG access time error | 04h | |
| | | Reserved | 0Eh | |
| | | VMAIFG Vacant memory access | 10h | |
| | | JMBINIFG JTAG mailbox input | 12h | |
| | | JMBOUTIFG JTAG mailbox output | 14h | |
| | | SBDIFG FRAM single bit error | 16h | |
| | | Reserved | 18h to 1Eh | Lowest |
| **SYSUNIV, User NMI** | 019Ah | No interrupt pending | 00h | |
| | | NMIFG NMI pin | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah to 1Eh | Lowest |

### 5.10.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

**Table 5-7. DMA Trigger Assignments (1)**

| TRIGGER | CHANNEL 0 | CHANNEL 1 | CHANNEL 2 |
|---|---|---|---|
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | Reserved | Reserved | Reserved |
| 6 | Reserved | Reserved | Reserved |
| 7 | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 8 | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 9 | TB1CCR0 CCIFG (2) | TB1CCR0 CCIFG (2) | TB1CCR0 CCIFG (2) |
| 10 | TB1CCR2 CCIFG (2) | TB1CCR2 CCIFG (2) | TB1CCR2 CCIFG (2) |
| 11 | TB2CCR0 CCIFG (3) | TB2CCR0 CCIFG (3) | TB2CCR0 CCIFG (3) |
| 12 | TB2CCR2 CCIFG (3) | TB2CCR2 CCIFG (3) | TB2CCR2 CCIFG (3) |
| 13 | Reserved | Reserved | Reserved |
| 14 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 15 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 16 | UCA1RXIFG (4) | UCA1RXIFG (4) | UCA1RXIFG (4) |
| 17 | UCA1TXIFG (4) | UCA1TXIFG (4) | UCA1TXIFG (4) |
| 18 | UCB0RXIFG0 | UCB0RXIFG0 | UCB0RXIFG0 |
| 19 | UCB0TXIFG0 | UCB0TXIFG0 | UCB0TXIFG0 |
| 20 | UCB0RXIFG1 | UCB0RXIFG1 | UCB0RXIFG1 |
| 21 | UCB0TXIFG1 | UCB0TXIFG1 | UCB0TXIFG1 |
| 22 | UCB0RXIFG2 | UCB0RXIFG2 | UCB0RXIFG2 |
| 23 | UCB0TXIFG2 | UCB0TXIFG2 | UCB0TXIFG2 |
| 24 | UCB0RXIFG3 | UCB0RXIFG3 | UCB0RXIFG3 |
| 25 | UCB0TXIFG3 | UCB0TXIFG3 | UCB0TXIFG3 |
| 26 | ADC10IFGx (5) | ADC10IFGx (5) | ADC10IFGx (5) |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

(1) If a reserved trigger source is selected, no trigger is generated.
(2) Only on devices with TB1, otherwise reserved
(3) Only on devices with TB2, otherwise reserved
(4) Only on devices with eUSCI_A1, otherwise reserved
(5) Only on devices with ADC, otherwise reserved

### 5.10.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each eUSCI module contains two portions, A and B.

The eUSCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430FR5739-EP series include one or two eUSCI_An modules (eUSCI_A0, eUSCI_A1) and one eUSCI_Bn module (eUSCI_B).

### 5.10.10 TA0, TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. Each can support multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 5-8. TA0 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 3-P1.2 | TA0CLK | TACLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| 3-P1.2 | TA0CLK | $\overline{\text{TACLK}}$ | | | | |
| 28-P1.6 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 28-P1.6 |
| 34-P2.3 | TA0.0 | CCI0B | | | | 34-P2.3 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 1-P1.0 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 1-P1.0 |
| | CDOUT (internal) | CCI1B | | | | ADC10 (internal) (1) ADC10SHSx = {1} |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 2-P1.1 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 2-P1.1 |
| | ACLK (internal) | CCI2B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

(1) Only on devices with ADC

## Table 5-9. TA1 Signal Connections

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 2-P1.1 | TA1CLK | TACLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| 2-P1.1 | TA1CLK | $\overline{\text{TACLK}}$ | | | | |
| 29-P1.7 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | 29-P1.7 |
| 35-P2.4 | TA1.0 | CCI0B | | | | 35-P2.4 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 3-P1.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 3-P1.2 |
| | CDOUT (internal) | CCI1B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 8-P1.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 8-P1.3 |
| | ACLK (internal) | CCI2B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

### 5.10.11 TB0, TB1, TB2

TB0, TB1, and TB2 are 16-bit timers/counters (Timer_B type) with three capture/compare registers each. Each can support multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 5-10. TB0 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 21-P2.0 | TB0CLK | TBCLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| 21-P2.0 | TB0CLK | $\overline{\text{TBCLK}}$ | | | | |
| 22-P2.1 | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | 22-P2.1 |
| 17-P2.5 | TB0.0 | CCI0B | | | | 17-P2.5 |
| | $DV_{SS}$ | GND | | | | ADC10 (internal) (1) ADC10SHSx = {2} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 9-P1.4 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 9-P1.4 |
| | CDOUT (internal) | CCI1B | | | | ADC10 (internal) (1) ADC10SHSx = {3} |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 10-P1.5 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 10-P1.5 |
| | ACLK (internal) | CCI2B | | | | |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

(1) Only on devices with ADC

## Table 5-11. TB1 Signal Connections (1)

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 26-P3.6 | TB1CLK | TBCLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| 26-P3.6 | TB1CLK | $\overline{\text{TBCLK}}$ | | | | |
| 23-P2.2 | TB1.0 | CCI0A | CCR0 | TB0 | TB1.0 | 23-P2.2 |
| 18-P2.6 | TB1.0 | CCI0B | | | | 18-P2.6 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 28-P1.6 | TB1.1 | CCI1A | CCR1 | TB1 | TB1.1 | 28-P1.6 |
| 24-P3.4 | TB1.1 | CCI1B | | | | 24-P3.4 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 29-P1.7 | TB1.2 | CCI2A | CCR2 | TB2 | TB1.2 | 29-P1.7 |
| 25-P3.5 | TB1.2 | CCI2B | | | | 25-P3.5 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

(1) TB1 is not present on all device types.

## Table 5-12. TB2 Signal Connections (1)

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|---|
| 24-P3.4 | TB2CLK | TBCLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| 24-P3.4 | TB2CLK | $\overline{\text{TBCLK}}$ | | | | |
| 21-P2.0 | TB2.0 | CCI0A | CCR0 | TB0 | TB2.0 | 21-P2.0 |
| 15-P4.0 | TB2.0 | CCI0B | | | | 15-P4.0 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 22-P2.1 | TB2.1 | CCI1A | CCR1 | TB1 | TB2.1 | 22-P2.1 |
| 26-P3.6 | TB2.1 | CCI1B | | | | 26-P3.6 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| 23-P2.2 | TB2.2 | CCI2A | CCR2 | TB2 | TB2.2 | 23-P2.2 |
| 27-P3.7 | TB2.2 | CCI2B | | | | 27-P3.7 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

(1) TB2 is not present on all device types.

### 5.10.12 ADC10_B

The ADC10_B module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with a lower limit and an upper limit allows CPU-independent result monitoring with three window comparator interrupt flags.

### 5.10.13 Comparator_D

The primary function of the Comparator_D module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### 5.10.14 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### 5.10.15 Shared Reference (REF)

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

### 5.10.16 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

### 5.10.17 Peripheral File Map

Table 5-13 provides the base address and offset range of all available peripherals.

**Table 5-13. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| Special Functions (see Table 5-14) | 0100h | 000h-01Fh |
| PMM (see Table 5-15) | 0120h | 000h-010h |
| FRAM Control (see Table 5-16) | 0140h | 000h-00Fh |
| CRC16 (see Table 5-17) | 0150h | 000h-007h |
| Watchdog (see Table 5-18) | 015Ch | 000h-001h |
| CS (see Table 5-19) | 0160h | 000h-00Fh |
| SYS (see Table 5-20) | 0180h | 000h-01Fh |
| Shared Reference (see Table 5-21) | 01B0h | 000h-001h |
| Port P1, P2 (see Table 5-22) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 5-23) | 0220h | 000h-01Fh |
| Port PJ (see Table 5-24) | 0320h | 000h-01Fh |
| TA0 (see Table 5-25) | 0340h | 000h-02Fh |
| TA1 (see Table 5-26) | 0380h | 000h-02Fh |
| TB0 (see Table 5-27) | 03C0h | 000h-02Fh |
| TB1 (see Table 5-28) | 0400h | 000h-02Fh |
| TB2 (see Table 5-29) | 0440h | 000h-02Fh |
| Real-Time Clock (RTC_B) (see Table 5-30) | 04A0h | 000h-01Fh |
| 32-Bit Hardware Multiplier (see Table 5-31) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 5-32) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 5-32) | 0510h | 000h-00Ah |
| DMA Channel 1 (see Table 5-32) | 0520h | 000h-00Ah |
| DMA Channel 2 (see Table 5-32) | 0530h | 000h-00Ah |
| MPU Control (see Table 5-33) | 05A0h | 000h-00Fh |
| eUSCI_A0 (see Table 5-34) | 05C0h | 000h-01Fh |
| eUSCI_A1 (see Table 5-35) | 05E0h | 000h-01Fh |
| eUSCI_B0 (see Table 5-36) | 0640h | 000h-02Fh |
| ADC10_B (see Table 5-37) | 0700h | 000h-03Fh |
| Comparator_D (see Table 5-38) | 08C0h | 000h-00Fh |

**Table 5-14. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**Table 5-15. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 Control 0 | PM5CTL0 | 10h |

**Table 5-16. FRAM Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| FRAM control 0 | FRCTLCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

**Table 5-17. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

**Table 5-18. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**Table 5-19. CS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |

**Table 5-20. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

**Table 5-21. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

**Table 5-22. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Dh |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

**Table 5-23. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P3 selection 1 | P3SEL1 | 0Ch |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 complement selection | P3SELC | 16h |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 selection 0 | P4SEL0 | 0Bh |
| Port P4 selection 1 | P4SEL1 | 0Dh |
| Port P4 complement selection | P4SELC | 17h |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

**Table 5-24. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ selection 0 | PJSEL0 | 0Ah |
| Port PJ selection 1 | PJSEL1 | 0Ch |
| Port PJ complement selection | PJSELC | 16h |

**Table 5-25. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter register | TA0R | 10h |
| Capture/compare register 0 | TA0CCR0 | 12h |
| Capture/compare register 1 | TA0CCR1 | 14h |
| Capture/compare register 2 | TA0CCR2 | 16h |
| TA0 expansion register 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

**Table 5-26. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter register | TA1R | 10h |
| Capture/compare register 0 | TA1CCR0 | 12h |
| Capture/compare register 1 | TA1CCR1 | 14h |
| Capture/compare register 2 | TA1CCR2 | 16h |
| TA1 expansion register 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**Table 5-27. TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| TB0 register | TB0R | 10h |
| Capture/compare register 0 | TB0CCR0 | 12h |
| Capture/compare register 1 | TB0CCR1 | 14h |
| Capture/compare register 2 | TB0CCR2 | 16h |
| TB0 expansion register 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

**Table 5-28. TB1 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB1 control | TB1CTL | 00h |
| Capture/compare control 0 | TB1CCTL0 | 02h |
| Capture/compare control 1 | TB1CCTL1 | 04h |
| Capture/compare control 2 | TB1CCTL2 | 06h |
| TB1 register | TB1R | 10h |
| Capture/compare register 0 | TB1CCR0 | 12h |
| Capture/compare register 1 | TB1CCR1 | 14h |
| Capture/compare register 2 | TB1CCR2 | 16h |
| TB1 expansion register 0 | TB1EX0 | 20h |
| TB1 interrupt vector | TB1IV | 2Eh |

**Table 5-29. TB2 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB2 control | TB2CTL | 00h |
| Capture/compare control 0 | TB2CCTL0 | 02h |
| Capture/compare control 1 | TB2CCTL1 | 04h |
| Capture/compare control 2 | TB2CCTL2 | 06h |
| TB2 register | TB2R | 10h |
| Capture/compare register 0 | TB2CCR0 | 12h |
| Capture/compare register 1 | TB2CCR1 | 14h |
| Capture/compare register 2 | TB2CCR2 | 16h |
| TB2 expansion register 0 | TB2EX0 | 20h |
| TB2 interrupt vector | TB2IV | 2Eh |

**Table 5-30. Real-Time Clock Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds, RTC counter register 1 | RTCSEC, RTCNT1 | 10h |
| RTC minutes, RTC counter register 2 | RTCMIN, RTCNT2 | 11h |
| RTC hours, RTC counter register 3 | RTCHOUR, RTCNT3 | 12h |
| RTC day of week, RTC counter register 4 | RTCDOW, RTCNT4 | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion register | BIN2BCD | 1Ch |
| BCD-to-binary conversion register | BCD2BIN | 1Eh |

**Table 5-31. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

**Table 5-32. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Ah |

**Table 5-33. MPU Control Registers (Base Address: 05A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| MPU control 0 | MPUCTL0 | 00h |
| MPU control 1 | MPUCTL1 | 02h |
| MPU Segmentation Register | MPUSEG | 04h |
| MPU access management | MPUSAM | 06h |

**Table 5-34. eUSCI_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI _A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA0BR0 | 06h |
| eUSCI_A baud rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

**Table 5-35. eUSCI_A1 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI _A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA1BR0 | 06h |
| eUSCI_A baud rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

**Table 5-36. eUSCI_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B received address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI I2C slave address | UCB0I2CSA | 20h |
| eUSCI interrupt enable | UCB0IE | 2Ah |
| eUSCI interrupt flags | UCB0IFG | 2Ch |
| eUSCI interrupt vector word | UCB0IV | 2Eh |

**Table 5-37. ADC10_B Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC10_B Control register 0 | ADC10CTL0 | 00h |
| ADC10_B Control register 1 | ADC10CTL1 | 02h |
| ADC10_B Control register 2 | ADC10CTL2 | 04h |
| ADC10_B Window Comparator Low Threshold | ADC10LO | 06h |
| ADC10_B Window Comparator High Threshold | ADC10HI | 08h |
| ADC10_B Memory Control Register 0 | ADC10MCTL0 | 0Ah |
| ADC10_B Conversion Memory Register | ADC10MEM0 | 12h |
| ADC10_B Interrupt Enable | ADC10IE | 1Ah |
| ADC10_B Interrupt Flags | ADC10IGH | 1Ch |
| ADC10_B Interrupt Vector Word | ADC10IV | 1Eh |

**Table 5-38. Comparator_D Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comparator_D control register 0 | CDCTL0 | 00h |
| Comparator_D control register 1 | CDCTL1 | 02h |
| Comparator_D control register 2 | CDCTL2 | 04h |
| Comparator_D control register 3 | CDCTL3 | 06h |
| Comparator_D interrupt register | CDINT | 0Ch |
| Comparator_D interrupt vector word | CDIV | 0Eh |

# 6 Input/Output Schematics

## 6.1 Port P1, P1.0 to P1.2, Input/Output With Schmitt Trigger

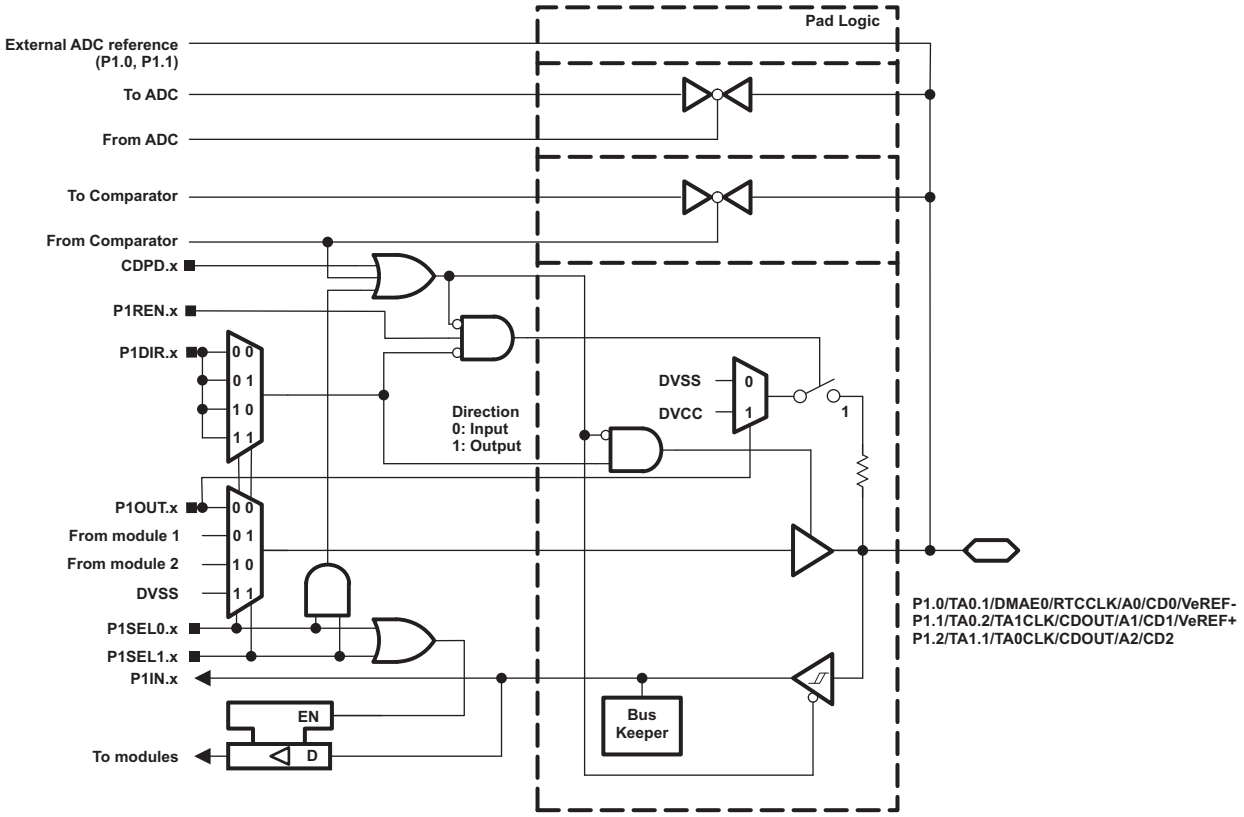


**Table 6-1. Port P1 (P1.0 to P1.2) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA0.1/DMAE0/RTCCLK/A0/CD0/VeREF- | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI1A | 0 | 0 | 1 |
| | | TA0.1 | 1 | | |
| | | DMAE0 | 0 | 1 | 0 |
| | | RTCCLK | 1 | | |
| | | A0 (1) (2)<br>CD0 (1) (3)<br>VeREF- (1) (2) | X | 1 | 1 |
| P1.1/TA0.2/TA1CLK/CDOUT/A1/CD1/VeREF+ | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI2A | 0 | 0 | 1 |
| | | TA0.2 | 1 | | |
| | | TA1CLK | 0 | 1 | 0 |
| | | CDOUT | 1 | | |
| | | A1 (1) (2)<br>CD1 (1) (3)<br>VeREF+ (1) (2) | X | 1 | 1 |
| P1.2/TA1.1/TA0CLK/CDOUT/A2/CD2 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | | |
| | | TA0CLK | 0 | 1 | 0 |
| | | CDOUT | 1 | | |
| | | A2 (1) (2)<br>CD2 (1) (3) | X | 1 | 1 |

(1) Setting P1SEL1.x and P1SEL0.x disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) Not available on all devices and package types.
(3) Setting the CDPD.x bit of the comparator disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

## 6.2 Port P1, P1.3 to P1.5, Input/Output With Schmitt Trigger

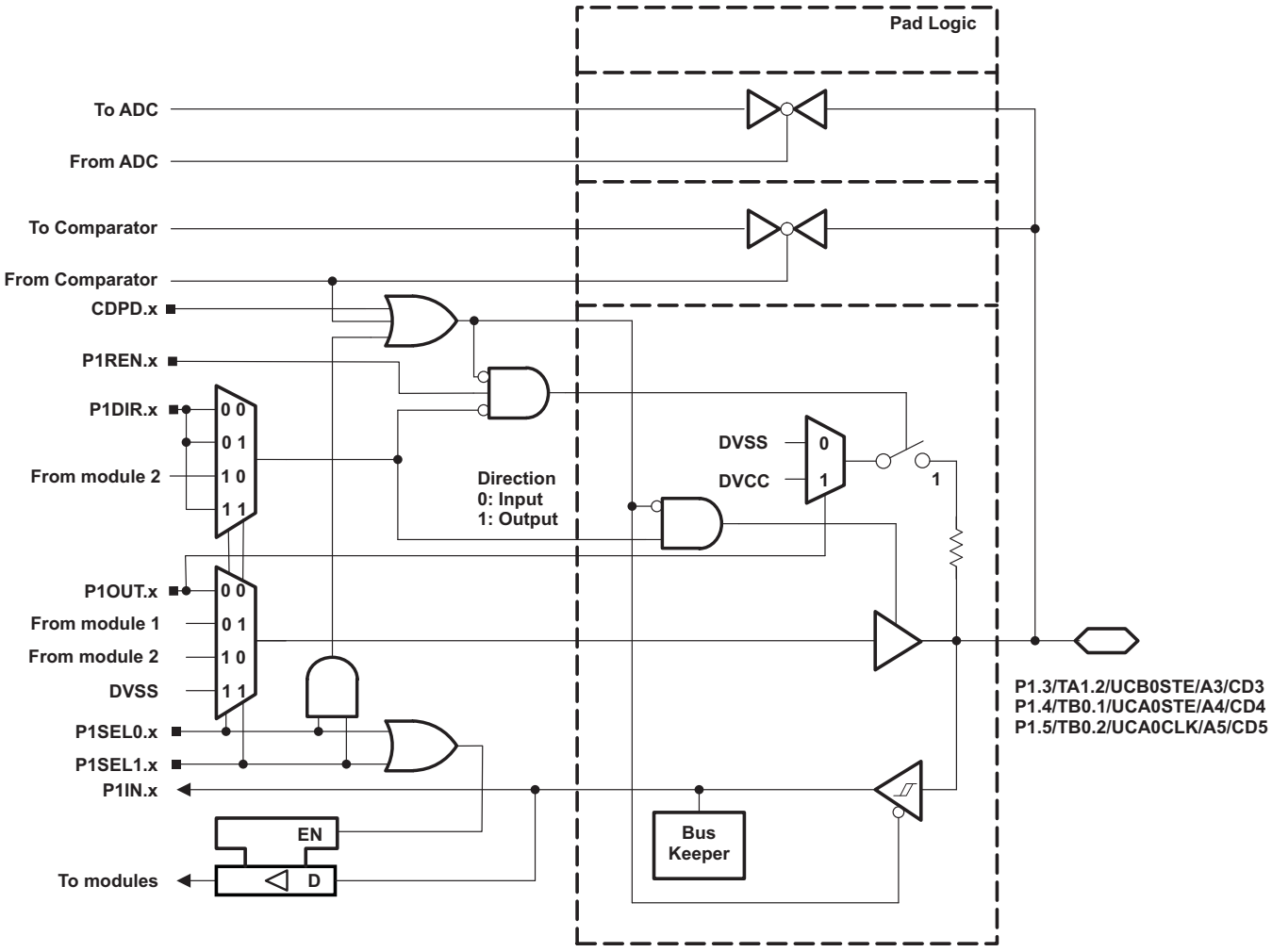


**Table 6-2. Port P1 (P1.3 to P1.5) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.3/TA1.2/UCB0STE/A3/CD3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI2A | 0 | 0 | 1 |
| | | TA1.2 | 1 | | |
| | | UCB0STE | X (1) | 1 | 0 |
| | | A3 (2) (3)<br>CD3 (2) (4) | X | 1 | 1 |
| P1.4/TB0.1/UCA0STE/A4/CD4 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI1A | 0 | 0 | 1 |
| | | TB0.1 | 1 | | |
| | | UCA0STE | X (5) | 1 | 0 |
| | | A4 (2) (3)<br>CD4 (2) (4) | X | 1 | 1 |
| P1.5/TB0.2/UCA0CLK/A5/CD5 | 5 | P1.5(I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI2A | 0 | 0 | 1 |
| | | TB0.2 | 1 | | |
| | | UCA0CLK | X (5) | 1 | 0 |
| | | A5 (2) (3)<br>CD5 (2) (4) | X | 1 | 1 |

(1) Direction controlled by eUSCI_B0 module.
(2) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit
(5) Direction controlled by eUSCI_A0 module.

## 6.3 Port P1, P1.6 to P1.7, Input/Output With Schmitt Trigger

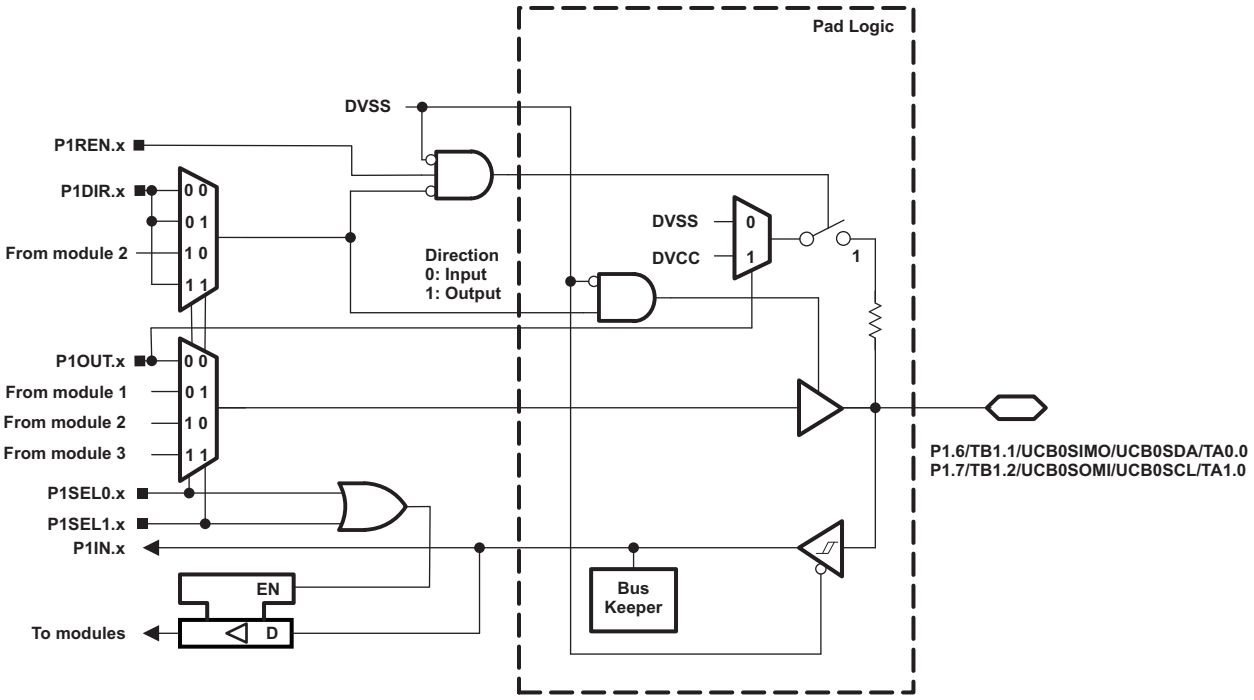



**Table 6-3. Port P1 (P1.6 to P1.7) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.6/TB1.1/UCB0SIMO/UCB0SDA/TA0.0 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI1A (1) | 0 | 0 | 1 |
| | | TB1.1 (1) | 1 | | |
| | | UCB0SIMO/UCB0SDA | X (2) | 1 | 0 |
| | | TA0.CCI0A | 0 | 1 | 1 |
| | | TA0.0 | 1 | | |
| P1.7/TB1.2/UCB0SOMI/UCB0SCL/TA1.0 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI2A (1) | 0 | 0 | 1 |
| | | TB1.2 (1) | 1 | | |
| | | UCB0SOMI/UCB0SCL | X (2) | 1 | 0 |
| | | TA1.CCI0A | 0 | 1 | 1 |
| | | TA1.0 | 1 | | |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_B0 module.

## 6.4 Port P2, P2.0 to P2.2, Input/Output With Schmitt Trigger

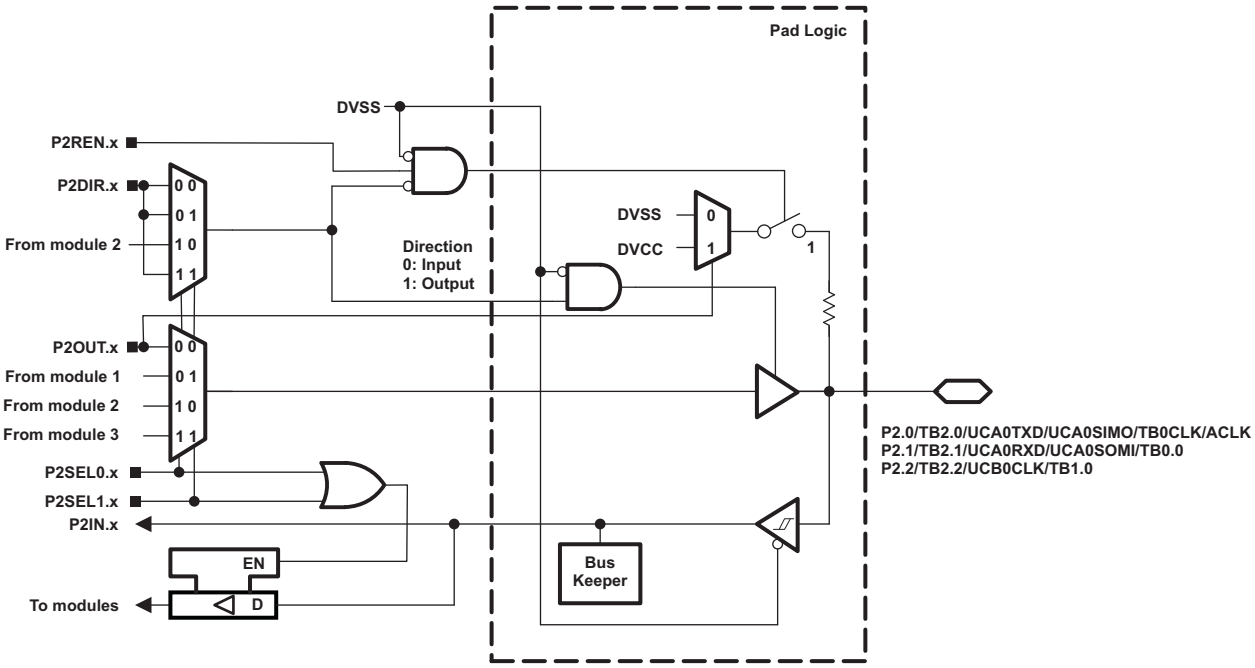



**Table 6-4. Port P2 (P2.0 to P2.2) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.0/TB2.0/UCA0TXD/UCA0SIMO/TB0CLK/ACLK | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI0A (1) | 0 | 0 | 1 |
| | | TB2.0 (1) | 1 | | |
| | | UCA0TXD/UCA0SIMO | X (2) | 1 | 0 |
| | | TB0CLK | 0 | 1 | 1 |
| | | ACLK | 1 | | |
| P2.1/TB2.1/UCA0RXD/UCA0SOMI/TB0.0 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI1A (1) | 0 | 0 | 1 |
| | | TB2.1 (1) | 1 | | |
| | | UCA0RXD/UCA0SOMI | X (2) | 1 | 0 |
| | | TB0.CCI0A | 0 | 1 | 1 |
| | | TB0.0 | 1 | | |
| P2.2/TB2.2/UCB0CLK/TB1.0 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI2A (1) | 0 | 0 | 1 |
| | | TB2.2 (1) | 1 | | |
| | | UCB0CLK | X (3) | 1 | 0 |
| | | TB1.CCI0A (1) | 0 | 1 | 1 |
| | | TB1.0 (1) | 1 | | |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_B0 module.

## 6.5 Port P2, P2.3 to P2.4, Input/Output With Schmitt Trigger

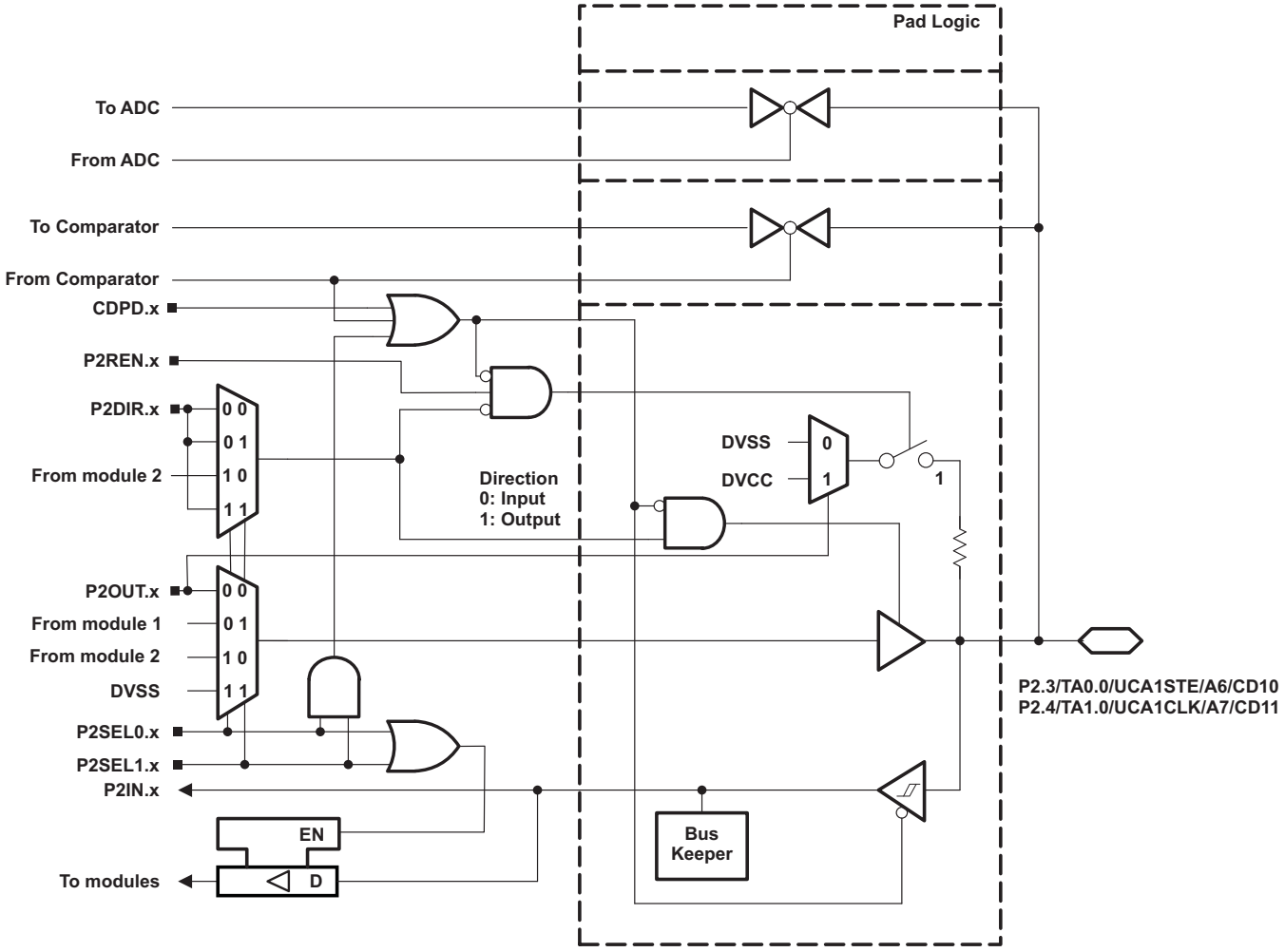


**Table 6-5. Port P2 (P2.3 to P2.4) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.3/TA0.0/UCA1STE/A6/CD10 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI0B | 0 | 0 | 1 |
| | | TA0.0 | 1 | | |
| | | UCA1STE | X (1) | 1 | 0 |
| | | A6 (2) (3)<br>CD10 (2) (4) | X | 1 | 1 |
| P2.4/TA1.0/UCA1CLK/A7/CD11 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI0B | 0 | 0 | 1 |
| | | TA1.0 | 1 | | |
| | | UCA1CLK | X (1) | 1 | 0 |
| | | A7 (2) (3)<br>CD11 (2) (4) | X | 1 | 1 |

(1) Direction controlled by eUSCI_A1 module.
(2) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

## 6.6 Port P2, P2.5 to P2.6, Input/Output With Schmitt Trigger

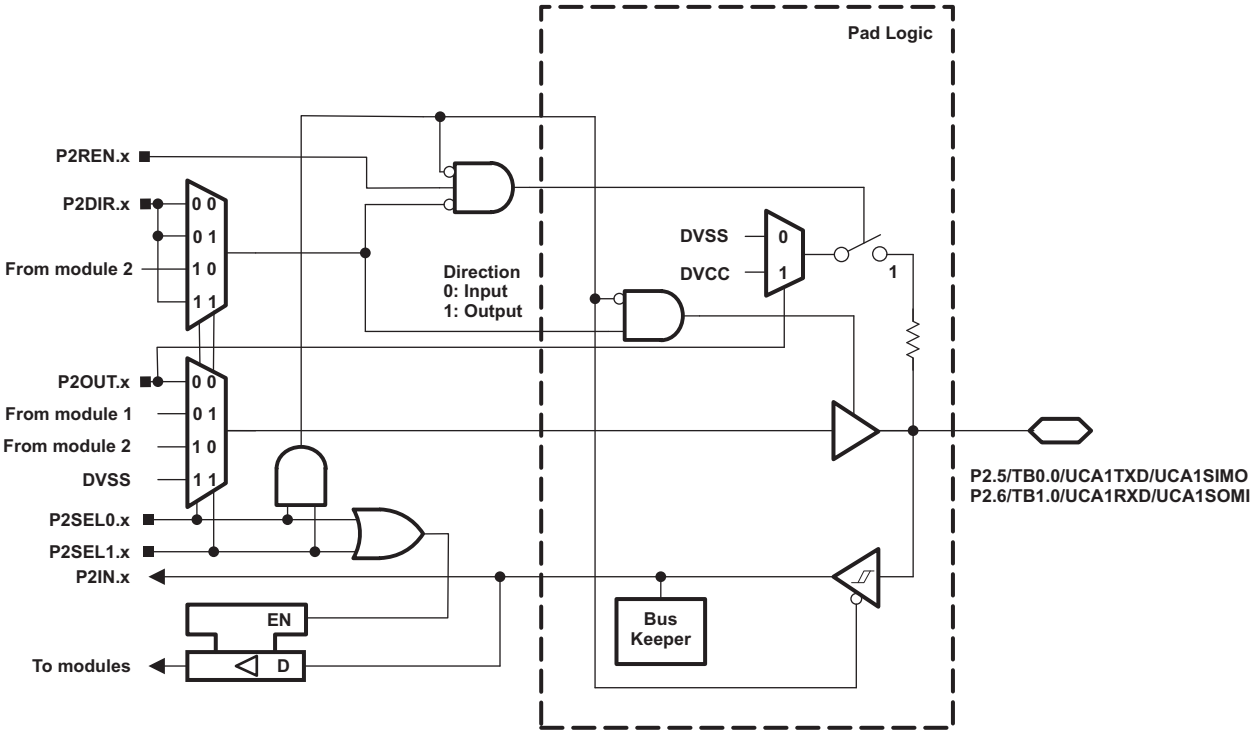



**Table 6-6. Port P2 (P2.5 to P2.6) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.5/TB0.0/UCA1TXD/UCA1SIMO | 5 | P2.5(I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI0B (1) | 0 | 0 | 1 |
| | | TB0.0 (1) | 1 | | |
| | | UCA1TXD/UCA1SIMO (1) | X (2) | 1 | 0 |
| P2.6/TB1.0/UCA1RXD/UCA1SOMI | 6 | P2.6(I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI0B (1) | 0 | 0 | 1 |
| | | TB1.0 (1) | 1 | | |
| | | UCA1RXD/UCA1SOMI (1) | X (2) | 1 | 0 |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_A1 module.

## 6.7 Port P2, P2.7, Input/Output With Schmitt Trigger

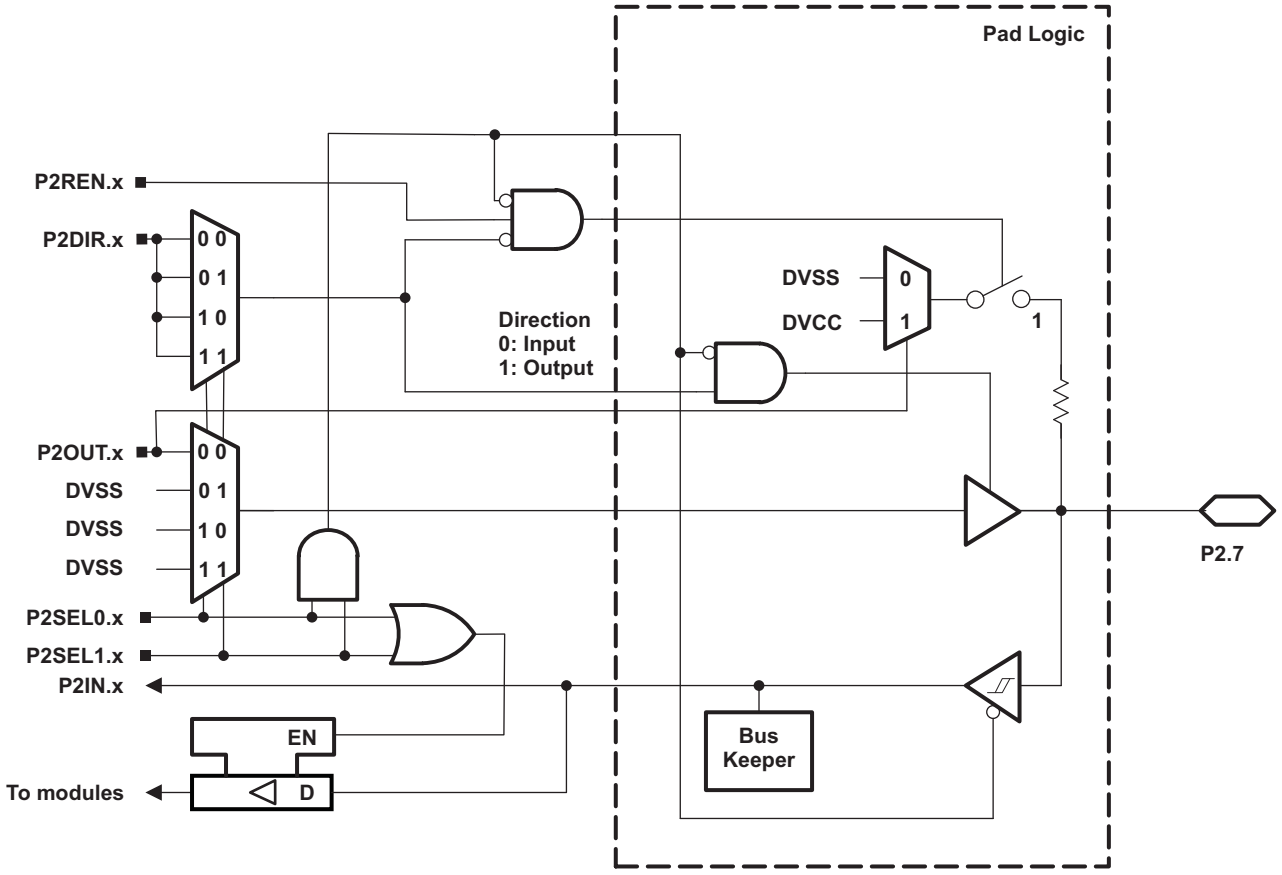



**Table 6-7. Port P2 (P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.7 | 7 | P2.7(I/O) (1) | I: 0; O: 1 | 0 | 0 |

(1) Not available on all devices and package types.

## 6.8 Port P3, P3.0 to P3.3, Input/Output With Schmitt Trigger

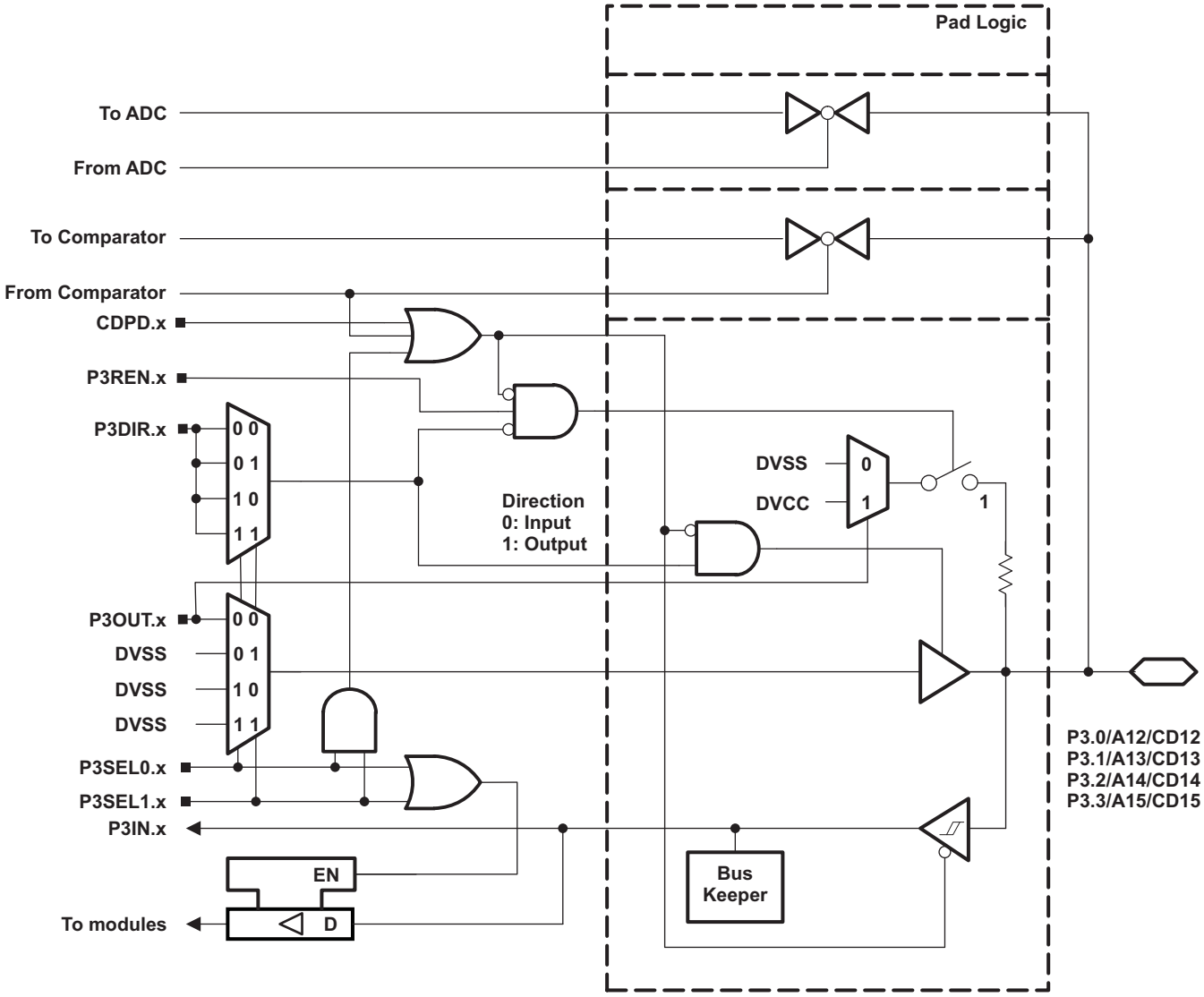


**Table 6-8. Port P3 (P3.0 to P3.3) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.0/A12/CD12 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A12 (1) (2)<br>CD12 (1) (3) | X | 1 | 1 |
| P3.1/A13/CD13 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A13 (1) (2)<br>CD13 (1) (3) | X | 1 | 1 |
| P3.2/A14/CD14 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A14 (1) (2)<br>CD14 (1) (3) | X | 1 | 1 |
| P3.3/A15/CD15 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A15 (1) (2)<br>CD15 (1) (3) | X | 1 | 1 |

(1) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) Not available on all devices and package types.
(3) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

## 6.9 Port P3, P3.4 to P3.6, Input/Output With Schmitt Trigger

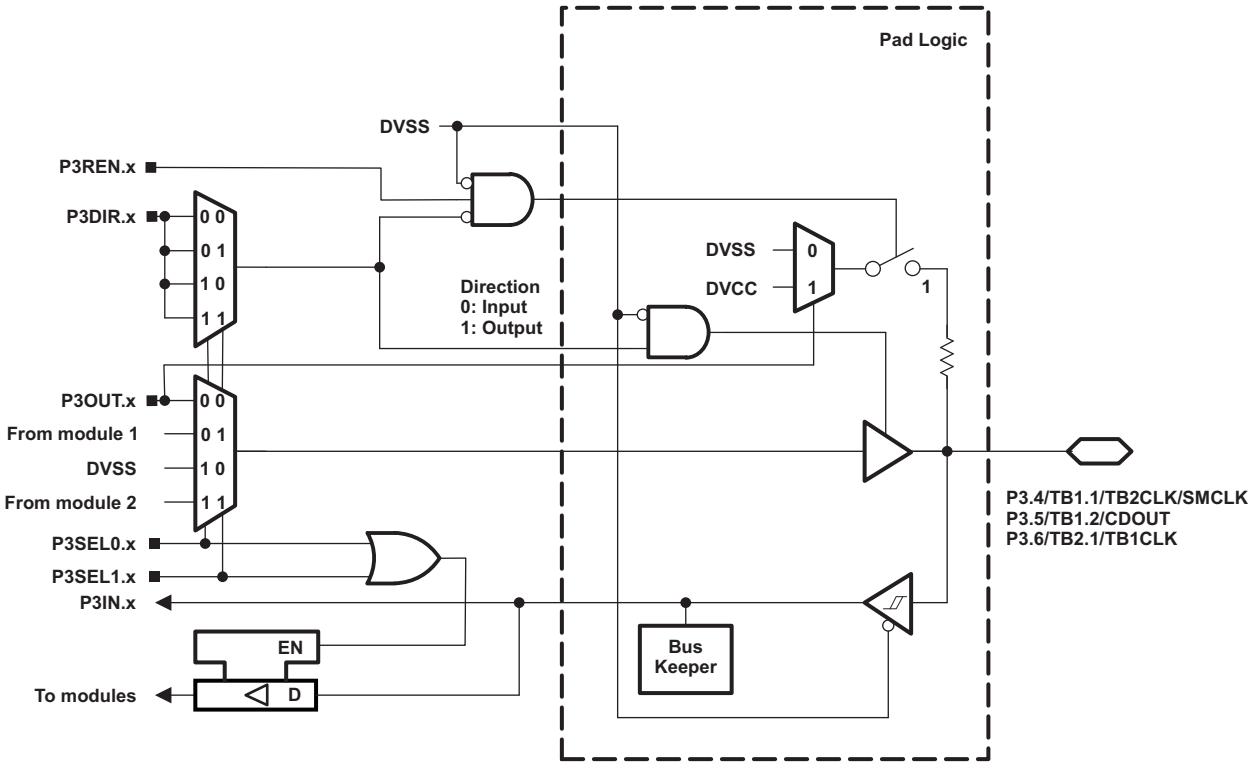



**Table 6-9. Port P3 (P3.4 to P3.6) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.4/TB1.1/TB2CLK/SMCLK | 4 | P3.4 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI1B (1) | 0 | 0 | 1 |
| | | TB1.1 (1) | 1 | | |
| | | TB2CLK (1) | 0 | 1 | 1 |
| | | SMCLK (1) | 1 | | |
| P3.5/TB1.2/CDOUT | 5 | P3.5 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI2B (1) | 0 | 0 | 1 |
| | | TB1.2 (1) | 1 | | |
| | | CDOUT (1) | 1 | 1 | 1 |
| P3.6/TB2.1/TB1CLK | 6 | P3.6 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI1B (1) | 0 | 0 | 1 |
| | | TB2.1 (1) | 1 | | |
| | | TB1CLK (1) | 0 | 1 | 1 |

(1) Not available on all devices and package types.

## 6.10 Port P3, P3.7, Input/Output With Schmitt Trigger

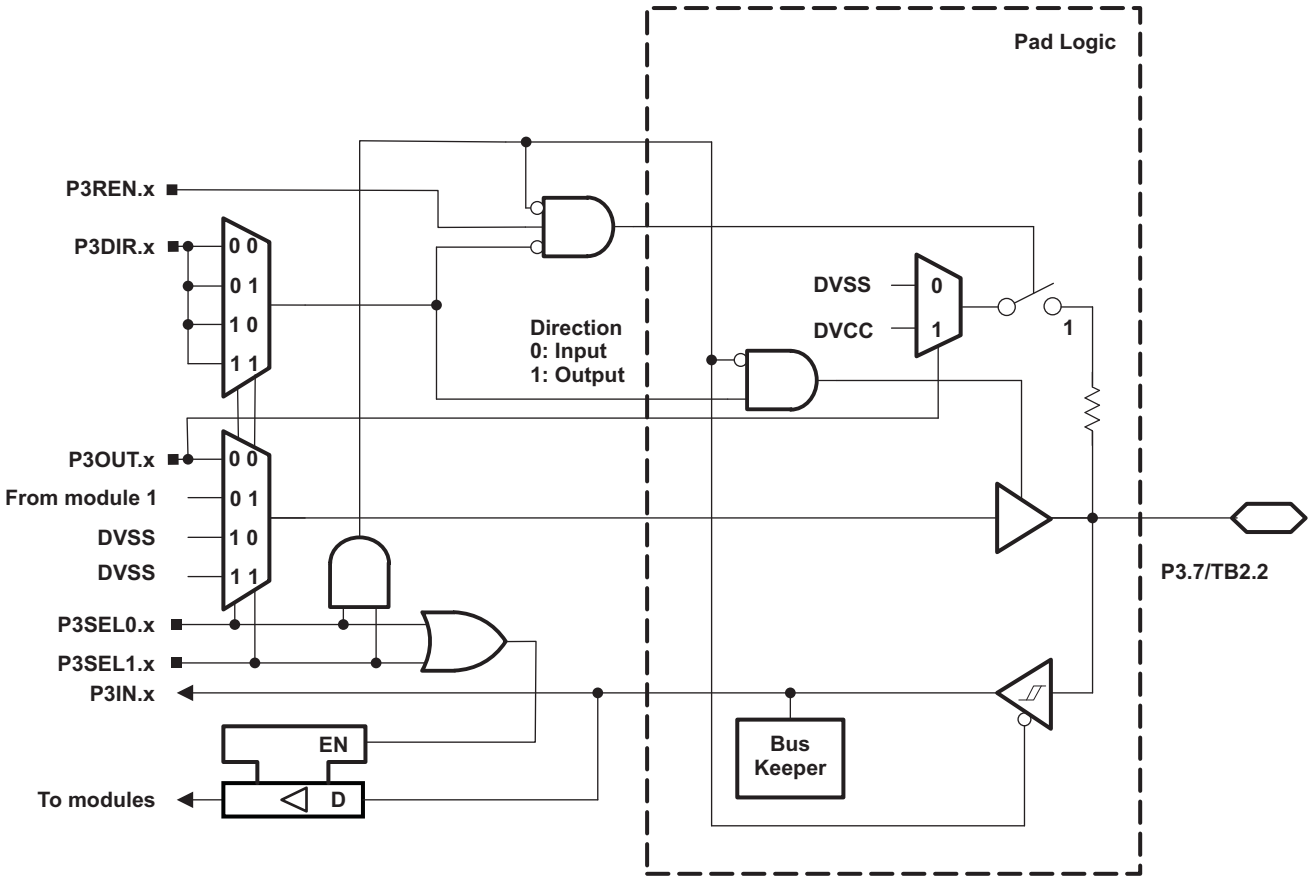



**Table 6-10. Port P3 (P3.7) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.7/TB2.2 | 7 | P3.7 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI2B (1) | 0 | 0 | 1 |
| | | TB2.2 (1) | 1 | | |

(1) Not available on all devices and package types.

## 6.11 Port P4, P4.0, Input/Output With Schmitt Trigger

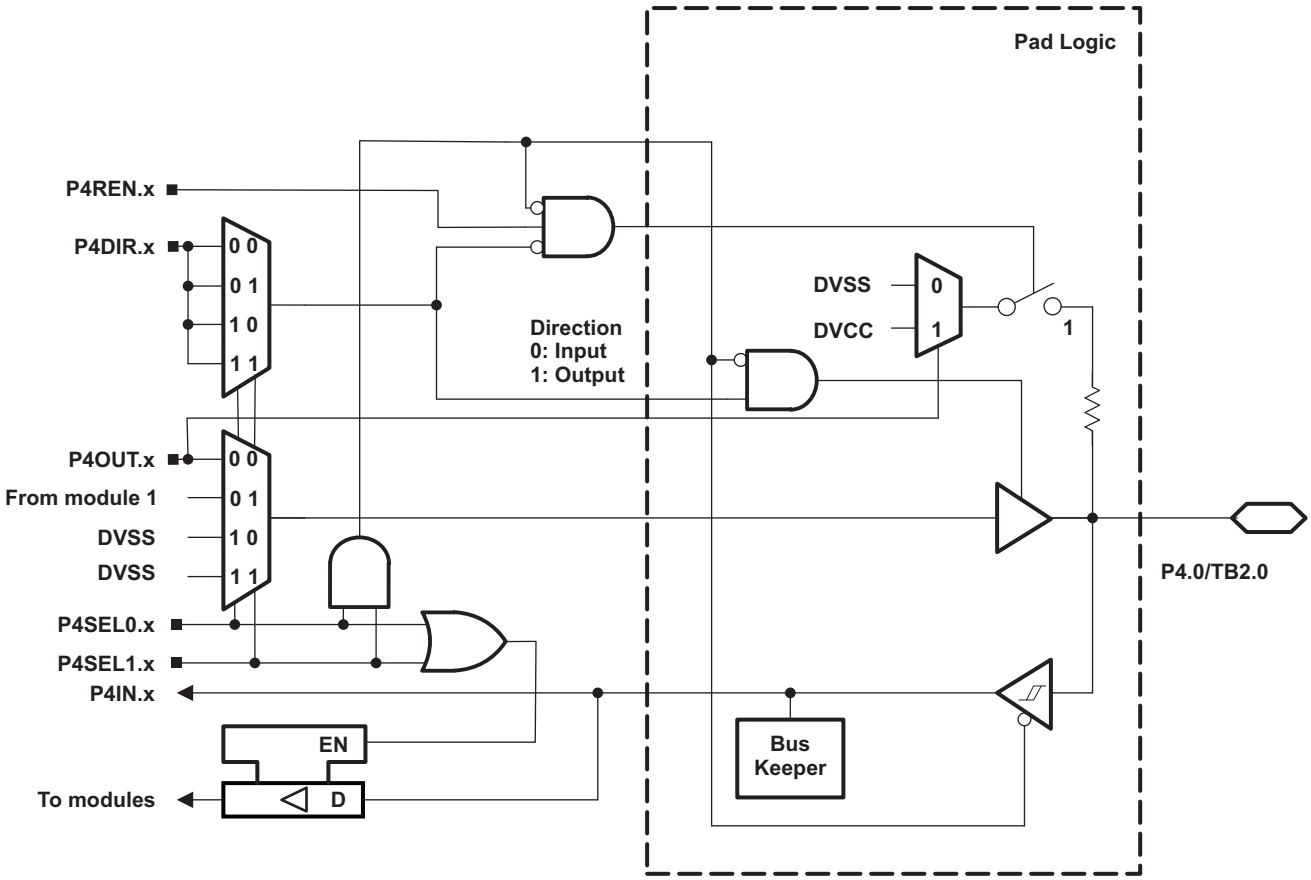



**Table 6-11. Port P4 (P4.0) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.0/TB2.0 | 0 | P4.0 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI0B (1) | 0 | 0 | 1 |
| | | TB2.0 (1) | 1 | | |

(1) Not available on all devices and package types.

## 6.12 Port P4, P4.1, Input/Output With Schmitt Trigger

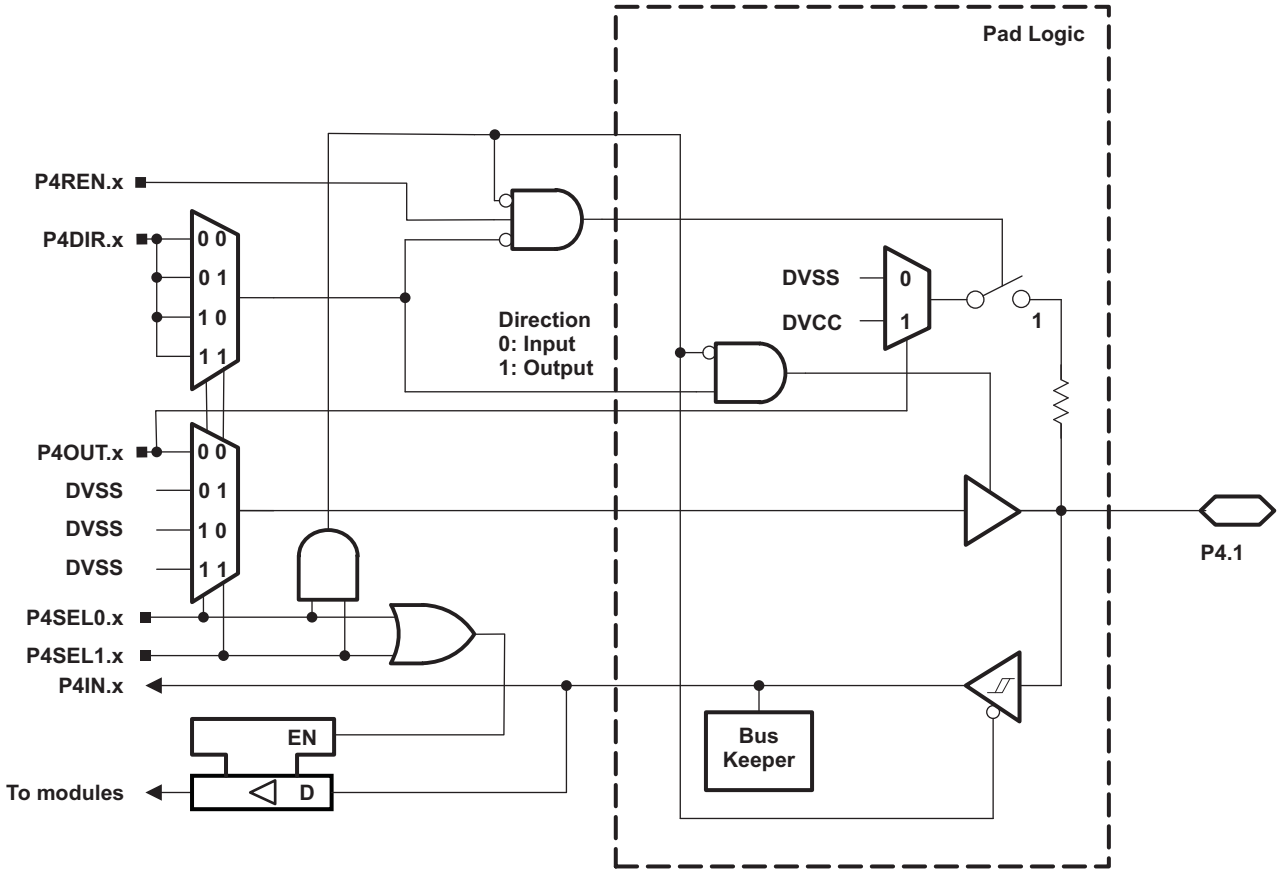
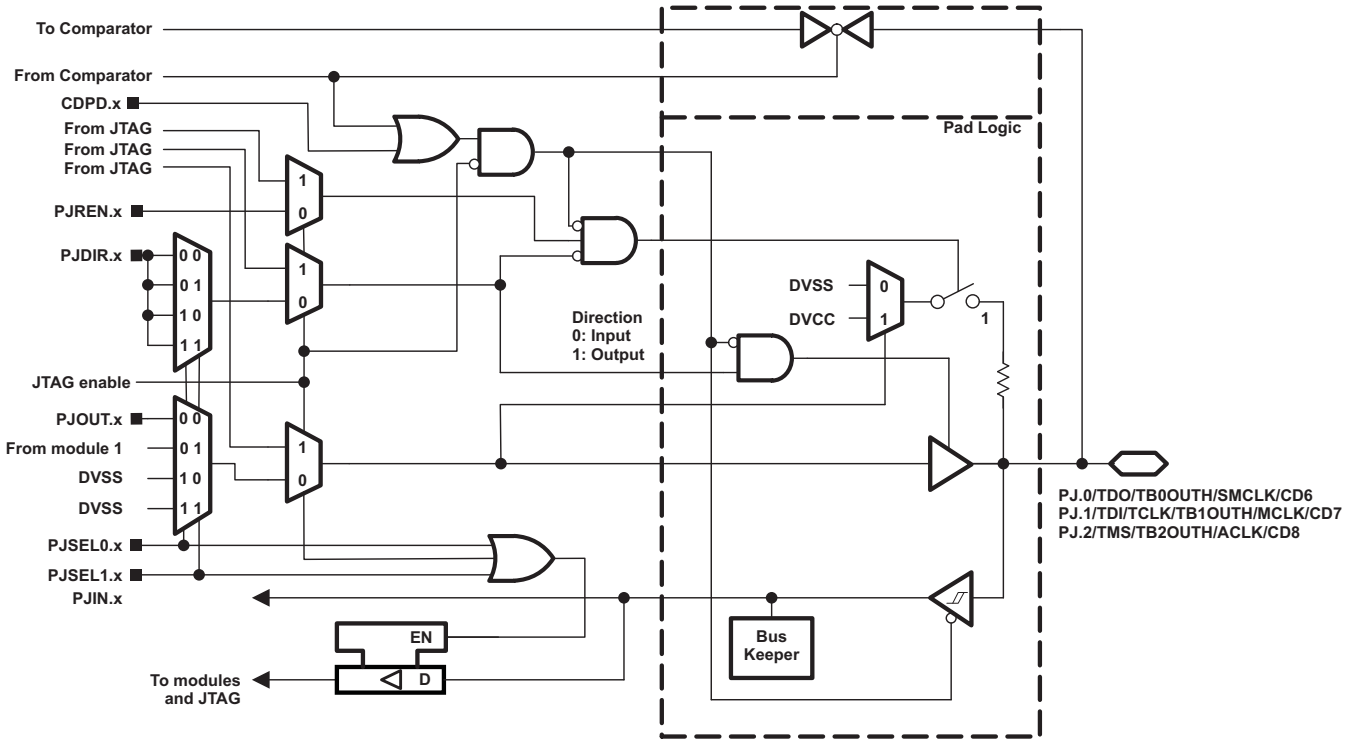



**Table 6-12. Port P4 (P4.1) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.1 | 1 | P4.1 (I/O) (1) | I: 0; O: 1 | 0 | 0 |

(1) Not available on all devices and package types.

## 6.13 Port J, J.0 to J.3 JTAG pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output



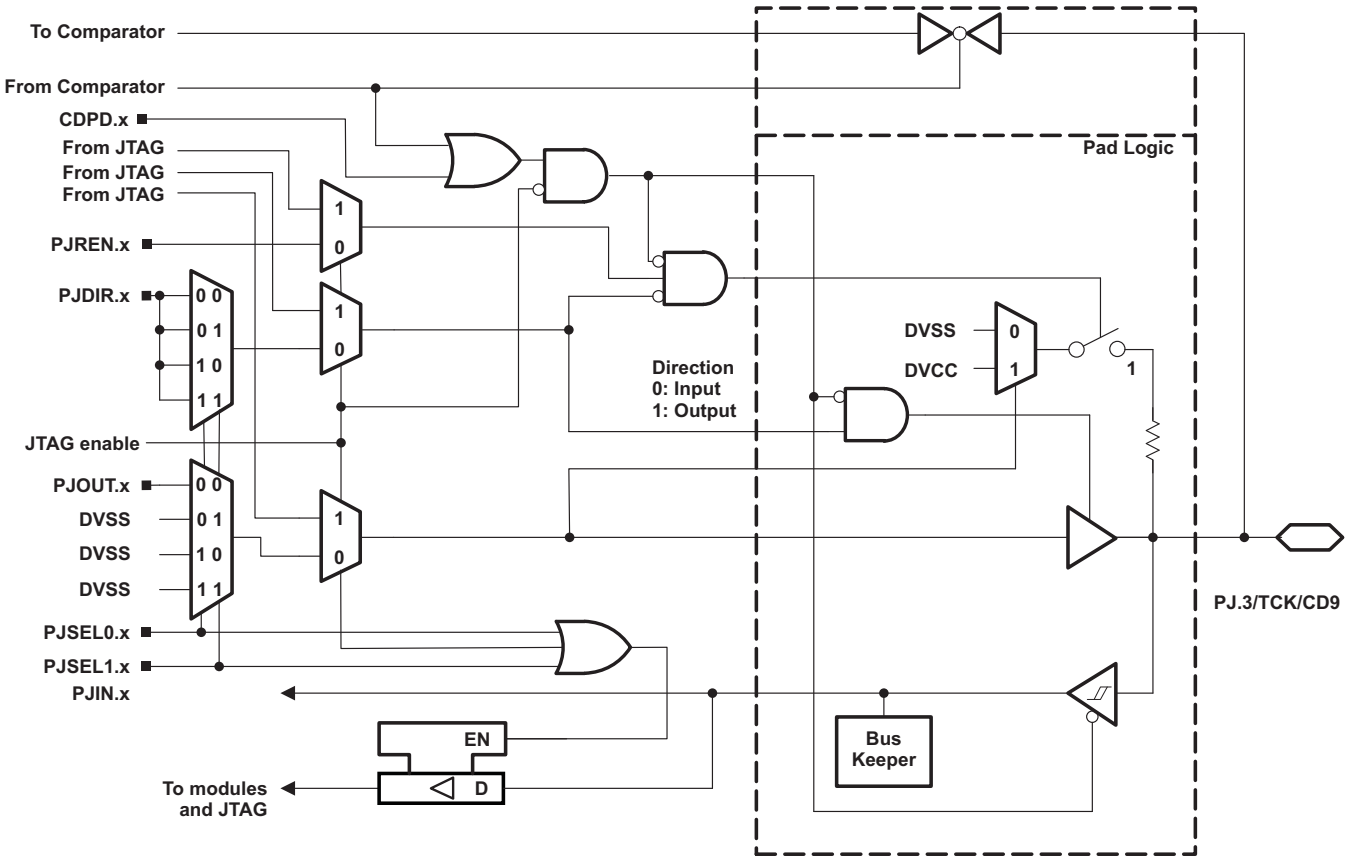
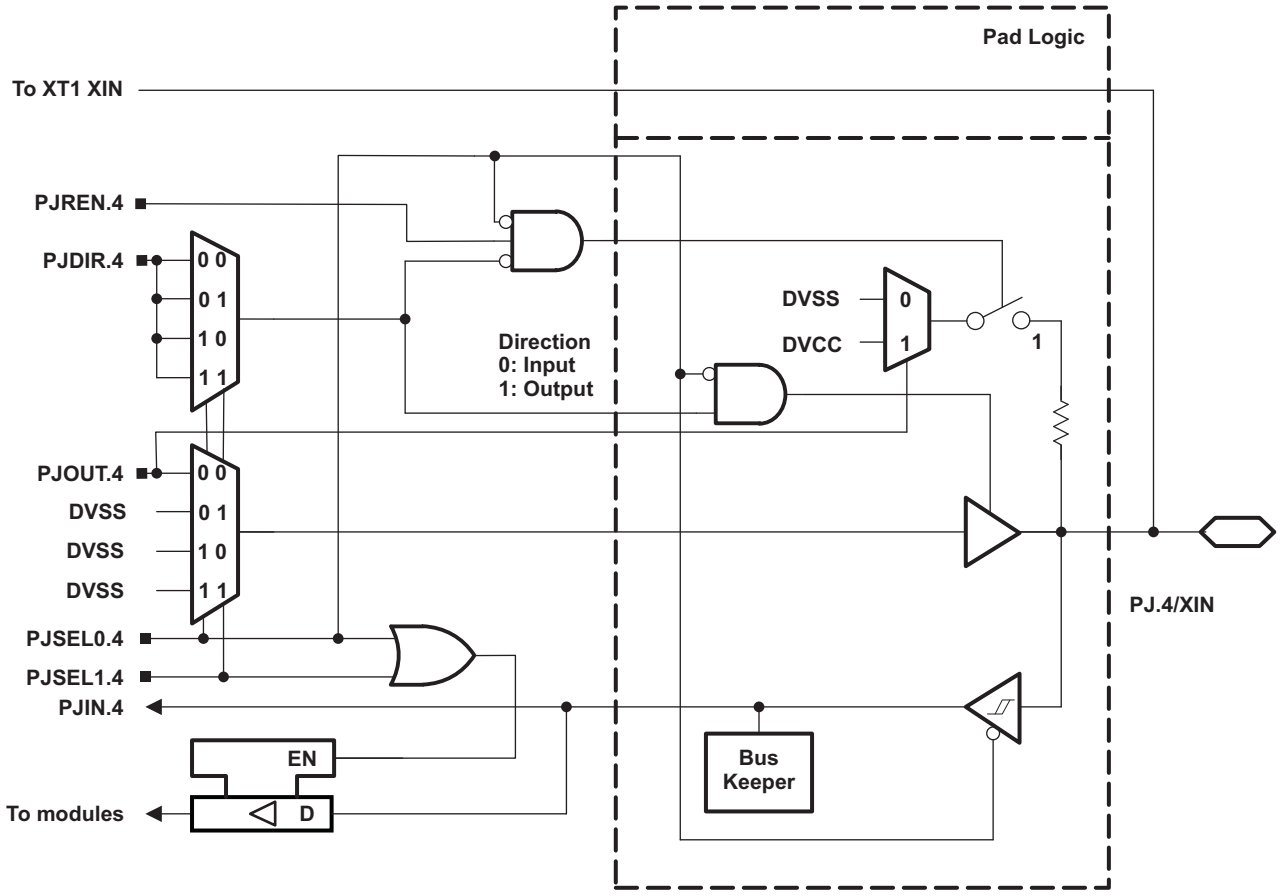

To Comparator
From Comparator
CDPD.x
From JTAG
From JTAG
From JTAG
PJREN.x
PJDIR.x
0 0
0 1
1 0
1 1
JTAG enable
PJOUT.x
DVSS
DVSS
DVSS
PJSEL0.x
PJSEL1.x
PJIN.x
1
0
EN
D
To modules and JTAG
Direction 0: Input 1: Output
Pad Logic
DVSS
DVCC
Bus Keeper
PJ.3/TCK/CD9

**Table 6-13. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS/ SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.x | PJSEL0.x |
| PJ.0/TDO/TB0OUTH/SMCLK/CD6 | 0 | PJ.0 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TDO (3) | X | X | X |
| | | TB0OUTH | 0 | 0 | 1 |
| | | SMCLK | 1 | | |
| | | CD6 | X | 1 | 1 |
| PJ.1/TDI/TCLK/TB1OUTH/MCLK/CD7 | 1 | PJ.1 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TDI/TCLK (3) (4) | X | X | X |
| | | TB1OUTH | 0 | 0 | 1 |
| | | MCLK | 1 | | |
| | | CD7 | X | 1 | 1 |
| PJ.2/TMS/TB2OUTH/ACLK/CD8 | 2 | PJ.2 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TMS (3) (4) | X | X | X |
| | | TB2OUTH | 0 | 0 | 1 |
| | | ACLK | 1 | | |
| | | CD8 | X | 1 | 1 |
| PJ.3/TCK/CD9 | 3 | PJ.3 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TCK (3) (4) | X | X | X |
| | | CD9 | X | 1 | 1 |

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made by the SYS module or by the Spy-Bi-Wire four-wire entry sequence. PJSEL1.x and PJSEL0.x have no effect in these cases.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

## 6.14 Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger



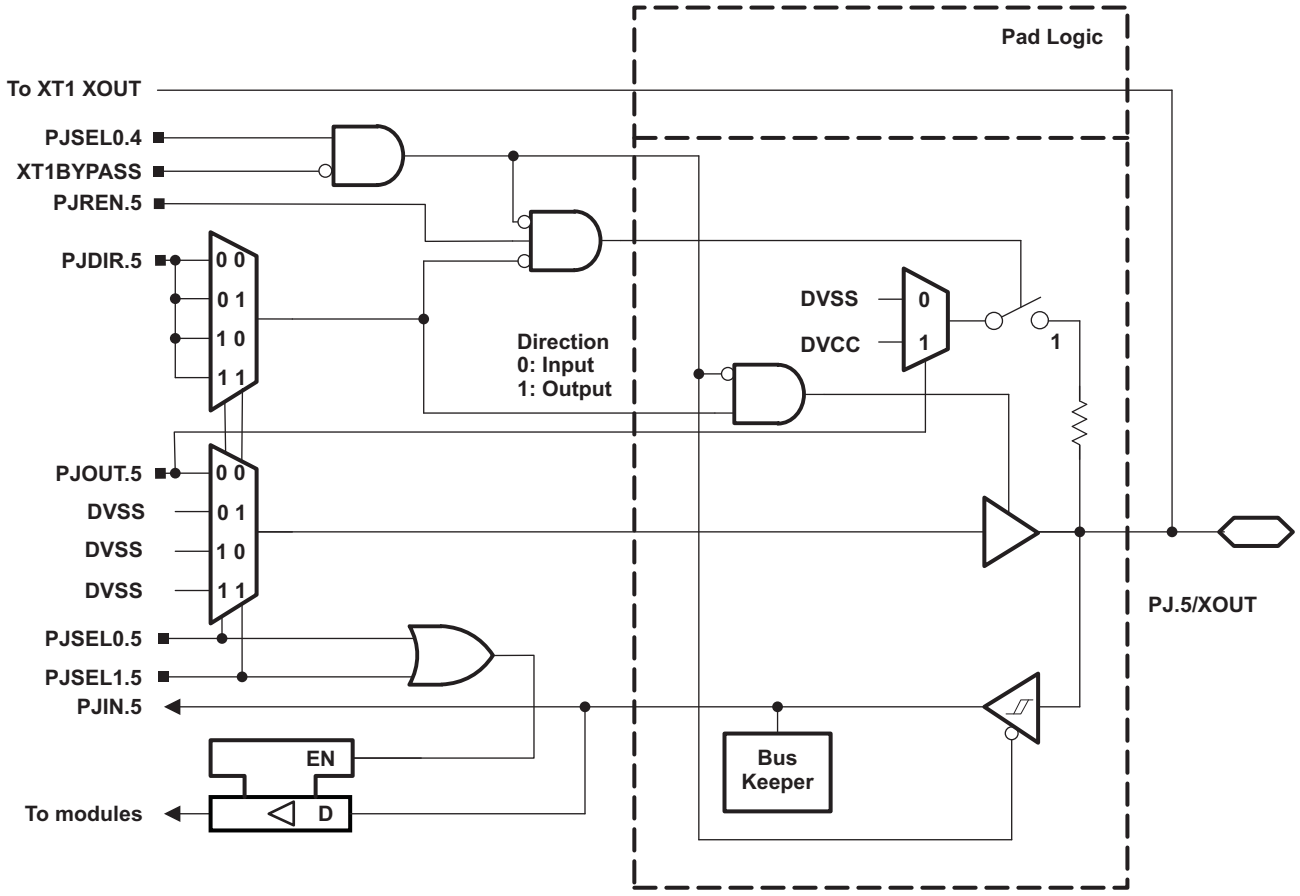



**Table 6-14. Port PJ (PJ.4 and PJ.5) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS/SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.5 | PJSEL0.5 | PJSEL1.4 | PJSEL0.4 | XT1 BYPASS |
| PJ.4/XIN | 4 | PJ.4 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | XIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | XIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.5/XOUT | 5 | PJ.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | X |
| | | XOUT crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | PJ.5 (I/O) (3) | I: 0; O: 1 | X | X | 0 | 1 | 1 |

(1) X = Don't care
(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When XT1BYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are do not care. When XT1BYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.

# 7 Device Descriptors (TLV)

Table 7-1 and Table 7-2 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

**Table 7-1. Device Descriptor Table (1)**

| | Description | Address | FR5739 | FR5738 | FR5737 | FR5736 | FR5735 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **Info Block** | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 03h | 02h | 01h | 77h | 76h |
| | Device ID | 01A05h | 81h | 81h | 81h | 81h | 81h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit |
| **Die Record** | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | per unit | per unit | per unit | per unit | per unit |
| | | 01A13h | per unit | per unit | per unit | per unit | per unit |
| **ADC10 Calibration** | ADC10 Calibration Tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 Calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | per unit | per unit | NA | NA | per unit |
| | | 01A17h | per unit | per unit | NA | NA | per unit |
| | ADC Offset | 01A18h | per unit | per unit | NA | NA | per unit |
| | | 01A19h | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah | per unit | per unit | NA | NA | per unit |
| | | 01A1Bh | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch | per unit | per unit | NA | NA | per unit |
| | | 01A1Dh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh | per unit | per unit | NA | NA | per unit |
| | | 01A1Fh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h | per unit | per unit | NA | NA | per unit |
| | | 01A21h | per unit | per unit | NA | NA | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h | per unit | per unit | NA | NA | per unit |
| | | 01A23h | per unit | per unit | NA | NA | per unit |

(1) NA = Not applicable

**Table 7-1. Device Descriptor Table (1) (continued)**

| | Description | Address | FR5739 | FR5738 | FR5737 | FR5736 | FR5735 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h | per unit | per unit | NA | NA | per unit |
| | | 01A25h | per unit | per unit | NA | NA | per unit |
| **REF Calibration** | REF Calibration Tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V Reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V Reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

**Table 7-2. Device Descriptor Table (1)**

| | Description | Address | FR5734 | FR5733 | FR5732 | FR5731 | FR5730 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **Info Block** | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 00h | 7Fh | 75h | 7Eh | 7Ch |
| | Device ID | 01A05h | 81h | 80h | 81h | 80h | 80h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit |
| **Die Record** | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | per unit | per unit | per unit | per unit | per unit |
| | | 01A13h | per unit | per unit | per unit | per unit | per unit |
| **ADC10 Calibration** | ADC10 Calibration Tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 Calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | per unit | NA | NA | per unit | per unit |
| | | 01A17h | per unit | NA | NA | per unit | per unit |
| | ADC Offset | 01A18h | per unit | NA | NA | per unit | per unit |
| | | 01A19h | per unit | NA | NA | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah | per unit | NA | NA | per unit | per unit |
| | | 01A1Bh | per unit | NA | NA | per unit | per unit |

(1) NA = Not applicable

**Table 7-2. Device Descriptor Table [(1)] (continued)**

| | Description | Address | FR5734 | FR5733 | FR5732 | FR5731 | FR5730 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch | per unit | NA | NA | per unit | per unit |
| | | 01A1Dh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh | per unit | NA | NA | per unit | per unit |
| | | 01A1Fh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h | per unit | NA | NA | per unit | per unit |
| | | 01A21h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h | per unit | NA | NA | per unit | per unit |
| | | 01A23h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h | per unit | NA | NA | per unit | per unit |
| | | 01A25h | per unit | NA | NA | per unit | per unit |
| **REF Calibration** | REF Calibration Tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V Reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V Reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

# 8 器件和文档支持

## 8.1 器件支持

### 8.1.1 开始使用

TI 还提供了立即入门必备的所有硬件平台和软件组件以及工具！ 不仅如此，TI 还拥有众多辅助组件以满足您的需求。 要获得 MSP430™ MCU 产品线、可用开发工具和评估套件，以及高级开发资源，请访问 MSP430 入门网页。

### 8.1.2 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

#### 8.1.2.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* (SLAU157) for details on the available features.

| MSP430 Architecture | 4-Wire JTAG | 2-Wire JTAG | Break-points (N) | Range Break-points | Clock Control | State Sequencer | Trace Buffer | LPMx.5 Debugging Support |
|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | Yes | Yes | 3 | Yes | Yes | No | No | Yes |

#### 8.1.2.2 Recommended Hardware Options

##### 8.1.2.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

| Package | Target Board and Programmer Bundle | Target Board Only |
|---|---|---|
| 40-pin VQFN (RHA) | MSP-FET430U40A | MSP-TS430RHA40A |

##### 8.1.2.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

##### 8.1.2.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

##### 8.1.2.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

| Part Number | PC Port | Features | Provider |
|---|---|---|---|
| MSP-GANG | Serial and USB | Program up to eight devices at a time. Works with PC or standalone. | Texas Instruments |

#### 8.1.2.3 Recommended Software Options

##### 8.1.2.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

#### 8.1.2.3.2 MSP430Ware

MSP430Ware is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

#### 8.1.2.3.3 Command-Line Programmer

MSP430 Flasher is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 microcontroller without the need for an IDE.

### 8.1.3 器件和开发工具命名规则

为了指明产品开发周期所处的阶段，TI 为所有 MSP430 MCU 器件和支持工具的产品型号分配了前缀。 每个 MSP430 MCU 商用系列产品成员具有以下三个前缀中的一个：MSP，PMS 或 XMS（例如，MSP430F5259）。 德州仪器 (TI) 建议为其支持的工具使用三个可能前缀指示符中的两个：MSP 和 MSPX。 这些前缀代表了产品从工程原型机（其中 XMS 针对器件，而 MSPX 针对工具）直到完全合格的生产器件和工具（其中 MSP 针对器件，而 MSP 针对工具）的产品开发进化阶段。

器件开发进化流程：

**XMS** - 试验器件不一定代表最终器件的电气技术规格

**PMS** - 最终的芯片模型符合器件的电气技术规格，但是未经完整的质量和可靠性验证

**MSP** - 完全合格的生产器件

支持工具开发进化流程：

**MSPX** - 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

**MSP** – 完全合格的开发支持产品

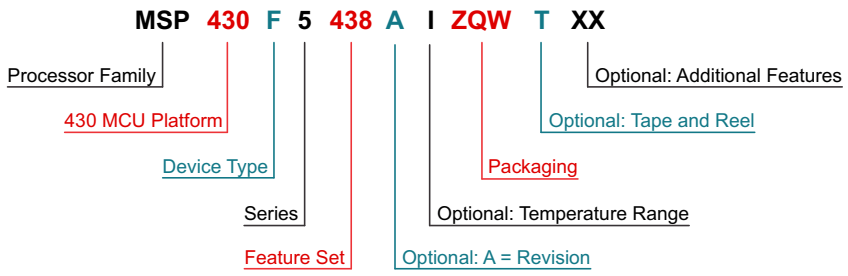
XMS 和 PMS 器件和 MSPX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

MSP 器件和 MSP 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（XMS 和 PMS）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀包括封装类型（例如，PZP）和温度范围（如，T）。图 8-1 提供了读取任一系列产品成员完整器件名称的图例。




| | | |
|---|---|---|
| **Processor Family** | CC = Embedded RF Radio<br>MSP = Mixed Signal Processor<br>XMS = Experimental Silicon<br>PMS = Prototype Device | |
| **430 MCU Platform** | TI's Low Power Microcontroller Platform | |
| **Device Type** | **Memory Type**<br>C = ROM<br>F = Flash<br>FR = FRAM<br>G = Flash or FRAM (Value Line)<br>L = No Nonvolatile Memory | **Specialized Application**<br>AFE = Analog Front End<br>BT = Preprogrammed with *Bluetooth*<br>BQ = Contactless Power<br>CG = ROM Medical<br>FE = Flash Energy Meter<br>FG = Flash Medical<br>FW = Flash Electronic Flow Meter |
| **Series** | 1 Series = Up to 8 MHz<br>2 Series = Up to 16 MHz<br>3 Series = Legacy<br>4 Series = Up to 16 MHz w/ LCD | 5 Series = Up to 25 MHz<br>6 Series = Up to 25 MHz w/ LCD<br>0 = Low Voltage Series |
| **Feature Set** | Various Levels of Integration Within a Series | |
| **Optional: A = Revision** | N/A | |
| **Optional: Temperature Range** | S = 0°C to 50°C<br>C = 0°C to 70°C<br>I = -40°C to 85°C<br>T = -40°C to 105°C | |
| **Packaging** | www.ti.com/packaging | |
| **Optional: Tape and Reel** | T = Small Reel<br>R = Large Reel<br>No Markings = Tube or Tray | |
| **Optional: Additional Features** | -EP = Enhanced Product (-40°C to 105°C)<br>-HT = Extreme Temperature Parts (-55°C to 150°C)<br>-Q1 = Automotive Q100 Qualified | |

图 **8-1.** 器件命名规则

## 8.2 文档支持

以下文档描述了 MSP430FR5739-EP MCU。 www.ti.com.cn 网站上提供了这些文档的副本。

**SLAU272** *MSP430FR57xx 系列用户指南。* 这款器件系列内所提供的全部模块和外设的详细信息。

**SLAZ392** ***MSP430FR5739** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ391** ***MSP430FR5738** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ390** ***MSP430FR5737** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ389** ***MSP430FR5736** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ388** ***MSP430FR5735** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ387** ***MSP430FR5734** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ386** ***MSP430FR5733** 器件勘误表。* 描述了针对这款器件每个芯片修订版本功能技术规格的已知例

外情况。

**SLAZ385** ***MSP430FR5732 器件勘误表。*** 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ384** ***MSP430FR5731 器件勘误表。*** 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

**SLAZ383** ***MSP430FR5730 器件勘误表。*** 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

## 8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
*TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.4 商标

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## 8.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

# 9 机械封装和可订购信息

## 9.1 封装信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| M430FR5739SRHATEP | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 85 | M430 FR5739EP |
| M430FR5739SRHATEP.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 85 | M430 FR5739EP |
| V62/14644-01XE | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -55 to 85 | M430 FR5739EP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF MSP430FR5739-EP :**

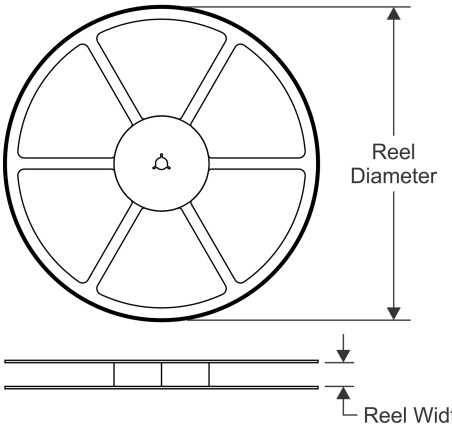
- Catalog : MSP430FR5739

NOTE: Qualified Version Definitions:

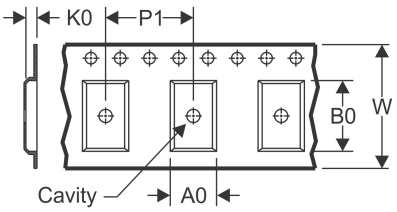
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

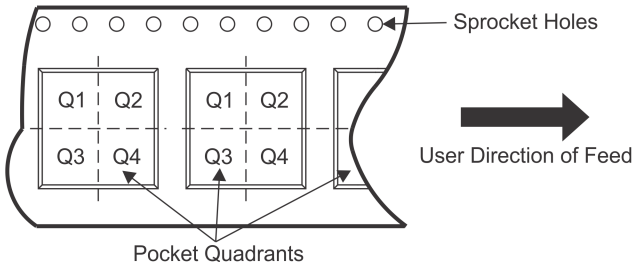



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

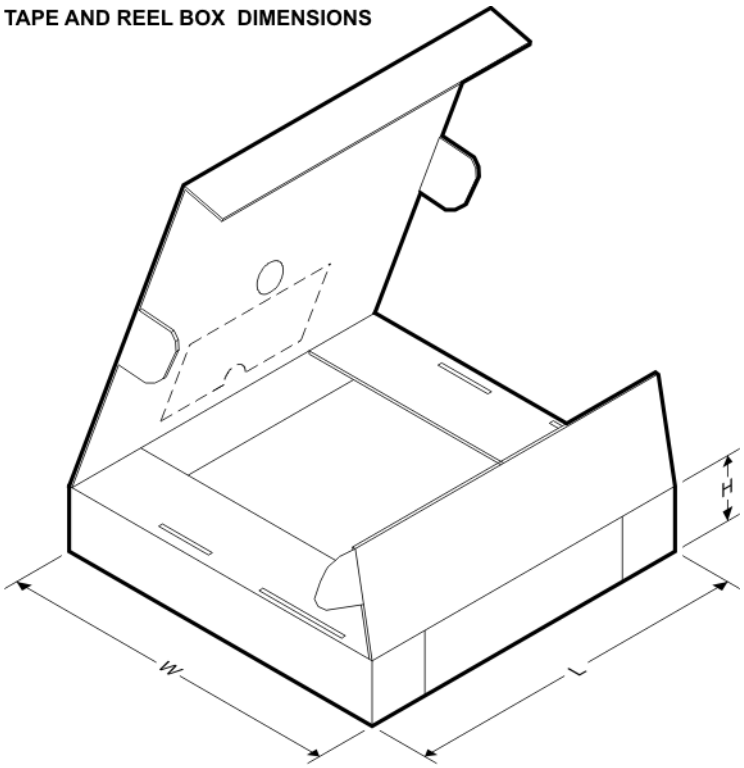
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| M430FR5739SRHATEP | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| M430FR5739SRHATEP | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

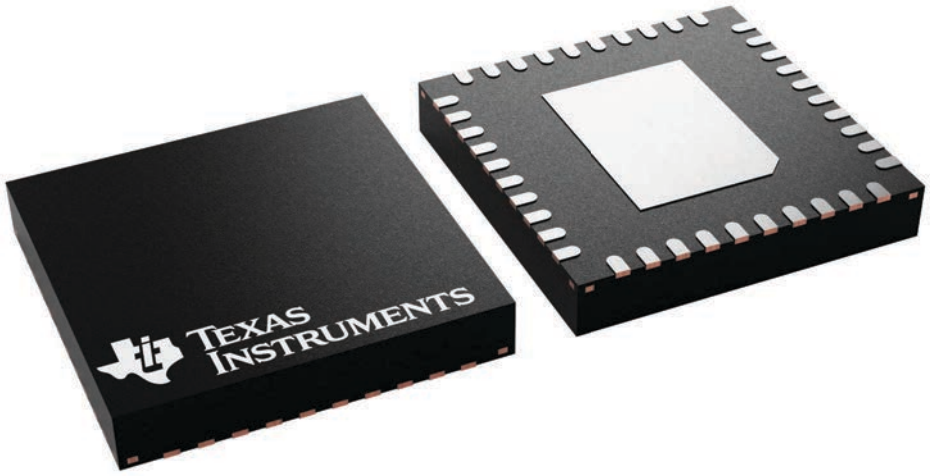
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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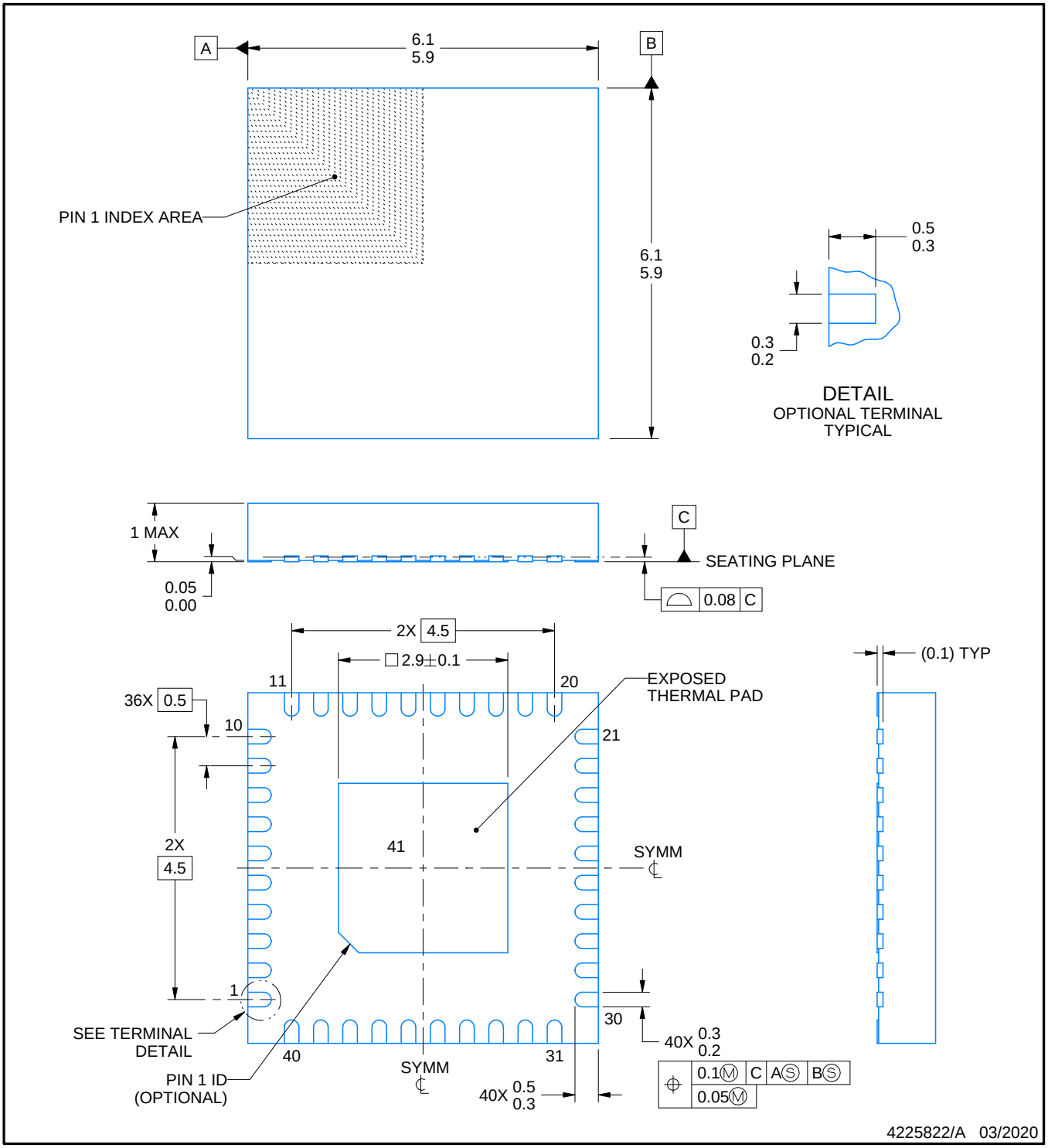
# PACKAGE OUTLINE

## RHA0040D

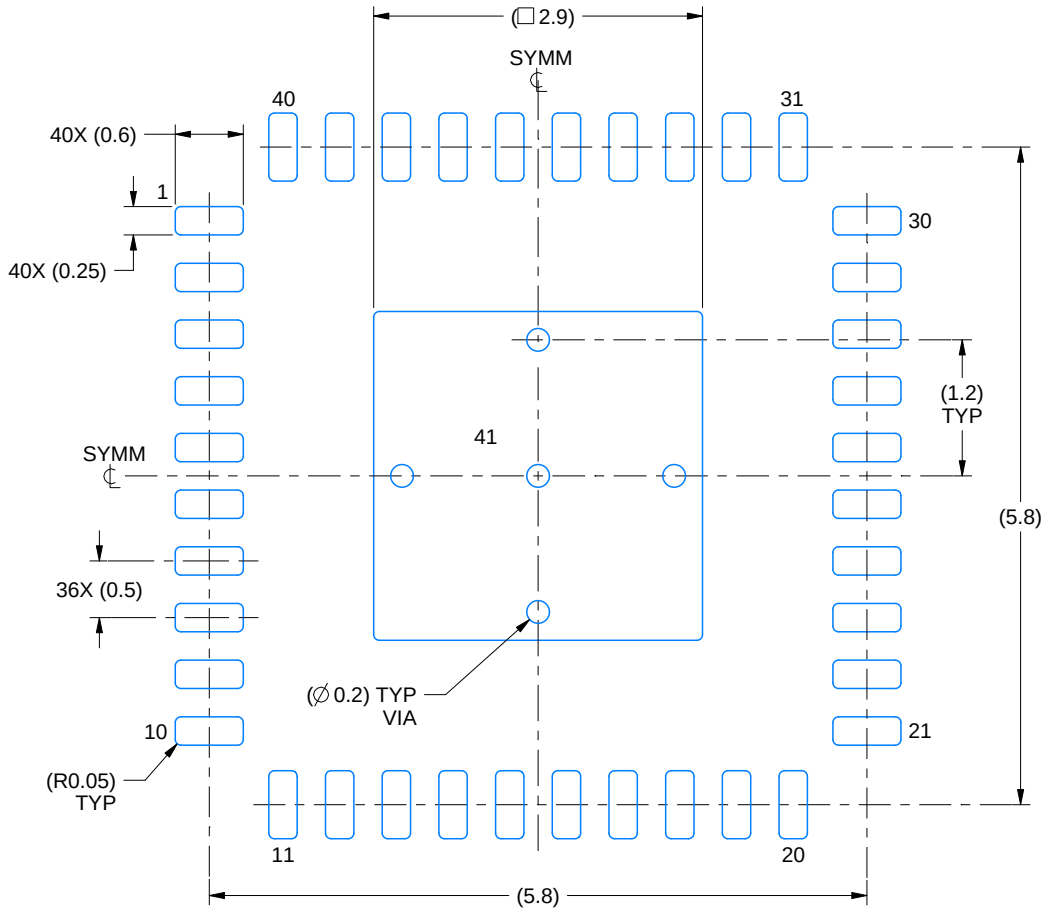
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

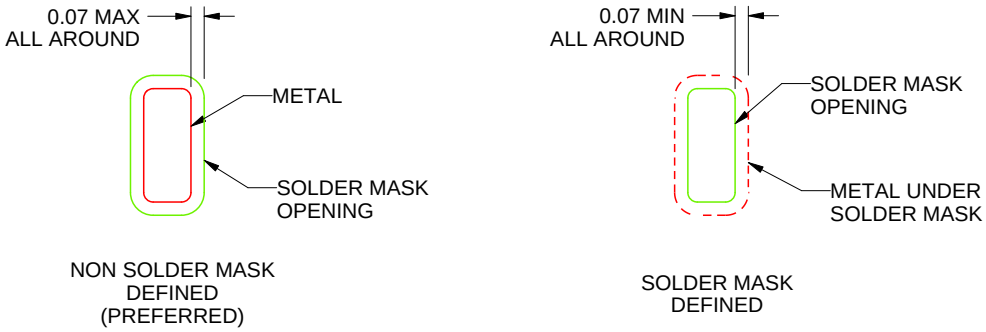



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:15X




SOLDER MASK DETAILS

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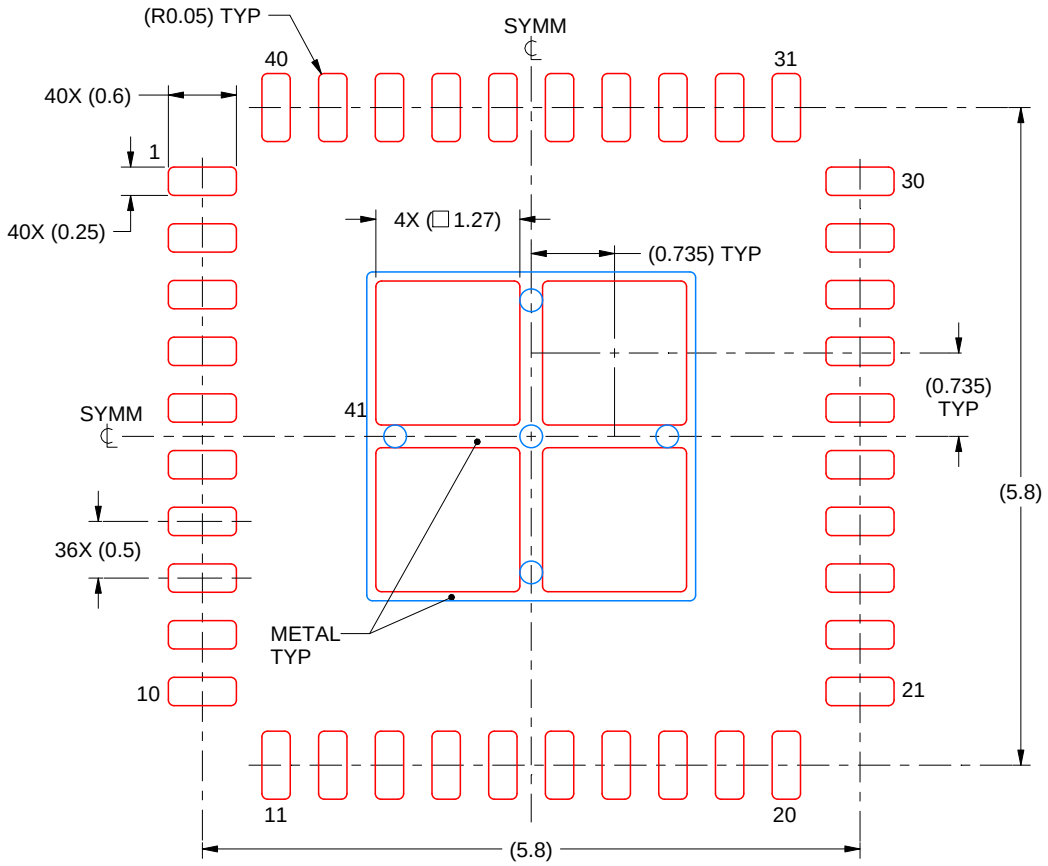
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月