TEXAS INSTRUMENTS
MSP430F5259, MSP430F5258, MSP430F5257, MSP430F5256
MSP430F5255, MSP430F5254, MSP430F5253, MSP430F5252
ZHCSER2D – MAY 2013 – REVISED OCTOBER 2020

MSP430F525x 混合信号微控制器

1 特性

- 双电源电压器件
  - 主电源（AVCC、DVCC）
    - 由外部电源供电：从 3.6V 低至 1.8V
    - 多达 18 个通用 I/O，支持多达 8 个外部中断
  - 低压接口电源 (DVIO)
    - 由单独的外部电源供电：1.62 V 至 1.98 V
    - 多达 35 个通用 I/O，支持多达 16 个外部中断
    - 串行通信
- 超低功耗
  - 工作模式 (AM)：所有系统时钟均工作 在 8MHz、3.0V 且闪存程序执行时为 290µA/MHz（典型值） 在 8MHz、3.0V 且 RAM 程序执行时为 150µA/MHz（典型值）
  - 待机模式 (LPM3)：含晶体的实时时钟 (RTC)、看门狗、电源监控器可用，完全 RAM 保持，快速唤醒：2.2V 时为 2.1µA，3.0V 时为 2.3µA（典型值） 低功耗振荡器 (VLO)、通用计数器、看门狗、电源监控器可用，完全 RAM 保持，快速唤醒：3.0V 时为 1.6µA（典型值）
  - 关闭模式 (LPM4)：完全 RAM 保持、电源监控器可用、快速唤醒：3.0V 时为 1.3µA（典型值）
  - 关断模式 (LPM4.5)：3.0V 时为 0.18µA（典型值）
- 在 3.5 µ s（典型值）内从待机模式唤醒
- 16 位 RISC 架构，扩展存储器，高达 25MHz 的系统时钟
- 灵活的电源管理系统
  - 具有可编程稳压内核电源电压的完全集成 LDO
  - 电源电压监控、监视和欠压保护
- 单一时钟系统
  - 针对频率稳定的锁相环 (FLL) 控制环路
  - 低功耗低频内部时钟源 (VLO)
  - 低频修整内部基准源 (REFO)
  - 32kHz 手表晶振 (XT1)
  - 高达 32MHz 的高频晶体 (XT2)
- 配有五个捕捉/比较寄存器的 16 位计时器 TA0，Timer_A
- 配有三个捕捉/比较寄存器的 16 位计时器 TA1，Timer_A
- 配有三个捕捉/比较寄存器的 16 位计时器 TA2，Timer_A
- 具有七个捕捉/比较影子寄存器的 16 位计时器 TB0，Timer_B
- 四个通用串行通信接口
  - USCI_A0、A1、A2 和 A3 均支持：
    - 具有自动波特率检测功能的增强型通用异步收发器 (UART)
    - 红外数据通讯 (IrDA) 编码器和解码器
    - 同步 SPI
  - USCI_B0、B1、B2 和 B3 均支持：
    - I^2C
    - 同步串行外设接口 (SPI)
- 带内部基准、采样保持功能的 10 位模数转换器 (ADC)
- 比较器
- 硬件乘法器支持 32 位运算
- 串行板上编程，无需外部编程电压
- 3 通道内部 DMA
- 具有 RTC 功能的基本定时器
- 器件比较汇总了可用的产品系列成员和封装

2 应用

- “常开型”系统控制器
- 电源管理集线器
- Bluetooth® 控制器
- 模拟和数字传感器融合系统
- 数据记录器
- 通用应用

3 说明

使用一款“始终开启”的超低功耗系统控制器，可为手机和平板电脑等便携式设备显著降低功耗。当高耗电的应用处理器和触摸屏控制器关闭时，这些控制器可充当传感器集线器并监视用户激励信号（例如，读取惯性传感器或触摸传感器）和重要的系统参数（例如，电池健康状况和温度）。之后，微控制器会根据用户输入或者在出现故障需要 CPU 干预时“唤醒”系统。

MSP430F525x 系列是 1.8V 双电源 I/O 产品系列中最新推出的产品（以前仅提供 MSP430F522x），专为“常开型”系统控制器应用而设计。凭借 1.8V I/O，无需进行外部电平转换即可无缝连接至应用处理器和其他器件，同时 MCU 的主电源可处于更高的电压轨上。

与 MSP430F522x 相比，MSP430F525x 的 RAM 容量翻了两番 (32KB)，串行接口数量也翻了一倍（四个 USCI_A 和四个 USCI_B）。MSP430F525x 还采用 4 个 16 位计时器、1 个高性能 10 位 ADC、1 个硬件乘法器、DMA、1 个比较器和 1 个具有警报功能的 RTC 模块。MSP430F525x 在工作模式下（从闪存运行）的电流消耗为 290 µA/MHz（典型值），在待机模式 (LPM3) 下的电流消耗为 1.6µA（典型值）。MSP430F525x 可在 3.5µs（典型值）内切换至工作模式，因此非常适合“常开型”低功耗应用。

MSP430F525x 的主要优势如下：

- 高达 32KB 的 RAM，支持复杂的传感器集线器算法以及键盘控制和电源管理等高级聚合。
- 四个 USCI_A 和四个 USCI_B 模块，支持八个专用硬件串行接口（例如，四个 I^2C 和四个 SPI）并行工作，从而快速而稳定地与传感器或外设进行通信。
- 多达 35 个可在 1.8V 电压轨中使用的 I/O。

有关完整的模块说明，请参阅 *MSP430F5xx 和 MSP430F6xx 系列用户指南*。有关设计指南，请参阅 *使用 MSP430F522x 和 MSP430F521x 器件进行设计*。

器件信息

器件型号(1)	封装	封装尺寸(2)
MSP430F5259IRGC	VQFN (64)	9mm x 9mm
MSP430F5252IZXH	nFBGA (80)	5mm × 5mm
MSP430F5252IZQE(3)	MicroStar Junior™ BGA (80)	5mm × 5mm

(1) 如需获得所有可用器件的最新部件、封装和订购信息，请参阅*封装选项附录*（节 11）或浏览 TI 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参阅*机械数据*（节 11 中）。
(3) 采用 ZQE (MicroStar Junior BGA) 封装的所有可订购器件型号均已更改为“最后可采购期限”状态。有关此状态的详细信息，请访问产品生命周期页面。

4 Functional Block Diagram

图 4-1 shows the functional block diagram.

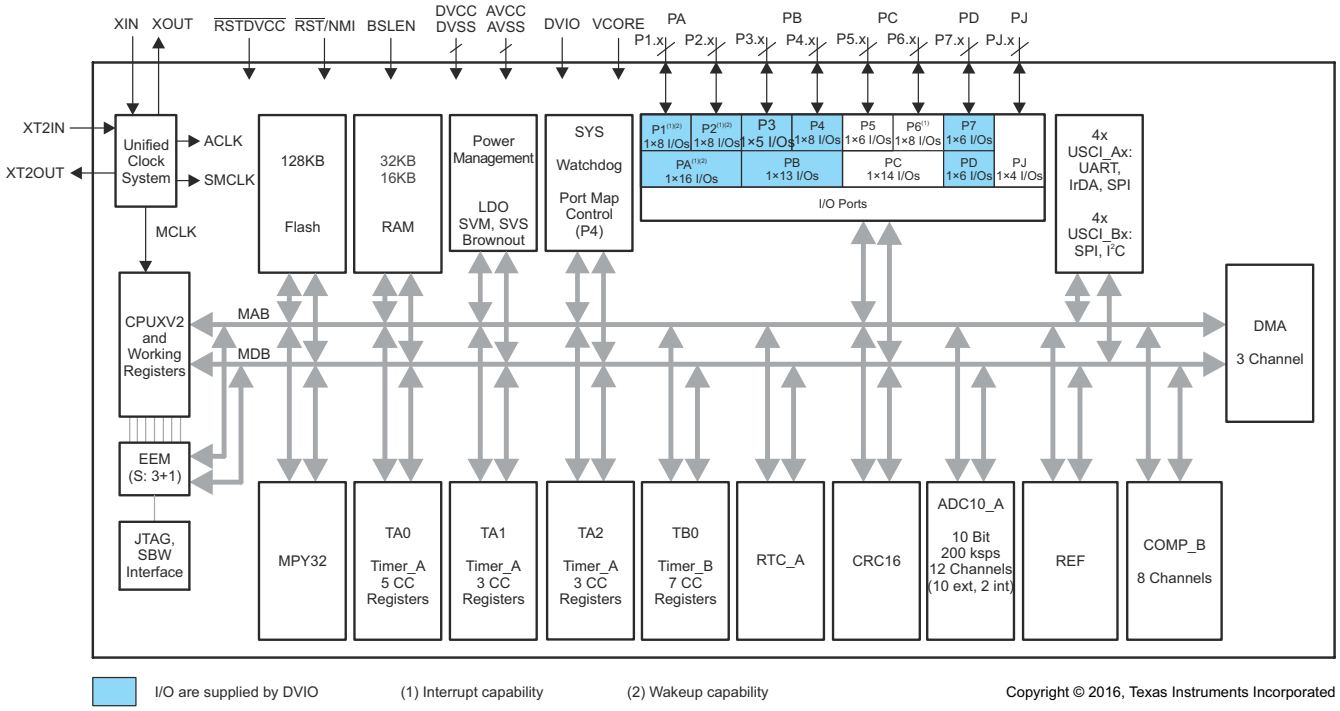


图 4-1. Functional Block Diagram

Table of Contents

5 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from revision C to revision D

Changes from September 28, 2018 to October 20, 2020	Page
• 更新了整个文档中的章节、表格、图和交叉参考的编号	1
• 通篇添加了 nFBGA 封装 (ZXH) 信息	1
• 器件信息中添加了有关采用 ZQE 封装的所有可订购器件型号的状态变化说明	1
• Corrected the description of the P2.3/UCB3SOMI/UCB3SCL signals in 表 7-1, *Terminal Functions*	10
• Changed the MAX value of the I_{ERASE} and I_{MERASE}, I_{BANK} parameters in 节 8.47, *Flash Memory*	44

Changes from revision B to revision C

Changes from November 26, 2015 to September 27, 2018	Page
• Added 节 6.1, *Related Products*	7
• Added color to P1.0 (pin H2) and DVSS (pin F9) to indicate supply from DVIO in 图 7-2, *80-Pin ZXH or ZQE Package (Top View)*	8
• Added typical conditions statements at the beginning of 节 8, *Specifications*	15
• Changed the MIN value of the $V_{(DVCC\_BOR\_hys)}$ parameter from 60 mV to 50 mV in 节 8.26, *PMM, Brownout Reset (BOR)*	31
• Updated notes (1) and (2) and added note (3) in 节 8.32, *Wake-up Times From Low-Power Modes and Reset*	33
• Removed ADC10DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in 节 8.42, *10-Bit ADC, Timing Parameters*, because ADC10CLK is after division	40
• Added second row for t_{EN_CMP} with Test Conditions of "CBPWRMD = 10" and MAX value of 100 µs in 节 8.46, *Comparator_B*	43
• Renamed FCTL4.MGR0 and MGR1 bits in the $f_{MCLK,MGR}$ parameter in 节 8.47, *Flash Memory*, to be consistent with header files	44
• Added links to the custom BSL430 package download in 节 9.5, *Bootloader (BSL)*	50
• Replaced former section *Development Tools Support* with 节 10.3, *Tools and Software*	98
• Updated list of related documentation in 节 10.4, *Documentation Support*	100

Changes from revision A to revision B

Changes from July 31, 2013 to November 25, 2015	Page
• 通篇更改了格式和结构，包括添加了章节编号	1
• 添加了 *器件信息* 表	1
• Moved 节 4, *Functional Block Diagram*	3
• Added 16KB RAM option in 图 4-1, *Functional Block Diagram*	3
• Added 节 6, *Device Comparison*, and moved 表 6-1 to it	7
• Added 节 7, *Terminal Configuration and Functions*, and moved pinout drawings and terminal functions table to it	8
• Added indication of terminals powered by DVIO in RGC pinout	8
• Added indication of terminals powered by DVIO in ZQE pinout	8
• Removed preview YFF pinout	8
• Added SUPPLY column and removed YFF column in 表 7-1, *Terminal Functions*	10
• Added 节 8.2, *ESD Ratings*	15
• Added note on C_{VCORE}	15
• Added 节 8.6, *Thermal Resistance Characteristics*	20

- Moved note on R_{Pull} from 节 8.7 to 节 8.8 21
- Changed TYP value of $C_{L,eff}$ with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF in 节 8.21, *Crystal Oscillator, XT1, Low-Frequency Mode* 27
- Corrected Test Conditions (removed V_{REF-}) for all parameters in 节 8.43 41
- Updated Test Conditions for all parameters in 节 8.43, *10-Bit ADC, Linearity Parameters*: changed from "C_{VREF+} = 20 pF" to "C_{VeREF+} = 20 pF"; changed from "$(V_{eREF+} - V_{eREF-})$min ≤ $(V_{eREF+} - V_{eREF-})$" to "1.4 V ≤ $(V_{eREF+} - V_{eREF-})$"..... 41
- Added "C_{VeREF+} = 20 pF" to E_I Test Conditions..... 41
- Added "ADC10SREFx = 11b" to Test Conditions for E_G and E_T 41
- Corrected Test Conditions (removed V_{REF-}) for V_{eREF+}, V_{eREF-}, and $(V_{eREF+} - V_{eREF-})$ parameters in 节 8.44, *REF, External Reference* 41
- Changed MIN value of $AV_{CC(min)}$ with Test Conditions of "REFVSEL = {0} for 1.5 V" from 2.2 V to 1.8 V in 节 8.45, *REF, Built-In Reference* 42
- Corrected spelling of MRG bits in $f_{MCLK,MRG}$ parameter symbol and description..... 44
- Throughout document, changed all instances of "bootstrap loader" to "bootloader"..... 50
- Added note to clarify that all JTAG pins are on DVCC..... 52
- Added note to indicate that all SBW pins are on DVCC..... 53
- Corrected spelling of NMIIFG in 表 9-10, *System Module Interrupt Vector Registers* 58
- Removed YFF package information from 表 9-12, *TA0 Signal Connections* 60
- Removed YFF package information from 表 9-13, *TA1 Signal Connections* 61
- Removed YFF package information from 表 9-14, *TA2 Signal Connections* 62
- Removed YFF package information from 表 9-15, *TB0 Signal Connections* 63
- Changed 图 9-8, *Port P5 (P5.3) Diagram* (added P5SEL.2 and XT2BYPASS inputs with AND and OR gates) 85
- Changed P5SEL.3 column from X to 0 for "P5.3 (I/O)" rows..... 85
- Changed 图 9-10, *Port P5 (P5.5) Diagram* (added P5SEL.5 input and OR gate)..... 87
- Changed P5SEL.5 column from X to 0 for "P5.5 (I/O)" rows..... 87
- Added 节 10 and moved *Development Tools Support*, *Device and Development Tool Nomenclature*, *Trademarks*, and *Electrostatic Discharge Caution* sections to it..... 96
- Added 节 11, *Mechanical, Packaging, and Orderable Information* 103

Changes from initial release to revision A

REVISION	CHANGES
SLAS903A July 2013	Updated PRODUCT PREVIEW release. Added 节 2. Changed 节 3. Added *Development Tools Support* and 节 10.2.
SLAS903 July 2013	PRODUCT PREVIEW release

6 Device Comparison

表 6-1 summarizes the available family members.

表 6-1. Device Comparison

DEVICE(1) (2)	FLASH (KB)	SRAM (KB)	Timer_A(3)	Timer_B(4)	USCI		ADC10_A (Ch)	COMP_B (Ch)	I/Os DVCC(5)	I/Os DVIO(6)	BSL TYPE	PACKAGE
					CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I²C						
MSP430F5259	128	32	5, 3, 3	7	4	4	10 ext, 2 int	8	18	35	I²C	64 RGC, 80 ZXH, 80 ZQE
MSP430F5258	128	32	5, 3, 3	7	4	4	N/A	8	18	35	I²C	64 RGC, 80 ZXH, 80 ZQE
MSP430F5257	128	16	5, 3, 3	7	4	4	10 ext, 2 int	8	18	35	I²C	64 RGC, 80 ZXH, 80 ZQE
MSP430F5256	128	16	5, 3, 3	7	4	4	N/A	8	18	35	I²C	64 RGC, 80 ZXH, 80 ZQE
MSP430F5255	128	32	5, 3, 3	7	4	4	10 ext, 2 int	8	18	35	UART	64 RGC, 80 ZXH, 80 ZQE
MSP430F5254	128	32	5, 3, 3	7	4	4	N/A	8	18	35	UART	64 RGC, 80 ZXH, 80 ZQE
MSP430F5253	128	16	5, 3, 3	7	4	4	10 ext, 2 int	8	18	35	UART	64 RGC, 80 ZXH, 80 ZQE
MSP430F5252	128	16	5, 3, 3	7	4	4	N/A	8	18	35	UART	64 RGC, 80 ZXH, 80 ZQE

(1) For the most current package and ordering information, see the *Package Option Addendum* in 节 11, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(5) All of these I/Os are on a single voltage rail supplied by DVCC.
(6) All of these I/Os are on a single voltage rail supplied by DVIO.

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power microcontrollers

One platform. One ecosystem. Endless possibilities.

Companion products for MSP430F5259

Review products that are frequently purchased or used in conjunction with this product.

Reference designs

Find reference designs that leverage the best in TI technology to solve your system-level challenges.

7 Terminal Configuration and Functions

7.1 Pin Diagrams

图 7-1 shows the pinout of the 64-pin RGC package.

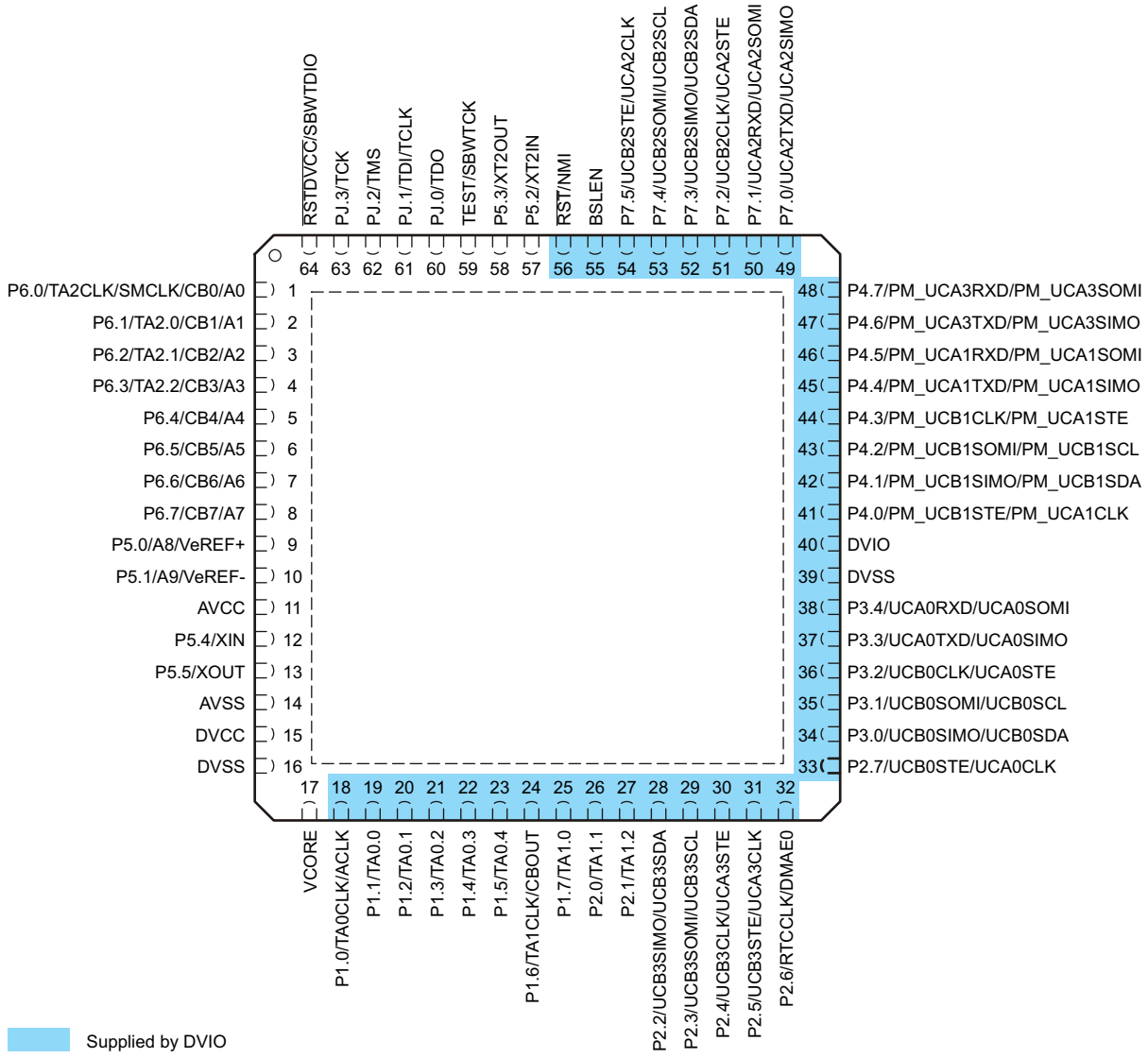


图 7-1. 64-Pin RGC Package (Top View)

图 7-2 shows the pinout of the 80-pin ZXH or ZQE package.

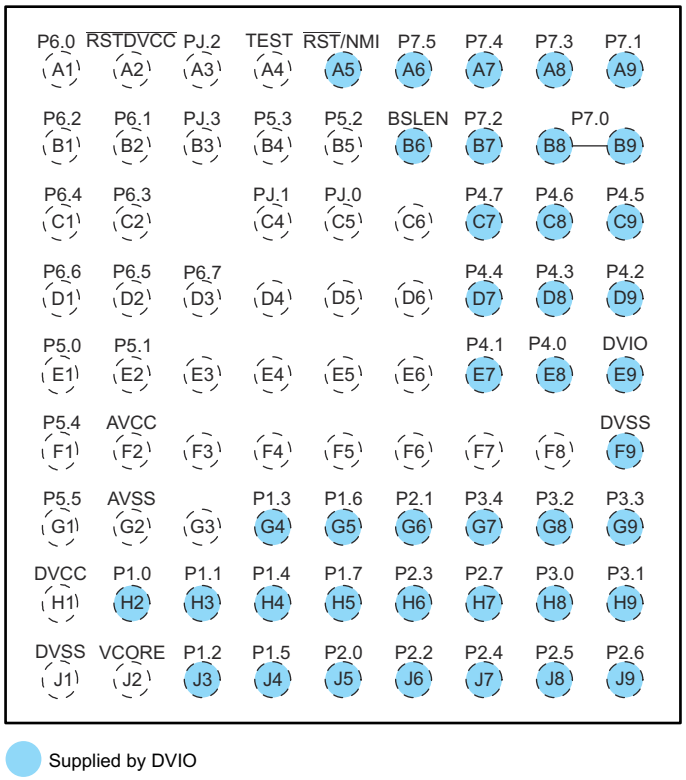


图 7-2. 80-Pin ZXH or ZQE Package (Top View)

7.2 Signal Descriptions

表 7-1 describes the device signals.

表 7-1. Terminal Functions

TERMINAL			I/O(1)	SUPPLY	DESCRIPTION
NAME	NO.(2)				
	RGC	ZXH, ZQE			
P6.0/TA2CLK/SMCLK/CB0/A0	1	A1	I/O	DVCC	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input SMCLK output Comparator_B input CB0 Analog input A0 for ADC (not available on all device types)
P6.1/TA2.0/CB1/A1	2	B2	I/O	DVCC	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output Comparator_B input CB1 Analog input A1 for ADC (not available on all device types) BSL transmit output
P6.2/TA2.1/CB2/A2	3	B1	I/O	DVCC	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output Comparator_B input CB2 Analog input A2 for ADC (not available on all device types) BSL receive input
P6.3/TA2.2/CB3/A3	4	C2	I/O	DVCC	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output Comparator_B input CB3 Analog input A3 for ADC (not available on all device types)
P6.4/CB4/A4	5	C1	I/O	DVCC	General-purpose digital I/O with port interrupt Comparator_B input CB4 Analog input A4 for ADC (not available on all device types)
P6.5/CB5/A5	6	D2	I/O	DVCC	General-purpose digital I/O with port interrupt Comparator_B input CB5 Analog input A5 for ADC (not available on all device types)
P6.6/CB6/A6	7	D1	I/O	DVCC	General-purpose digital I/O with port interrupt Comparator_B input CB6 Analog input A6 for ADC (not available on all device types)
P6.7/CB7/A7	8	D3	I/O	DVCC	General-purpose digital I/O with port interrupt Comparator_B input CB7 Analog input A7 for ADC (not available on all device types)
P5.0/A8/VeREF+	9	E1	I/O	DVCC	General-purpose digital I/O Analog input A8 for ADC (not available on all device types) Input for an external reference voltage to the ADC (not available on all device types)
P5.1/A9/VeREF-	10	E2	I/O	DVCC	General-purpose digital I/O Analog input A9 for ADC (not available on all device types) Negative terminal for the ADC reference voltage for an external applied reference voltage (not available on all device types)
AVCC	11	F2			Analog power supply

表 7-1. Terminal Functions (continued)

TERMINAL			I/O[1]	SUPPLY	DESCRIPTION
NAME	NO.[2]				
	RGC	ZXH, ZQE			
P5.4/XIN	12	F1	I/O	DVCC	General-purpose digital I/O Input terminal for crystal oscillator XT1[3]
P5.5/XOUT	13	G1	I/O	DVCC	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS	14	G2			Analog ground supply
DVCC	15	H1			Digital power supply
DVSS	16	J1			Digital ground supply
VCORE[4]	17	J2		DVCC	Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK[5]	18	H2	I/O	DVIO	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0[5]	19	H3	I/O	DVIO	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output
P1.2/TA0.1[5]	20	J3	I/O	DVIO	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output
P1.3/TA0.2[5]	21	G4	I/O	DVIO	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3[5]	22	H4	I/O	DVIO	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4[5]	23	J4	I/O	DVIO	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT[5]	24	G5	I/O	DVIO	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0[5]	25	H5	I/O	DVIO	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.0/TA1.1[5]	26	J5	I/O	DVIO	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2[5]	27	G6	I/O	DVIO	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/UCB3SIMO/UCB3SDA[5]	28	J6	I/O	DVIO	General-purpose digital I/O with port interrupt Slave in, master out – USCI_B3 SPI mode I^2C data – USCI_B3 I^2C mode
P2.3/UCB3SOMI/UCB3SCL[5]	29	H6	I/O	DVIO	General-purpose digital I/O with port interrupt Slave out, master in – USCI_B3 SPI mode I^2C clock – USCI_B3 I^2C mode
P2.4/UCB3CLK/UCA3STE[5]	30	J7	I/O	DVIO	General-purpose digital I/O with port interrupt Clock signal input – USCI_B3 SPI slave mode Clock signal output – USCI_B3 SPI master mode Slave transmit enable – USCI_A3 SPI mode

表 7-1. Terminal Functions (continued)

TERMINAL			I/O[1]	SUPPLY	DESCRIPTION
NAME	NO.[2]				
	RGC	ZXH, ZQE			
P2.5/UCB3STE/UCA3CLK[5]	31	J8	I/O	DVIO	General-purpose digital I/O with port interrupt Slave transmit enable – USCI_B3 SPI mode Clock signal input – USCI_A3 SPI slave mode Clock signal output – USCI_A3 SPI master mode
P2.6/RTCCLK/DMAE0[5]	32	J9	I/O	DVIO	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input
P2.7/UCB0STE/UCA0CLK[5]	33	H7	I/O	DVIO	General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA[5]	34	H8	I/O	DVIO	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I^2C data – USCI_B0 I^2C mode
P3.1/UCB0SOMI/UCB0SCL[5]	35	H9	I/O	DVIO	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I^2C clock – USCI_B0 I^2C mode
P3.2/UCB0CLK/UCA0STE[5]	36	G8	I/O	DVIO	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO[5]	37	G9	I/O	DVIO	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.4/UCA0RXD/UCA0SOMI[5]	38	G7	I/O	DVIO	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
DVSS	39	F9			Digital ground supply
DVIO[6]	40	E9			Digital I/O power supply
P4.0/PM_UCB1STE/ PM_UCA1CLK[5]	41	E8	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA[5]	42	E7	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I^2C data – USCI_B1 I^2C mode

表 7-1. Terminal Functions (continued)

TERMINAL			I/O[1]	SUPPLY	DESCRIPTION
NAME	NO.[2]				
	RGC	ZXH, ZQE			
P4.2/PM_UCB1SOMI/ PM_UCB1SCL[5]	43	D9	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I^2C clock – USCI_B1 I^2C mode
P4.3/PM_UCB1CLK/ PM_UCA1STE[5]	44	D8	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
P4.4/PM_UCA1TXD/ PM_UCA1SIMO[5]	45	D7	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI[5]	46	C9	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_UCA3TXD/ PM_UCA3SIMO[5]	47	C8	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A3 UART mode Default mapping: Slave in, master out – USCI_A3 SPI mode
P4.7/PM_UCA3RXD/ PM_UCA3SOMI[5]	48	C7	I/O	DVIO	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A3 UART mode Default mapping: Slave out, master in – USCI_A3 SPI mode
P7.0/UCA2TXD/UCA2SIMO[5]	49	B8, B9	I/O	DVIO	General-purpose digital I/O Transmit data – USCI_A2 UART mode Slave in, master out – USCI_A2 SPI mode
P7.1/UCA2RXD/UCA2SOMI[5]	50	A9	I/O	DVIO	General-purpose digital I/O Receive data – USCI_A2 UART mode Slave out, master in – USCI_A2 SPI mode
P7.2/UCB2CLK/UCA2STE[5]	51	B7	I/O	DVIO	General-purpose digital I/O Clock signal input – USCI_B2 SPI slave mode Clock signal output – USCI_B2 SPI master mode Slave transmit enable – USCI_A2 SPI mode
P7.3/UCB2SIMO/UCB2SDA[5]	52	A8	I/O	DVIO	General-purpose digital I/O Slave in, master out – USCI_B2 SPI mode I^2C data – USCI_B2 I^2C mode
P7.4/UCB2SOMI/UCB2SCL[5]	53	A7	I/O	DVIO	General-purpose digital I/O Slave out, master in – USCI_B2 SPI mode I^2C clock – USCI_B2 I^2C mode

表 7-1. Terminal Functions (continued)

TERMINAL			I/O[1]	SUPPLY	DESCRIPTION
NAME	NO.[2]				
	RGC	ZXH, ZQE			
P7.5/UCB2STE/UCA2CLK[5]	54	A6	I/O	DVIO	General-purpose digital I/O Slave transmit enable – USCI_B2 SPI mode Clock signal input – USCI_A2 SPI slave mode Clock signal output – USCI_A2 SPI master mode
BSLEN[5]	55	B6	I	DVIO	BSL enable with internal pulldown
$\overline{\text{RST}}$/NMI[5]	56	A5	I	DVIO	Reset input active low[7] [8] Nonmaskable interrupt input[7]
P5.2/XT2IN	57	B5	I/O	DVCC	General-purpose digital I/O Input terminal for crystal oscillator XT2[9]
P5.3/XT2OUT	58	B4	I/O	DVCC	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK[10]	59	A4	I	DVCC	Test mode pin – Selects four wire JTAG operation Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated
PJ.0/TDO[11]	60	C5	I/O	DVCC	General-purpose digital I/O JTAG test data output port
PJ.1/TDI/TCLK[11]	61	C4	I/O	DVCC	General-purpose digital I/O JTAG test data input or test clock input
PJ.2/TMS[11]	62	A3	I/O	DVCC	General-purpose digital I/O JTAG test mode select
PJ.3/TCK[11]	63	B3	I/O	DVCC	General-purpose digital I/O JTAG test clock
$\overline{\text{RSTDVCC}}$/SBWTDIO[11]	64	A2	I/O	DVCC	Reset input active low[12] Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated
Reserved	N/A	[13]			Reserved
QFN Pad	Pad	N/A			QFN package pad. Connection to V_{SS} recommended.

(1) I = input, O = output
(2) N/A = not available
(3) When in crystal bypass mode, XIN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC or DVSS to DVIO. In this case, the pin must be configured properly for the intended input swing.
(4) VCORE is for internal use only. No external current loading is possible. VCORE should be connected only to the recommended capacitor value, C_{VCORE} (see 节 8.3).
(5) This pin function is supplied by DVIO. See 节 8.8 for input and output requirements.
(6) The voltage on DVIO is not supervised or monitored.
(7) This pin is configurable as reset or NMI and resides on the DVIO supply domain. When driven from external, the input swing levels from DVSS to DVIO are required.
(8) When this pin is configured as reset, the internal pullup resistor is enabled by default.
(9) When in crystal bypass mode, XT2IN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC or DVSS to DVIO. In this case, the must pin be configured properly for the intended input swing.
(10) See 节 9.5.1 and 节 9.6 for use with BSL and JTAG functions, respectively.
(11) See 节 9.6 for use with JTAG function.
(12) This nonconfigurable reset resides on the DVCC supply domain and has an internal pullup to DVCC. When driven from external, input swing levels from DVSS to DVCC are required. This reset must be used for Spy-Bi-Wire communication and is not the same $\overline{\text{RST}}$/NMI reset as found on other devices in the MSP430 family. Refer to 节 9.5.1 and 节 9.6 for details regarding the use of this pin.
(13) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

8 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	– 0.3	4.1	V
Voltage applied at V_{IO} to V_{SS}	– 0.3	2.2	V
Voltage applied to any pin (excluding VCORE and V_{IO} pins)(2)	– 0.3	V_{CC} + 0.3	V
Voltage applied to V_{IO} pins	– 0.3	V_{IO} + 0.2	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (3)	– 55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

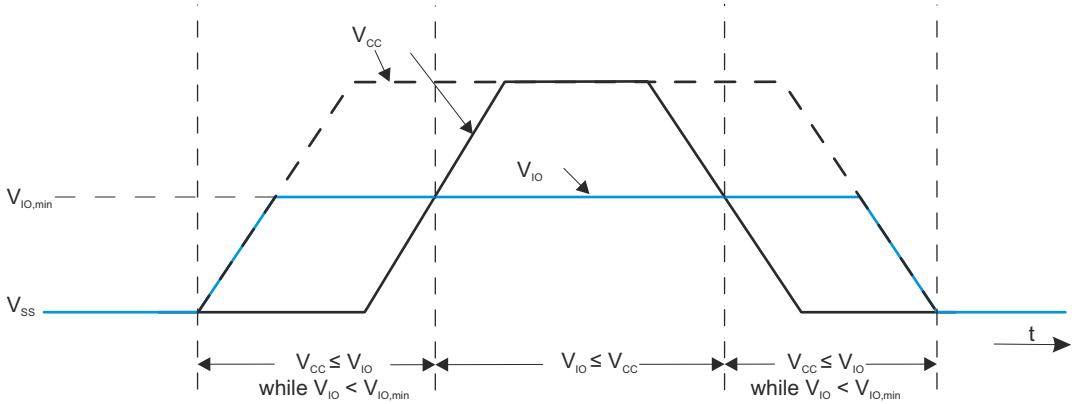
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AV_{CC} = DV_{CC})(1) (2) (3)	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
V_{IO}	Supply voltage applied to DVIO referenced to V_{SS} (2)		1.62		1.98	V
V_{SS}	Supply voltage (AV_{SS} = DV_{SS})			0		V
T_A	Operating free-air temperature		– 40		85	°C
T_J	Operating junction temperature		– 40		85	°C
C_{VCORE}	Recommended capacitor at VCORE(4)			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(5) (see 图 8-3)	PMMCOREVx = 0 (default condition), 1.8 V ⩽ V_{CC} ⩽ 3.6 V	0		8.0	MHz
		PMMCOREVx = 1, 2.0 V ⩽ V_{CC} ⩽ 3.6 V	0		12.0	
		PMMCOREVx = 2, 2.2 V ⩽ V_{CC} ⩽ 3.6 V	0		20.0	
		PMMCOREVx = 3, 2.4 V ⩽ V_{CC} ⩽ 3.6 V	0		25.0	

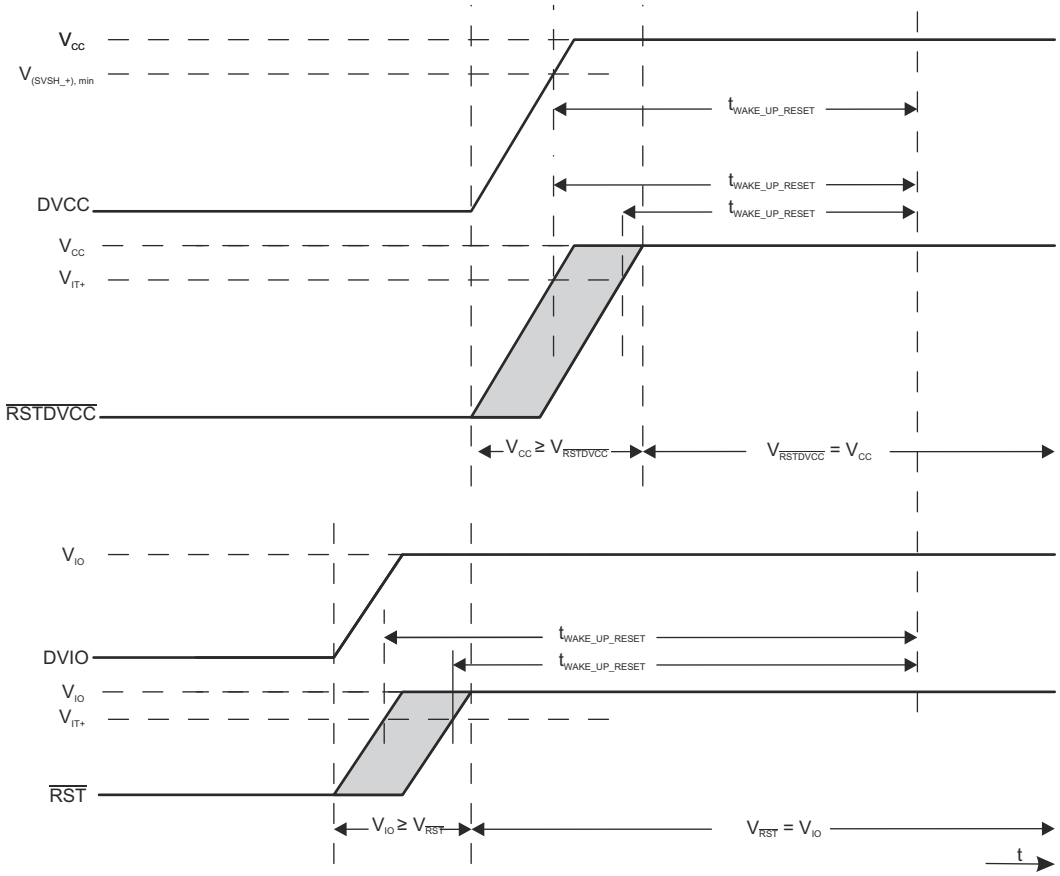
(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.

(2) During V_{CC} and V_{IO} power up, it is required that $V_{IO} \geqslant V_{CC}$ during the ramp up phase of V_{IO}. During V_{CC} and V_{IO} power down, it is required that $V_{IO} \geqslant V_{CC}$ during the ramp down phase of V_{IO} (see 图 8-1).
(3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the 节 8.28 threshold parameters for the exact values and further details.
(4) TI recommends a capacitor tolerance of ±20% or better.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



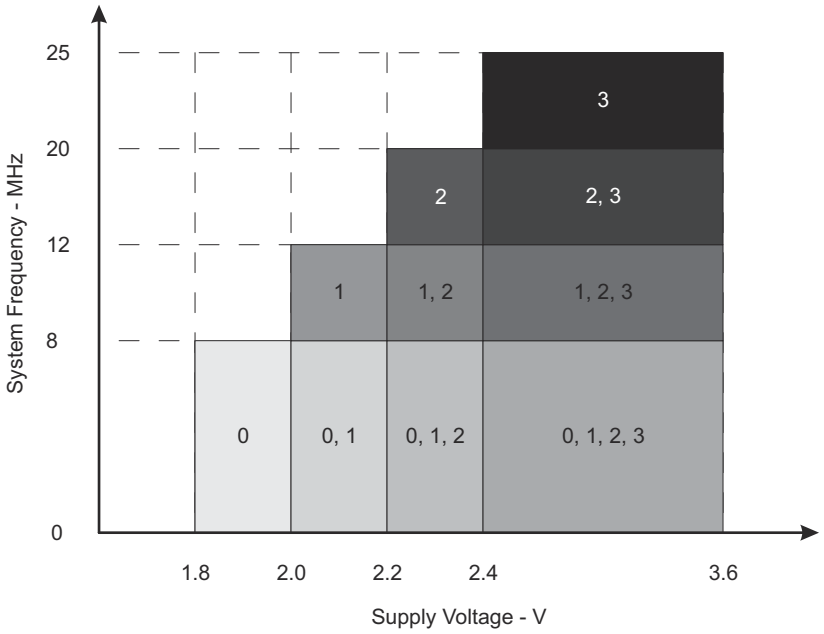
NOTE: The device supports continuous operation with $V_{CC} = V_{SS}$ while V_{IO} is fully within its specification. During this time, the general-purpose I/Os that reside on the V_{IO} supply domain are configured as inputs and pulled down to V_{SS} through their internal pulldown resistors. $\overline{RST}$/NMI is high impedance. BSLEN is configured as an input and is pulled down to V_{SS} through its internal pulldown resistor. When V_{CC} reaches above the BOR threshold, the general-purpose I/Os become high-impedance inputs (no pullup or pulldown enabled), $\overline{RST}$/NMI becomes an input pulled up to V_{IO} through its internal pullup resistor, and BSLEN remains pulled down to V_{SS} through its internal pulldown resistor.
NOTE: Under certain condtions during the rising transition of V_{CC}, the general-purpose I/Os that reside on the V_{IO} supply domain may actively transition high momentarily before settling to high-impedance inputs. These voltage transitions are temporary (typically resolving to high impedance inputs when V_{CC} exceeds approximately 0.9 V) and are bounded by the V_{IO} supply.

图 8-1. V_{CC} and V_{IO} Power Sequencing



NOTE:The device remains in reset based on the conditions of the $\overline{RSTDVCC}$ and $\overline{RST}$ pins and the voltage present on DVCC voltage supply. If $\overline{RSTDVCC}$ or $\overline{RST}$ is held at a logic low or if DVCC is below the SVSH_+ minimum threshold, the device remains in its reset condition; that is, these conditions form a logical OR with respect to device reset.

图 8-2. Reset Timing



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

图 8-3. Maximum System Frequency

8.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3.0 V	0	0.36	0.47	2.32	2.60							mA
			1	0.40		2.65		4.0	4.4					
			2	0.44		2.90		4.3		7.1	7.7			
			3	0.46		3.10		4.6		7.6		10.1	11.0	
$I_{AM, RAM}$	RAM	3.0 V	0	0.20	0.29	1.20	1.30							mA
			1	0.22		1.35		2.0	2.2					
			2	0.24		1.50		2.2		3.7	4.2			
			3	0.26		1.60		2.4		3.9		5.3	6.2	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

8.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	TEMPERATURE (T_A)								UNIT
				– 40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3) (9)	2.2 V	0	73		78	91	84		93	103	µA
		3.0 V	3	89		95	105	101		112	124	
I_{LPM2}	Low-power mode 2(4) (9)	2.2 V	0	6.7		6.7	12	10.6		13	29	µA
		3.0 V	3	7.2		7.2	13	11.6		14	30	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(5) (9)	2.2 V	0	1.8		2.1		3.4		8.4		µA
			1	1.9		2.2		3.6		8.7		
			2	2.0		2.4		3.8		9.0		
		3.0 V	0	2.0		2.3	3.1	3.6		8.6	24	
			1	2.1		2.5		3.8		8.9		
			2	2.2		2.6		3.9		9.2		
			3	2.3		2.7	4.1	4.0		9.2	25	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(6) (9)	3.0 V	0	1.3		1.6	2.9	2.6		8.5	24	µA
			1	1.3		1.6		2.8		8.8		
			2	1.4		1.7		2.9		9.2		
			3	1.5		1.8	3.2	2.9		9.2	25	
I_{LPM4}	Low-power mode 4(7) (9)	3.0 V	0	1.1		1.3	1.7	2.6		7.5	22	µA
			1	1.3		1.4		2.7		7.7		
			2	1.4		1.4		2.8		7.9		
			3	1.5		1.5	1.8	2.8		7.9	23	
$I_{LPM4.5}$	Low-power mode 4.5(8)	3.0 V		0.15		0.18	0.35	0.26		0.5	1.0	µA
I_{DVIO_START}	Current supplied from DVIO while DVCC = AVCC = 0 V, DVIO = 1.62 V to 1.98 V, All DVIO I/O floating including BSLEN and $\overline{RST}$/NMI	0 V		1.40		1.40	2.0	1.45		1.5	2.1	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for the watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
(4) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCO setting = 1-MHz operation, DCO bias generator enabled.)
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(7) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(8) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(9) Current for brownout and high-side supervisor (SVS_H) normal mode included. Low-side supervisor (SVS_L) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.

8.6 Thermal Resistance Characteristics

THERMAL METRIC(1) (2)			VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, still air	VQFN 64 (RGC)	29.3	°C/W
		BGA 80 (ZQE)	52.0	
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	VQFN 64 (RGC)	14.2	°C/W
		BGA 80 (ZQE)	23.9	
$R_{\theta JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance	VQFN 64 (RGC)	1.1	°C/W
		BGA 80 (ZQE)	N/A(3)	
$R_{\theta JB}$	Junction-to-board thermal resistance	VQFN 64 (RGC)	8.2	°C/W
		BGA 80 (ZQE)	29.3	
Ψ_{JT}	Junction-to-package-top thermal characterization parameter	VQFN 64 (RGC)	0.2	°C/W
		BGA 80 (ZQE)	0.5	
Ψ_{JB}	Junction-to-board thermal characterization parameter	VQFN 64 (RGC)	8.1	°C/W
		BGA 80 (ZQE)	29.3	

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R_{\theta JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = not applicable

8.7 Schmitt-Trigger Inputs – General-Purpose I/O DVCC Domain (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, $\overline{\text{RSTDVCC}}$)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) These same parametrics apply to the clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

8.8 Schmitt-Trigger Inputs – General-Purpose I/O DVIO Domain (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5, $\overline{\text{RST}}$/NMI, BSLEN)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IO}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.0 V	1.62 V	0.8		1.25	V
			1.98 V	1.1		1.40	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.0 V	1.62 V	0.3		0.7	V
			1.98 V	0.5		1.0	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 3.0 V	1.62 V to 1.98 V	0.3		0.8	V
R_{Pull}	Pullup or pulldown resistor[1]	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{IO}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{IO}			5		pF

(1) Also applies to the $\overline{\text{RST}}$ pin when the pullup or pulldown resistor is enabled.

8.9 Inputs – Interrupts DVCC Domain Port P6 (P6.0 to P6.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing[1]	External trigger pulse duration to set interrupt flag	1.8 V, 3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

8.10 Inputs – Interrupts DVIO Domain Ports P1 and P2 (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IO} [2]	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing[1]	External trigger pulse duration to set interrupt flag, V_{CC} = 1.8 V or 3.0 V	1.62 V to 1.98 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.
(2) In all test conditions, $V_{IO} \leq V_{CC}$.

8.11 Leakage Current – General-Purpose I/O DVCC Domain (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See (1) (2)	1.8 V, 3 V	–50	50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

8.12 Leakage Current – General-Purpose I/O DVIO Domain (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IO} (1)	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See (2) (3)	1.62 V to 1.98 V	–50	50	nA

(1) In all test conditions, $V_{IO} \leq V_{CC}$.
(2) The leakage current is measured with V_{SS} or V_{IO} applied to the corresponding pins, unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

8.13 Outputs – General-Purpose I/O DVCC Domain (Full Drive Strength) (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA(1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA(1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

8.14 Outputs – General-Purpose I/O DVCC Domain (Reduced Drive Strength) (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = – 1 mA(1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = – 3 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = – 2 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = – 6 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) Selecting reduced drive strength may reduce EMI.

8.15 Outputs – General-Purpose I/O DVIO Domain (Full Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IO} (2)	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = – 100 µA(1)	1.62 V to 1.98 V	V_{IO} – 0.05	V_{IO}	V
		$I_{(OHmax)}$ = – 3 mA(1)		V_{IO} – 0.25	V_{IO}	
		$I_{(OHmax)}$ = – 6 mA(1)		V_{IO} – 0.50	V_{IO}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	1.62 V to 1.98 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 6 mA(1)		V_{SS}	V_{SS} + 0.50	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) In all test conditions, $V_{IO} \leq V_{CC}$.

8.16 Outputs – General-Purpose I/O DVIO Domain (Reduced Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	V_{IO} (3)	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = – 100 µA(1)	1.62 V to 1.98 V	V_{IO} – 0.05	V_{IO}	V
		$I_{(OHmax)}$ = – 1 mA(1)		V_{IO} – 0.25	V_{IO}	
		$I_{(OHmax)}$ = – 2 mA(1)		V_{IO} – 0.50	V_{IO}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	1.62 V to 1.98 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 2 mA(1)		V_{SS}	V_{SS} + 0.50	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) Selecting reduced drive strength may reduce EMI.
(3) In all test conditions, $V_{IO} \leq V_{CC}$.

8.17 Output Frequency – General-Purpose I/O DVCC Domain (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	See (1) (2)	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	
f_{Port_CLK}	Clock output frequency	ACLK, SMCLK, or MCLK, C_L = 20 pF(2)	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

8.18 Output Frequency – General-Purpose I/O DVIO Domain (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	See (1) (2)	V_{IO} = 1.62 V to 1.98 V(3), PMMCOREVx = 0		16	MHz
			V_{IO} = 1.62 V to 1.98 V(3), PMMCOREVx = 3		25	
f_{Port_CLK}	Clock output frequency	ACLK, SMCLK, or MCLK, C_L = 20 pF(2)	V_{IO} = 1.62 V to 1.98 V(3), PMMCOREVx = 0		16	MHz
			V_{IO} = 1.62 V to 1.98 V(3), PMMCOREVx = 3		25	

(1) A resistive divider with 2 × R1 between V_{IO} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{IO} at the specified toggle frequency.
(3) In all test conditions, $V_{IO} \leqslant V_{CC}$.

8.19 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

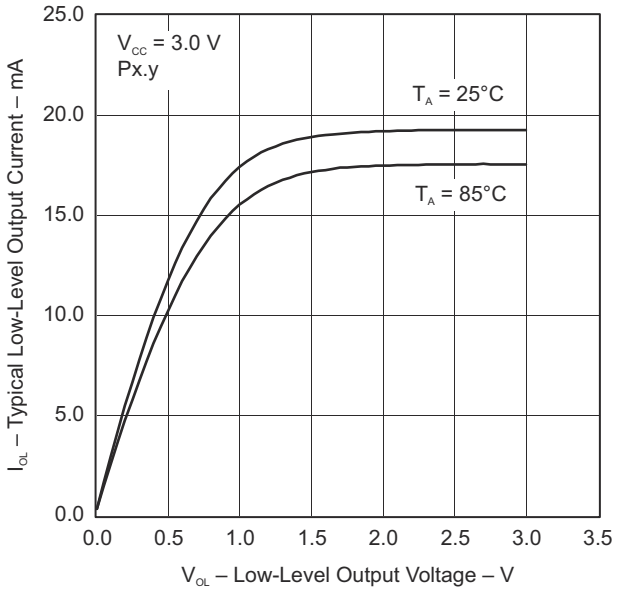


图 8-4. Typical Low-Level Output Current vs Low-Level Output Voltage

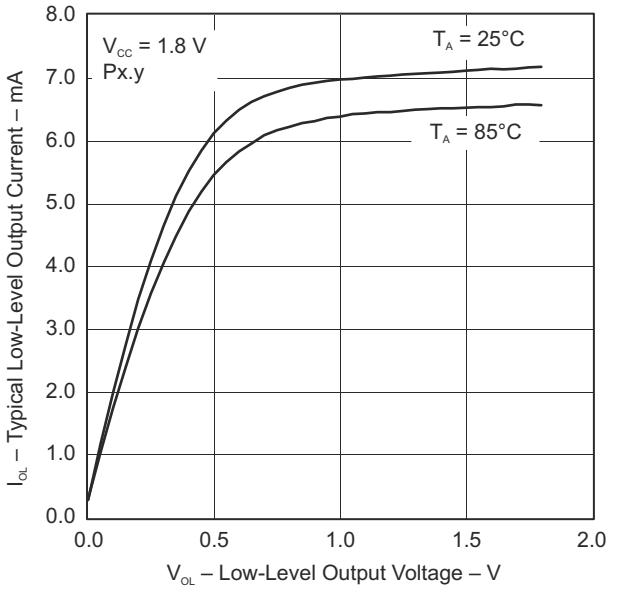


图 8-5. Typical Low-Level Output Current vs Low-Level Output Voltage

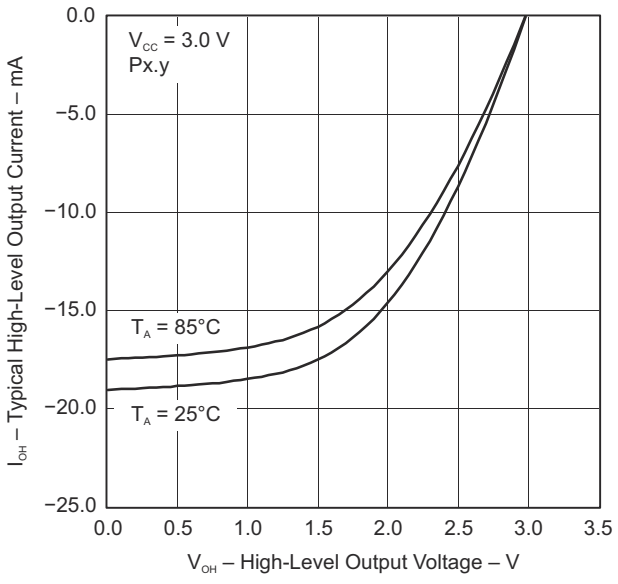


图 8-6. Typical High-Level Output Current vs High-Level Output Voltage

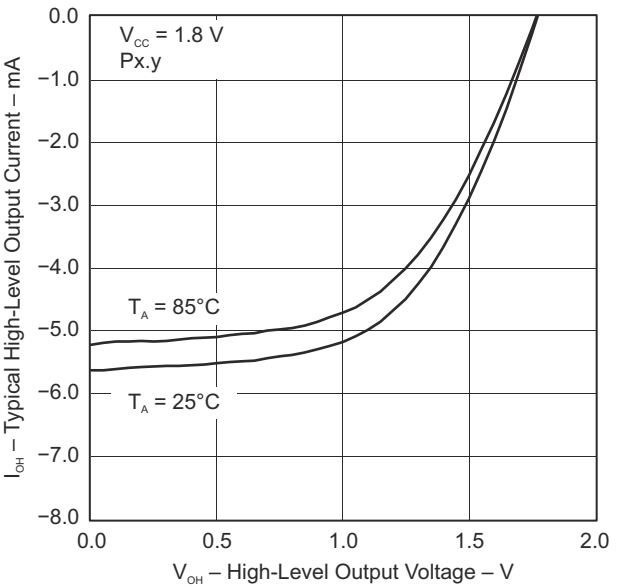


图 8-7. Typical High-Level Output Current vs High-Level Output Voltage

8.20 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

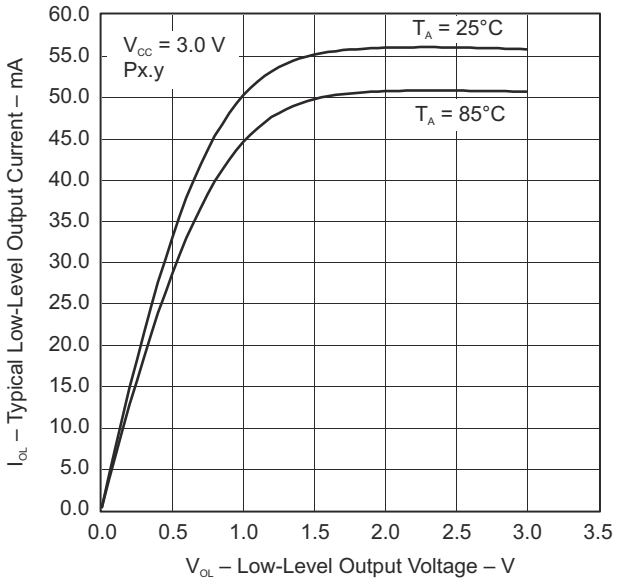


图 8-8. Typical Low-Level Output Current vs Low-Level Output Voltage

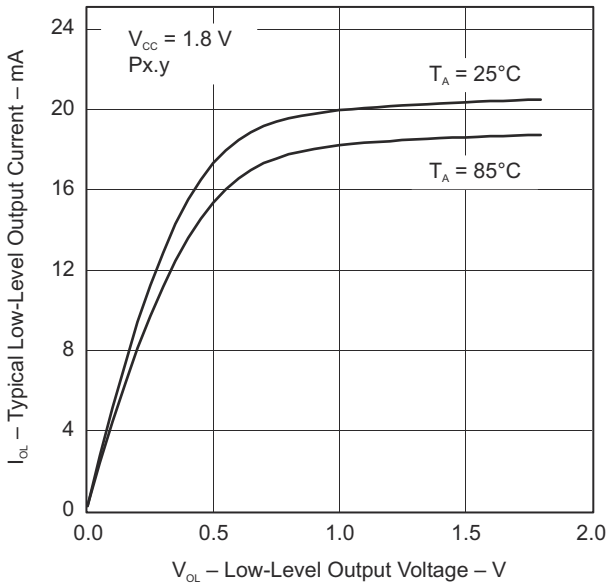


图 8-9. Typical Low-Level Output Current vs Low-Level Output Voltage

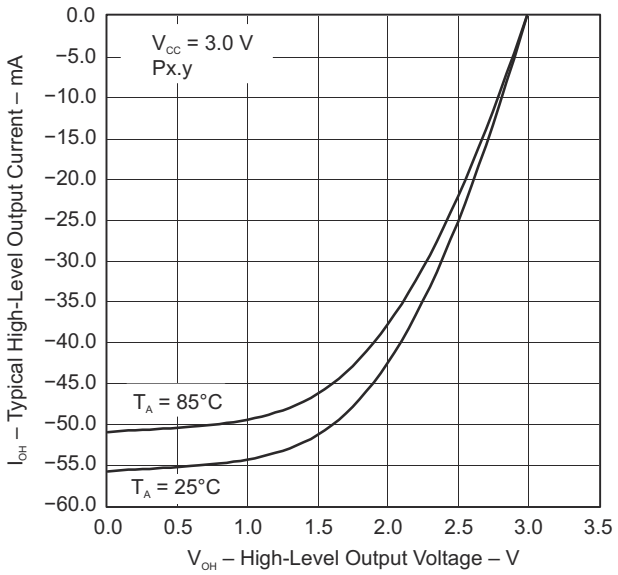


图 8-10. Typical High-Level Output Current vs High-Level Output Voltage

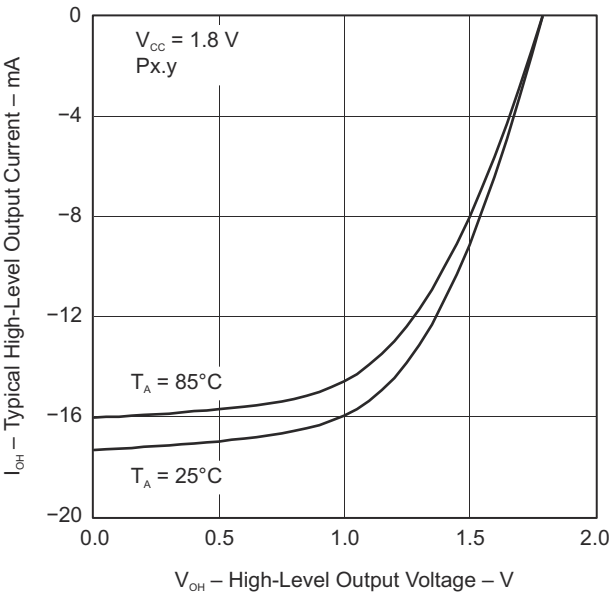


图 8-11. Typical High-Level Output Current vs High-Level Output Voltage

8.21 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3.0 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1(2) (3) XT1BYPASSLV = 0 or 1		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals(4)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(5)	XTS = 0, XCAPx = 0(6)			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30%		70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(7)	XTS = 0, XT1BYPASS = 1(8), XT1BYPASSLV = 0 or 1		10		10000	Hz
$t_{START,LF}$	Start-up time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3.0 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square-wave with parametrics defined in the Schmitt-Trigger Inputs section of this data sheet. When in crystal bypass mode, XIN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC (XT1BYPASSLV = 0) or DVSS to DVIO (XT1BYPASSLV = 1). In this case, it is required that the pin be configured properly for the intended input swing.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but each application should be evaluated based on the actual crystal selected:
- For XT1DRIVEx = 0, $C_{L,eff} \leqslant 6$ pF
- For XT1DRIVEx = 1, 6 pF $\leqslant C_{L,eff} \leqslant$ 9 pF
- For XT1DRIVEx = 2, 6 pF $\leqslant C_{L,eff} \leqslant$ 10 pF
- For XT1DRIVEx = 3, $C_{L,eff} \geqslant 6$ pF

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

8.22 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 0,	3.0 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 1,			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 2,			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, T_A = 25°C, XT2BYPASS = 0, XT2DRIVEx = 3,			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0(3)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0(3)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0(3)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0(3)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1(4) (3) XT2BYPASSLV = 0 or 1		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Start-up time	f_{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3.0 V		0.5		ms
		f_{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6) (1)				1		pF
	Duty cycle	Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8), XT2BYPASSLV = 0 or 1		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.

- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square-wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. When in crystal bypass mode, XT2IN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC (XT2BYPASSLV = 0) or DVSS to DVIO (XT2BYPASSLV = 1). In this case, it is required that the pin be configured properly for the intended input swing.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals. Typically, an effective load capacitance of up to 18 pF can be supported.

8.23 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

8.24 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V	–3.5%		3.5%	
		T_A = 25°C	3 V	–1.5%		1.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

8.25 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40%	50%	60%	
df_{DCO}/dT	DCO frequency temperature drift(2)	f_{DCO} = 1 MHz		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift(3)	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n, 0),MAX} \leqslant f_{DCO} \leqslant f_{DCO(n, 31),MIN}$, where $f_{DCO(n, 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

(2) Calculated using the box method: (MAX(– 40°C to 85°C) – MIN(– 40°C to 85°C)) / MIN(– 40°C to 85°C) / (85°C – (– 40°C))

(3) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

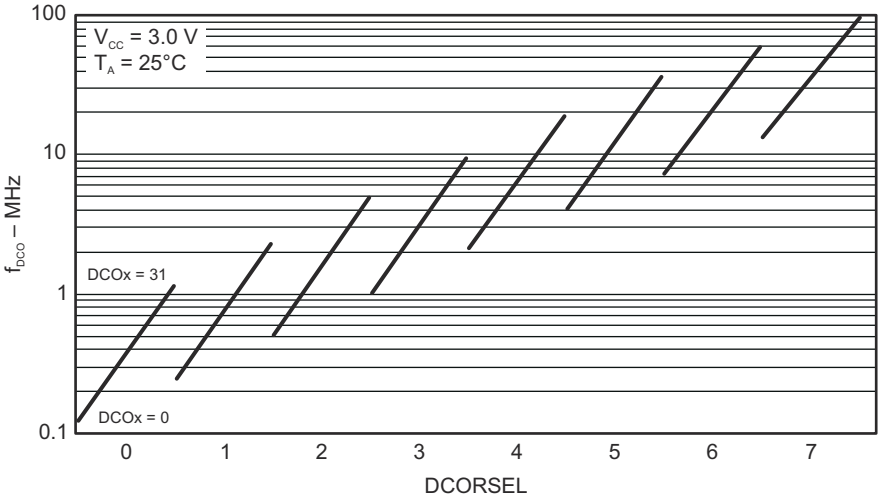


图 8-12. Typical DCO Frequency

8.26 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DVCC\_BOR\_IT-}$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s			1.45	V
$V_{DVCC\_BOR\_IT+}$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s	0.80	1.30	1.50	V
$V_{DVCC\_BOR\_hys}$	BOR_H hysteresis		50		250	mV
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

8.27 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.90		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.80		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.60		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.40		V
V_{CORE3}(LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.94		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.84		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.64		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.44		V

8.28 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level(1)	SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	
		SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
		SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level(1)	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVSHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVSHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVSHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0 → 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.

8.29 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE= 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
$V_{(SVMH)}$	SVM_H on or off voltage level(1)	SVMHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVMHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVMHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVMHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVMHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVMHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVMHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0 → 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.

8.30 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		100		

8.31 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 0		200		
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		100		

8.32 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode[1]	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geqslant$ 4.0 MHz		3.5	7.5	µs
			1.0 MHz < f_{MCLK} < 4.0 MHz		4.5	9	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode[2] [3]	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	175	µs
$t_{WAKE-UP-LPM5}$	Wake-up time from LPM4.5 to active mode[4]				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode[4]				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-FAST}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-SLOW}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.

(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.

(4) This value represents the time from the wake-up event to the reset vector execution.

8.33 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	V_{IO}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V	1.62 V to 1.8 V		25	MHz
			3.0 V	1.62 V to 1.98 V		25	
$t_{TA,cap}$	Timer_A capture timing(1)	All capture inputs, minimum pulse duration required for capture	1.8 V	1.62 V to 1.8 V	20		ns
			3.0 V	1.62 V to 1.98 V	20		

(1) The external signal sets the interrupt flag every time the minimum parameters are met. It may be set even with trigger signals shorter than $t_{TA,cap}$.

8.34 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	V_{IO}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	1.8 V	1.62 V to 1.8 V		25	MHz
			3.0 V	1.62 V to 1.98 V		25	
$t_{TB,cap}$	Timer_B capture timing(1)	All capture inputs, minimum pulse duration required for capture	1.8 V	1.62 V to 1.8 V	20		ns
			3.0 V	1.62 V to 1.98 V	20		

(1) The external signal sets the interrupt flag every time the minimum parameters are met. It may be set even with trigger signals shorter than $t_{TB,cap}$.

8.35 USCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			1	MHz

8.36 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	V_{IO}	MIN	MAX	UNIT
t_τ	UART receive deglitch time(1)	1.8 V	1.62 V to 1.80 V	50	600	ns
		3.0 V	1.62 V to 1.98 V	50	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

8.37 USCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz

8.38 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see 图 8-13 and 图 8-14)

PARAMETER		TEST CONDITIONS	V_{CC}	V_{IO}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK or ACLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	55		ns
			3.0 V	1.62 V to 1.98 V	55		
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	35		
			3.0 V	1.62 V to 1.98 V	35		
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	0		ns
			3.0 V	1.62 V to 1.98 V	0		
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	0		
			3.0 V	1.62 V to 1.98 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V	1.62 V to 1.80 V		20	ns
			3.0 V	1.62 V to 1.98 V		20	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V	1.62 V to 1.98 V		16	
			3.0 V	1.62 V to 1.98 V		16	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	–10		ns
			3.0 V	1.62 V to 1.98 V	–10		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	–10		
			3.0 V	1.62 V to 1.98 V	–10		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 图 8-13 and 图 8-14.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 图 8-13 and 图 8-14.

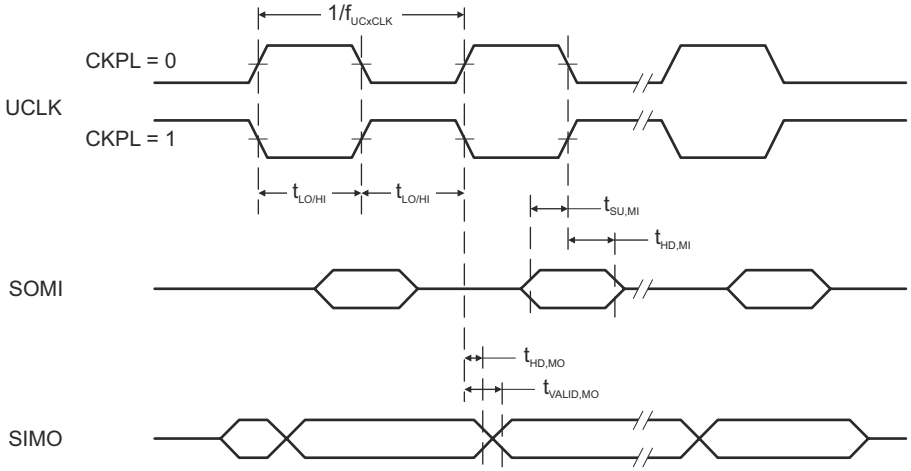


图 8-13. SPI Master Mode, CKPH = 0

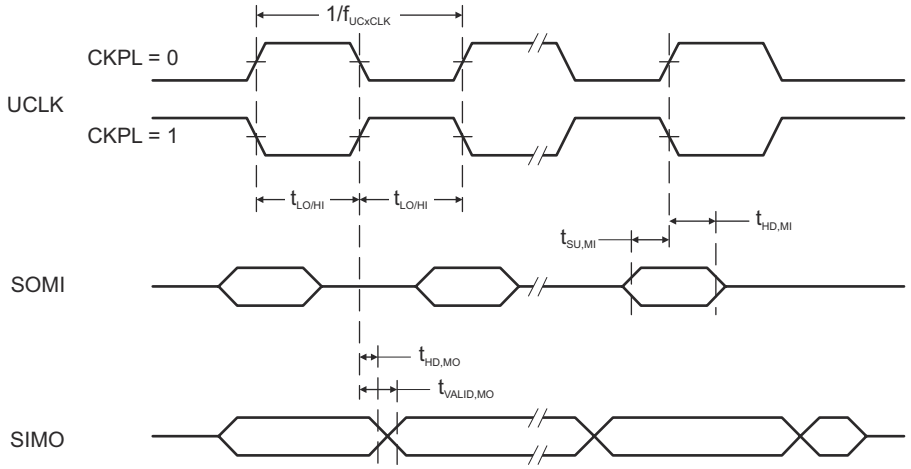


图 8-14. SPI Master Mode, CKPH = 1

8.39 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see 图 8-15 and 图 8-16)

PARAMETER		TEST CONDITIONS	V_{CC}	V_{IO}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	12		ns
			3.0 V	1.62 V to 1.98 V	12		
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	10		
			3.0 V	1.62 V to 1.98 V	10		
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	6		ns
			3.0 V	1.62 V to 1.98 V	6		
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	6		
			3.0 V	1.62 V to 1.98 V	6		
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V		65	ns
			3.0 V	1.62 V to 1.98 V		65	
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V		45	
			3.0 V	1.62 V to 1.98 V		45	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V		35	ns
			3.0 V	1.62 V to 1.98 V		35	
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V		25	
			3.0 V	1.62 V to 1.98 V		25	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	5		ns
			3.0 V	1.62 V to 1.98 V	5		
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	5		
			3.0 V	1.62 V to 1.98 V	5		
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	5		ns
			3.0 V	1.62 V to 1.98 V	5		
		PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	5		
			3.0 V	1.62 V to 1.98 V	5		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V	1.62 V to 1.80 V		75	ns
			3.0 V	1.62 V to 1.98 V		75	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V	1.62 V to 1.98 V		50	
			3.0 V	1.62 V to 1.98 V		50	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	1.62 V to 1.80 V	10		ns
			3.0 V	1.62 V to 1.98 V	10		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	1.62 V to 1.98 V	10		
			3.0 V	1.62 V to 1.98 V	10		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 图 8-15 and 图 8-16.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 图 8-15 and 图 8-16.

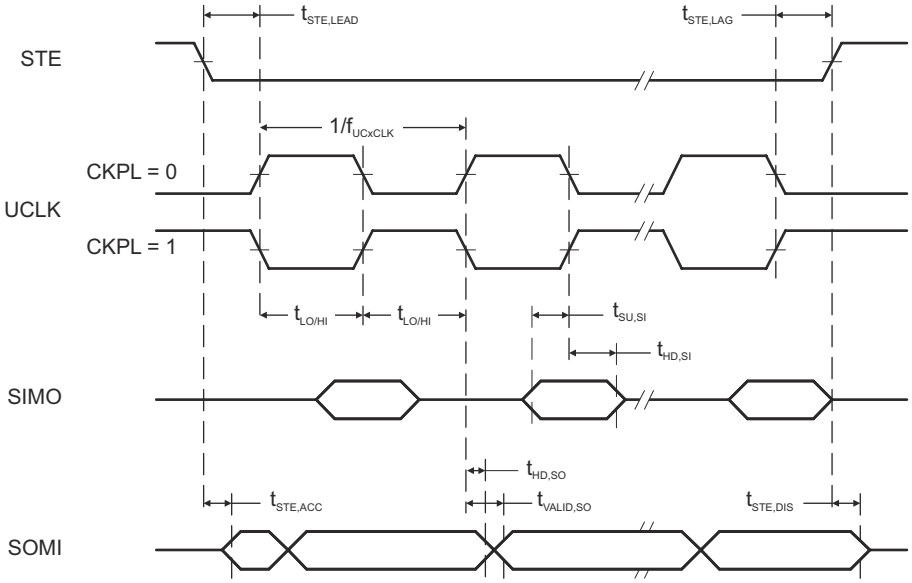


图 8-15. SPI Slave Mode, CKPH = 0

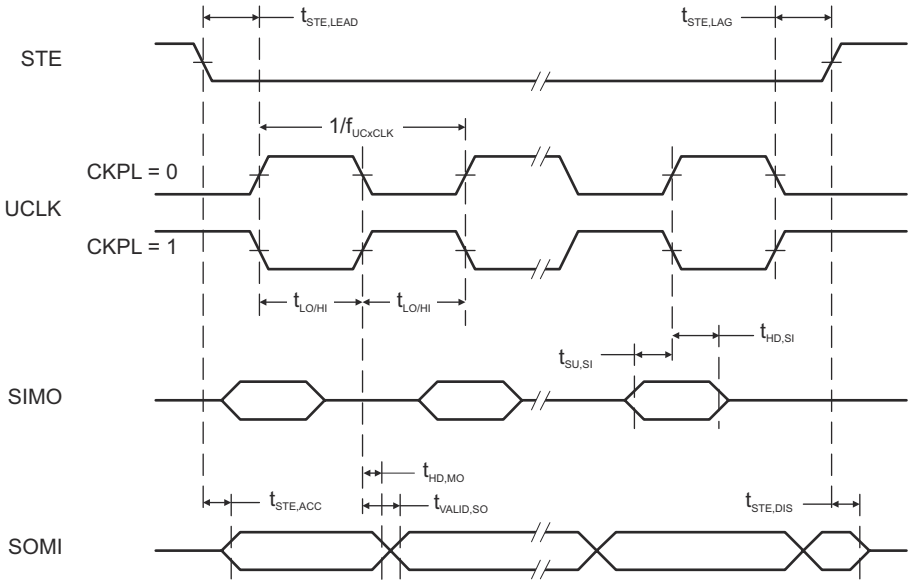


图 8-16. SPI Slave Mode, CKPH = 1

8.40 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-17)

PARAMETER		TEST CONDITIONS	V_{CC}	V_{IO} (1)	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	1.62 V to 1.98 V	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \leqslant$ 100 kHz	2.2 V, 3 V	1.62 V to 1.98 V	4.0		µs
		f_{SCL} > 100 kHz			0.6		
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \leqslant$ 100 kHz	2.2 V, 3 V	1.62 V to 1.98 V	4.7		µs
		f_{SCL} > 100 kHz			0.6		
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	1.62 V to 1.98 V	0		ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	1.62 V to 1.98 V	250		ns
$t_{SU,STO}$	Setup time for STOP	$f_{SCL} \leqslant$ 100 kHz	2.2 V, 3 V	1.62 V to 1.98 V	4.0		µs
		f_{SCL} > 100 kHz			0.6		
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V, 3 V	1.62 V to 1.98 V	50	600	ns

(1) In all test conditions, $V_{IO} \leqslant V_{CC}$

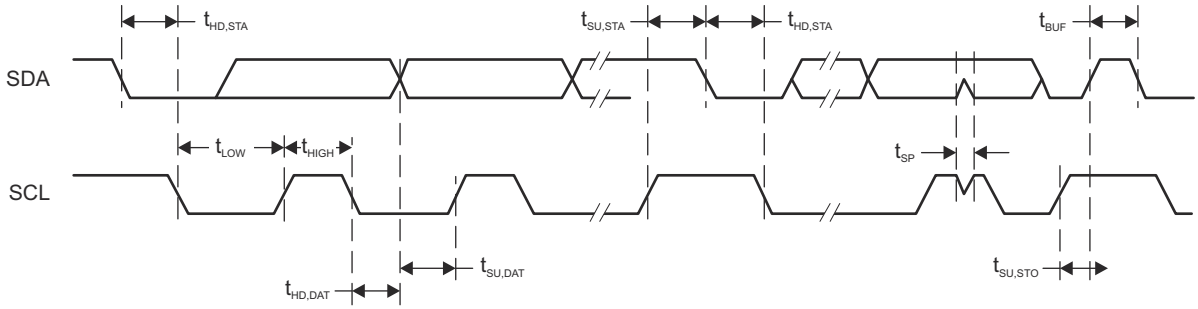


图 8-17. I²C Mode Timing

8.41 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		1.8		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals		0		AV_{CC}	V
I_{ADC10_A}	Operating supply current into AVCC terminal, REF module and reference buffer off	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00	2.2 V		60	100	µA
			3 V		75	110	
	Operating supply current into AVCC terminal, REF module on, reference buffer on	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01	3 V		113	150	µA
	Operating supply current into AVCC terminal, REF module off, reference buffer on	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V	3 V		105	140	µA
	Operating supply current into AVCC terminal, REF module off, reference buffer off	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V	3 V		70	110	µA
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad	2.2 V		3.5		pF
R_I	Input MUX ON resistance	AV_{CC} > 2 V, 0 V ≤ V_{Ax} ≤ AV_{CC}				36	kΩ
		1.8 V < AV_{CC} < 2 V, 0 V ≤ V_{Ax} ≤ AV_{CC}				96	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. See 节 8.44.

8.42 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$		For specified performance of ADC10_A linearity parameters	2.2 V, 3 V	0.45	5	5.5	MHz
$f_{ADC10OSC}$	Internal ADC10_A oscillator(3)	ADC10DIV = 0, $f_{ADC10CLK}$ = $f_{ADC10OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode $f_{ADC10OSC}$ = 4 MHz to 5 MHz	2.2 V, 3 V	2.4		3.0	µs
		External $f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0			12 × 1 / $f_{ADC10CLK}$		
$t_{ADC10ON}$	Turnon settling time of the ADC	See (1)				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 96 k Ω, C_I = 3.5 pF(2)	1.8 V	3			µs
			3.0 V	1			µs

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(2) Approximately 8 Tau (τ) are needed to get an error of less than ±0.5 LSB
(3) The ADC10OSC is sourced directly from MODOSC inside the UCS.

8.43 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	$1.4\ V \leqslant (V_{eREF+} - V_{eREF-}) \leqslant 1.6\ V$, $C_{VeREF+} = 20\ pF$	2.2 V, 3 V			±1.0	LSB
		$1.6\ V < (V_{eREF+} - V_{eREF-}) \leqslant V_{AVCC}$, $C_{VeREF+} = 20\ pF$				±1.0	
E_D	Differential linearity error	$1.4\ V \leqslant (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$	2.2 V, 3 V			±1.0	LSB
E_O	Offset error	$1.4\ V \leqslant (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$, Internal impedance of source $R_S < 100\ \Omega$	2.2 V, 3 V			±1.0	LSB
E_G	Gain error	$1.4\ V \leqslant (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$, ADC10SREFx = 11b	2.2 V, 3 V			±1.0	LSB
E_T	Total unadjusted error	$1.4\ V \leqslant (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$, ADC10SREFx = 11b	2.2 V, 3 V		±1.0	±2.0	LSB

8.44 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{eREF-}$ (2)		1.4	AV_{CC}	V
V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{eREF-}$ (3)		0	1.2	V
$(V_{eREF+} - V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{eREF-}$ (4)		1.4	AV_{CC}	V
I_{VeREF+}, I_{VeREF-}	Static input current	$1.4\ V \leqslant V_{eREF+} \leqslant V_{AVCC}$, $V_{eREF-} = 0\ V$, $f_{ADC10CLK} = 5\ MHz$, ADC10SHTx = 0x0001, Conversion rate 200 ksps	2.2 V, 3 V	–26	26	μA
		$1.4\ V \leqslant V_{eREF+} \leqslant V_{AVCC}$, $V_{eREF-} = 0\ V$, $f_{ADC10CLK} = 5\ MHZ$, ADC10SHTX = 0x1000, Conversion rate 20 ksps	2.2 V, 3 V	–1	1	μA
C_{VREF+}, C_{VREF-}	Capacitance at VeREF+ or VeREF- terminal	See (5)		10		μF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide*.

8.45 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage	REFVSEL = {2} for 2.5 V REFON = 1	3 V	2.445	2.486	2.527	V
		REFVSEL = {1} for 2.0 V REFON = 1	3 V	1.94	1.97	2.01	
		REFVSEL = {0} for 1.5 V REFON = 1	2.2 V, 3 V	1.461	1.485	1.511	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal(1)	$f_{ADC10CLK}$ = 5.0 MHz REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V	3 V		18	24	µA
		$f_{ADC10CLK}$ = 5.0 MHz REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V	3 V		15.5	21	µA
		$f_{ADC10CLK}$ = 5.0 MHz REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V	3 V		13.5	21	µA
TC_{REF+}	Temperature coefficient of built-in reference(2)	I_{VREF+} = 0 A REFVSEL = {0, 1, 2}, REFON = 1			30	50	ppm/°C
I_{SENSOR}	Operating supply current into AVCC terminal(4)	REFON = 0, INCH = 0Ah, ADC10ON = N/A, T_A = 30°C	2.2 V		20	22	µA
			3 V		20	22	
V_{SENSOR}	See (5)	ADC10ON = 1, INCH = 0Ah, T_A = 30°C	2.2 V		770		mV
			3 V		770		
V_{MID}	AVCC divider at channel 11	ADC10ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(6)	ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB		30			µs
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(7)	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB		1			µs
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1			120		µV/V
PSRR_AC	Power supply rejection ratio (AC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1			6.4		mV/V
t_{SETTLE}	Settling time of reference voltage(3)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), REFVSEL = {0, 1, 2}, REFON = 0 → 1			75		µs

(1) The internal reference current is supplied from terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(3) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.
(4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(5) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(7) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

8.46 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00, CBON = 1, CBRSx = 00	1.8 V			38	µA
			2.2 V		31	38	
			3 V		32	39	
		CBPWRMD = 01, CBON = 1, CBRSx = 00	2.2 V, 3 V		10	17	
		CBPWRMD = 10, CBON = 1, CBRSx = 00	2.2 V, 3 V		0.2	0.85	
V_{REF}	Reference voltage level	CBREFLx = 01, CBREFACC = 0	⩾1.8V	1.400	1.43	1.472	V
		CBREFLx = 10, CBREFACC = 0	⩾2.2V	1.864	1.90	1.960	
		CBREFLx = 11, CBREFACC = 0	⩾3.0V	2.32	2.37	2.44	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Includes REF module current	CBREFACC = 0, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0	2.2 V, 3 V		33	40	µA
		CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0	2.2 V, 3 V		17	22	
V_{IC}	Common mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00		– 20		20	mV
		CBPWRMD = 01, 10		– 10		10	
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	On (switch closed)			3	4	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.5	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t_{EN_CMP}	Comparator enable time	CBON = 0 → 1, CBPWRMD = 00 or 01			1	2	µs
		CBON = 0 → 1, CBPWRMD = 10				100	
t_{EN_REF}	Resistor reference enable time	CBON = 0 → 1			1.0	1.5	µs
TC_{REF}	Temperature coefficient reference					50	ppm/ °C
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

8.47 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_J	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DVCC during program			3	5	mA
I_{ERASE}	Average supply current from DVCC during erase			6	15	mA
I_{MERASE}, I_{BANK}	Average supply current from DVCC during mass erase or bank erase			6	15	mA
t_{CPT}	Cumulative program time(1)				16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	25°C	100			years
t_{Word}	Word or byte program time(2)		64		85	µs
$t_{Block, 0}$	Block program time for first byte or word(2)		49		65	µs
$t_{Block, 1 – (N – 1)}$	Block program time for each additional byte or word, except for last byte or word(2)		37		49	µs
$t_{Block, N}$	Block program time for last byte or word(2)		55		73	µs
t_{Erase}	Erase time for segment, mass erase, and bank erase when available(2)		23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write mode and block write mode.
(2) These values are hardwired into the state machine of the flash controller.

8.48 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	V_{IO}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	1.62 V to 1.98 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	1.62 V to 1.98 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)		1.62 V to 1.98 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time	2.2 V, 3 V	1.62 V to 1.98 V	15		100	µs
f_{TCK}	TCK input frequency for 4-wire JTAG(2)	2.2 V	1.62 V to 1.98 V	0		5	MHz
		3 V	1.62 V to 1.98 V	0		10	
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	1.62 V to 1.98 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

8.49 DVIO BSL Entry

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-18)

PARAMETER		V_{CC}	V_{IO}	MIN	MAX	UNIT
$t_{SU, BSLEN}$	Setup time, BSLEN to $\overline{RST}$/NMI(1)	2.2 V, 3 V	1.62 V to 1.98 V	100		ns
$t_{HO, BSLEN}$	Hold time, BSLEN to $\overline{RST}$/NMI(2)	2.2 V, 3 V	1.62 V to 1.98 V	350		µs

(1) AVCC, DVCC, DVIO stable and within specification.
(2) BSLEN must remain logic high long enough for the boot code to detect its level and enter the BSL sequence. After the minimum hold time is achieved, BSLEN is a don't care.

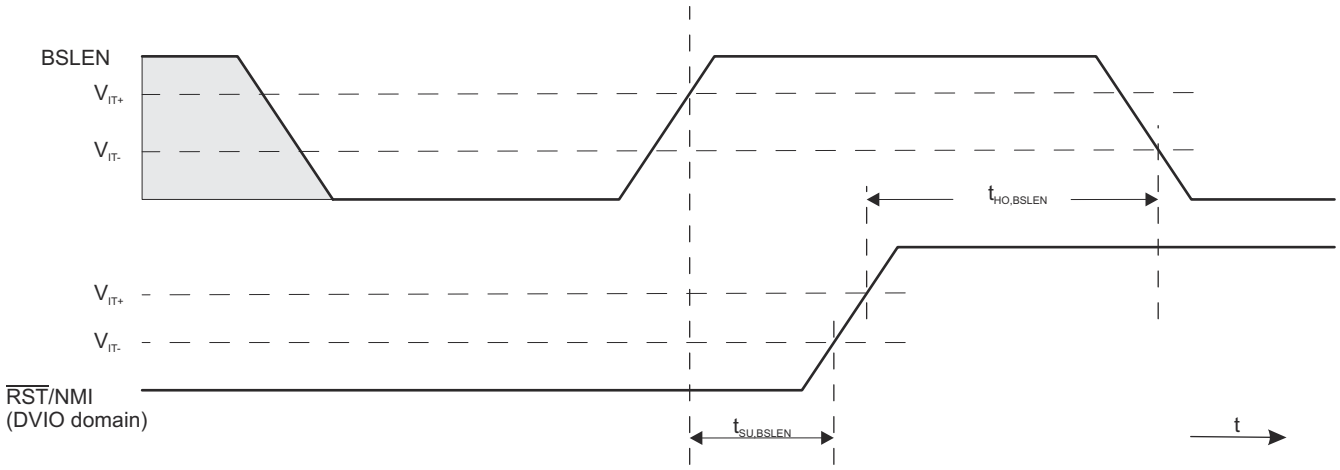


图 8-18. DVIO BSL Entry Timing

9 Detailed Description

9.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see 图 9-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

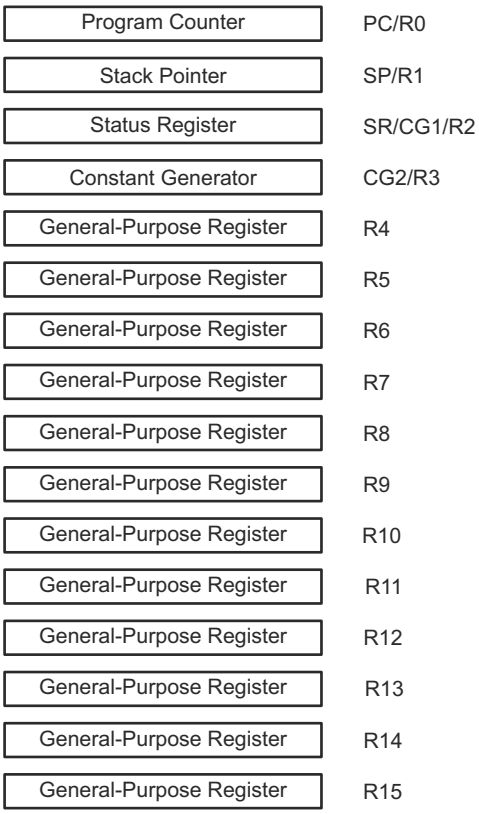


图 9-1. Integrated CPU Registers

9.2 Operating Modes

These MCUs have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following seven operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up input from $\overline{\text{RST}}$/NMI, P1, or P2

9.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see 表 9-1). The vector contains the 16-bit address of the interrupt-handler instruction sequence.

表 9-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation PMM password violation	WDTIFG, KEYV (SYSRSTIV)(1) (3)	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) (1) (3)	(Non)maskable	0FFFAh	61
COMP_B	Comparator B interrupt flags (CBIV)(1) (2)	Maskable	0FFF8h	60
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (2)	Maskable	0FFF6h	59
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (2)	Maskable	0FFF4h	58
Watchdog timer interval timer mode	WDTIFG	Maskable	0FFF2h	57
USCI_A1 receive or transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (2)	Maskable	0FFF0h	56
USCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (2)	Maskable	0FFEEh	55
ADC10_A	ADC10IFG0(1) (2) (5)	Maskable	0FFECh	54
USCI_A2 receive or transmit	UCA2RXIFG, UCA2TXIFG (UCA2IV)(1) (2)	Maskable	0FFEAh	53
USCI_B2 receive or transmit	UCB2RXIFG, UCB2TXIFG (UCB2IV)(1) (2)	Maskable	0FFE8h	52
TA0	TA0CCR0 CCIFG0(2)	Maskable	0FFE6h	51
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (2)	Maskable	0FFE4h	50
Reserved	Reserved(4)	Maskable	0FFE2h	49
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1) (2)	Maskable	0FFE0h	48
USCI_A3 receive or transmit	UCA3RXIFG, UCA3TXIFG (UCA3IV)(1) (2)	Maskable	0FFDEh	47
USCI_B3 receive or transmit	UCB3RXIFG, UCB3TXIFG (UCB3IV)(1) (2)	Maskable	0FFDCh	46
TB0	TB0CCR0 CCIFG0 (2)	Maskable	0FFDAh	45
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV)(1) (2)	Maskable	0FFD8h	44
TA1	TA1CCR0 CCIFG0(2)	Maskable	0FFD6h	43
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (2)	Maskable	0FFD4h	42
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV)(1) (2)	Maskable	0FFD2h	41
TA2	TA2CCR0 CCIFG0(2)	Maskable	0FFD0h	40
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1) (2)	Maskable	0FFCEh	39
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV)(1) (2)	Maskable	0FFCCh	38
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1) (2)	Maskable	0FFCAh	37
I/O Port P6	P6IFG.0 to P6IFG.7 (P6IV)(1) (2)	Maskable	0FFC8h	36

表 9-1. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved	Reserved(4)		0FFC6h	35
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) Interrupt flags are in the module.
(3) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.
(5) Only on devices with ADC, otherwise reserved

9.4 Memory Organization

表 9-2 summarizes the memory map of the microcontrollers.

表 9-2. Memory Organization

		MSP430F5259, MSP430F5258, MSP430F5255, MSP430F5254	MSP430F5257, MSP430F5256, MSP430F5253, MSP430F5252
Memory (flash)	Total Size	128KB	128KB
Main: interrupt vector		00FFFFh to 00FF80h	00FFFFh to 00FF80h
Main: code memory	Bank D	32KB 002A3FFh to 0022400h	32KB 002A3FFh to 0022400h
	Bank C	32KB 00223FFh to 001A400h	32KB 00223FFh to 001A400h
	Bank B	32KB 001A3FFh to 0012400h	32KB 001A3FFh to 0012400h
	Bank A	32KB 00123FFh to 00A400h	32KB 00123FFh to 00A400h
RAM	Sector 7	4KB 00A3FFh to 009400h	N/A(1)
	Sector 6	4KB 0093FFh to 008400h	N/A
	Sector 5	4KB 0083FFh to 007400h	N/A
	Sector 4	4KB 0073FFh to 006400h	N/A
	Sector 3	4KB 0063FFh to 005400h	4KB 0063FFh to 005400h
	Sector 2	4KB 0053FFh to 004400h	4KB 0053FFh to 004400h
	Sector 1	4KB 0043FFh to 003400h	4KB 0043FFh to 003400h
	Sector 0	4KB 0033FFh to 002400h	4KB 0033FFh to 002400h
TI factory memory (ROM)	A	128 bytes 001BFFh to 001B80h	128 bytes 001BFFh to 001B80h
	B	128 bytes 001B7Fh to 001B00h	128 bytes 001B7Fh to 001B00h
	C	128 bytes 001AFFh to 001A80h	128 bytes 001AFFh to 001A80h
	D	128 bytes 001A7Fh to 001A00h	128 bytes 001A7Fh to 001A00h

表 9-2. Memory Organization (continued)

		MSP430F5259, MSP430F5258, MSP430F5255, MSP430F5254	MSP430F5257, MSP430F5256, MSP430F5253, MSP430F5252
Information memory (flash)	Info A	128 bytes 0019FFh to 001980h	128 bytes 0019FFh to 001980h
	Info B	128 bytes 00197Fh to 001900h	128 bytes 00197Fh to 001900h
	Info C	128 bytes 0018FFh to 001880h	128 bytes 0018FFh to 001880h
	Info D	128 bytes 00187Fh to 001800h	128 bytes 00187Fh to 001800h
Bootloader (BSL) memory (flash)	BSL 3	512 bytes 0017FFh to 001600h	512 bytes 0017FFh to 001600h
	BSL 2	512 bytes 0015FFh to 001400h	512 bytes 0015FFh to 001400h
	BSL 1	512 bytes 0013FFh to 001200h	512 bytes 0013FFh to 001200h
	BSL 0	512 bytes 0011FFh to 001000h	512 bytes 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 0h	4KB 000FFFh to 0h

(1) N/A = Not available

9.5 Bootloader (BSL)

Note

Devices from TI come factory programmed with either an I²C-based BSL or a timer-based UART BSL. See 表 6-1 to determine which BSL type is implemented.

9.5.1 Bootloader – I²C

The I²C BSL enables users to program the flash memory or RAM using a I²C serial interface. Access to the device memory through the BSL is protected by an user-defined password.

When using the BSL, it requires a specific entry sequence on the $\overline{\text{RST}}$/NMI and BSLEN pins. 表 9-3 lists the required pins and their functions. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the BSL and its implementation, see the *MSP430 Flash Devices Bootloader (BSL) User's Guide*. BSL firmware images are available for download in the Custom BSL430 package.

Note

To invoke the BSL from the DVIO domain, the $\overline{\text{RST}}$/NMI pin and BSLEN pins must be used for the entry sequence. It is critical not to confuse the $\overline{\text{RST}}$/NMI pin with the $\overline{\text{RSTDVCC}}$/SBWTDIO pin. In many other MSP430 devices, SBWTDIO is shared with the $\overline{\text{RST}}$/NMI pin, and $\overline{\text{RSTDVCC}}$ does not exist. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

表 9-3. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI	External reset
BSLEN	Enable BSL
P4.1/PM_UCB1SDA	I^2C data
P4.2/ PM_UCB1SCL	I^2C clock
DVCC, AVCC	Device power supply
DVIO	I/O power supply
DVSS	Ground supply

9.5.2 Bootloader – UART

The UART BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. Because the F525x have split I/O power domains, it is possible to interface with the BSL from either the DVCC or DVIO supply domains. This is useful when the MSP430 is interfacing to a host on the DVIO supply domain. The BSL interface on the DVIO supply domain (see 表 9-5) uses the USCI_A0 module configured as a UART. The BSL interface on the DVCC supply domain (see 表 9-4) uses a timer-based UART.

For applications that have BSL communication based on the DVCC supply domain, entry to the BSL requires a specific sequence on the $\overline{\text{RSTDVCC}}$/SBWTDIO and TEST/SBWTCK pins.

Note

Devices that are factory programmed with an UART BSL use the DVCC power supply domain pin configuration per default (see 表 9-4).

Note

To invoke the BSL from the DVCC domain, the $\overline{\text{RSTDVCC}}$/SBWTDIO pin and TEST/SBWTCK pin must be used for the entry sequence. It is critical not to confuse the $\overline{\text{RST}}$/NMI pin with the $\overline{\text{RSTDVCC}}$/SBWTDIO pin. In many other MSP430 devices, SBWTDIO is shared with the $\overline{\text{RST}}$/NMI pin, and $\overline{\text{RSTDVCC}}$ does not exist. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

表 9-4. DVCC BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RSTDVCC}}$/SBWTDIO	External reset
TEST/SBWTCK	Enable BSL
P6.1	Data transmit
P6.2	Data receive
DVCC, AVCC	Device power supply
DVIO	I/O power supply
DVSS	Ground supply

When using the DVIO supply domain for the BSL, entry to the BSL requires a specific sequence on the $\overline{\text{RST}}$/NMI and BSLEN pins. 表 9-5 lists the required pins and their functions. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the BSL and its implementation, see the *MSP430 Flash Device Bootloader (BSL) User's Guide*. BSL firmware images are available for download in the Custom BSL430 package. The BSL on the DVIO supply domain uses the USCI_A0 module configured as a UART.

Note

To invoke the BSL from the DVIO domain, the $\overline{\text{RST}}$/NMI pin and the BSLEN pin must be used for the entry sequence (see 节 8.49). It is critical not to confuse the $\overline{\text{RST}}$/NMI pin with the $\overline{\text{RSTDVCC}}$/SBWTDIO pin. In many other MSP430 devices, SBWTDIO is shared with the $\overline{\text{RST}}$/NMI pin, and $\overline{\text{RSTDVCC}}$ does not exist. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

表 9-5. DVIO BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI	External reset
BSLEN	Enable BSL
P3.3	Data transmit
P3.4	Data receive
DVCC, AVCC	Device power supply
DVIO	I/O power supply
DVSS	Ground supply

9.6 JTAG Operation

9.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RSTDVCC}}$/SBWTDIO is required to interface with MSP430 development tools and device programmers. 表 9-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

Note

All JTAG I/O pins are supplied by DVCC.

Note

Traditionally, on other MSP430 devices, the $\overline{\text{RST}}$/NMI pin is used for SBWTDIO, so care must be taken not to mistakenly use the incorrect pin. On the F525x series of devices, it is required to use $\overline{\text{RSTDVCC}}$ for SBWTDIO as shown in 表 9-6. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

表 9-6. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RSTDVCC}}$/SBWTDIO	IN	External reset
DVCC, AVCC		Device power supply
DVIO		I/O power supply
DVSS		Ground supply

9.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 9-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

Note

All SBW I/O pins are supplied by DVCC.

Note

Traditionally, on other MSP430 devices, the $\overline{\text{RST}}$/NMI pin is used for SBWTDIO, so care must be taken not to mistakenly use the incorrect pin. On the F525x series of devices, it is required to use $\overline{\text{RSTDVCC}}$ for SBWTDIO as shown in 表 9-7. Additional information can be found in *Designing With MSP430F522x and MSP430F521x Devices*.

表 9-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RSTDVCC}}$/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
DVCC, AVCC		Device power supply
DVIO		I/O power supply
DVSS		Ground supply

9.7 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

9.8 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to reduce leakage; however, all data are lost during power down.

Features of the RAM include:

- RAM memory has n sectors. The sizes of the sectors can be found in 节 9.4, *Memory Organization*.
- Each sector 0 to n can be complete disabled; however, all data in a sector are lost when it is disabled.
- Each sector 0 to n automatically enters low-power retention mode when possible.

9.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

9.9.1 Digital I/O

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wake-up input capability is available for all bits of ports P1, P2.
- All bits of port P6 support edge-selectable interrupt input.
- All instructions support read and write access to port-control registers.
- Ports can be accessed byte-wise or word-wise in pairs.

9.9.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4 (see 表 9-8).

表 9-8. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOUT0	–	COMP_B output
	PM_TB0CLK	TB0 clock input	–
2	PM_ADC10CLK	–	ADC10CLK
	PM_DMAE0	DMAE0 input	–
3	PM_SVMOUT	–	SVM output
	PM_TB0OUTH	TB0 high-impedance input TB0OUTH	–
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (direction controlled by USCI – input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (direction controlled by USCI – output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I^2C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I^2C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	COMP_B output
18	PM_MCLK	None	MCLK

表 9-8. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
19	PM_RTCCLK	None	RTCCLK output
20	PM_UCA0RXD	USCI_A0 UART RXD (direction controlled by USCI – input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
21	PM_UCA0TXD	USCI_A0 UART TXD (direction controlled by USCI – output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
22	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI)	
23	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I^2C clock (open drain and direction controlled by USCI)	
24	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I^2C data (open drain and direction controlled by USCI)	
25	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI)	
26	PM_UCA3RXD	USCI_A3 UART RXD (direction controlled by USCI – input)	
	PM_UCA3SOMI	USCI_A3 SPI slave out master in (direction controlled by USCI)	
27	PM_UCA3TXD	USCI_A3 UART TXD (direction controlled by USCI – output)	
	PM_UCA3SIMO	USCI_A3 SPI slave in master out (direction controlled by USCI)	
28	PM_UCB3SIMO	USCI_B3 SPI slave in master out (direction controlled by USCI)	
	PM_UCB3SDA	USCI_B3 I^2C data (open drain and direction controlled by USCI)	
29	PM_UCB3SOMI	USCI_B3 SPI slave out master in (direction controlled by USCI)	
	PM_UCB3SCL	USCI_B3 I^2C clock (open drain and direction controlled by USCI)	
30	Reserved	Reserved	
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals	

(1) The value of the PM_ANALOG mnemonic is 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

表 9-9 lists the default settings for all pins that support port mapping.

表 9-9. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I^2C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I^2C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI – output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI – input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_UCA3TXD/PM_UCA3SIMO	USCI_A3 UART TXD (Direction controlled by USCI – output) USCI_A3 SPI slave in master out (direction controlled by USCI)	
P4.7/P4MAP7	PM_UCA3RXD/PM_UCA3SOMI	USCI_A3 UART RXD (Direction controlled by USCI – input) USCI_A3 SPI slave out master in (direction controlled by USCI)	

9.9.3 Oscillator and System Clock

The clock system is supported by the Unified Clock System (UCS) module, which includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3.5 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

9.9.4 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

9.9.5 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

9.9.6 Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer or counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

9.9.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

9.9.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These functions include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader (BSL) entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism using JTAG that is called a JTAG mailbox and that can be used in the application. 表 9-10 lists the SYS module interrupt vector registers.

表 9-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT time-out (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

9.9.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral (see 表 9-11).

表 9-11. DMA Trigger Assignments

TRIGGER(1)	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	UCA2RXIFG	UCA2RXIFG	UCA2RXIFG
10	UCA2TXIFG	UCA2TXIFG	UCA2TXIFG
11	UCB2RXIFG	UCB2RXIFG	UCB2RXIFG
12	UCB2TXIFG	UCB2TXIFG	UCB2TXIFG
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC10IFG0(2)	ADC10IFG0(2)	ADC10IFG0(2)
25	UCA3RXIFG	UCA3RXIFG	UCA3RXIFG
26	UCA3TXIFG	UCA3TXIFG	UCA3TXIFG
27	UCB3RXIFG	UCB3RXIFG	UCB3RXIFG
28	UCB3TXIFG	UCB3TXIFG	UCB3TXIFG
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no trigger is generated.
(2) Only on devices with ADC; reserved on devices without ADC

9.9.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I^2C.

The MSP430F525x include four complete USCI modules (n = 0, 1, 2, 3).

9.9.11 TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 supports multiple captures or compares, PWM outputs, and interval timing (see 表 9-12). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 9-12. TA0 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
RGC, ZXH, ZQE						RGC, ZXH, ZQE
18, H2 - P1.0	TA0CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
18, H2 - P1.0	TA0CLK	$\overline{\text{TACLK}}$				
19, H3 - P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	19, H3 - P1.1
	DVSS	CCI0B				
	DVSS	GND				
	DVCC	V_{CC}				
20, J3 - P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	20, J3 - P1.2
	CBOUT (internal)	CCI1B				ADC10 (internal) ADC10SHSx = {1}
	DVSS	GND				
	DVCC	V_{CC}				
21, G4 - P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	21, G4 - P1.3
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				
22, H4 - P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	22, H4 - P1.4
	DVSS	CCI3B				
	DVSS	GND				
	DVCC	V_{CC}				
23, J4 - P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	23, J4 - P1.5
	DVSS	CCI4B				
	DVSS	GND				
	DVCC	V_{CC}				

9.9.12 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 supports multiple captures or compares, PWM outputs, and interval timing (see 表 9-13). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 9-13. TA1 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
RGC, ZQE						RGC, ZQE
24, G5 - P1.6	TA1CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
24, G5 - P1.6	TA1CLK	$\overline{\text{TACLK}}$				
25, H5 - P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	25, H5 - P1.7
	DVSS	CCI0B				
	DVSS	GND				
	DVCC	V_{CC}				
26, J5 - P2.0	TA1.1	CCI1A	CCR1	TA1	TA1.1	26, J5 - P2.0
	CBOUT (internal)	CCI1B				
	DVSS	GND				
	DVCC	V_{CC}				
27, G6 - P2.1	TA1.2	CCI2A	CCR2	TA2	TA1.2	27, G6 - P2.1
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				

9.9.13 TA2

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 supports multiple captures or compares, PWM outputs, and interval timing (see 表 9-14). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 9-14. TA2 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
RGC, ZXH, ZQE						RGC, ZXH, ZQE
1, A1 - P6.0	TA2CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
1, A1 - P6.0	TA2CLK	$\overline{\text{TACLK}}$				
2, B2 - P6.1	TA2.0	CCI0A	CCR0	TA0	TA2.0	2, B2 - P6.1
	DVSS	CCI0B				
	DVSS	GND				
	DVCC	V_{CC}				
3, B1 - P6.2	TA2.1	CCI1A	CCR1	TA1	TA2.1	3, B1 - P6.2
	CBOUT (internal)	CCI1B				
	DVSS	GND				
	DVCC	V_{CC}				
4, C2 - P6.3	TA2.2	CCI2A	CCR2	TA2	TA2.2	4, C2 - P6.3
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				

9.9.14 TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 supports multiple captures or compares, PWM outputs, and interval timing (see 表 9-15). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 9-15. TB0 Signal Connections

INPUT PIN NUMBER RGC, ZXH, ZQE	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER RGC, ZXH, ZQE
(1)	TB0CLK	TBCLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
(1)	TB0CLK	$\overline{\text{TBCLK}}$				
(1)	TB0.0	CCI0A	CCR0	TB0	TB0.0	(1)
(1)	TB0.0	CCI0B				ADC10 (internal) ADC10SHSx = {2}
	DVSS	GND				
	DVCC	V_{CC}				
(1)	TB0.1	CCI1A	CCR1	TB1	TB0.1	(1)
	CBOUT (internal)	CCI1B				ADC10 (internal) ADC10SHSx = {3}
	DVSS	GND				
	DVCC	V_{CC}				
(1)	TB0.2	CCI2A	CCR2	TB2	TB0.2	(1)
(1)	TB0.2	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				
(1)	TB0.3	CCI3A	CCR3	TB3	TB0.3	(1)
(1)	TB0.3	CCI3B				
	DVSS	GND				
	DVCC	V_{CC}				
(1)	TB0.4	CCI4A	CCR4	TB4	TB0.4	(1)
(1)	TB0.4	CCI4B				
	DVSS	GND				
	DVCC	V_{CC}				
(1)	TB0.5	CCI5A	CCR5	TB5	TB0.5	(1)
(1)	TB0.5	CCI5B				
	DVSS	GND				
	DVCC	V_{CC}				
(1)	TB0.6	CCI6A	CCR6	TB6	TB0.6	(1)
	ACLK (internal)	CCI6B				
	DVSS	GND				
	DVCC	V_{CC}				

(1) Timer functions can be selected by the port mapping controller.

9.9.15 Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

9.9.16 ADC10_A

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

9.9.17 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

9.9.18 Reference (REF) Module Voltage Reference

The REF module generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

9.9.19 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

9.9.20 Peripheral File Map

表 9-16 lists the base address for the registers of each peripheral module.

表 9-16. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see 表 9-17)	0100h	000h to 01Fh
PMM (see 表 9-18)	0120h	000h to 010h
Flash Control (see 表 9-19)	0140h	000h to 00Fh
CRC16 (see 表 9-20)	0150h	000h to 007h
RAM Control (see 表 9-21)	0158h	000h to 001h
Watchdog (see 表 9-22)	015Ch	000h to 001h
UCS (see 表 9-23)	0160h	000h to 01Fh
SYS (see 表 9-24)	0180h	000h to 01Fh
Shared Reference (see 表 9-25)	01B0h	000h to 001h
Port Mapping Control (see 表 9-26)	01C0h	000h to 002h
Port Mapping Port P4 (see 表 9-26)	01E0h	000h to 007h
Port P1, P2 (see 表 9-27)	0200h	000h to 01Fh
Port P3, P4 (see 表 9-28)	0220h	000h to 00Bh
Port P5, P6 (see 表 9-29)	0240h	000h to 01Fh
Port P7 (see 表 9-30)	0260h	000h to 00Bh
Port PJ (see 表 9-31)	0320h	000h to 01Fh
TA0 (see 表 9-32)	0340h	000h to 02Eh
TA1 (see 表 9-33)	0380h	000h to 02Eh
TB0 (see 表 9-34)	03C0h	000h to 02Eh
TA2 (see 表 9-35)	0400h	000h to 02Eh
Real-Time Clock (RTC_A) (see 表 9-36)	04A0h	000h to 01Bh
32-Bit Hardware Multiplier (see 表 9-37)	04C0h	000h to 02Fh
DMA General Control (see 表 9-38)	0500h	000h to 00Fh
DMA Channel 0 (see 表 9-38)	0510h	000h to 00Ah
DMA Channel 1 (see 表 9-38)	0520h	000h to 00Ah
DMA Channel 2 (see 表 9-38)	0530h	000h to 00Ah
USCI_A0 (see 表 9-39)	05C0h	000h to 01Fh
USCI_B0 (see 表 9-40)	05E0h	000h to 01Fh
USCI_A1 (see 表 9-41)	0600h	000h to 01Fh
USCI_B1 (see 表 9-42)	0620h	000h to 01Fh
USCI_A2 (see 表 9-39)	0640h	000h to 01Fh
USCI_B2 (see 表 9-40)	0660h	000h to 01Fh
USCI_A3 (see 表 9-41)	0680h	000h to 01Fh
USCI_B3 (see 表 9-42)	06A0h	000h to 01Fh
ADC10_A (see 表 9-47)	0740h	000h to 01Fh
Comparator_B (see 表 9-48)	08C0h	000h to 00Fh

表 9-17. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

表 9-18. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

表 9-19. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

表 9-20. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

表 9-21. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

表 9-22. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

表 9-23. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h
UCS control 9	UCSCTL9	12h

表 9-24. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

表 9-25. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

表 9-26. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key/ID	PMAPKEYID	00h
Port mapping control	PMAPCTL	02h
Port P4.0 mapping	P4MAP0	00h
Port P4.1 mapping	P4MAP1	01h
Port P4.2 mapping	P4MAP2	02h
Port P4.3 mapping	P4MAP3	03h
Port P4.4 mapping	P4MAP4	04h
Port P4.5 mapping	P4MAP5	05h
Port P4.6 mapping	P4MAP6	06h
Port P4.7 mapping	P4MAP7	07h

表 9-27. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

表 9-28. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

表 9-29. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh
Port P6 interrupt vector word	P6IV	1Eh
Port P6 interrupt edge select	P6IES	19h
Port P6 interrupt enable	P6IE	1Bh
Port P6 interrupt flag	P6IFG	1Dh

表 9-30. Port P7 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 resistor enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah

表 9-31. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h

表 9-32. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

表 9-33. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

表 9-34. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

表 9-35. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

表 9-36. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter 1	RTCSEC/RTCNT1	10h
RTC minutes/counter 2	RTCMIN/RTCNT2	11h
RTC hours/counter 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

表 9-37. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

表 9-38. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

表 9-39. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

表 9-40. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

表 9-41. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

表 9-42. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

表 9-43. USCI_A2 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA2CTL1	00h
USCI control 0	UCA2CTL0	01h
USCI baud rate 0	UCA2BR0	06h
USCI baud rate 1	UCA2BR1	07h
USCI modulation control	UCA2MCTL	08h
USCI status	UCA2STAT	0Ah
USCI receive buffer	UCA2RXBUF	0Ch
USCI transmit buffer	UCA2TXBUF	0Eh
USCI LIN control	UCA2ABCTL	10h
USCI IrDA transmit control	UCA2IRTCTL	12h
USCI IrDA receive control	UCA2IRRCTL	13h
USCI interrupt enable	UCA2IE	1Ch
USCI interrupt flags	UCA2IFG	1Dh
USCI interrupt vector word	UCA2IV	1Eh

表 9-44. USCI_B2 Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB2CTL1	00h
USCI synchronous control 0	UCB2CTL0	01h
USCI synchronous bit rate 0	UCB2BR0	06h
USCI synchronous bit rate 1	UCB2BR1	07h
USCI synchronous status	UCB2STAT	0Ah
USCI synchronous receive buffer	UCB2RXBUF	0Ch
USCI synchronous transmit buffer	UCB2TXBUF	0Eh
USCI I2C own address	UCB2I2COA	10h
USCI I2C slave address	UCB2I2CSA	12h
USCI interrupt enable	UCB2IE	1Ch
USCI interrupt flags	UCB2IFG	1Dh
USCI interrupt vector word	UCB2IV	1Eh

表 9-45. USCI_A3 Registers (Base Address: 0680h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA3CTL1	00h
USCI control 0	UCA3CTL0	01h
USCI baud rate 0	UCA3BR0	06h
USCI baud rate 1	UCA3BR1	07h
USCI modulation control	UCA3MCTL	08h
USCI status	UCA3STAT	0Ah
USCI receive buffer	UCA3RXBUF	0Ch
USCI transmit buffer	UCA3TXBUF	0Eh
USCI LIN control	UCA3ABCTL	10h
USCI IrDA transmit control	UCA3IRTCTL	12h
USCI IrDA receive control	UCA3IRRCTL	13h
USCI interrupt enable	UCA3IE	1Ch
USCI interrupt flags	UCA3IFG	1Dh

表 9-45. USCI_A3 Registers (Base Address: 0680h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI interrupt vector word	UCA3IV	1Eh

表 9-46. USCI_B3 Registers (Base Address: 06A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB3CTL1	00h
USCI synchronous control 0	UCB3CTL0	01h
USCI synchronous bit rate 0	UCB3BR0	06h
USCI synchronous bit rate 1	UCB3BR1	07h
USCI synchronous status	UCB3STAT	0Ah
USCI synchronous receive buffer	UCB3RXBUF	0Ch
USCI synchronous transmit buffer	UCB3TXBUF	0Eh
USCI I2C own address	UCB3I2COA	10h
USCI I2C slave address	UCB3I2CSA	12h
USCI interrupt enable	UCB3IE	1Ch
USCI interrupt flags	UCB3IFG	1Dh
USCI interrupt vector word	UCB3IV	1Eh

表 9-47. ADC10_A Registers (Base Address: 0740h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_A control 0	ADC10CTL0	00h
ADC10_A control 1	ADC10CTL1	02h
ADC10_A control 2	ADC10CTL2	04h
ADC10_A window comparator low threshold	ADC10LO	06h
ADC10_A window comparator high threshold	ADC10HI	08h
ADC10_A memory control 0	ADC10MCTL0	0Ah
ADC10_A conversion memory	ADC10MEM0	12h
ADC10_A interrupt enable	ADC10IE	1Ah
ADC10_A interrupt flags	ADC10IGH	1Ch
ADC10_A interrupt vector word	ADC10IV	1Eh

表 9-48. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control 0	CBCTL0	00h
Comp_B control 1	CBCTL1	02h
Comp_B control 2	CBCTL2	04h
Comp_B control 3	CBCTL3	06h
Comp_B interrupt	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

9.10 Input/Output Diagrams

9.10.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

图 9-2 shows the port diagram. 表 9-49 summarizes the selection of the pin function.

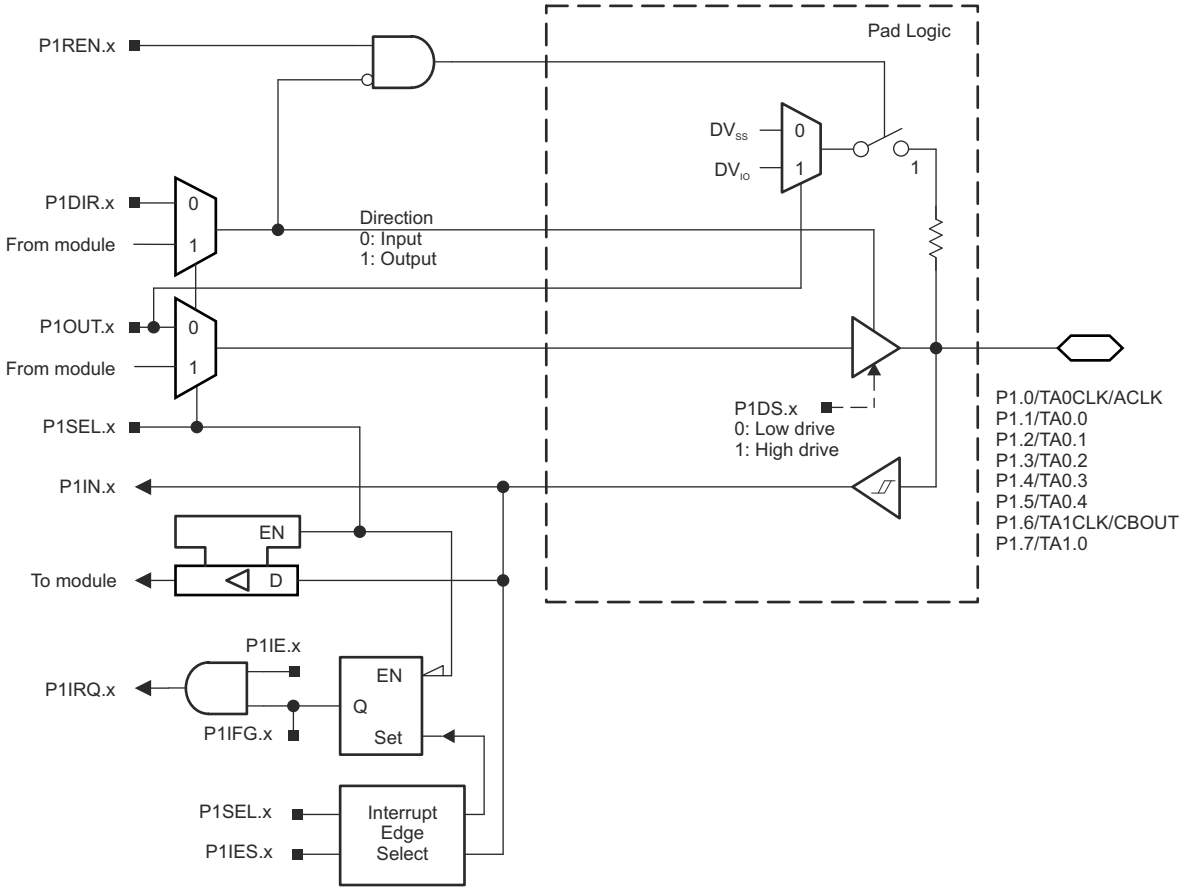


图 9-2. Port P1 (P1.0 to P1.7) Diagram

表 9-49. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

9.10.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

图 9-3 shows the port diagram. 表 9-50 summarizes the selection of the pin function.

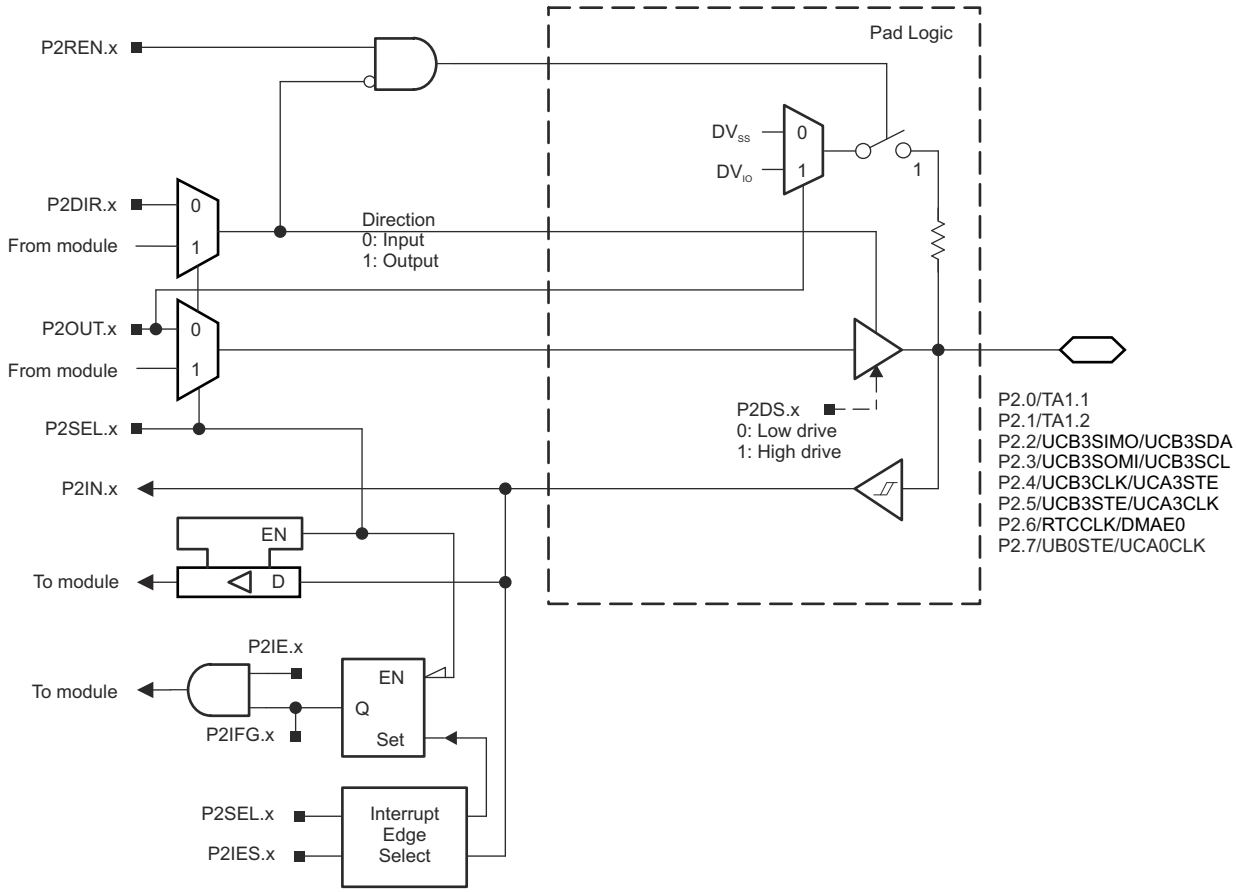


图 9-3. Port P2 (P2.0 to P2.7) Diagram

表 9-50. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P2DIR.x	P2SEL.x
P2.0/TA1.1	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.1/TA1.2	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.2/UCB3SIMO/UCB3SDA	2	P2.2 (I/O)	I: 0; O: 1	0
		UCB3SIMO/UCB3SDA	X	1
P2.3/UCB3SOMI/UCB3SCL	3	P2.3 (I/O)	I: 0; O: 1	0
		UCB3SOMI/UCB3SCL	X	1
P2.4/UCB3CLK/UCA3STE	4	P2.4 (I/O)	I: 0; O: 1	0
		UCB3CLK/UCA3STE(2) (3)	X	1
P2.5/UCB3STE/UCA3CLK	5	P2.5 (I/O)	I: 0; O: 1	0
		UCB3STE/UCA3CLK(2) (4)	X	1
P2.6/RTCCLK/DMAE0	6	P2.6 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		RTCCLK	1	1
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK(2) (5)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCB3CLK function takes precedence over UCA3STE function. If the pin is required as UCB3CLK input or output, USCI A3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) UCA3CLK function takes precedence over UCB3STE function. If the pin is required as UCA3CLK input or output, USCI_B3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

9.10.3 Port P3 (P3.0 to P3.4) Input/Output With Schmitt Trigger

图 9-4 shows the port diagram. 表 9-51 summarizes the selection of the pin function.

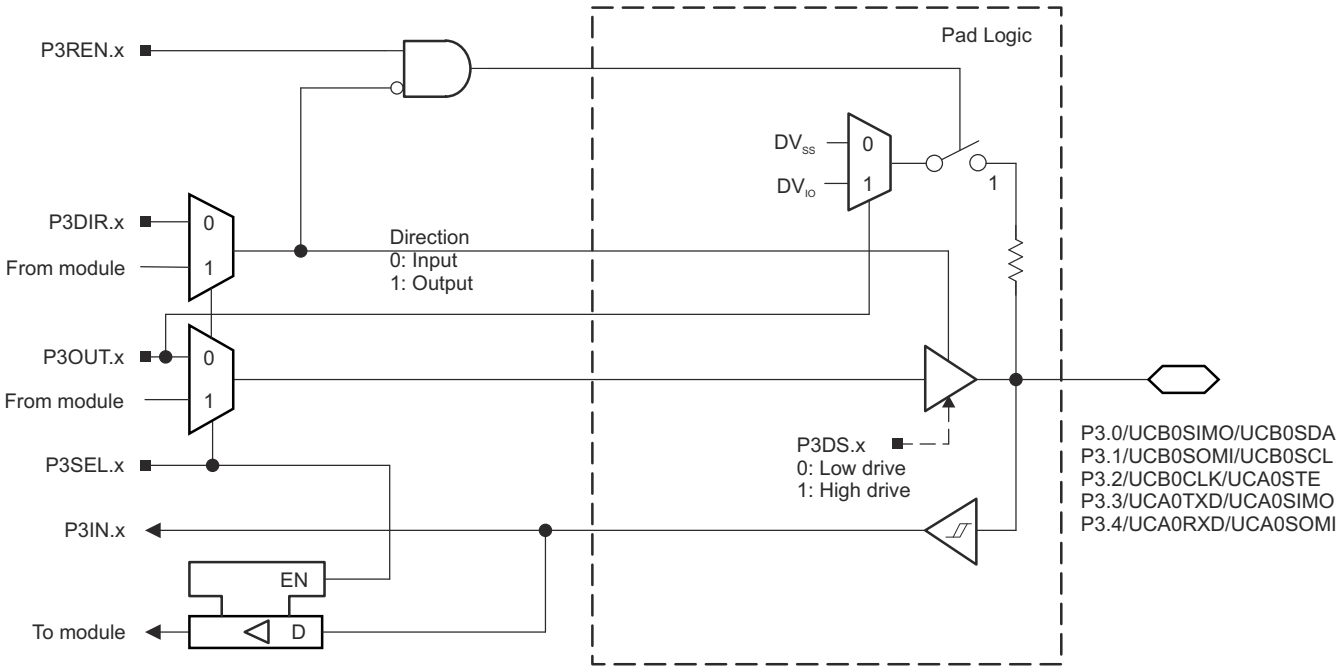


图 9-4. Port P3 (P3.0 to P3.4) Diagram

表 9-51. Port P3 (P3.0 to P3.4) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(2) (3)	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(2) (3)	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(2) (4)	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(2)	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(2)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

9.10.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

图 9-5 shows the port diagram. 表 9-52 summarizes the selection of the pin function.

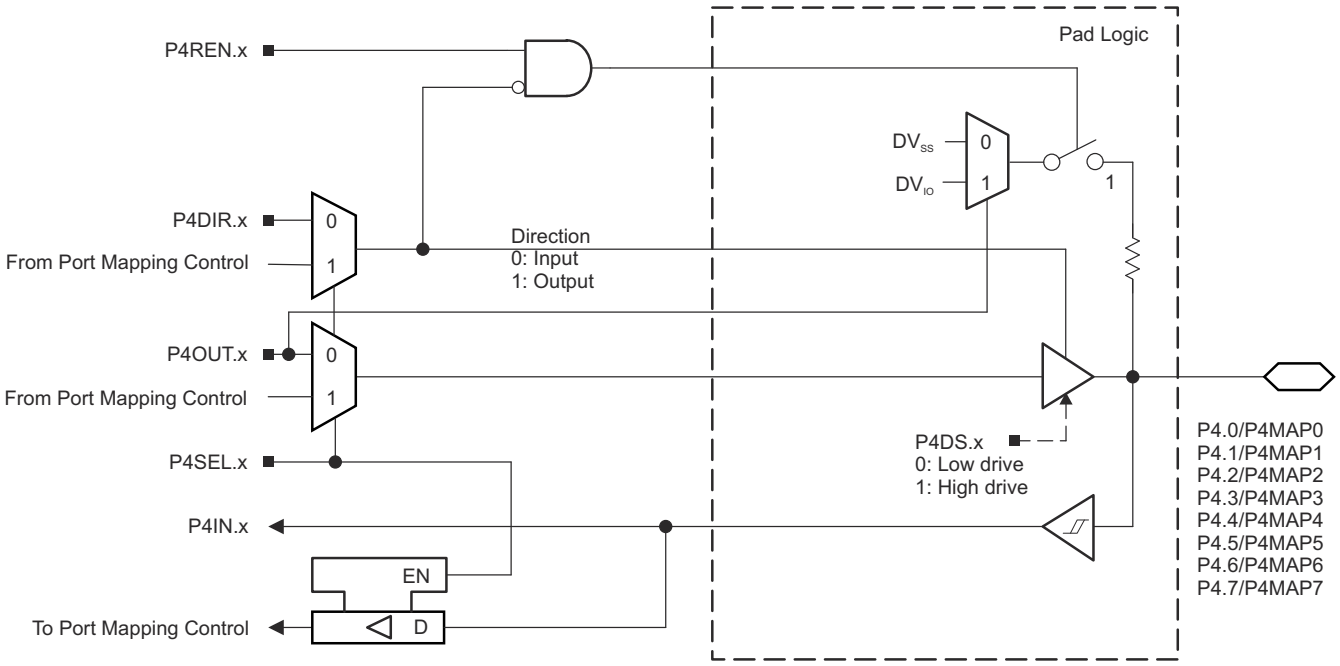


图 9-5. Port P4 (P4.0 to P4.7) Diagram

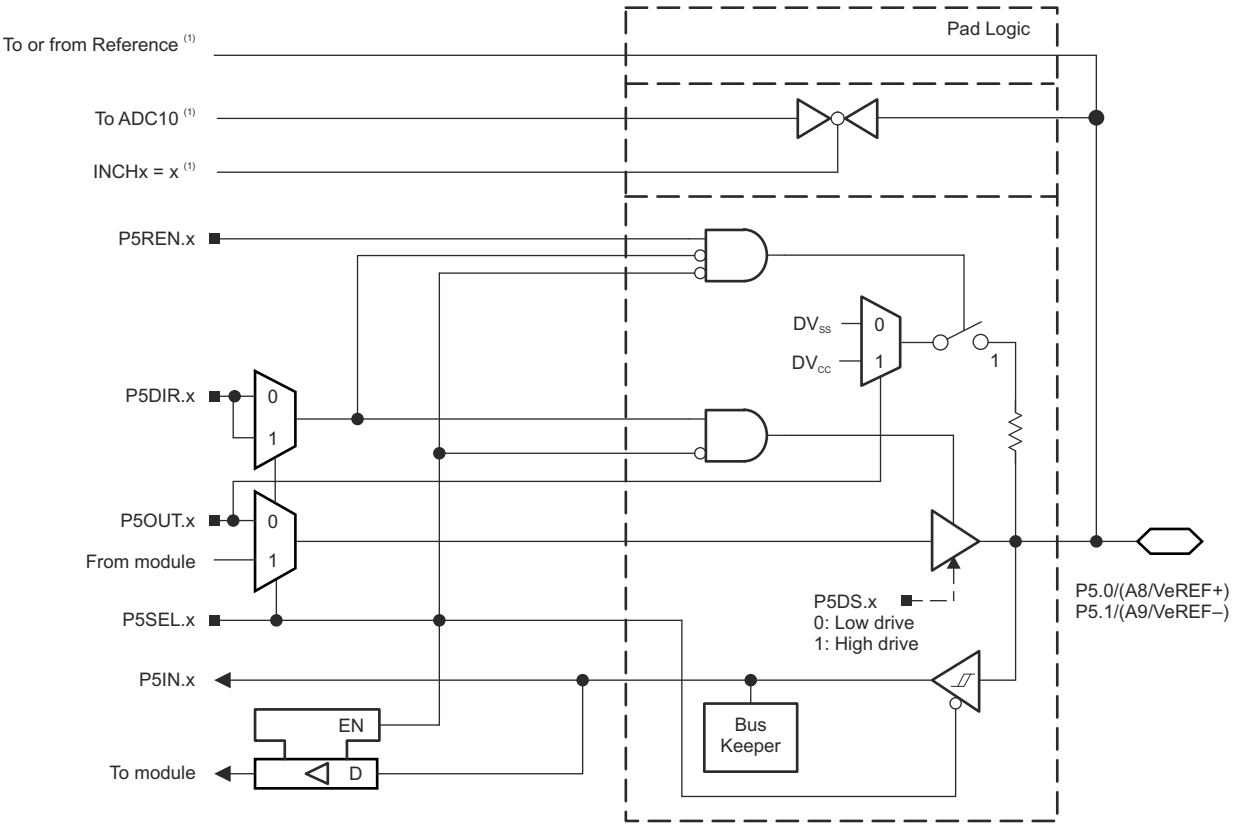
表 9-52. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x(2)	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	⩽ 30

(1) X= Don't care
(2) The direction of some mapped secondary functions are controlled directly by the module. See 表 9-8 for specific direction control information of mapped secondary functions.

9.10.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

图 9-6 shows the port diagram. 表 9-53 summarizes the selection of the pin function.



(1) not available for MSPF430F5258
MSPF430F5256
MSPF430F5254
MSPF430F5252

图 9-6. Port P5 (P5.0 and P5.1) Diagram

表 9-53. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL.x	REFOUT(3)
P5.0/A8/VeREF+	0	P5.0 (I/O)(2)	I: 0; O: 1	0	X
		A8/VeREF+(4)	X	1	0
P5.1/A9/VeREF –	1	P5.1 (I/O)(2)	I: 0; O: 1	0	X
		A9/VeREF – (5)	X	1	0

(1) X = Don't care
(2) Default condition
(3) REFOUT resides in the REF module.
(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC10_A. Channel A8, when selected with the INCHx bits, is connected to the VeREF+ pin.
(5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC10_A. Channel A9, when selected with the INCHx bits, is connected to the VeREF- pin.

9.10.6 Port P5 (P5.2 and P5.3) Input/Output With Schmitt Trigger

图 9-7 and 图 9-8 show the port diagrams. 表 9-54 summarizes the selection of the pin function.

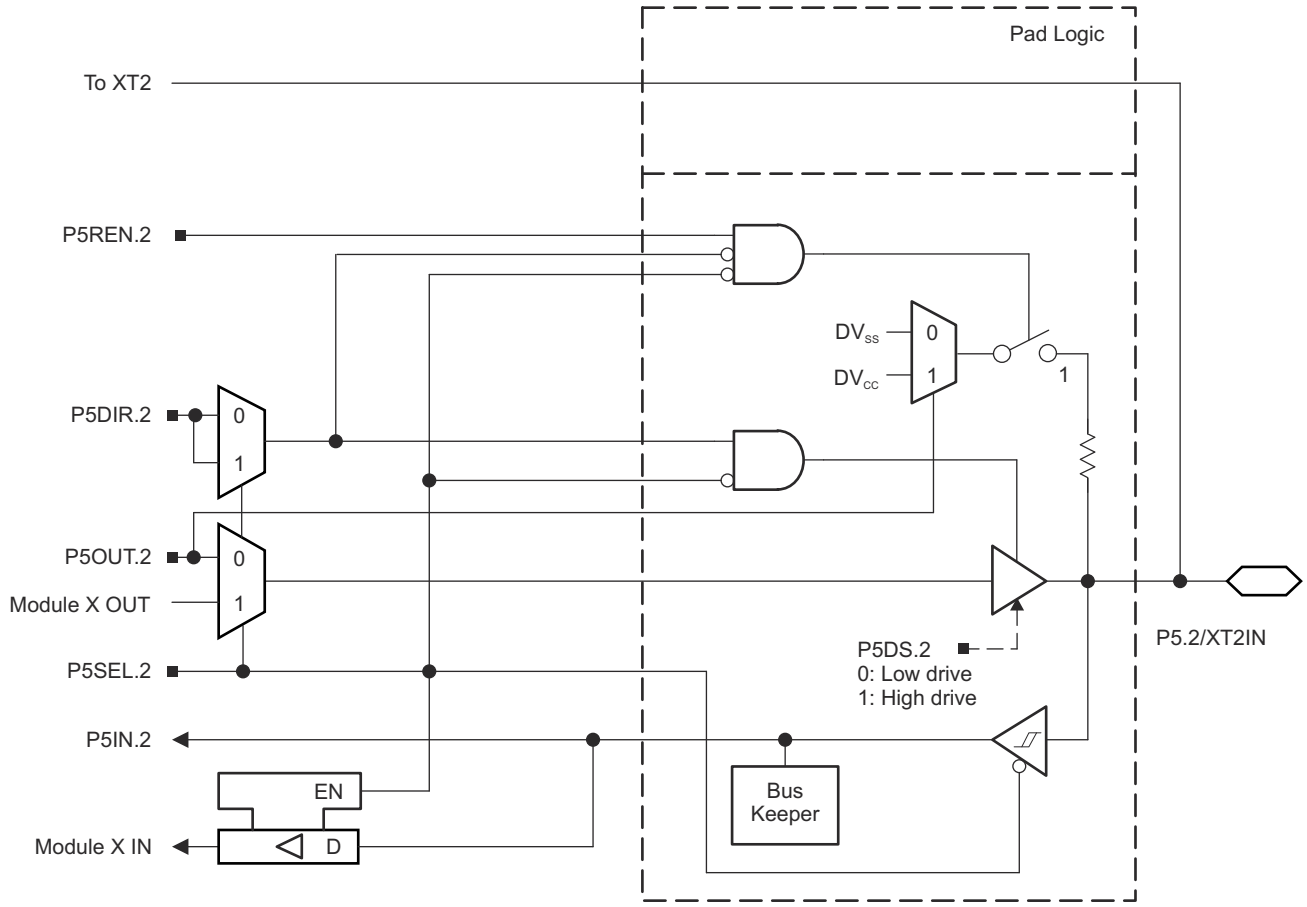


图 9-7. Port P5 (P5.2) Diagram

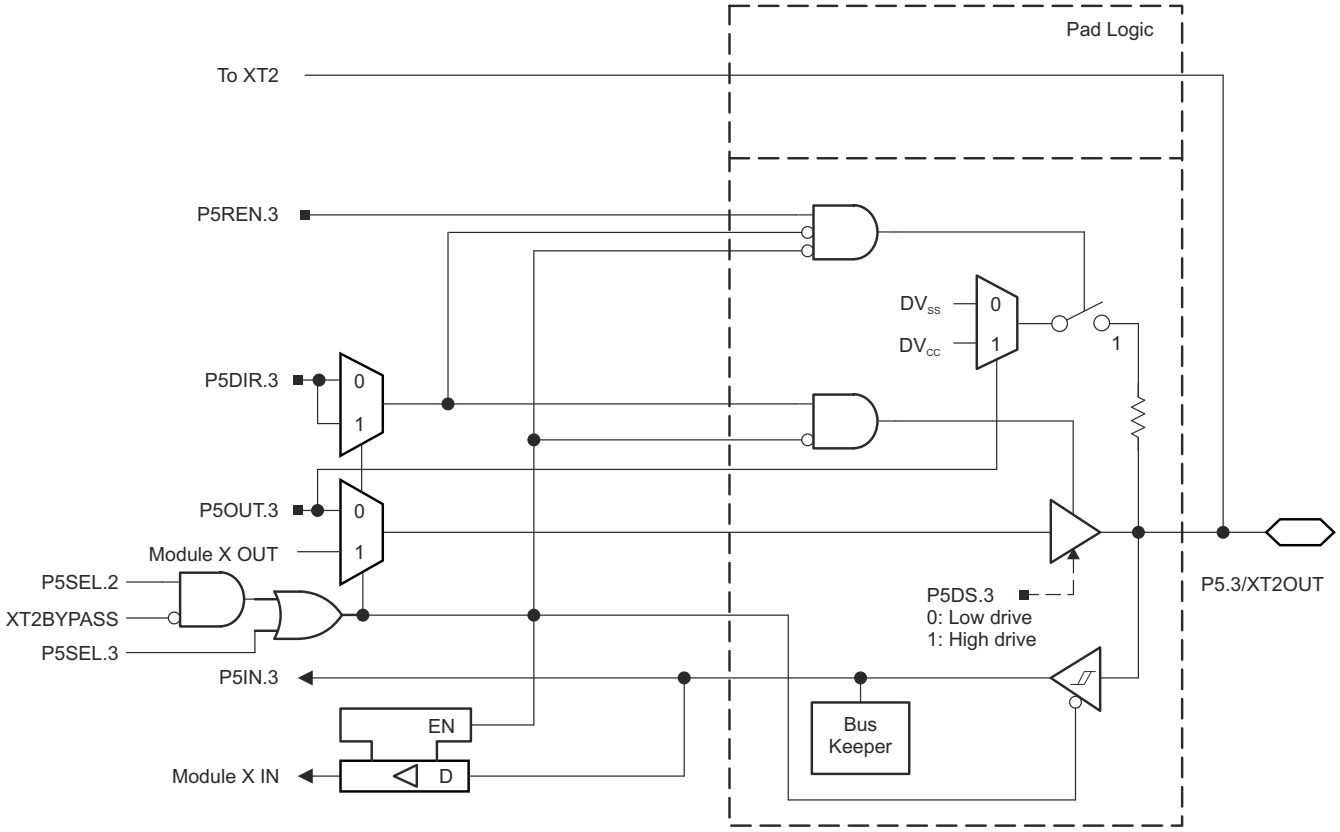


图 9-8. Port P5 (P5.3) Diagram

表 9-54. Port P5 (P5.2 and P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	0	X
		XT2OUT crystal mode(3)	X	1	X	0
		P5.3 (I/O)(3)	X	1	0	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

9.10.7 Port P5 (P5.4 and P5.5) Input/Output With Schmitt Trigger

图 9-9 and 图 9-10 show the port diagrams. 表 9-55 summarizes the selection of the pin function.

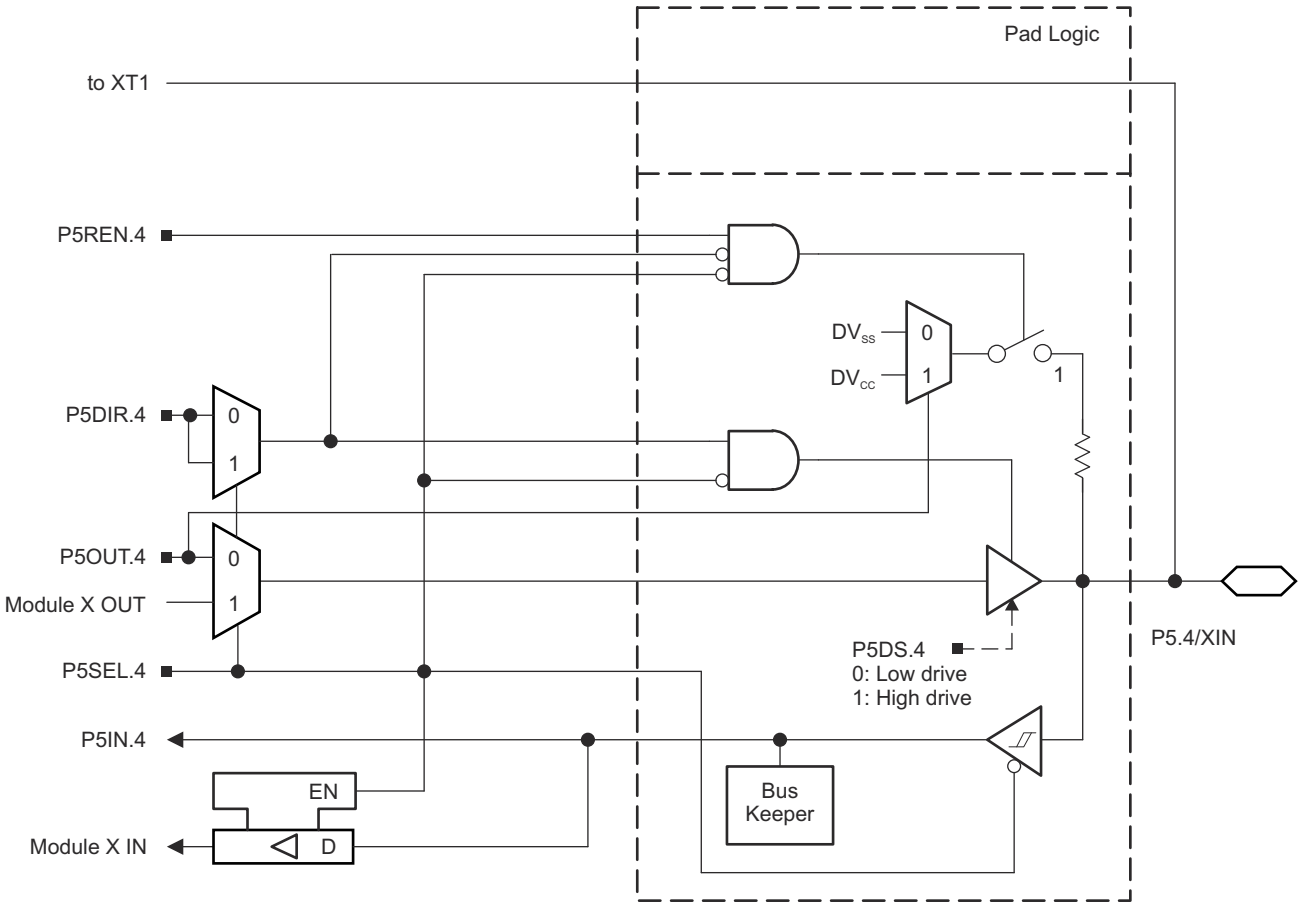


图 9-9. Port P5 (P5.4) Diagram

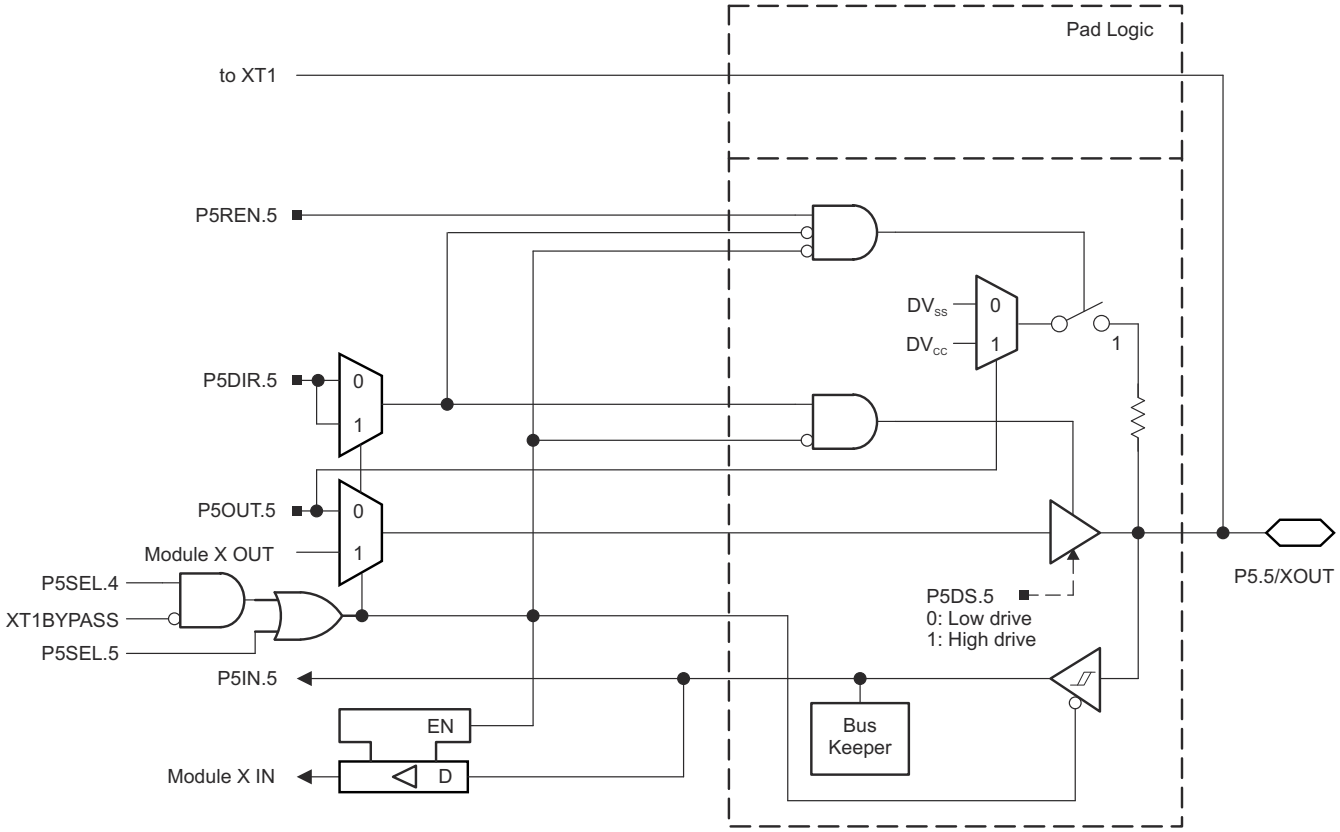


图 9-10. Port P5 (P5.5) Diagram

表 9-55. Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode(2)	X	1	X	0
		XIN bypass mode(2)	X	1	X	1
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	0	X
		XOUT crystal mode(3)	X	1	X	0
		P5.5 (I/O)(3)	X	1	0	1

(1) X = Don't care
(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

9.10.8 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

图 9-11 shows the port diagram. 表 9-56 summarizes the selection of the pin function.

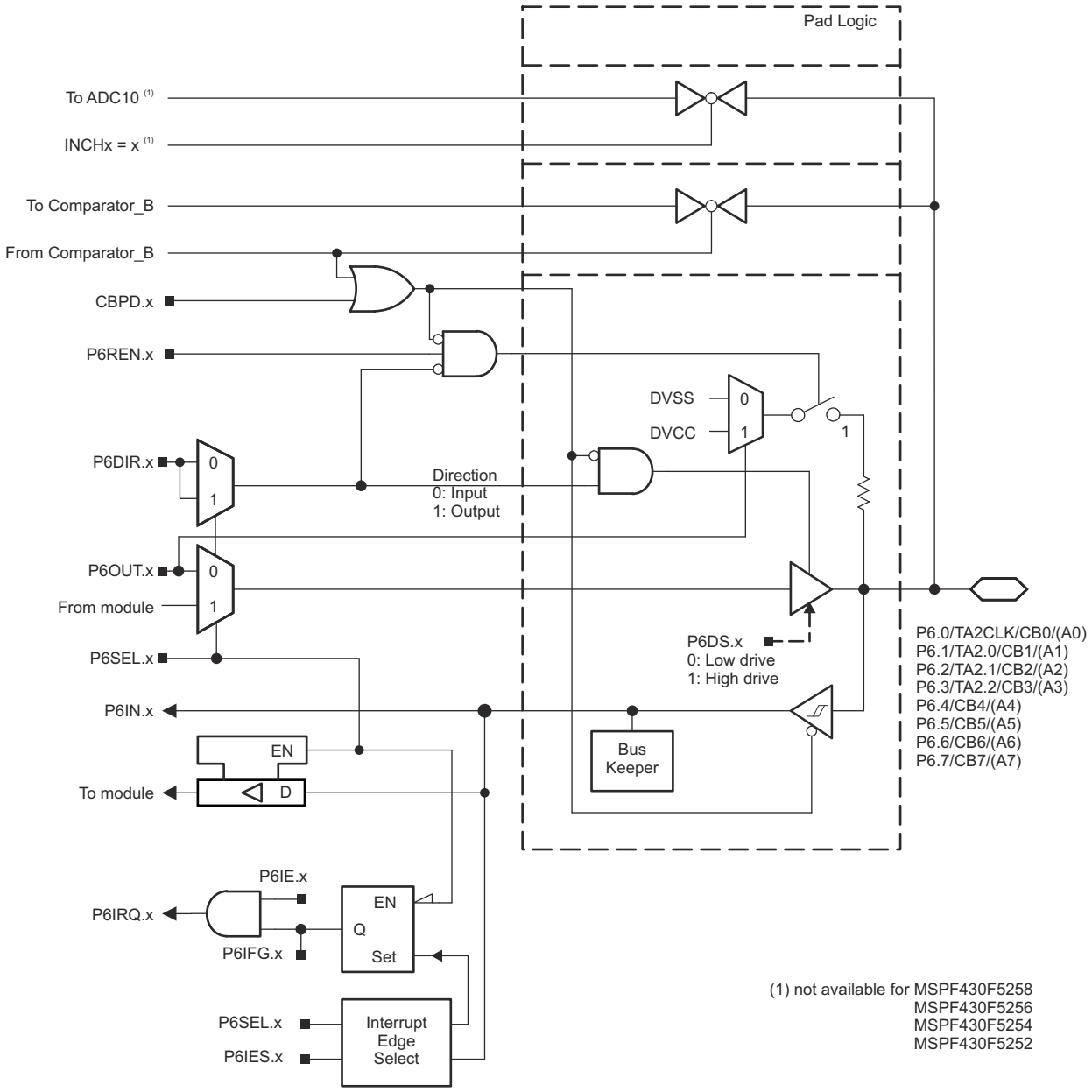


图 9-11. Port P6 (P6.0 to P6.7) Diagram

表 9-56. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P6DIR.x	P6SEL.x	CBPD
P6.0/TA2CLK/SMCLK/CB0/(A0)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		TA2CLK	0	1	0
		SMCLK	1	1	0
		A0	X	X	1
		CB0(1)	X	X	1
P6.1/TA2.0/CB1/(A1)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		TA2.CCI0A	0	1	0
		TA2.0	1	1	0
		A1	X	X	1
		CB1(1)	X	X	1
P6.2/TA2.1/CB2/(A2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		TA2.CCI1A	0	1	0
		TA2.1	1	1	0
		A2	X	X	1
		CB2(1)	X	X	1
P6.3/TA2.1/CB3/(A3)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		TA2.CCI2A	0	1	0
		TA2.2	1	1	0
		A3	X	X	1
		CB3(1)	X	X	1
P6.4/CB4/(A4)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4	X	X	1
		CB4(1)	X	X	1
P6.5/CB5/(A5)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5	X	X	1
		CB5(1)	X	X	1
P6.6/CB6/(A6)	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6	X	X	1
		CB6(1)	X	X	1
P6.7/CB7/(A7)	7	P6.7 (I/O)	I: 0; O: 1	0	0
		A7	X	X	1
		CB7(1)	X	X	1

(1) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

9.10.9 Port P7 (P7.0 to P7.5) Input/Output With Schmitt Trigger

图 9-12 shows the port diagram. 表 9-57 summarizes the selection of the pin function.

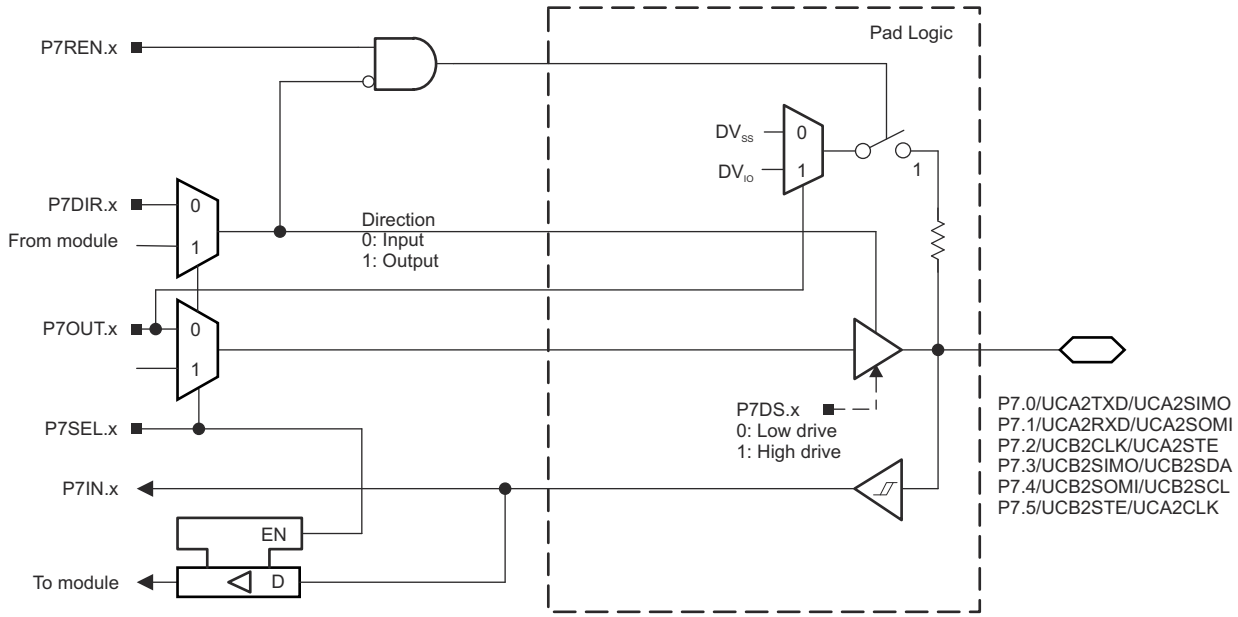


图 9-12. Port P7 (P7.0 to P7.5) Diagram

表 9-57. Port P7 (P7.0 to P7.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P7DIR.x	P7SEL.x
P7.0/UCA2TXD/UCA2SIMO(2)	0	P7.0 (I/O)	I: 0; O: 1	0
		UCA2TXD/UCA2SIMO(1)	X	1
P7.1/UCA2RXD/UCA2SOMI(2)	1	P7.1 (I/O)	I: 0; O: 1	0
		UCA2RXD/UCA2SOMI(1)	X	1
P7.2/UCB2CLK/UCA2STE(2)	2	P7.2 (I/O)	I: 0; O: 1	0
		UCB2CLK/UCA2STE(1) (3)	X	1
P7.3/UCB2SIMO/UCB2SDA(2)	3	P7.3 (I/O)	I: 0; O: 1	0
		UCB2SIMO/UCB2SDA(1) (4)	X	1
P7.4/UCB2SOMI/UCB2SCL(2)	4	P7.4 (I/O)	I: 0; O: 1	0
		UCB2SOMI/UCB2SCL(1) (4)	X	1
P7.5/UCB2STE/UCA2CLK(2)	5	P7.5 (I/O)	I: 0; O: 1	0
		UCB2STE/UCA2CLK(1)	X	1

(1) Setting P7SEL.x bit disables the output driver and the input Schmitt trigger.
(2) The pin direction is controlled by the USCI module.
(3) UCB2CLK function takes precedence over UCA2STE function. If the pin is required as UCB2CLK input or output, USCI_A2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

9.10.10 Port J (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

图 9-13 shows the port diagram. 表 9-58 summarizes the selection of the pin function.

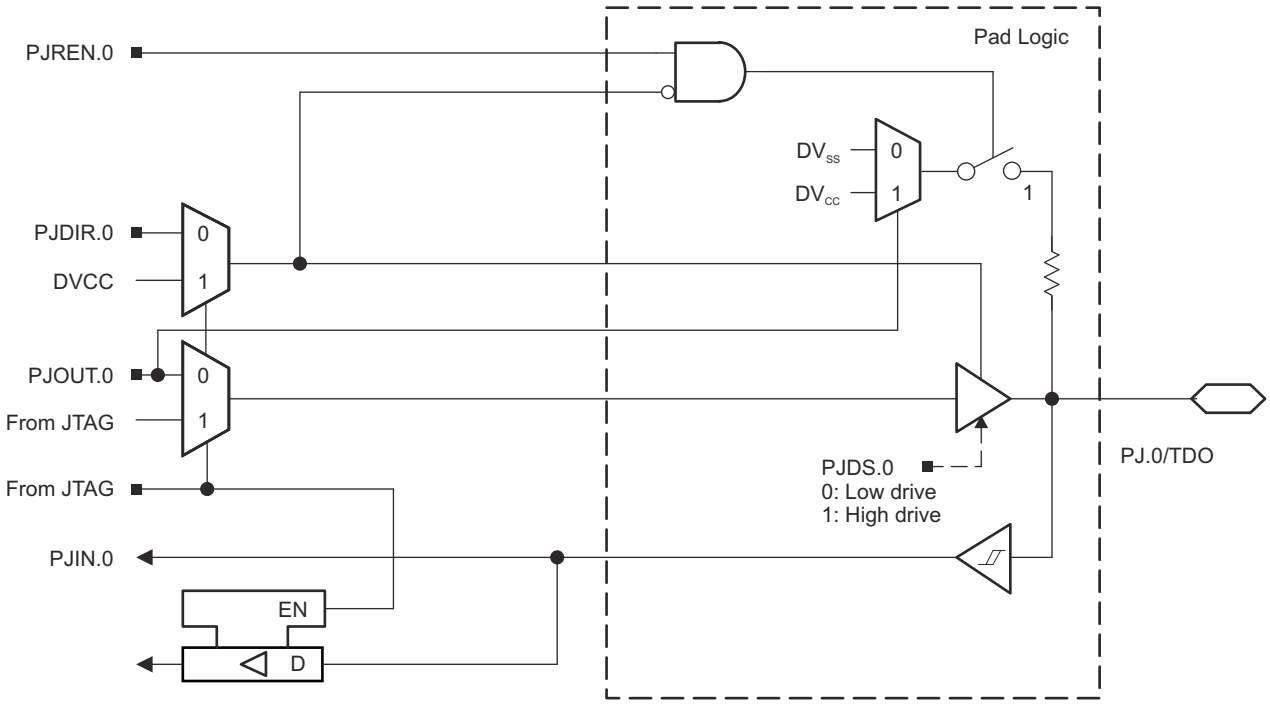


图 9-13. Port PJ (PJ.0) Diagram

9.10.11 Port J (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

图 9-14 shows the port diagram. 表 9-58 summarizes the selection of the pin function.

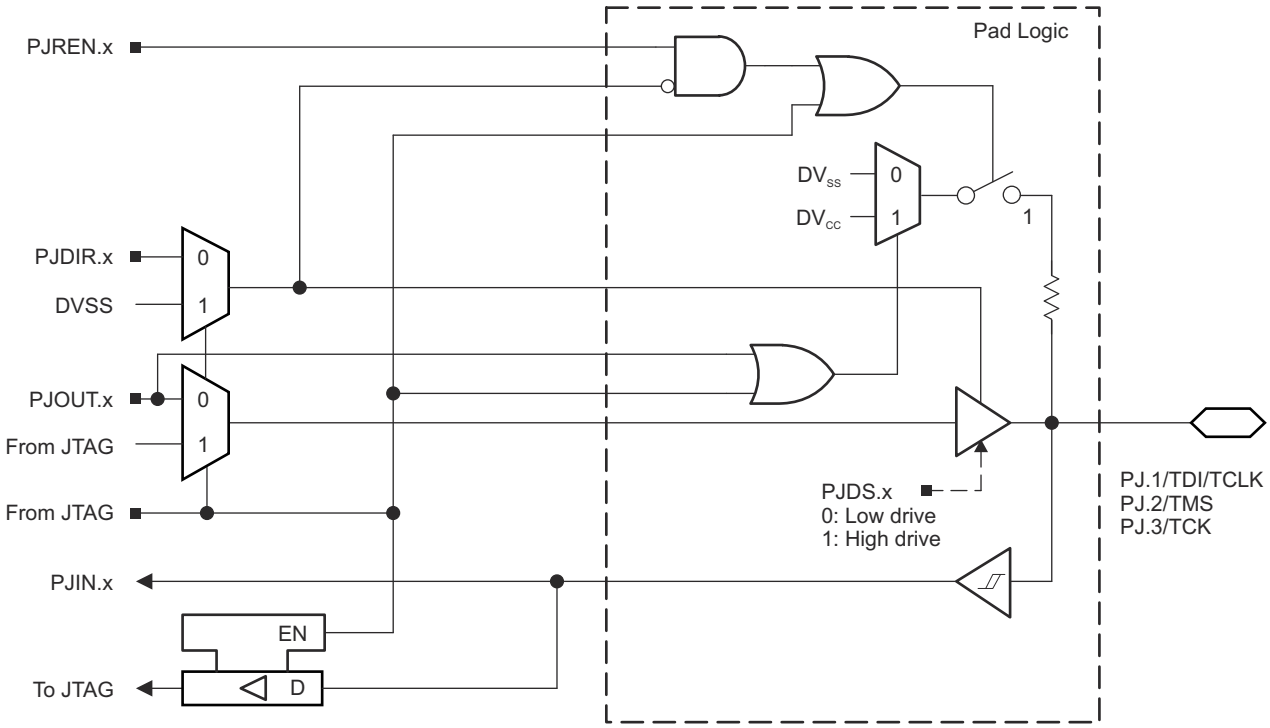


图 9-14. Port PJ (PJ.1 to PJ.3) Diagram

表 9-58. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)(2)	I: 0; O: 1
		TDO(3)	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)(2)	I: 0; O: 1
		TDI/TCLK(3) (4)	X
PJ.2/TMS	2	PJ.2 (I/O)(2)	I: 0; O: 1
		TMS(3) (4)	X
PJ.3/TCK	3	PJ.3 (I/O)(2)	I: 0; O: 1
		TCK(3) (4)	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

9.11 Device Descriptors

表 9-59 and 表 9-60 list the contents of the device descriptor tag-length-value (TLV) structure for each device type.

表 9-59. MSP430F5259, MSP430F5257, MSP430F5255, MSP430F5253 Device Descriptor Table

DESCRIPTION[1]		ADDRESS	SIZE (bytes)	VALUE			
				F5259	F5257	F5255	F5253
Info Block	Info length	01A00h	1	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	FF	01	03	05
	Device ID	01A05h	1	81	82	82	82
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit
ADC10 Calibration	ADC10 calibration tag	01A14h	1	13h	13h	13h	13h
	ADC10 calibration length	01A15h	1	10h	10h	10h	10h
	ADC gain factor	01A16h	2	Per unit	Per unit	Per unit	Per unit
	ADC offset	01A18h	2	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 30°C	01A1Ah	2	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 85°C	01A1Ch	2	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	2	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	2	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	2	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	2	Per unit	Per unit	Per unit	Per unit
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit

(1) NA = Not applicable, blank = unused and reads FFh.

表 9-60. MSP430F5258, MSP430F5256, MSP430F5254, MSP430F5252 Device Descriptor Table

DESCRIPTION[1]		ADDRESS	SIZE (bytes)	VALUE			
				F5258	F5256	F5254	F5252
Info Block	Info length	01A00h	1	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	00	02	04	06
	Device ID	01A05h	1	82	82	82	82
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit
ADC10 Calibration	ADC10 calibration tag	01A14h	1	13h	13h	13h	13h
	ADC10 calibration length	01A15h	1	10h	10h	10h	10h
	ADC gain factor	01A16h	2	blank	blank	blank	blank
	ADC offset	01A18h	2	blank	blank	blank	blank
	ADC 1.5-V reference Temperature sensor 30°C	01A1Ah	2	blank	blank	blank	blank
	ADC 1.5-V reference Temperature sensor 85°C	01A1Ch	2	blank	blank	blank	blank
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	2	blank	blank	blank	blank
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	2	blank	blank	blank	blank
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	2	blank	blank	blank	blank
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	2	blank	blank	blank	blank
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit

(1) NA = Not applicable, blank = unused and reads FFh.

10 Device and Documentation Support

10.1 Getting Started and Next Steps

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the MSP430 ultra-low-power sensing and measurement MCUs overview.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

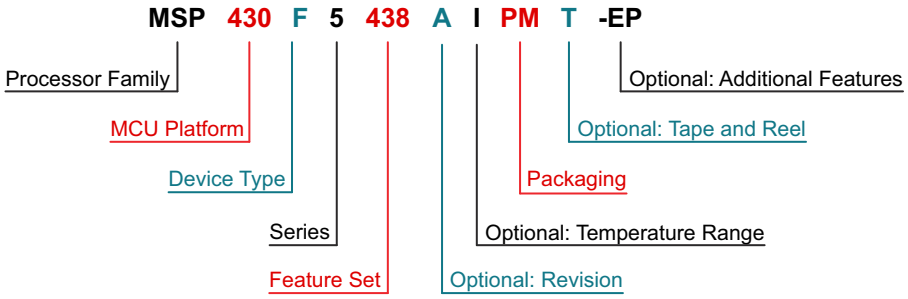
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. 图 10-1 provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory	**Specialized Application** AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series
Feature Set	Various levels of integration within a series	
Optional: Revision	Updated version of the base part number	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C) -Q1 = Automotive Q100 qualified	

图 10-1. Device Nomenclature

10.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 ultra-low-power MCUs – Tools & software.

表 10-1 lists the debug features of the MSP430F522x MCUs. See the *Code Composer Studio IDE for MSP430 MCUs User's Guide* for details on the available features.

表 10-1. Hardware Debug Features

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER	LPMx.5 DEBUGGING SUPPORT
MSP430Xv2	Yes	Yes	8	Yes	Yes	Yes	Yes	No

Design Kits and Evaluation Modules

64-pin target development board and MSP-FET programmer bundle for MSP430F5x MCUs

The MSP-FET430U64C is a powerful tool that includes the hardware and software required to complete much of your application development work. The flash memory can be erased and programmed in seconds with only a few keystrokes, and since the MSP430 flash is extremely low power, no external power supply is required.

64-pin target development board for MSP430F5x MCUs

The MSP-TS430RGC64C is a stand-alone 64-pin ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

Dual-mode Bluetooth CC2564 module with integrated antenna evaluation board

The CC2564MODAEM evaluation board contains the Bluetooth BR/EDR/LE HCI solution. Based on TI's CC2564B dual-mode Bluetooth single-chip device, the CC2564MODA is intended for evaluation and design purposes, reducing design effort and enabling fast time to market.

Software

MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430F525x Code Examples

C code examples that configure each of the integrated peripherals for various application needs.

MSP Driver Library

Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace™ Technology

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

IEC 60730 Software Package

The IEC 60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC 60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed Point Math Library for MSP

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating Point Math Library for MSP430

Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user's guide for an in depth look at the math library and relevant benchmarks.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

Command-Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which allows users to quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a Backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 Flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices.

10.4 Documentation Support

The following documents describe the MSP430F525x devices. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for links to the product folders, see 节 10.5). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, see the revision history of any revised document.

Errata

MSP430F5259 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5258 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5257 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5256 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5255 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5254 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5253 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F5252 Device Erratasheet

Describes the known exceptions to the functional specifications.

User's Guides

MSP430F5xx and MSP430F6xx Family User's Guide

Detailed information on the modules and peripherals available in this device family.

MSP430 Flash Devices Bootloader (BSL) User's Guide

The MSP430 bootloader (BSL, formerly known as the bootstrap loader) allows users to communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-Level ESD has become increasingly demanding as silicon technology scales to lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three ESD topics to help board designers and OEMs understand and design robust system-level designs: (1) Component-level ESD testing and system-level ESD testing; (2) General design guidelines for system-level ESD protection; (3) Introduction to System Efficient ESD Design (SEED), a co-design methodology of on-board and on-chip ESD protection.

Designing With MSP430F522x and MSP430F521x Devices

The MSP430F522x and MSP430F521x devices support a split supply I/O system that is essential in systems in which the MCU is required to interface with external devices (such as sensors or other processors) that operate at different voltage level compared to the MCU device supply. Additionally, the split supply input voltage range of the F522x and F521x devices starts as low as 1.62 V (see the device data sheet specifications), and this allows for nominal 1.8-V I/O interface without the need for external level translation. This application report describes the various design considerations to keep in mind while designing the F522x and F521x devices in an application.

10.5 Related Links

表 10-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430F5259	Click here	Click here	Click here	Click here	Click here
MSP430F5258	Click here	Click here	Click here	Click here	Click here
MSP430F5257	Click here	Click here	Click here	Click here	Click here
MSP430F5256	Click here	Click here	Click here	Click here	Click here
MSP430F5255	Click here	Click here	Click here	Click here	Click here
MSP430F5254	Click here	Click here	Click here	Click here	Click here
MSP430F5253	Click here	Click here	Click here	Click here	Click here
MSP430F5252	Click here	Click here	Click here	Click here	Click here

10.6 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

10.10 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5252IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5252
MSP430F5252IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5252
MSP430F5252IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5252
MSP430F5252IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5252
MSP430F5253IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5253
MSP430F5253IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5253
MSP430F5253IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5253
MSP430F5253IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5253
MSP430F5254IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5254
MSP430F5254IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5254
MSP430F5254IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5254
MSP430F5254IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5254
MSP430F5255IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5255
MSP430F5255IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5255
MSP430F5255IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5255
MSP430F5255IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5255
MSP430F5255IZQER	Obsolete	Production	BGA MICROSTAR JUNIOR (ZQE) | 80	-	-	Call TI	Call TI	-	F5255
MSP430F5256IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5256
MSP430F5256IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5256
MSP430F5256IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5256
MSP430F5256IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5256
MSP430F5257IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5257
MSP430F5257IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5257
MSP430F5257IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5257
MSP430F5257IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5257
MSP430F5258IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5258
MSP430F5258IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5258
MSP430F5258IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5258

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5258IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5258
MSP430F5259IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5259
MSP430F5259IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5259
MSP430F5259IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5259
MSP430F5259IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	F5259
MSP430F5259IZQE	Obsolete	Production	BGA MICROSTAR JUNIOR (ZQE) | 80	-	-	Call TI	Call TI	-	F5259

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

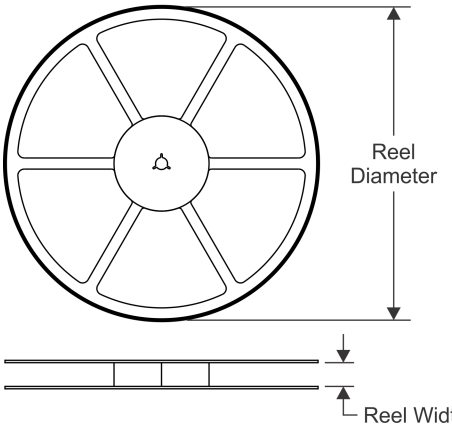
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

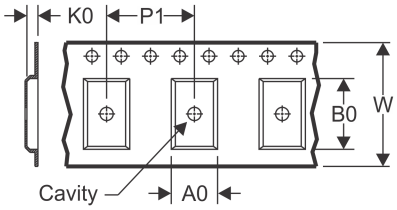
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

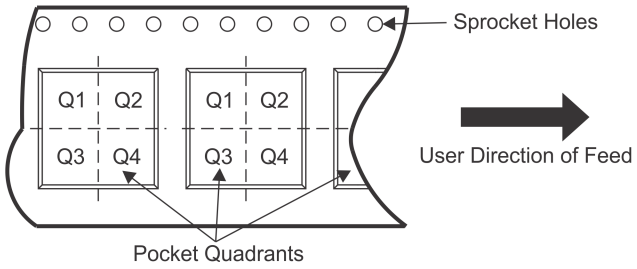


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

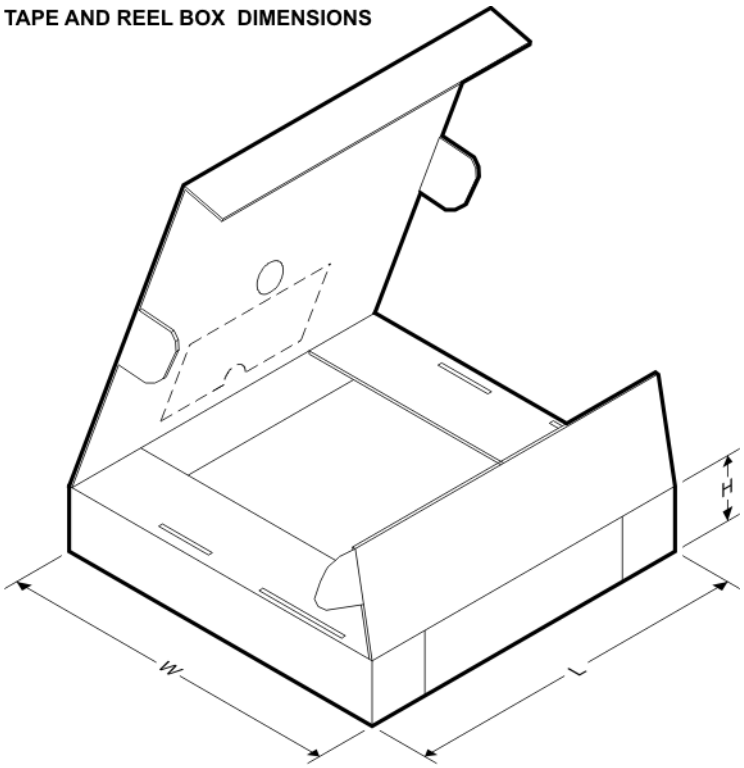
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5252IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5252IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5253IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5253IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5254IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5254IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5255IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5255IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5256IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5256IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5257IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5257IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5258IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5258IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5259IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430F5259IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5252IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5252IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5253IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5253IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5254IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5254IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5255IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5255IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5256IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5256IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5257IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5257IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5258IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5258IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5259IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5259IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0

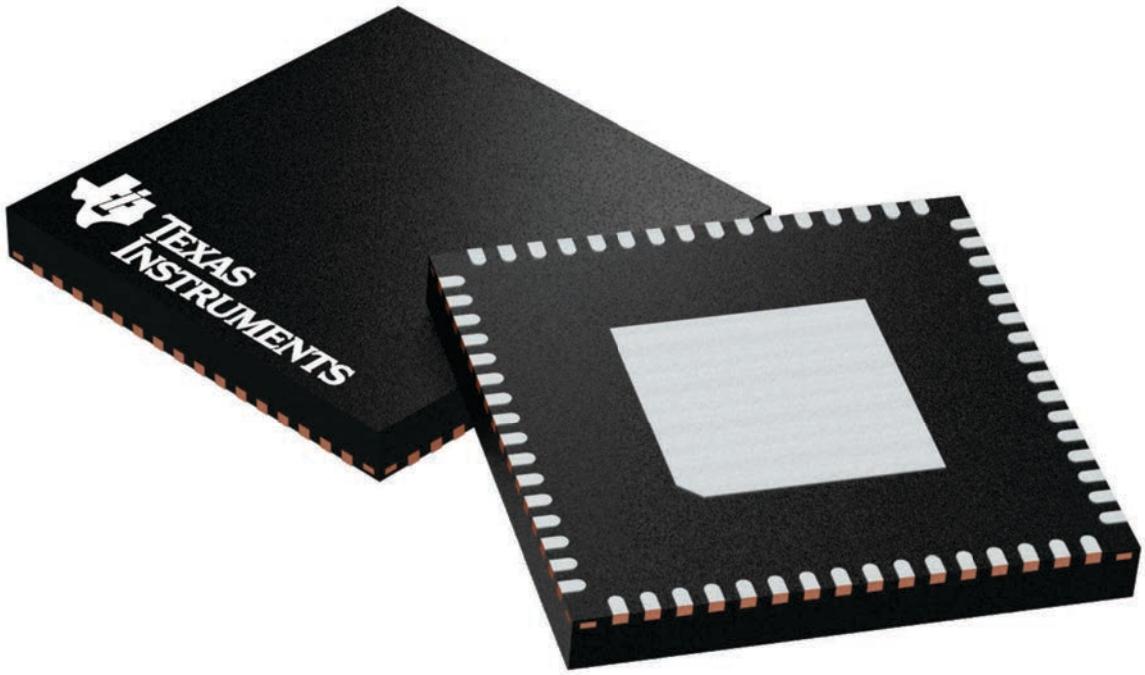
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

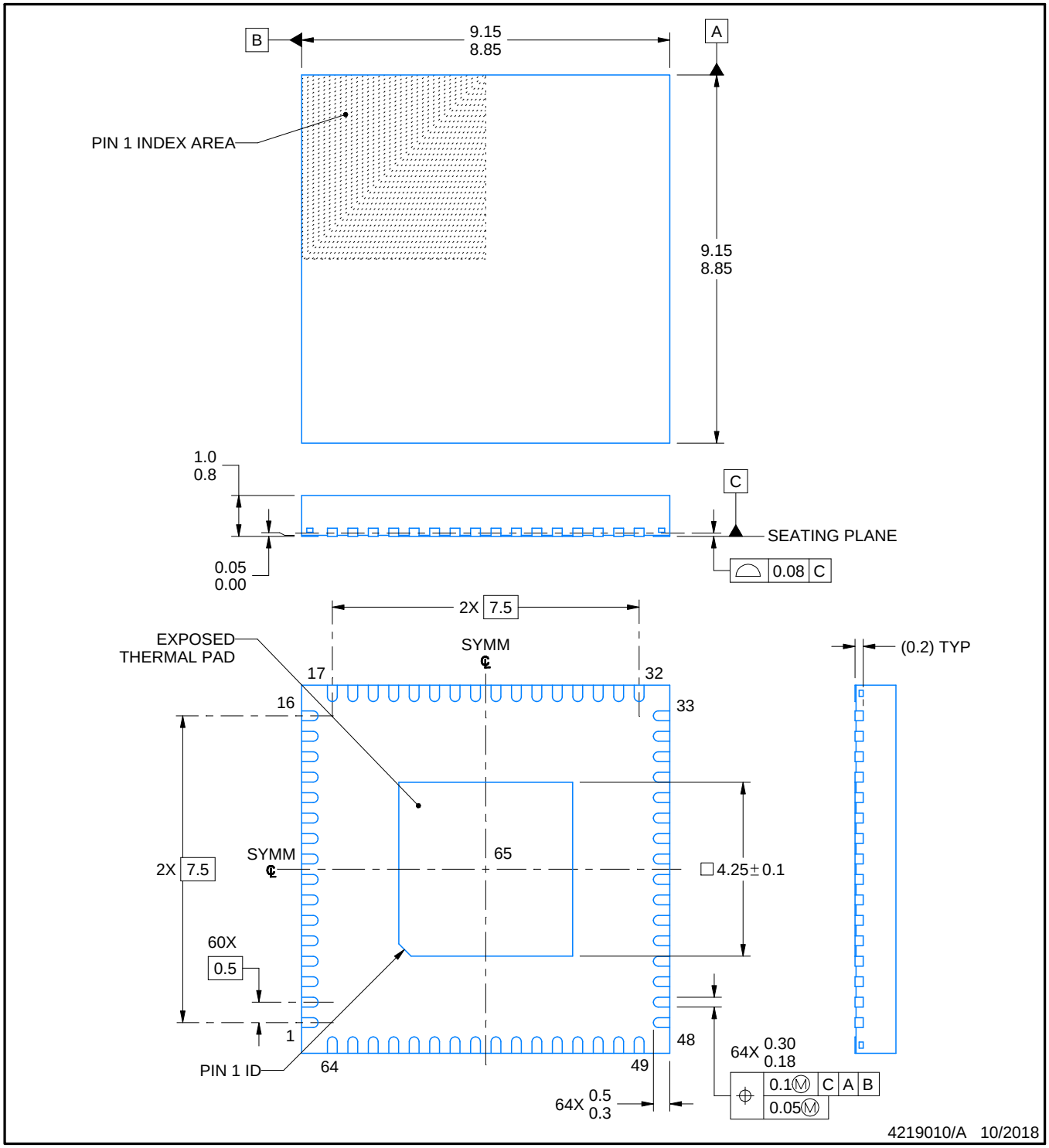
4224597/A

PACKAGE OUTLINE

RGC0064B

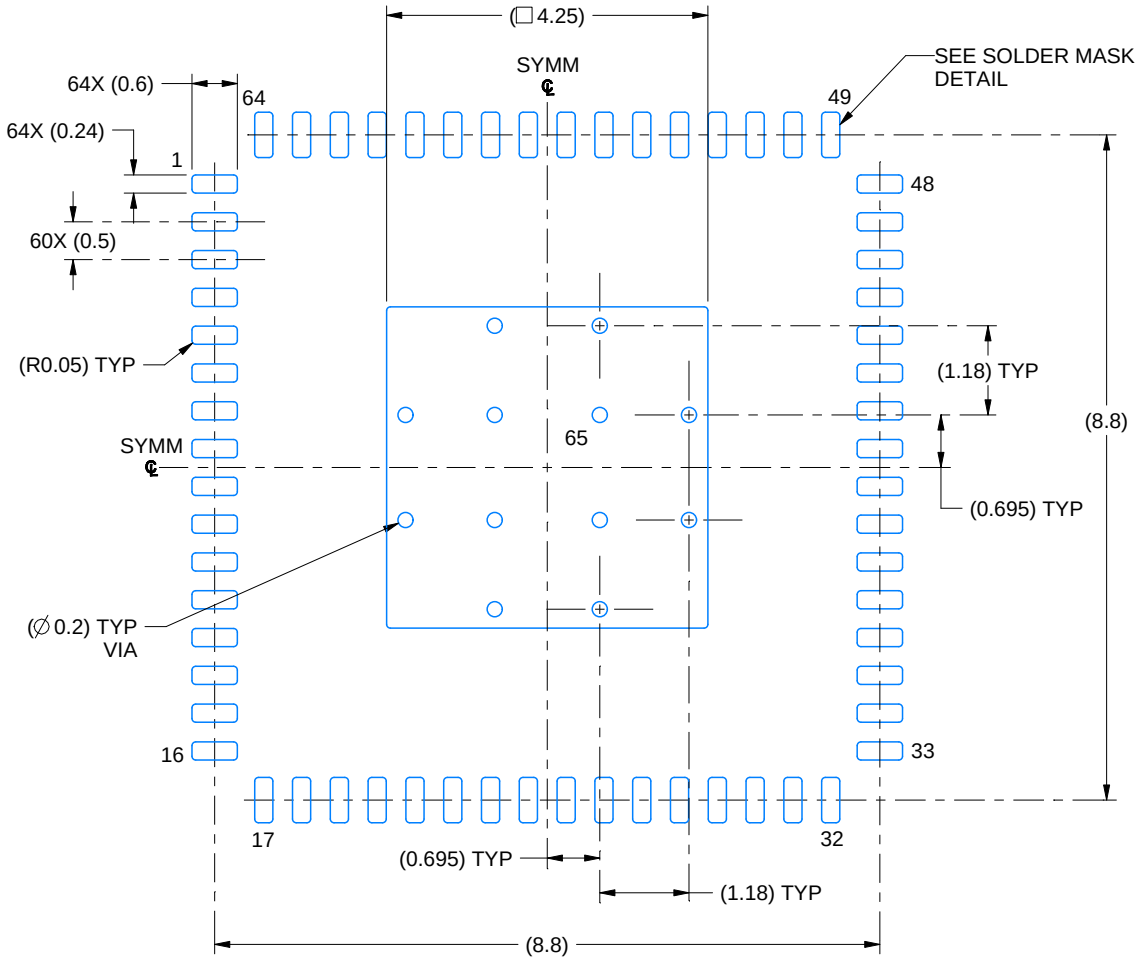
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

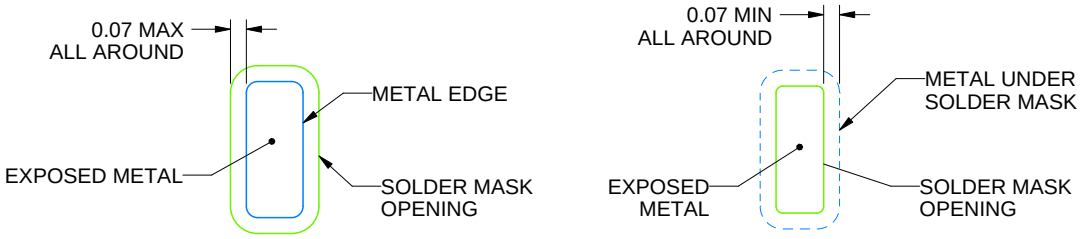


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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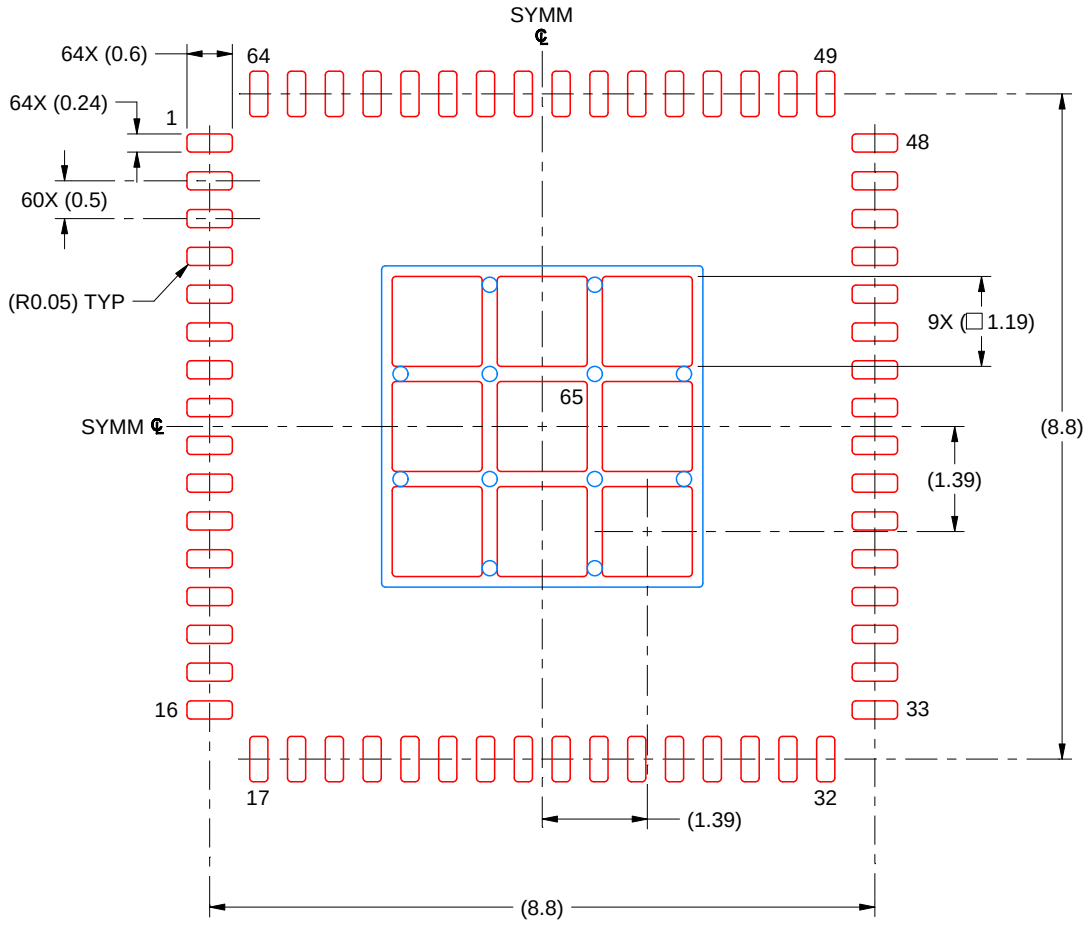
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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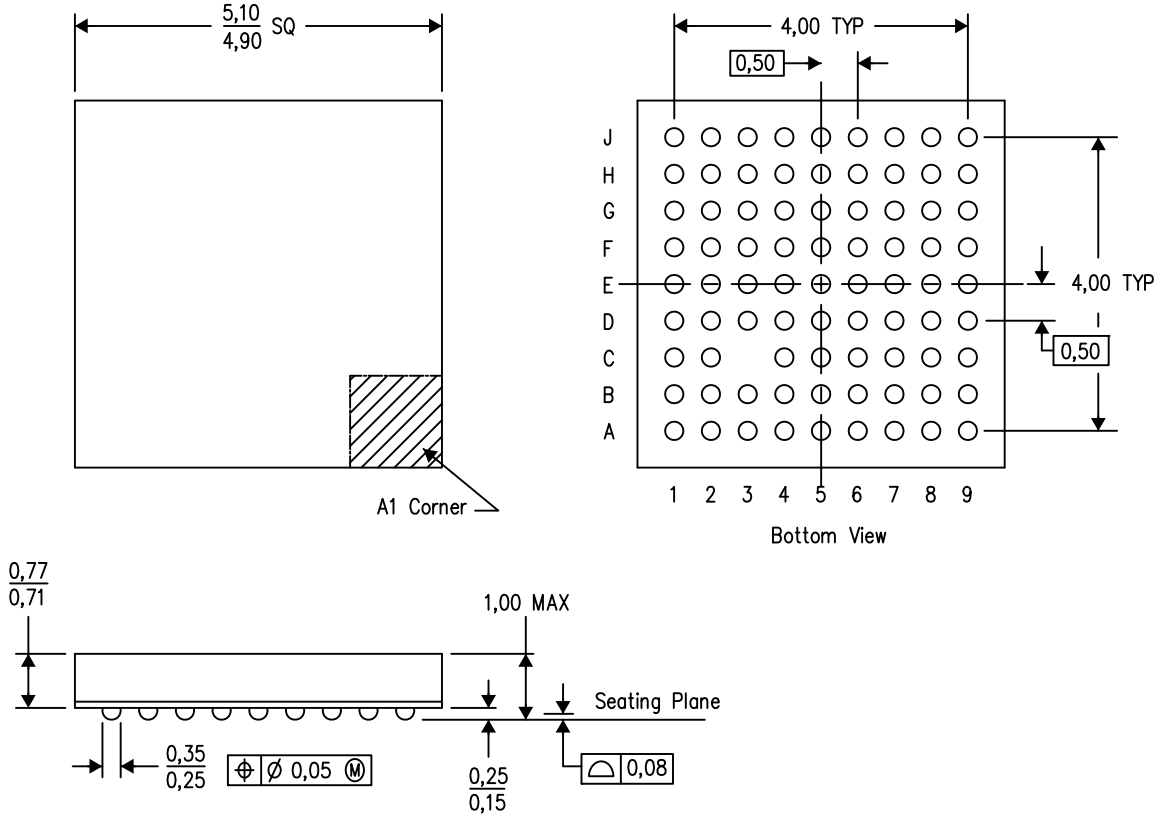
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334-6/G 09/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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