MCT8376Z-Q1 Sensored Trapezoidal Integrated FET BLDC Motor Driver

1 Features

- Three-phase BLDC motor driver with integrated Sensored Trapezoidal control
  - Hall Sensor based Trapezoidal (120°) commutation
  - Supports Analog or Digital Hall inputs
  - Configurable PWM modulation: Synchronous/ Asynchronous
  - Supports 48V systems
  - Supports up to 100kHz PWM frequency
  - Active Demagnetization to reduce power losses
  - Cycle-by-cycle current limit to limit phase current
- 4.5V to 65V operating voltage (70V abs max)
- High output current capability: 4.5A Peak
- Low MOSFET on-state resistance
  - 400mΩ $R_{DS(ON)}$ (HS + LS) at T_A = 25°C
- Reduced switching loss with 1.1V/ns slew rate and reverse recovery loss minimization technique
- Low audible noise and ease of motor control with ultra-low dead time < 200ns, and propagation delay < 100ns
- Low-power sleep mode
  - 1.5µA typical at V_{VM} = 24V, T_A = 25°C
- Flexible device configuration options
- Flexible device configuration options
  - MCT8376ZS-Q1: 5MHz 16bit SPI for device configuration and fault status
  - MCT8376ZH-Q1: Hardware pin-based configuration
- Supports 1.8V, 3.3V, and 5V logic inputs
- Built-in 3.3V (5%), 30mA LDO regulator
- Built-in 5V (5%), 30mA LDO regulator
- Integrated protection features
  - Supply under voltage lockout (UVLO)
  - Charge pump under voltage (CPUV)
  - Overcurrent protection (OCP)
  - Motor lock protection
  - Thermal warning and shutdown (OTW/OTSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over SPI

2 Applications

- Brushless-DC (BLDC) Motor Modules
- HVAC motors
- Office automation machines
- Factory automation and robotics
- Wireless antenna motor
- Drones

3 Description

The MCT8376Z-Q1 provides a single-chip code-free sensored trapezoidal control for driving 4.5V to 65V brushless-DC motors. The MCT8376Z-Q1 integrates three 1/2-H bridges with 70V absolute maximum voltage capability and a very low $R_{DS(ON)}$ of 400mΩ (high-side and low-side combined) to enable high power drive capability. Current is sensed using an integrated current sensing feature which eliminates the need for external sense resistors. Power management features with integrated LDO generate the necessary voltage rails for the device and can be used to power external circuits.

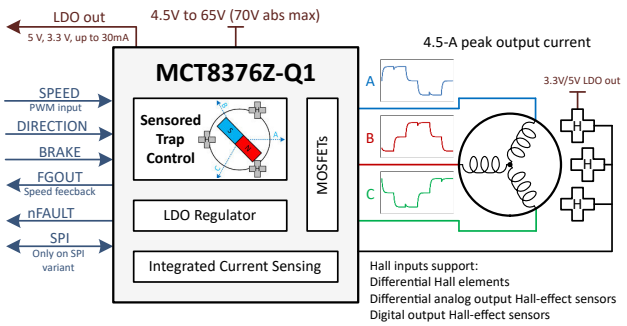
MCT8376Z-Q1 implements sensored trapezoidal control in a fixed-function state machine, so an external microcontroller is not required to spin the brushless-DC motor. The MCT8376Z-Q1 device integrates three analog hall comparators for position sensing to achieve sensored trapezoidal BLDC motor control. The control scheme is highly configurable through hardware pins or register settings ranging from motor current limiting behavior to fault response. The speed can be controlled through a PWM input.

There are a large number of protection features integrated into MCT8376Z-Q1, intended to protect the device, motor, and system against fault events.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCT8376ZH-Q1	VQFN (28)	6.00mm x 5.00mm
MCT8376ZS-Q1	VQFN (28)	6.00mm x 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematics

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4 Device Comparison Table

DEVICE	PACKAGES	INTERFACE
MCTV8376ZS-Q1	28-pin VQFN (6x5mm)	SPI
MCT8376ZH-Q1		Hardware

Table 4-1. MCT8376ZS-Q1 (SPI variant) vs. MCT8376ZH-Q1 (Hardware variant) configuration comparison

Parameters	MCT8376ZS-Q1 (SPI variant)	MCT8376ZH-Q1 (Hardware variant)
PWM mode settings	PWM_MODE (4 settings)	MODE pin (7 settings)
Slew rate settings	SLEW_RATE (4 settings)	GAIN_SLEW_tLOCK pin (2 settings)
CSA gain settings	CSA_GAIN (4 settings)	GAIN_SLEW_tLOCK pin (2 settings)
SDO pin configuration: mode, voltage	SDO_ODEN (2 settings), SDO_VSEL (2 settings), SDO_MD (2 settings)	Not Applicable
Current Limit configuration: Mode, reporting on nFAULT, Blanking time, 100% duty PWM frequency	ILIMFLT_MODE (2 settings), ILIM_MODE (2 settings), ILIM_BLANK_SEL (4 settings), PWM_100_FREQ_SEL (4 settings)	Current limit reporting on nFAULT is enabled, fixed to coast mode, blanking time set to 5.5µs for slew rate of 50 and 1.8µs for all other slew rates, the 100% duty input PWM cycle is fixed to 20kHz
Over voltage protection mode	OVP_MODE (2 settings), OVP_SEL (2 settings)	Over voltage protection is disabled
OCP configuration: Mode, level, deglitch	OCP_MODE (4 settings) , OCP_LVL (2 settings) ,OCP_DEG (4 settings) and OCP_TRETRY (2 settings)	Enabled with automatic retry mode, level is fixed to 4.5A with 1.25 us deglitch time, 5ms retry time
Active demagnetization: Enable, comparator threshold, comparator mask time, behaviour during fault	EN_ASR (2 settings), EN_AAR (2 settings), AD_COMP_TH (2 settings)	MODE (2 settings), active demag comparator threshold set to 100mA, comparator mask time set to 5.5µs for slew rate of 50 and 1.8µs for all other slew rates. ADMAG_TMARGIN set to 3.2µs, active demag is disabled during OCP and motor lock.
Over temperature warning	OTW_MODE (2 settings)	Reported on nFAULT
Direction settings	DIR (2 settings)	DIR pin (2 settings)
Lead angle settings	ADVANCE_LVL (8 settings)	ADVANCE pin (7 settings)
FGOUT configuration	FG_MODE (4 settings)	Fixed to 3x commutation frequency
Motor lock configuration: mode, detection and retry timing	MTR_LOCK_MODE (4 settings), MTR_LOCK_TDET (4 settings), MTR_LOCK_RETRY (2 settings)	Enabled with automatic retry, detection time of 500ms or 5s configured through MODE pin, and retry time of 10s.
Hall comparator configuration	HALL_HYS (2 settings)	Fixed to 5mV

5 Pin Configuration and Functions

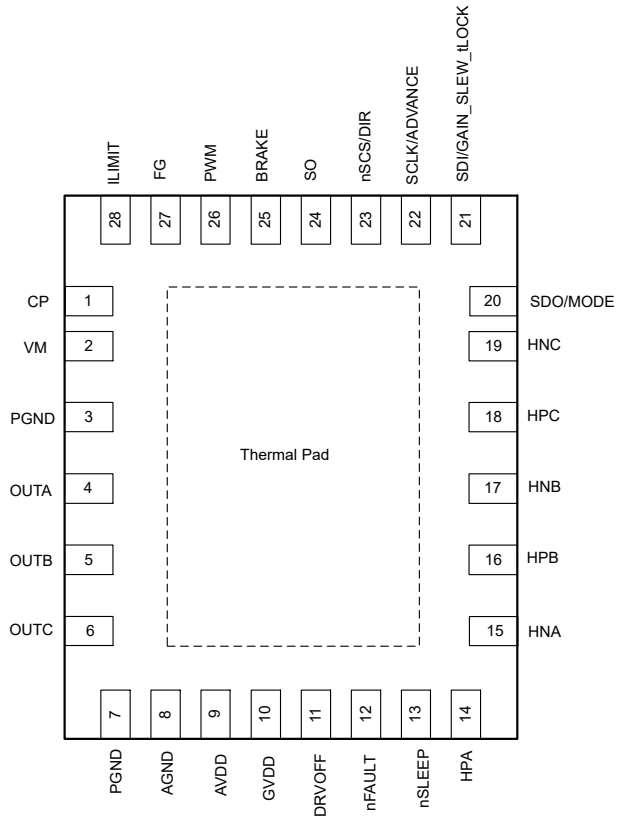


Figure 5-1. MCT8376Z-Q1 28-Pin VQFN With Exposed Thermal Pad Top View

Table 5-1. MCT8376Z-Q1 Pin Functions

PIN	28-pin VQFN Package		TYPE[1]	DESCRIPTION
NAME	MCT8376Z H-Q1	MCT8376Z S-Q1		
ADVANCE	22	-	I	Advance angle level setting. This pin is a 7-level input pin set by an external resistor.
AGND	8	8	GND	Device analog ground. Refer Section 9.4.1 for connections recommendation.
AVDD	9	9	PWR O	3.3V internal regulator output. Connect an X5R or X7R, 1µF, 6.3V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30mA externally.
GVDD	10	10	PWR O	5V internal regulator output. Connect an X5R or X7R, 1µF, 10V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30mA externally.
BRAKE	25	25	I	High → Brake the motor when High by turning all low side MOSFETs ON Low → normal operation
CP	1	1	PWR O	Charge pump output. Connect a X5R or X7R, 1µF, 16V ceramic capacitor between the CP and VM pins.
DIR	23	-	I	Direction pin for setting the direction of the motor rotation to clockwise or counterclockwise.
DRVOFF	11	11	I	When this pin is pulled high the six MOSFETs in the power stage are turned OFF making all outputs Hi-Z.
FG	27	27	I	Motor Speed indicator output. Open-drain output requires an external pull-up resistor to 1.8V to 5.0V. Motor Speed indicator can be set to different division factor of Hall signals.

Table 5-1. MCT8376Z-Q1 Pin Functions (continued)

PIN	28-pin VQFN Package		TYPE(1)	DESCRIPTION
NAME	MCT8376ZH-Q1	MCT8376ZS-Q1		
GAIN_SLEW_tLOCK	21	-	I	Motor lock detection time setting, CSA Gain and Slew Rate setting
HNA	15	15	I	Phase A hall element negative input. Noise filter capacitors are desirable, connected between the positive and negative hall inputs.
HNB	17	17	I	Phase B hall element negative input. Noise filter capacitors are desirable, connected between the positive and negative hall inputs.
HNC	19	19	I	Phase C hall element negative input. Noise filter capacitors are desirable, connected between the positive and negative hall inputs.
HPA	14	14	I	Phase A hall element positive input. Noise filter capacitors are desirable, connected between the positive and negative hall inputs.
HPB	16	16	I	Phase B hall element positive input. Noise filter capacitors are desirable, connected between the positive and negative hall inputs.
HPC	18	18	I	Phase C hall element positive input. Noise filter capacitors are desirable, connected between the positive and negative hall inputs.
ILIMIT	28	28		Sets the threshold for phase current used in cycle by cycle current limit.
MODE	20	-	I	PWM input mode and Hall configuration setting. This pin is a 7-level input pin set by an external resistor.
nFAULT	12	12	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V. If external supply is used to pull up nFAULT, verify that the external supply is pulled to >2.2V on power up.
nSCS	-	23	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSLEEP	13	13	I	Driver nSLEEP. When this pin is logic low, the device goes into a low-power sleep mode. An 20 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
OUTA	4	4	PWR O	Half bridge output A
OUTB	5	5	PWR O	Half bridge output B
OUTC	6	6	PWR O	Half bridge output C
PGND	3, 7	3, 7	GND	Device power ground. Refer Section 9.4.1 for connections recommendation.
PWM	26	26		PWM input for motor control. Set the duty cycle and switching frequency of the phase voltage of the motor
SCLK	-	22	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).
SDI	-	21	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	-	20	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
SO	24	24	O	Current sense amplifier output. Supports capacitive load or low pass filter (resistor in series and capacitor to GND).
VM	2	2	PWR I	Power supply. Connect to motor supply voltage; bypass to PGND with a 0.1µF capacitor plus one bulk capacitor rated for VM. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad			GND	Must be connected to analog ground.

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	70	V
Power supply voltage ramp (VM)		4	V/µs
Voltage difference between ground pins (PGND, AGND)	–0.6	0.6	V
Charge pump voltage (CP)	–0.3	V_M + 6.2	V
Analog regulators pin voltage (GVDD)	–0.3	5.75	V
Analog regulators pin voltage (AVDD)	-0.3	5.75	V
Analog pin input voltage (ILIMIT)	-0.3	5.75	V
Analog pin output voltage (SO)	-0.3	AVDD	V
Logic pin input voltage (DRVOFF, PWM, HPx, HNx, BRAKE, DIR, nSCS, nSLEEP, SCLK, SDI)	–0.3	5.75	V
Logic pin output voltage (nFAULT, SDO, FG)	–0.3	5.75	V
Multi-level pin input voltage (ADVANCE, GAIN_SLEW_tLOCK, MODE)	-0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_M + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings AUTO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	65	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			100	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			4	A
V_{IN}	Logic input voltage	DRVOFF, nSCS, nSLEEP, SCLK, SDI, PWM, BRAKE, DIR, HPx, HNx	–0.1		5.5	V
V_{IN}	Multilevel input voltage	ADVANCE, FG_SEL/LOCK_DET_TIME, MODE	-0.1		GVDD	
V_{OD}	Open drain pullup voltage	nFAULT, SDO, FG	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	2.2		AVDD	V
I_{OD}	Open drain output current	nFAULT, SDO, FG			5	mA
V_{VREF}	Voltage reference pin voltage	VREF		2.8	5.5	V
ILIMIT	Voltage reference for current limit	ILIMIT	-0.1		5.5	V
T_A	Operating ambient temperature		–40		125	°C

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		MCT8376ZH-Q1, MCT8376ZS-Q1	UNIT
		VQFN (NLG)	
		28 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6V, nSLEEP = 0, T_A = 25°C		1.5	3	µA
		nSLEEP = 0		2.5	8	µA
I_{VMS}	VM standby mode current	V_{VM} > 6V, nSLEEP = 1, PWM = 0, SPI = 'OFF', T_A = 25°C		6.6	8.2	mA
		nSLEEP = 1, PWM = 0, SPI = 'OFF'		6.6	8.2	mA
I_{VMS}	VM standby mode current	V_{VM} > 6V, nSLEEP = 1, PWM = 0, SPI = 'OFF', T_A = 25°C, ASR and AAR disabled		6.1	7.5	mA
I_{VMS}	VM standby mode current	nSLEEP = 1, PWM = 0, SPI = 'OFF', ASR and AAR disabled		6.1	7.5	mA
I_{VM}	VM operating mode current	V_{VM} > 6V, nSLEEP = 1, f_{PWM} = 20kHz		7.6	9.8	mA
		nSLEEP =1, f_{PWM} = 20kHz		7.6	9.8	mA
		nSLEEP =1, f_{PWM} =100kHz		10.1	13.4	mA
V_{GVDD}	Analog regulator voltage	0mA ≤ I_{GVDD} ≤ 30mA; (External Load); VM > 6V	4.75	5	5.25	V
V_{GVDD}	Analog regulator voltage	0mA ≤ I_{GVDD} ≤ 30mA; (External Load); VM = 4.5V	3.7		4.5	V
V_{AVDD}	Analog regulator voltage	0mA ≤ I_{AVDD} ≤ 30mA; (External Load)	3.1	3.3	3.465	V
I_{GVDD}	External analog regulator load	I_{AVDD} = 0mA			30	mA
I_{AVDD}	External analog regulator load	I_{GVDD} = 0mA			30	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM, (V_{VM} > 6V)	4	5	6	V
t_{PWM_LOW}	PWM low time required for motor lock detection			200		ms
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			5.5	ms
t_{SLEEP}	Sleep Pulse time	nSLEEP = 0 period to enter sleep mode	120			µs

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
LOGIC-LEVEL INPUTS (BRAKE, DIR, DRVOFF, nSLEEP, PWM, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	nSLEEP	1.6		5.5	V
		Other Pins	1.5		5.5	V
V_{HYS}	Input logic hysteresis	nSLEEP	95	300	425	mV
		Other PIns	180	300	425	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0V	–1		1	µA
I_{IH}	Input logic high current	nSLEEP, V_{PIN} (Pin Voltage) = 5V	15		35	µA
I_{IH}	Input logic high current	Other pins, V_{PIN} (Pin Voltage) = 5V	30		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	200	300	kΩ
		Other pins	70	100	130	kΩ
t_{GED}	Deglitch time	BRAKE, DIR, DRVOFF pins	0.6	1.15	1.7	µs
C_{ID}	Input capacitance			30		pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			300		mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0V			75	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5V	–1		25	µA
R_{PU}	Input pullup resistance		80	100	130	kΩ
C_{ID}	Input capacitance			30		pF
SEVEN-LEVEL INPUTS (ADVANCE, MODE, GAIN_SLEW_tLOCK)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.09*GVDD	V
V_{L2}	Input mode 2 voltage	22kΩ ± 5% to AGND	0.12*GVDD	0.15*GVDD	0.2*GVDD	V
V_{L3}	Input mode 3 voltage	100kΩ ± 5% to AGND	0.27*GVDD	0.33*GVDD	0.4*GVDD	V
V_{L4}	Input mode 4 voltage	Hi-Z	0.45*GVDD	0.5*GVDD	0.55*GVDD	V
V_{L5}	Input mode 5 voltage	100kΩ ± 5% to GVDD	0.6*GVDD	0.66*GVDD	0.73*GVDD	V
V_{L6}	Input mode 6 voltage	22kΩ ± 5% to GVDD	0.77*GVDD	0.85*GVDD	0.9*GVDD	V
V_{L7}	Input mode 7 voltage	Tied to GVDD	0.94*GVDD		GVDD	V
R_{PU}	Input pullup resistance	To GVDD	80	100	120	kΩ
R_{PD}	Input pulldown resistance	To AGND	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (FG, nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5V	–1		1	µA
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5mA, SDO_VSEL = 0	2.5		AVDD	V
V_{OH}	Output logic high voltage	I_{OP} = 5mA, SDO_VSEL = 1, V_{VM} > 6V	4		GVDD	V

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Output logic low leakage current	V_{OP} = 0V	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6V, I_{OUT} = 1A, T_A = 25°C		400	505	mΩ
		V_{VM} < 6V, I_{OUT} = 1A, T_A = 25°C		407	515	mΩ
		V_{VM} > 6V, I_{OUT} = 1A, T_J = 150°C		690	790	mΩ
		V_{VM} < 6V, I_{OUT} = 1A, T_J = 150°C		705	810	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24V, SLEW = 00b or SLEW pin tied to AGND, I_{OUTx} = 1A	630	1100	1760	V/us
		V_{VM} = 24V, SLEW = 01b or SLEW pin to Hi-Z, I_{OUTx} = 1A	260	500	900	V/us
		V_{VM} = 24V, SLEW = 10b or SLEW pin to 47kΩ +/- 5% to GVDD, I_{OUTx} = 1A	135	250	455	V/us
		V_{VM} = 24V, SLEW = 11b or SLEW pin tied to GVDD, I_{OUTx} = 1A	22	60	90	V/us
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24V, SLEW = 00b or SLEW pin tied to AGND, I_{OUTx} = 1A	500	1100	1760	V/us
		V_{VM} = 24V, SLEW = 01b or SLEW pin to Hi-Z, I_{OUTx} = 1A	240	500	845	V/us
		V_{VM} = 24V, SLEW = 10b or SLEW pin to 47kΩ +/- 5% to GVDD, I_{OUTx} = 1A	120	250	490	V/us
		V_{VM} = 24V, SLEW = 11b or SLEW pin tied to GVDD, I_{OUTx} = 1A	30	50	85	V/us
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1			2	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24V, SLEW = 00b or SLEW pin tied to AGND, HS driver ON to LS driver OFF		65	150	ns
		V_{VM} = 24V, SLEW = 01b or SLEW pin to Hi-Z, HS driver ON to LS driver OFF		100	250	ns
		V_{VM} = 24V, SLEW = 10b or SLEW pin to 47kΩ +/- 5% to GVDD, HS driver ON to LS driver OFF		100	250	ns
		V_{VM} = 24V, SLEW = 11b or SLEW pin tied to GVDD, HS driver ON to LS driver OFF		250	550	ns
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{VM} = 24V, PWM = 1 to OUTx transisition, SLEW = 00b or SLEW pin tied to AGND		35	85	ns
		V_{VM} = 24V, PWM = 1 to OUTx transisition, SLEW = 01b or SLEW pin to Hi-Z		40	100	ns
		V_{VM} = 24V, PWM = 1 to OUTx transisition, SLEW = 10b or SLEW pin to 47kΩ +/- 5% to GVDD		45	140	ns
		V_{VM} = 24 V, PWM = 1 to OUTx transisition, SLEW = 11b or SLEW pin tied to GVDD		1200	1900	ns
t_{MIN_PULSE}	Minimum output pulse width	SLEW = 00b or SLEW pin tied to AGND	110			ns
G_{CSA_ERR}	Current sense gain error	T_J = 25°C, 0A ≤ LS FET Current ≤ 2A (Current direction from PGND to OUTx)	-4		4	%

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{CSA_ERR}	Current sense gain error	0A ≤ LS FET Current ≤ 2A (Current direction from PGND to OUTx)	-6		6	%
CURRENT SENSE OUTPUT (SO)						
G_{CSA}	Current sense gain			0.4		V/A
G_{CSA}	Current sense gain			1		V/A
G_{CSA}	Current sense gain			2.5		V/A
G_{CSA}	Current sense gain			5		V/A
G_{CSA_ERR}	Current sense gain error	LS FET Current < 2A or 2A < LS FET Current < 4A; (Current direction from OUTx to PGND)		±6		%
FS_{POS}	Full scale positive current measurement	Current direction from PGND to OUTx in the LS FET	2			A
FS_{NEG}	Full scale negative current measurement	Current direction from OUTx to PGND in the LS FET			-3.5	A
V_{LINEAR}	SOX output voltage linear range		0.25		3	V
I_{OFFSET}	Current sense offset	Phase current = 0A		±10		mA
t_{SET}	Settling time to ±1%, 30pF	Step on SOX = 1.2V			1	µs
HALL COMPARATORS						
V_{ICM}	Input Common Mode Voltage (Hall)		0.5		GVDD – 1.2	V
V_{HYS}	Voltage hysteresis (SPI Device)	HALL_HYS = 0	1.5	5	8.5	mV
		HALL_HYS = 1	35	50	80	mV
	Voltage hysteresis (HW Device)		1.5	5	8.2	mV
ΔV_{HYS}	Hall comparator hysteresis difference	Between Hall A, Hall B and Hall C comparator	–12		12	mV
$V_{H(MIN)}$	Minimum Hall Differential Voltage		40			mV
I_I	Input leakage current	HPX = HNX = 0 V	–1		1	µA
t_{HDG}	Hall deglitch time		0.6	1.15	1.7	µs
PULSE-BY-PULSE CURRENT LIMIT						
V_{LIM}	Voltage on ILIMIT pin for cycle by cycle current limit		VAVDD/2		VAVDD/2 - 0.25	V
V_{LIM_DIS}	Voltage on ILIMIT pin for disabling cycle by cycle current limit		VAVDD		GVDD	V
I_{LIMIT}	Current limit corresponding to VLIM pin voltage range		0		4	A
I_{LIM_AC}	Current limit accuracy	VREF = 3.3V, ILIMIT > 1A	–6		6	%
I_{LIM_AC}	Current limit accuracy	VREF = 3.3V, 0.5 A < ILIMIT < 1A	–10		10	%
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 00b, HW variant		1.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 01b		2.25		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 10b		2.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 11b		3.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 00b, HW variant		5.5		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 01b		6		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 10b		6.5		µs

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 11b		7.5		µs
ADVANCE ANGLE						
θ_{ADV}	Advance Angle Setting (SPI Device)	ADVANCE_LVL = 000 b		0	1	°
		ADVANCE_LVL = 001 b	3	4	5	°
		ADVANCE_LVL = 010 b	6	7	8	°
		ADVANCE_LVL = 011 b	10	11	12	°
		ADVANCE_LVL = 100 b	13.5	15	16.5	°
		ADVANCE_LVL = 101 b	18	20	22	°
		ADVANCE_LVL = 110 b	22.5	25	27.5	°
		ADVANCE_LVL = 111 b	27	30	33	°
θ_{ADV}	Advance Angle Setting (HW Device)	Advance pin tied to AGND		0	1	°
		Advance pin tied to 22 kΩ ± 5% to AGND	3	4	5	°
		Advance pin tied to 100 kΩ ± 5% to AGND	10	11	12	°
		Advance pin tied to Hi-Z	13.5	15	16.5	°
		Advance pin tied to 100 kΩ ± 5% to GVDD	18	20	22	°
		Advance pin tied to 22 kΩ ± 5% to GVDD	22.5	25	27.5	°
		Advance pin tied to Tied to GVDD	27	30	33	°
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.2	4.35	4.5	V
		VM falling	4.0	4.15	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	65	200	415	mV
t_{UVLO}	Supply undervoltage deglitch time		3	6	10	µs
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_EN = 1, OVP_SEL = 0	60	62.5	65	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	58	61	63.5	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	32	33	34	V
V_{OVP_HYS}	Supply overvoltage protection (OVP) (SPI Device)	Rising to falling threshold, OVP_SEL = 1	0.74	0.8	0.85	V
		Rising to falling threshold, OVP_SEL = 0	1.35	1.45	1.55	V
t_{OVP}	Supply overvoltage deglitch time		2.5	6.5	12	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.1	2.7	3.2	V
		Supply falling	1.8	2.45	2.95	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	105	150	200	mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
V_{GVDD_UV}	GVDD regulator undervoltage lockout	Supply rising	3.1	3.3	3.5	V
V_{GVDD_UV}	GVDD regulator undervoltage lockout	Supply falling	2.9	3.1	3.3	V
$V_{GVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	145	190	265	mV

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 00b or 01b	4.5		9	A
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 10b or 11b	2.5		5	A
I_{OCP}	Overcurrent protection trip point (HW Device)	OCP pin tied to AGND or OCP pin HiZ	4.5		9	A
I_{OCP}	Overcurrent protection trip point (HW Device)	OCP tied to GVDD	2.5		5	A
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b	0.2	0.6	1.2	µs
		OCP_DEG = 01b	0.6	1.25	1.8	µs
		OCP_DEG = 10b	1	1.6	2.5	µs
		OCP_DEG = 11b	1.4	2	3	µs
	Overcurrent protection deglitch time (HW Device)		0.6	1.25	2	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_TRETRY=0	4	5	6	ms
		OCP_TRETRY=1	425	500	575	ms
t_{RETRY}	Overcurrent protection retry time (HW Device)		4	5	6	ms
t_{MTR_LOCK}	Motor lock detection time (SPI Device)	MOTOR_LOCK_TDET = 11b	225	250	275	ms
		MOTOR_LOCK_TDET = 10b	450	500	550	ms
		MOTOR_LOCK_TDET = 01b	900	1000	1100	ms
		MOTOR_LOCK_TDET = 00b	4500	5000	5500	ms
t_{MTR_LOCK}	Motor lock detection time (HW Device)		900	1000	1100	ms
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (SPI Device)	MOTOR_LOCK_RETRY = 1b	1.8	2	2.2	s
		MOTOR_LOCK_RETRY = 0b	9	10	11	s
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (HW Device)		9	10	11	s
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	160	170	180	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	175	185	195	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	25	30	35	°C

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	400			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			25	ns
t_{EN_SDO}	SDO enable delay time			50	ns

		MIN	NOM	MAX	UNIT
t_{DIS_SDO}	SDO disable delay time			50	ns

6.7 SPI Slave Mode Timings

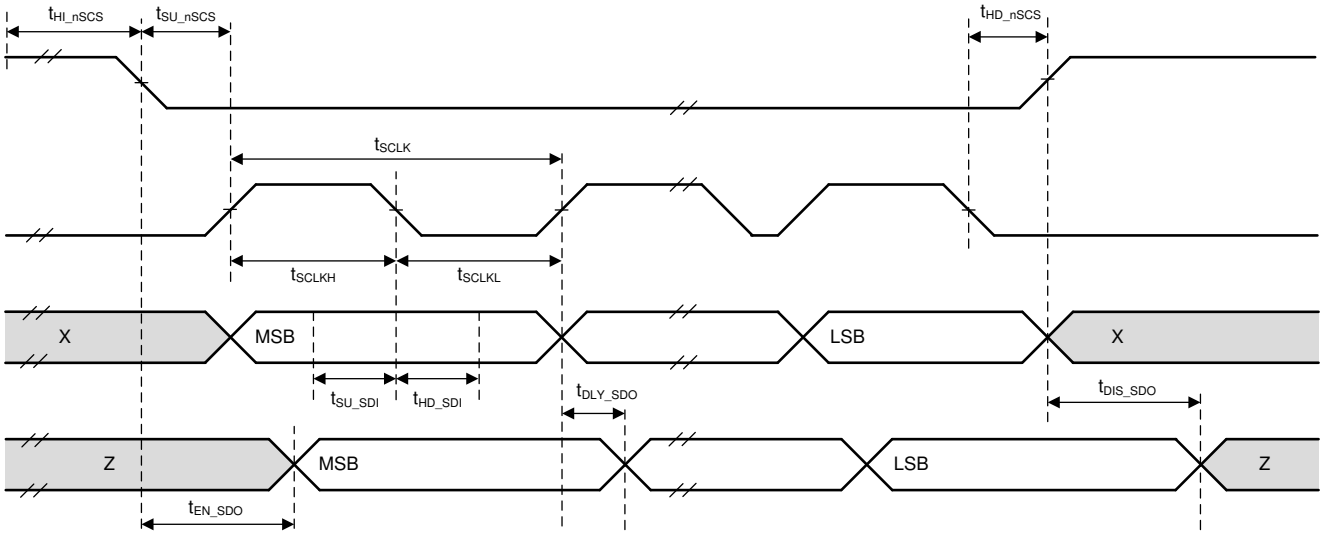


Figure 6-1. SPI Secondary Mode Timings

7 Detailed Description

7.1 Overview

The MCT8376Z-Q1 device is an integrated 400mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, and linear regulator for the external load. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events, and protect against dv/dt parasitic turnon of the internal power MOSFET.

The MCT8376Z-Q1 device integrates three-phase sensored trapezoidal commutation using analog or digital hall sensors for position detection.

In addition to the high level of device integration, the MCT8376Z-Q1 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD and GVDD undervoltage lockout (AVDD_UV, GVDD_UV), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The MCT8376Z-Q1 device in a VQFN surface-mount package. The VQFN package size is 6 mm × 5 mm.

7.2 Functional Block Diagram

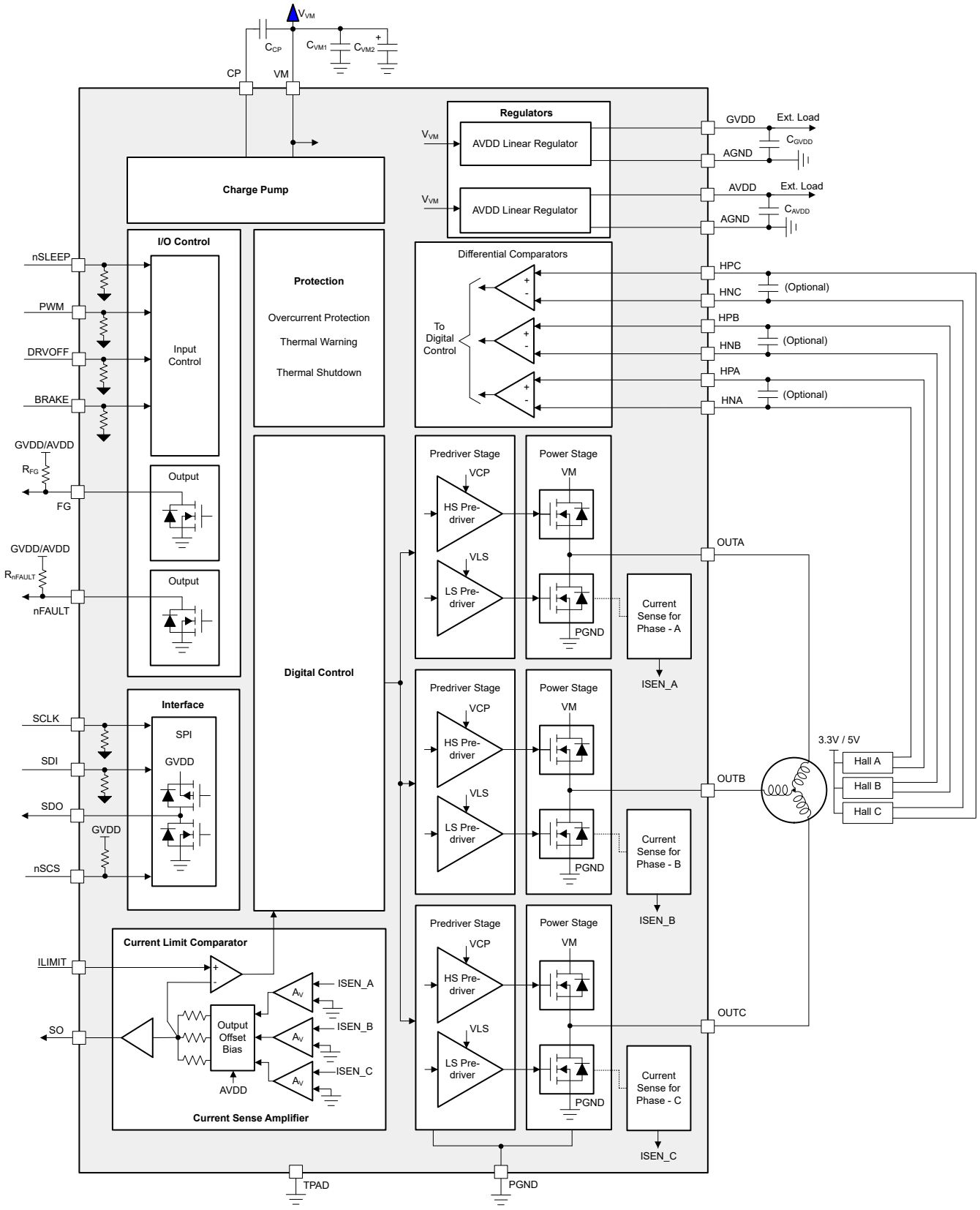


Figure 7-1. MCT8376ZS-Q1 Block Diagram

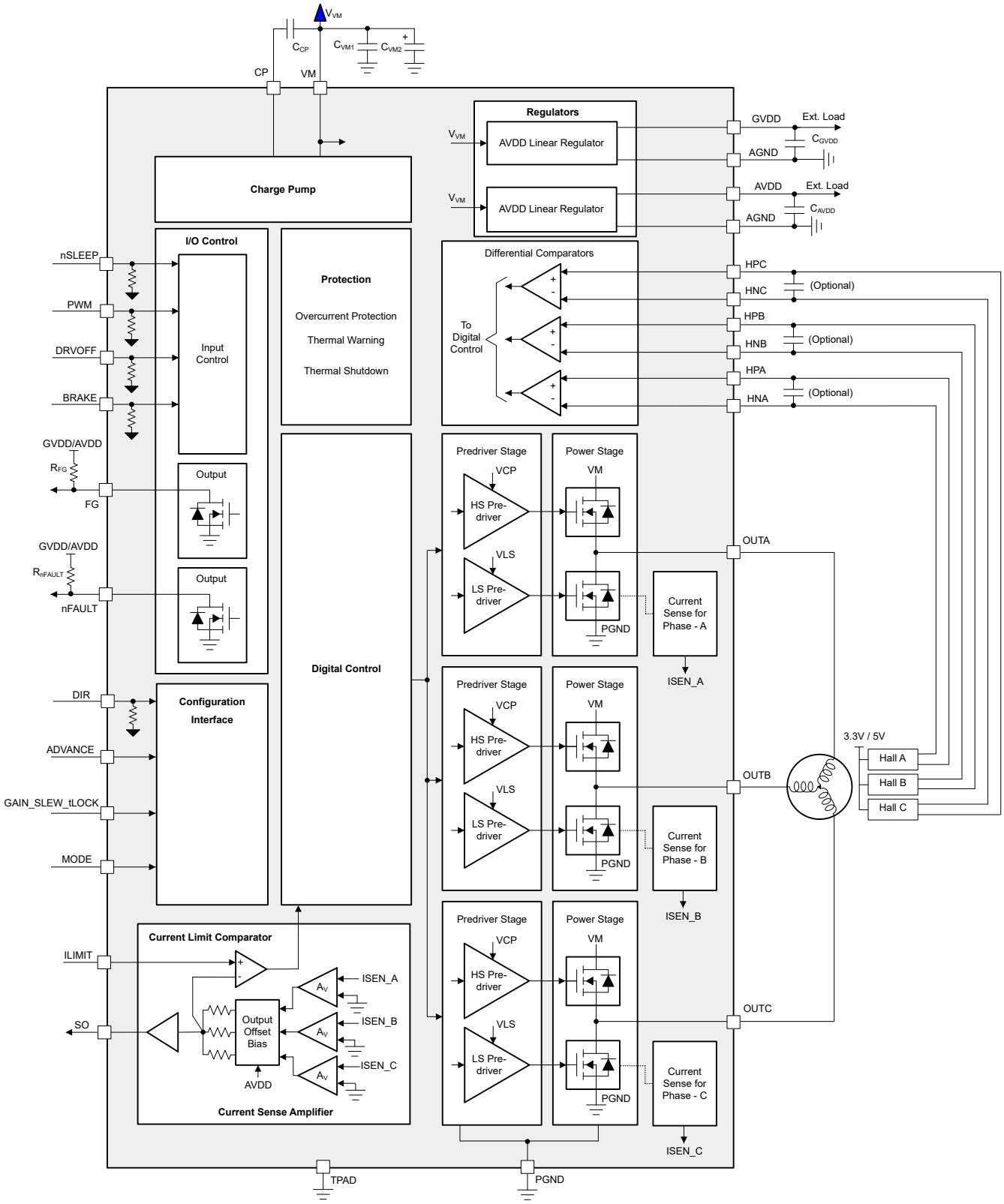


Figure 7-2. MCT8376ZH-Q1 Block Diagram

7.3 Feature Description

Table 7-1 lists the recommended values of the external components for the driver.

Table 7-1. MCT8376Z-Q1 External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	≥ 10µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X5R or X7R, 16V, 0.1µF capacitor
C_{GVDD}	GVDD	AGND	X5R or X7R, 1µF, ≥ 10V
C_{AVDD}	AVDD	AGND	X5R or X7R, 0.1µF, ≥ 6.3V
R_{nFAULT}	AVDD/GVDD	nFAULT	5.1kΩ, Pullup resistor
R_{FG}	AVDD/GVDD	nFAULT	5.1kΩ, Pullup resistor
$R_{ADVANCE}$	ADVANCE	AGND or GVDD	MCT8376ZH-Q1 hardware interface
R_{MODE}	MODE	AGND or GVDD	MCT8376ZH-Q1 hardware interface
$R_{GAIN\_SLEW\_tLOCK}$	GAIN_SLEW_tLOCK	AGND or GVDD	MCT8376ZH-Q1 hardware interface

Note

TI recommends to connect pull up on nFAULT even if nFAULT is not used to avoid undesirable entry into internal test mode. If external supply is used to pull up nFAULT, make sure that nFAULT is pulled to >2.2V on power up.

7.3.1 Output Stage

The MCT8376Z-Q1 device consists of an integrated 400mΩ (combined high-side and low-side FET's on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FET's across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

7.3.2 PWM Control Mode (1x PWM Mode)

The MCT8376Z-Q1 family of devices provides seven different control modes to support various commutation and control methods. The MCT8376Z-Q1 device provides a 1x PWM control mode for driving the BLDC motor in trapezoidal current-control mode. The MCT8376Z-Q1 device uses 6-step block commutation tables that are stored internally. This feature lets a three-phase BLDC motor be controlled using a single PWM sourced from a simple controller. The PWM is applied on the PWM pin and determines the output frequency and duty cycle of the half-bridges.

The MCT8376Z-Q1 family of devices supports both analog and digital hall inputs by changing mode input setting. Differential hall inputs should be connected to HPx and HNx pins (see Figure 7-3). Digital hall inputs should be connected to the HPx pins while keeping the HNx pins floating (see Figure 7-4).

The half-bridge output states are managed by the HPA, HNA, HPB, HNB, HPC and HNC pins in analog mode and HPA, HPB, HPC in digital mode which are used as state logic inputs. The state inputs are the position feedback of the BLDC motor. The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) as shown in Table 7-2.

Table 7-2. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 1	Connected to AGND	Analog Hall Input	Asynchronous	ASR and AAR Disabled

Table 7-2. PWM_MODE Configuration (continued)

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 2	Connected to AGND with R_{MODE1}	Digital Hall Input	Asynchronous	ASR and AAR Disabled
Mode 3	Connected to AGND with R_{MODE2}	Analog Hall Input	Synchronous	ASR and AAR Disabled
Mode 4	Hi-Z	Digital Hall Input	Synchronous	ASR and AAR Disabled
Mode 5	Connected to GVDD with R_{MODE2}	Analog Hall Input	Synchronous	ASR and AAR Enabled
Mode 6	Connected to GVDD with R_{MODE1}	Digital Hall Input	Synchronous	ASR and AAR Enabled
Mode 7	Connected to GVDD			

Note

Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set PWM to a low level before changing the MODE pin or PWM_MODE register.

7.3.2.1 Analog Hall Input Configuration

Figure 7-3 shows the connection of Analog Hall inputs to the driver. Analog hall elements are fed to the hall comparators, which zero crossing is used to generate the commutation logic.

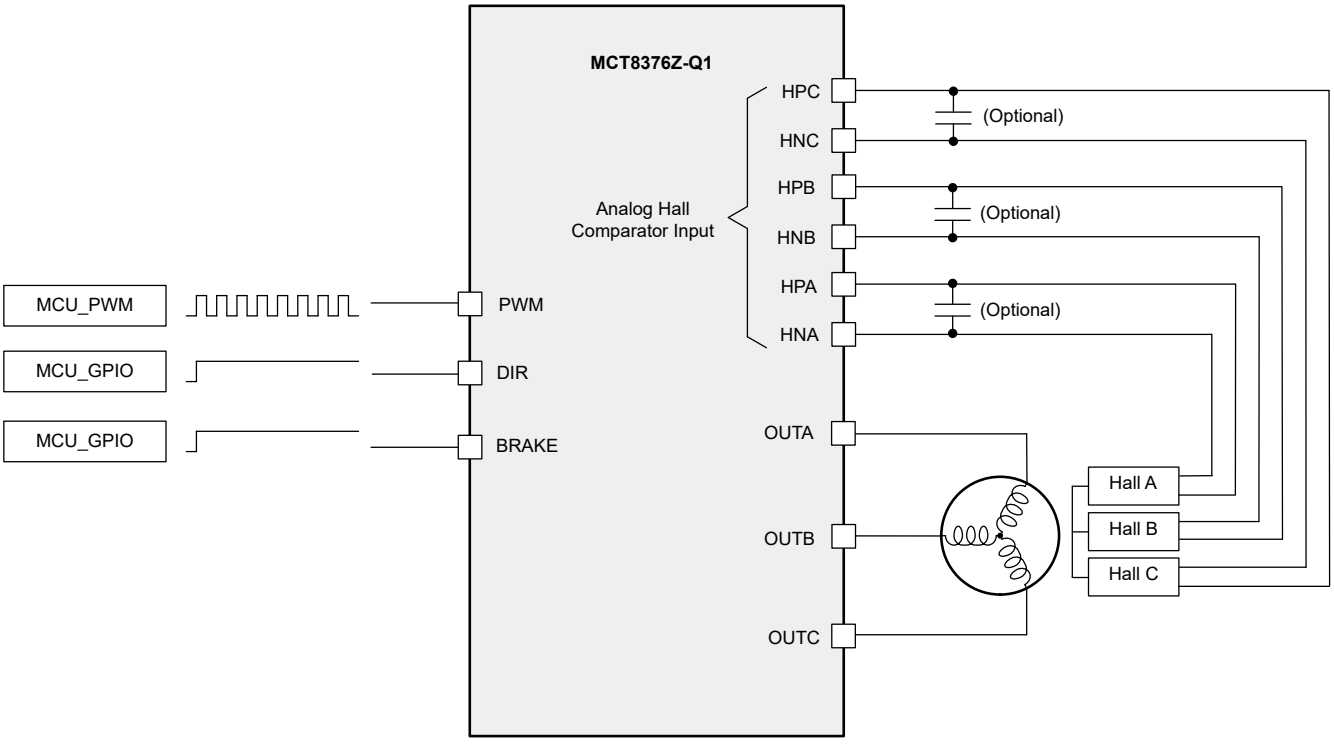


Figure 7-3. 1x PWM Mode with Analog Hall Input

Note

Texas Instruments recommends motor direction (DIR) change when the motor is stationary.

7.3.2.2 Digital Hall Input Configuration

Figure 7-4 shows the connection of Digital Hall inputs to the driver.

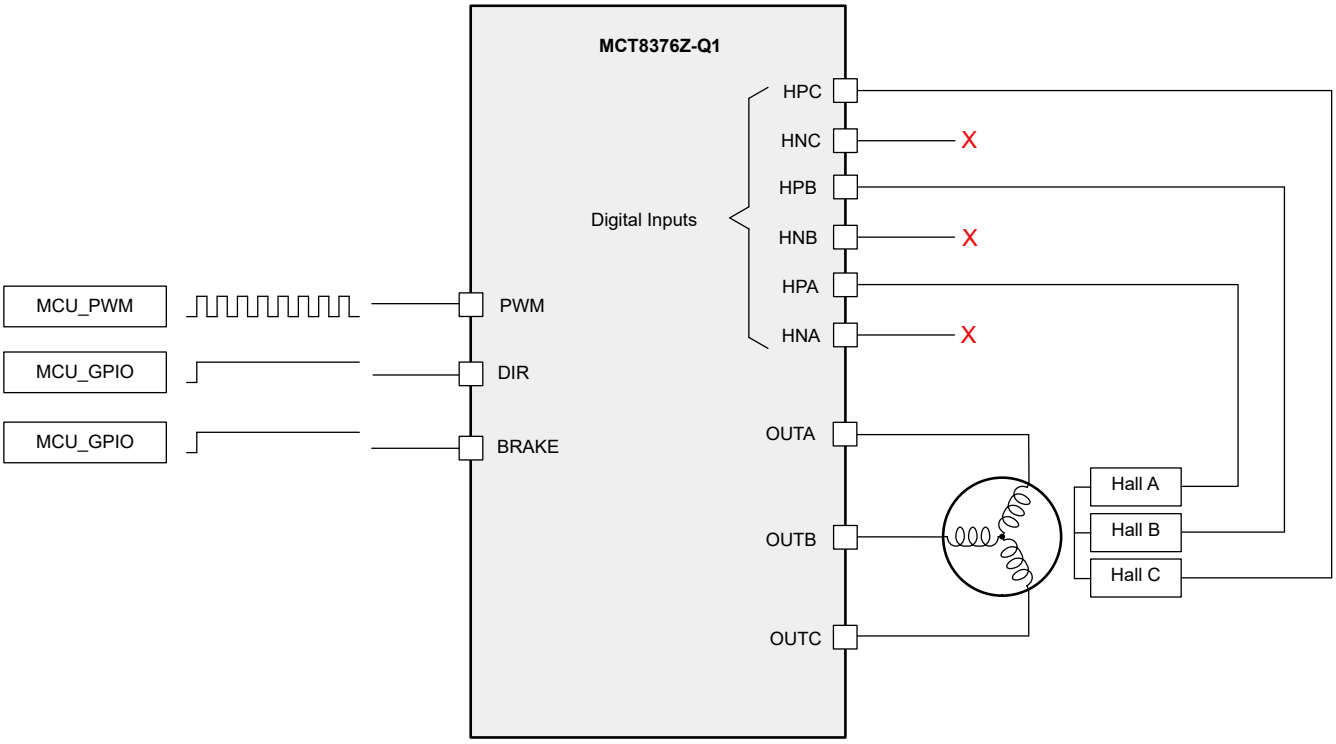


Figure 7-4. 1x PWM Mode with Digital Hall Input

7.3.2.3 Asynchronous Modulation

The DIR pin controls the direction of BLDC motor in either clockwise or counter-clockwise direction. Tie the DIR pin low if this feature is not required.

The BRAKE input halts the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled high. This brake is independent of the states of the other input pins. Tie the BRAKE pin low if this feature is not required.

Table 7-3 shows the configuration in 1x PWM mode with asynchronous modulation.

Table 7-3. Asynchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

7.3.2.4 Synchronous Modulation

Table 7-4 shows the configuration in 1x PWM mode with synchronous modulation.

Table 7-4. Synchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

7.3.2.5 Motor Operation

Figure 7-5 and Figure 7-6 shows the BLDC motor commutation with direction setting (DIR) as 0 and 1 respectively.

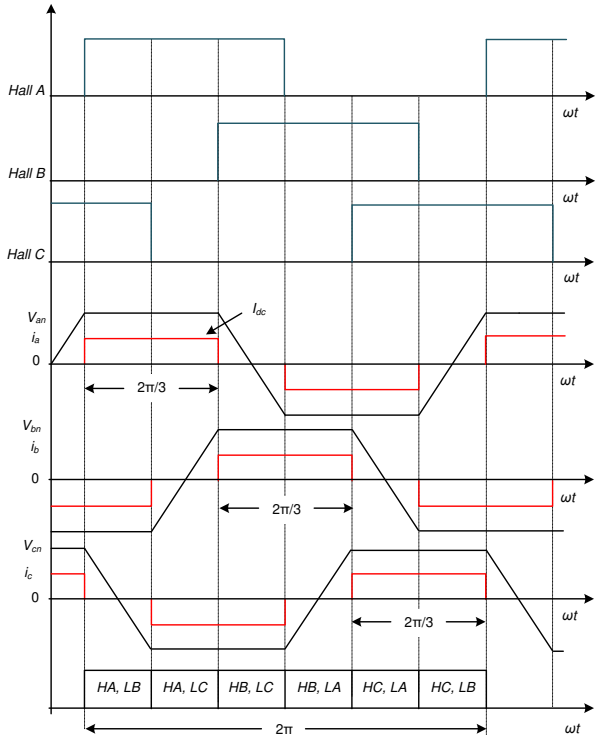


Figure 7-5. BLDC Motor Commutation with DIR = 0

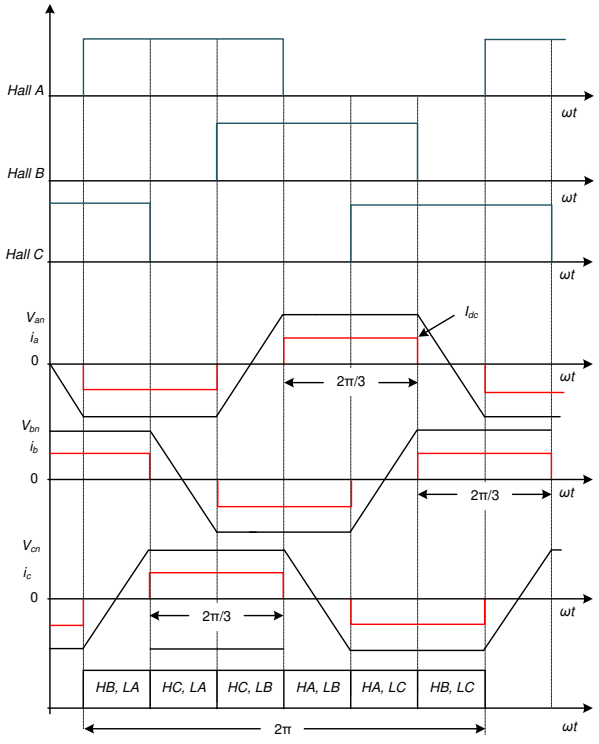


Figure 7-6. BLDC Motor Commutation with DIR = 1

7.3.3 Device Interface Modes

The MCT8376Z-Q1 family of devices supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate one interface version and potentially switch to another with minimal modifications to a design.

7.3.3.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the MCT8376Z-Q1. This support lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin can be configured to either open-drain or push-pull through SDO_MODE.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication.

For more information on the SPI, see Section 7.5.

7.3.3.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are ADVANCE, MODE, GAIN_SLEW_tLOCK and DIR. DIR pin is two level input (logic levels) where as ADVANCE, MODE, GAIN_SLEW_tCLK are seven level configuration inputs.

The hardware interface lets the application designer to configure the most common device by tying the pin logic high or logic low, or with a simple pullup or pull-down resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The MODE pin configures the PWM control mode.
- The GAIN_SLEW_tLOCK pin configures the CSA GAIN, output voltage slew rate and motor lock detection time.
- The ADVANCE pin configures the lead angle of the output with respect to hall signals.
- The DIR pin is used to configure the direction of rotation of the motor.

For more information on the hardware interface, see Section 7.3.9.

Note

VCC is external pull up voltage

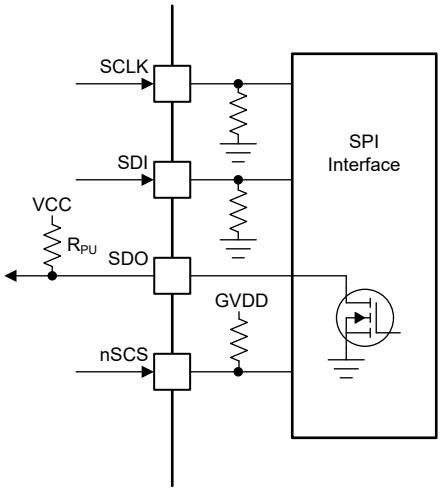


Figure 7-7. MCT8376ZS-Q1 SPI

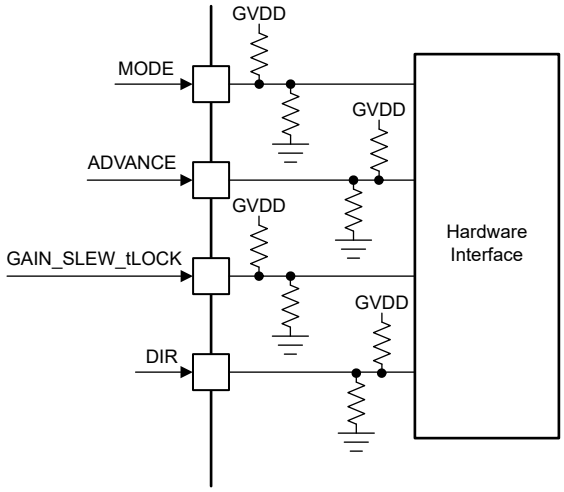


Figure 7-8. MCT8376ZH-Q1 Hardware Interface

7.3.4 AVDD and GVDD Linear Voltage Regulator

The MCT8376Z-Q1 family of devices integrates 3.3V and 5V linear regulators, making them available for external circuitry. The AVDD and GVDD regulators power the internal digital circuitry of the device and can also supply voltage to a low-power MCU or other circuitry supporting low current (up to 30mA). Place an X5R or X7R, 0.1µF, 6.3V ceramic capacitor near the AVDD pin to bypass the AVDD regulator's output, and route the capacitor directly back to the adjacent AGND ground pin. Place an X5R or X7R, 1µF, 10V ceramic capacitor near the GVDD pin to bypass the GVDD regulator's output, and connect directly to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3V.

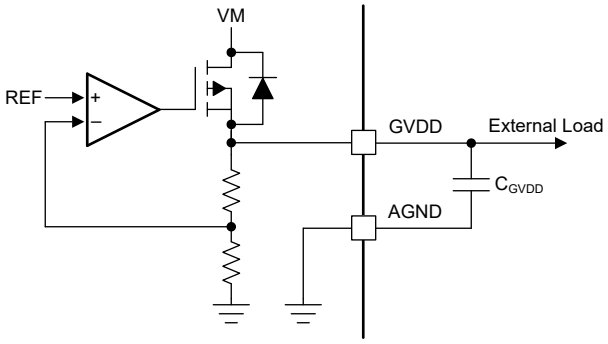


Figure 7-9. GVDD Linear Regulator Block Diagram

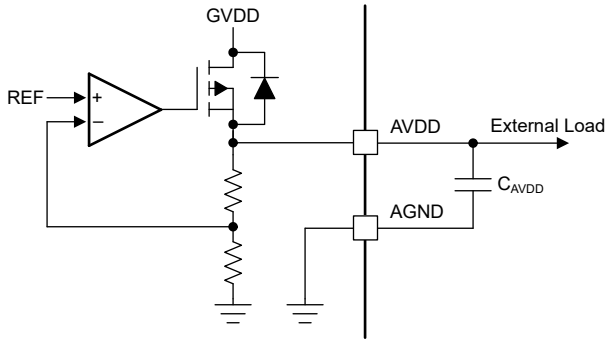


Figure 7-10. AVDD Linear Regulator Block Diagram

Use Equation 1 and Equation 2 to calculate the power dissipated in the device by the AVDD and GVDD linear regulator with VM as supply.

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

$$P = (V_{VM} - V_{GVDD}) \times I_{GVDD} \quad (2)$$

For example, at a V_{VM} of 24V, drawing 20mA out of AVDD results in power dissipation as shown in Equation 3.

$$P = (24V - 3.3V) \times 20mA = 414mW \quad (3)$$

Note

The combined external current support from both the linear regulators AVDD and GVDD is limited to 30mA. If 30mA of external load is connected to AVDD, then do not connect any external load to GVDD and vice versa.

7.3.5 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The MCT8376Z-Q1 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires one external capacitors for operation. See the block diagram, pin descriptions and see section (Section 7.3) for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low or during an over temperature shutdown.

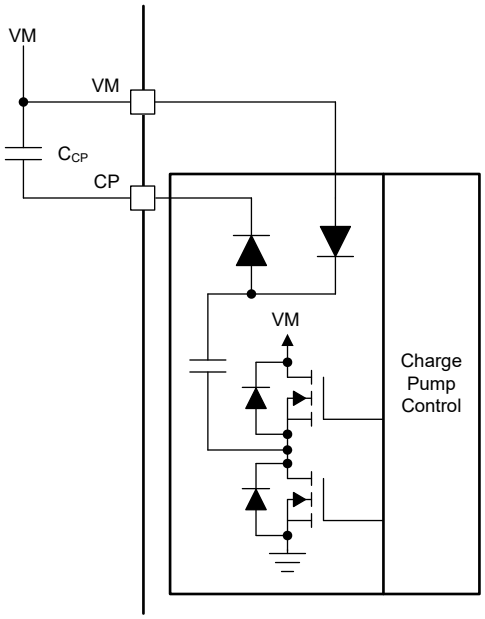


Figure 7-11. MCT8376Z-Q1 Charge Pump

7.3.6 Slew Rate Control

An adjustable gate-drive current control actively manages the MOSFETs in the half-bridges to achieve slew rate control. The MOSFET VDS slew rates critically influence the optimization of radiated emissions, the energy and duration of diode recovery spikes, and the switching voltage transients caused by parasitics. The rate of gate charge to the internal MOSFETs predominantly determines these slew rates, as shown in Figure 7-12.

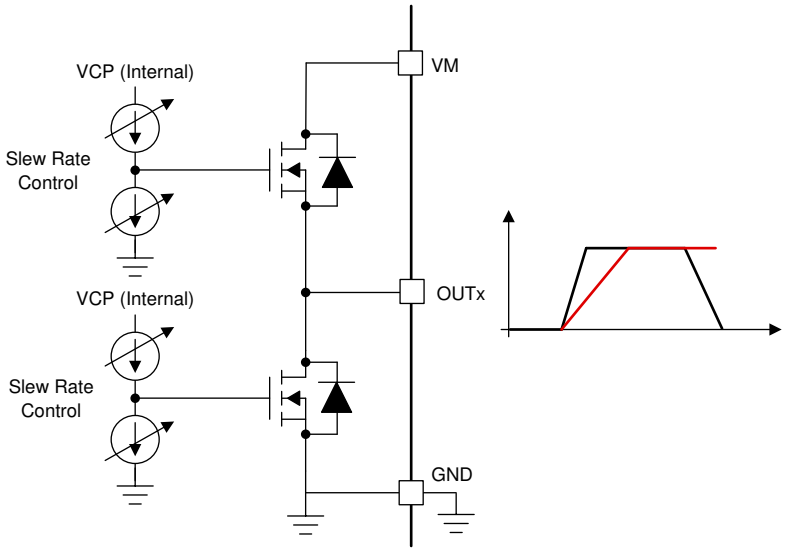


Figure 7-12. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted by the GAIN_SLEW_tLOCK pin as per Table 7-5 in hardware device variant or by using the SLEW bits in SPI device variant. Each half-bridge can be selected to either of a slew rate setting of 1.1V/ns, 0.5V/ns, 0.25V/ns, or 0.05V/ns in an SPI device. Each half-bridge can be selected to either a slew rate setting of 1.1V/ns or 0.25V/ns in a hardware device. The slew rate is calculated by the rise time and fall time of the voltage on the OUTx pin as shown in Figure 7-13.

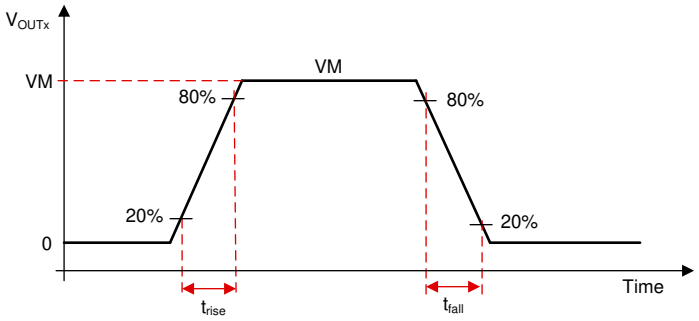


Figure 7-13. Slew Rate Timings

Note

The SLEW pin is sensed only during power up and the MCT8376ZH-Q1 device doesn't support slew rate change during operation. Slew rate can be changed during operation through register write in MCT8376ZS-Q1 device. TI recommends not to change the slew rate during operation.

7.3.7 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are maintained to avoid any shoot-through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and maintaining that VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in Figure 7-14 and Figure 7-15.

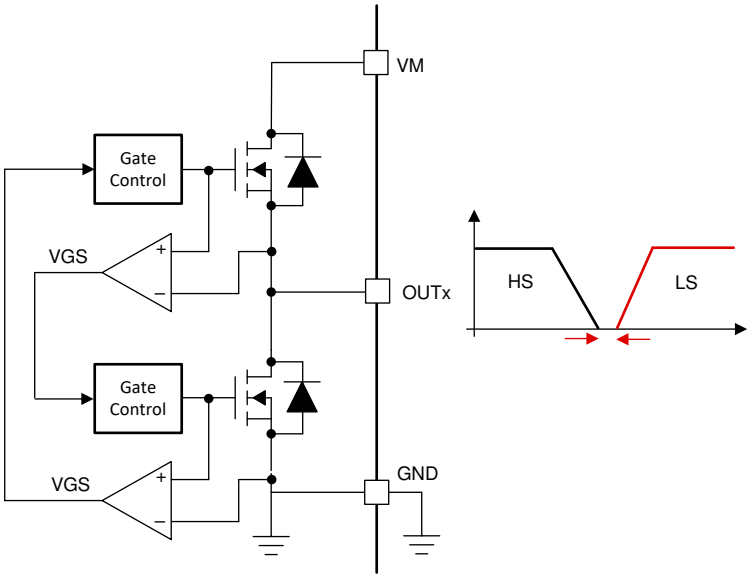


Figure 7-14. Cross Conduction Protection

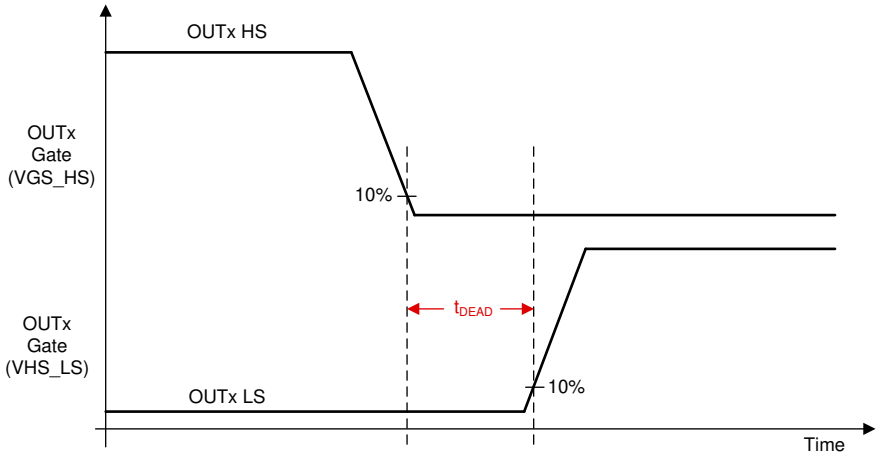


Figure 7-15. Dead Time

7.3.8 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage.

Note

During current limit mode or active demag mode a small digital delay is added as the input command propagates through the device, and user may see up to 300ns more delay during these modes.

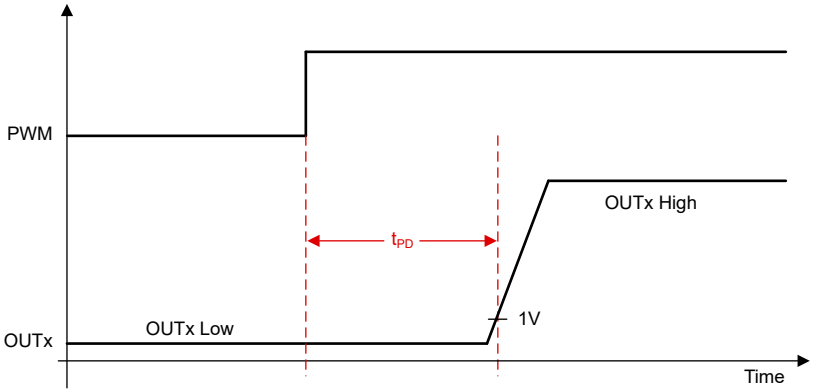


Figure 7-16. Propagation Delay Timing

7.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

7.3.9.1 Logic Level Input Pin (Internal Pulldown)

Figure 7-17 shows the input structure for the logic level pins, BRAKE, DIR, DRVOFF, nSLEEP, PWM, SCLK and SDI. The input can be with a voltage or external resistor. TI recommends to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

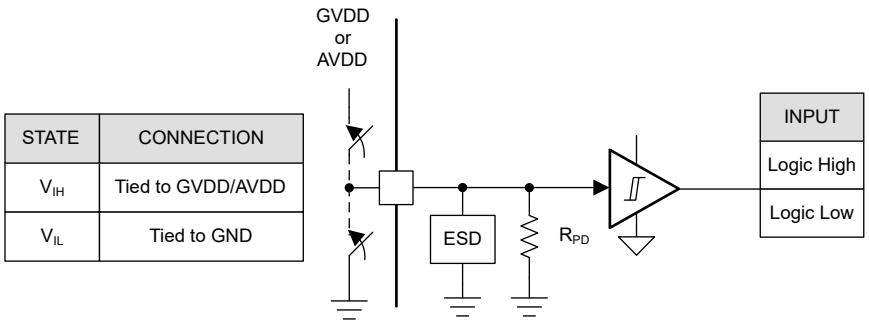


Figure 7-17. Logic-Level Input Pin Structure

7.3.9.2 Logic Level Input Pin (Internal Pullup)

Figure 7-18 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

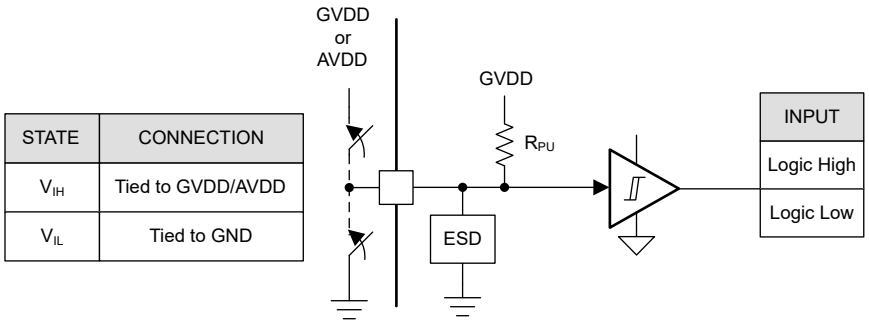


Figure 7-18. Logic nSCS

7.3.9.3 Open Drain Pin

Figure 7-19 shows the structure of the open-drain output pins, nFAULT, FGOUT and SDO in open drain mode. The open-drain output requires an external pullup resistor to function properly.

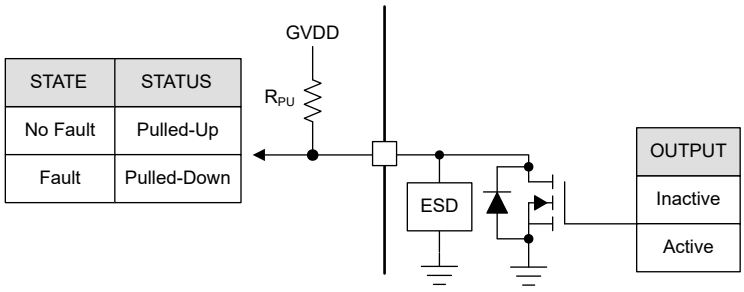


Figure 7-19. Open Drain

7.3.9.4 Push Pull Pin

Figure 7-20 shows the structure of SDO in push-pull mode. The SDO power supply in push pull mode can be selected to GVDD or AVDD by configuring SDO_VSEL.

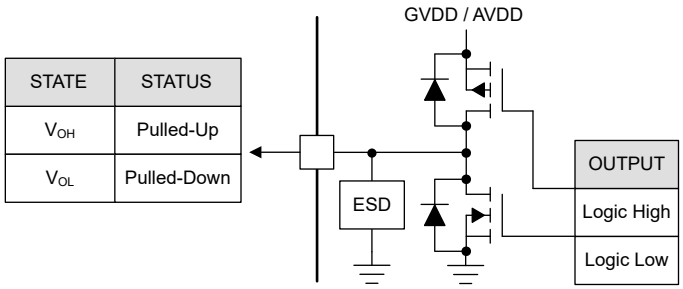


Figure 7-20. Push Pull

7.3.9.5 Seven Level Input Pin

Figure 7-21 shows the structure of the seven level input pins MODE, ADVANCE and GAIN_SLEW_tLOCK, on hardware interface devices. The input can be set with an external resistor.

STATE	RESISTANCE
V_{L1}	Tied to AGND
V_{L2}	22 kΩ ± 5% to AGND
V_{L3}	100 kΩ ± 5% to AGND
V_{L4}	Hi-Z (>2000 kΩ to AGND)
V_{L5}	100 kΩ ± 5% to GVDD
V_{L6}	22 kΩ ±5% to GVDD
V_{L7}	Tied to GVDD

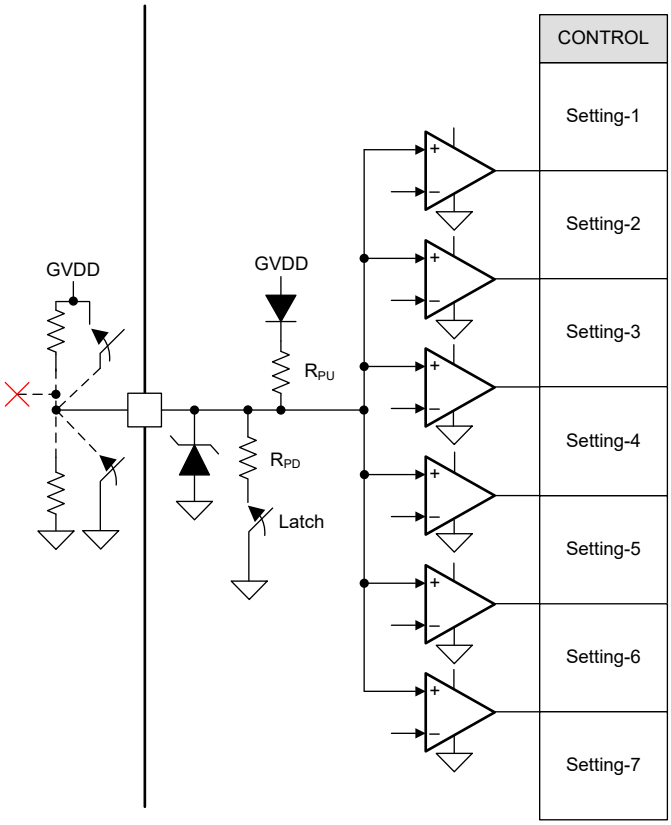


Figure 7-21. Seven Level Input Pin Structure

7.3.10 Current Sense Amplifier Output (SO)

The SO pin on the MCT8376Z-Q1 outputs an analog voltage proportional to current flowing in the low side FETs multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels which can be set by the GAIN pin (in hardware device variant) or the GAIN bits (in SPI device variant).

Figure 7-22 shows the internal architecture of the current sense amplifiers. The current sense is implemented with the sense FET on each low-side FET of the MCT8376Z-Q1 device. This current information is fed to the internal I/V converter, which generates the CSA output voltage on the SO pin based on the AVDD voltage and the Gain setting. The CSA output voltage can be calculated as :

$$V_{SO} = \left({}^{V_{AVDD}}/_{2}\right) + ((I_{OUTA} + I_{OUTB} + I_{OUTC}) \times GAIN/3) \quad (4)$$

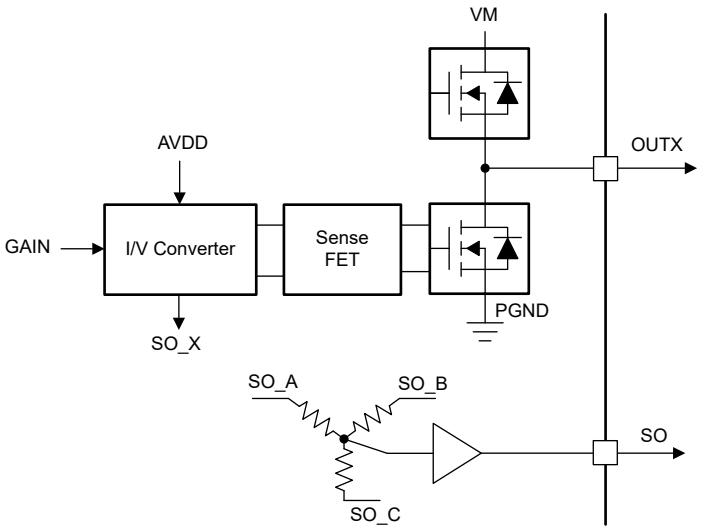


Figure 7-22. Integrated Current Sense Amplifier

The GAIN of the CSA can be adjusted by the GAIN_SLEW_tLOCK pin as per Table 7-5 in hardware device variant or by using the SLEW bits in SPI device variant. Each half-bridge can be selected to either of a slew rate setting of 1V/ns, 0.5V/ns, 0.25V/ns or 0.05V/ns in SPI device. Each half-bridge can be selected to either of a slew rate setting of 1.1V/ns or 0.25V/ns in hardware device. The slew rate is calculated by the rise time and fall time of the voltage on OUTx pin as shown in Figure 7-13.

Table 7-5. CSA GAIN, SLEW RATE, and LOCK DETCETION TIME setting in MCT8376ZH-Q1

Configuration	GAIN_SLEW_tLOCK Pin (Hardware Variant)	GAIN	SLEW	LOCK_DET_TIME
1	Connected to AGND	0.4V/A	1.1V/ns	500ms
2	Connected to AGND with R_{MODE1}	0.4V/A	1.1V/ns	5000ms
3	Connected to AGND with R_{MODE2}	0.4V/A	0.25V/ns	500ms
4	Hi-Z	0.4V/A	0.25V/ns	5000ms
5	Connected to GVDD with R_{MODE2}	2.5V/A	1.1V/ns	500ms
6	Connected to GVDD with R_{MODE1}	2.5V/A	1.1V/ns	5000ms
7	Connected to GVDD	2.5V/A	0.25V/ns	500ms

Note

The current sense amplifier supports only a low capacitive load at the output. TI recommends connecting the low pass filter with the resistor and capacitor on output of the current sense amplifier.

Note

The current sense amplifier supports dynamic gain change. The current sense amplifier supports dynamic gain change. The GAIN is sampled every 1ms through pin sensing in the HW variant and any GAIN change through SPI write (in the SPI variant). After receiving the GAIN change command, the new GAIN will be applied on the next rising edge of any PWM signal.

7.3.11 Active Demagnetization

MCT8376Z-Q1 family of devices has smart rectification features (active demagnetization) which decreases power losses in the device by reducing diode conduction losses. When this feature is enabled, the device

automatically turns ON the corresponding MOSFET whenever the device detects diode conduction. This feature can be configured with the MODE pins in hardware variants. In SPI device variants this can be configured through EN_ASR and EN_AAR bits. The smart rectification is classified into two categories of automatic synchronous rectification (ASR) mode and automatic asynchronous rectification (AAR) mode which are described in the sections below.

Note

In SPI device variants both bits, EN_ASR and EN_AAR need to be set to 1 to enable active demagnetization.

The MCT8376Z-Q1 device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS comparator compares with the ground (0V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. This comparator provides a reference point for the operation of active demagnetization features.

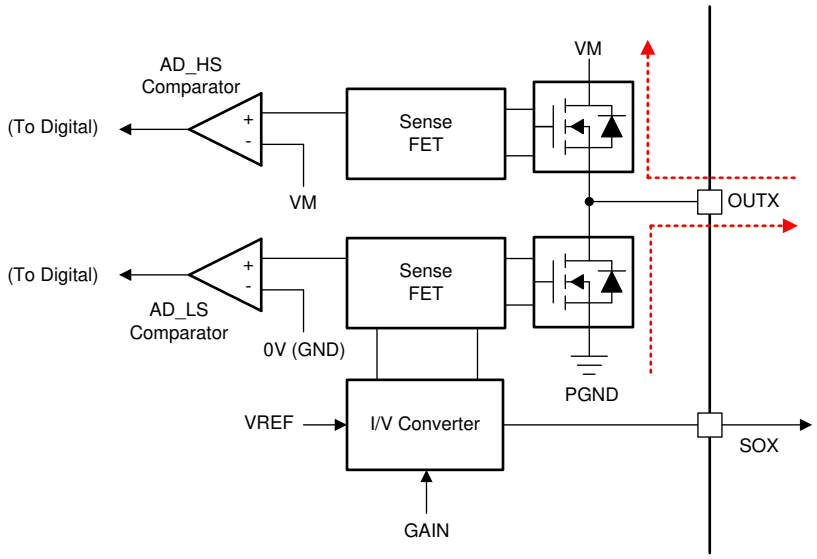


Figure 7-23. Active Demagnetization Operation

Table 7-6 shows the configuration of ASR and AAR mode in the MCT8376Z-Q1 device.

Table 7-6. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	ASR and AAR configuration	Hall Configuration	Modulation	ASR and AAR Mode
Mode 1	Connected to AGND	EN_ASR = 0, EN_AAR = 0	Analog Hall Input	Asynchronous	ASR and AAR Disabled
Mode 2	Connected to AGND with R_{MODE1}	EN_ASR = 0, EN_AAR = 0	Digital Hall Input	Asynchronous	ASR and AAR Disabled
Mode 3	Connected to AGND with R_{MODE2}	EN_ASR = 0, EN_AAR = 0	Analog Hall Input	Synchronous	ASR and AAR Disabled
Mode 4	Hi-Z	EN_ASR = 0, EN_AAR = 0	Digital Hall Input	Synchronous	ASR and AAR Disabled
Mode 5	Connected to GVDD with R_{MODE2}	EN_ASR = 1, EN_AAR = 1	Analog Hall Input	Synchronous	ASR and AAR Enabled
Mode 6	Connected to GVDD with R_{MODE1}	EN_ASR = 1, EN_AAR = 1	Digital Hall Input	Synchronous	ASR and AAR Enabled
Mode 7	Connected to GVDD				

Note

Active demagnetization disabled on an OCP event and a motor lock event.

7.3.11.1 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode is divided into two categories of ASR during commutation and ASR during PWM mode.

7.3.11.1.1 Automatic Synchronous Rectification in Commutation

Figure 7-24 shows the operation of active demagnetization during the BLDC motor commutation. As shown in Figure 7-24 (a), the current is flowing from HA to LC in one commutation state. During the commutation changeover as shown in Figure 7-24 (b), the HB switch is turned on, whereas the commutation current (due to motor inductance) in OUTA flows through the body diode of LA. This incorporates a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA for the commutation time as shown in Figure 7-24 (c).

Similarly the operation of high-side FET is realized in Figure 7-24 (d), (e) and (f).

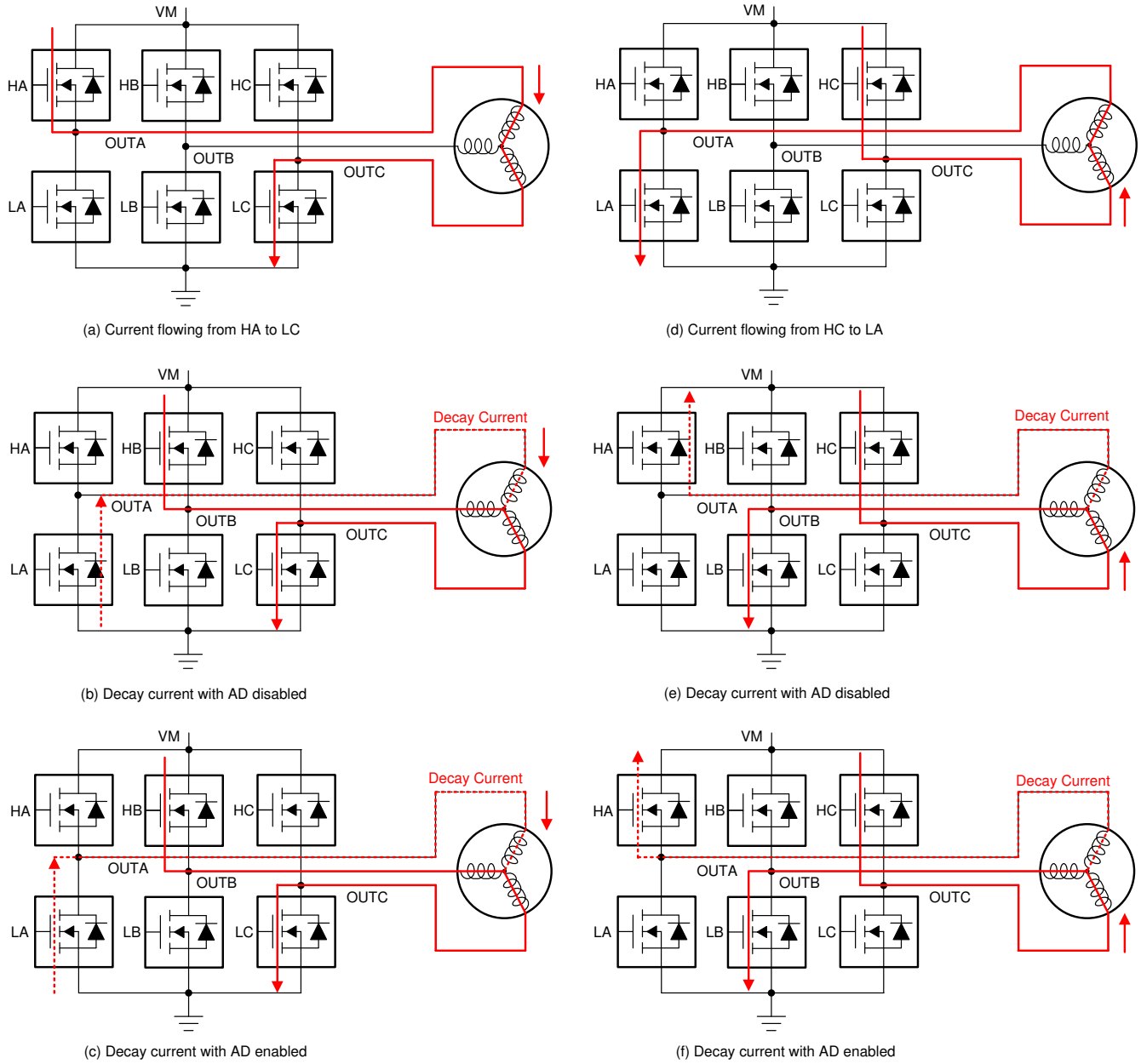
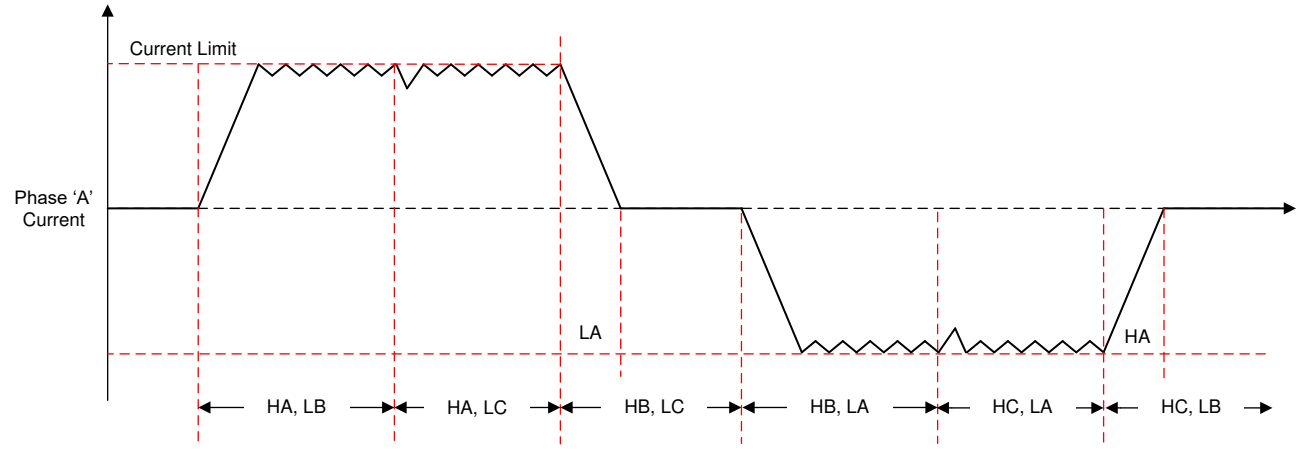


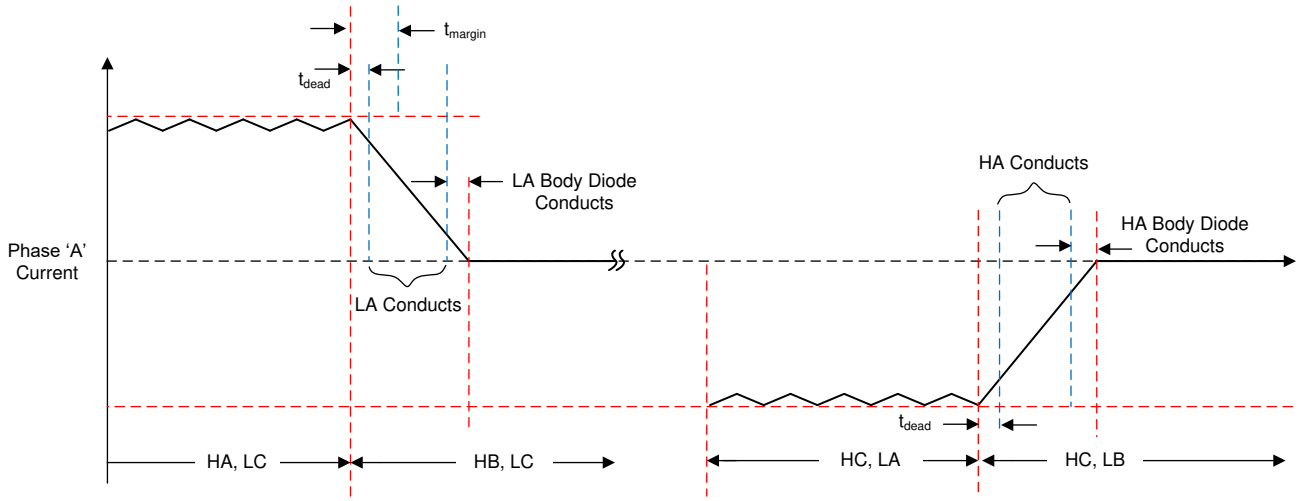
Figure 7-24. ASR in BLDC Motor Commutation

Figure 7-25 (a) shows the BLDC motor phase current waveforms for automatic synchronous rectification mode in BLDC motor operating with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

Figure 7-25 (b) shows the zoomed waveform of commutation cycle with details on the ASR mode start with margin time (t_{margin}) and ASR mode early stop due to active demag. comparator threshold and delays.



(a) Commutation current of Phase "A"



(b) Zoomed waveform of Active Demagnetization

Figure 7-25. Current Waveforms for ASR in BLDC Motor Commutation

7.3.11.1.2 Automatic Synchronous Rectification in PWM Mode

Figure 7-26 shows the operation of ASR in PWM mode. As shown in this figure, a PWM is applied only on the high-side FET, whereas the low-side FET is always off. During the PWM off time, current decays from the low-side FET which results in higher power losses. Therefore, this mode supports turning on the low-side FET during the low-side diode conduction.

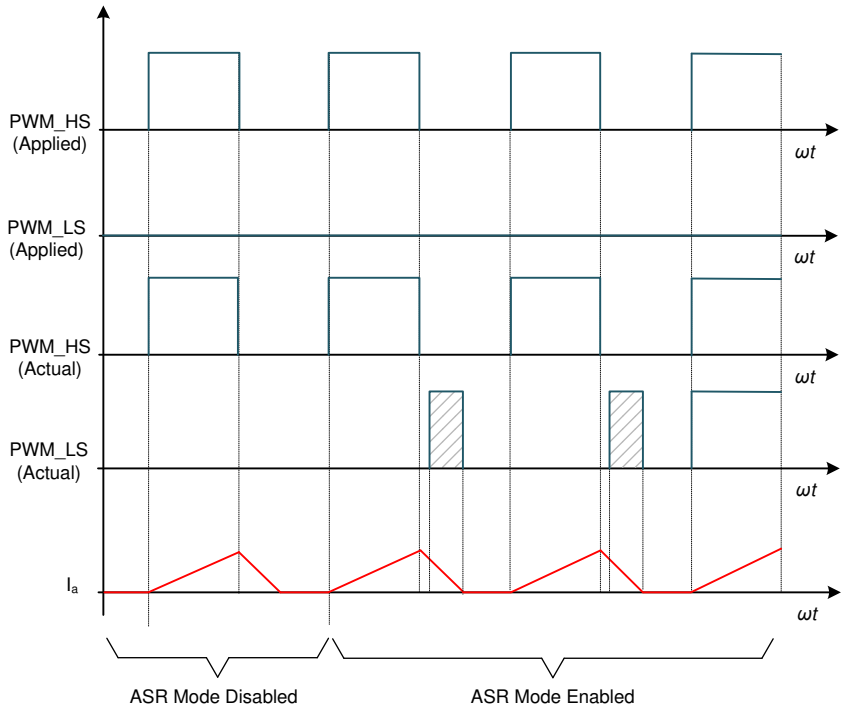


Figure 7-26. ASR in PWM Mode

7.3.11.2 Automatic Asynchronous Rectification Mode (AAR Mode)

Figure 7-27 shows the operation of AAR in PWM mode. As shown in this figure, a PWM is applied in a synchronous rectification to the high-side and low-side FETs. During the low-side FET conduction, for lower inductance motors, the current can decay to zero and becomes negative since low side FET is in on-state. This creates a negative torque on the BLDC motor operation. When AAR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management.

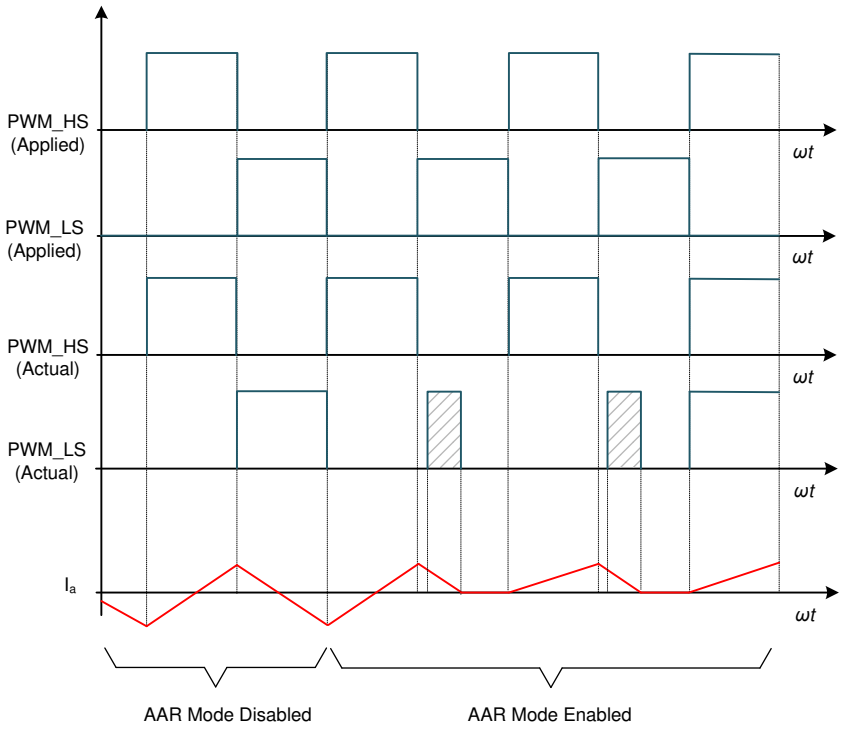


Figure 7-27. AAR in PWM Mode

7.3.12 Cycle-by-Cycle Current Limit

The current-limit circuitry utilizes the current sense amplifier output of the three phases compared with the voltage at ILIMIT pin. Figure 7-28 shows the implementation of current limit circuitry, the output of current sense amplifiers are combined with star connected resistive network. This measured voltage V_{MEAS} is compared with the external reference voltage V_{LIM} on ILIMIT pin to realize the current limit implementation. The relation between current sensed on three phases (I_{OUTx}) and V_{MEAS} threshold is given as:

$$V_{MEAS} = \left(V_{AVDD}/2\right) + \left((I_{OUTA} + I_{OUTB} + I_{OUTC}) \times GAIN/3\right) \quad (5)$$

where

- $V_{AVDD}$is the current sense amplifier supply
- I_{OUTX} is current flowing into the low-side MOSFET
- CSA_GAIN is the current sense amplifier gain

The current limit threshold can be adjusted by configuring the voltage at ILIMIT pin. Current limit varies linearly between 0A to 4A, as the voltage at ILIMIT pin varies from V_{AVDD}/2 to V_{MEAS}. A voltage more than V_{AVDD} can be applied to disable ILIMIT.

Current limit comparator output is blanked for a blanking time, on every rising and falling edge of PWM input signal and the output state of MCT8376Z-Q1 depends on the PWM status during blanking time. The blanking time is configured through ILIM_BLANK_SEL in SPI device and the blanking time is fixed to 5.5us for slew rate of 50 and 1.8us for all other slew rates in hardware variant.

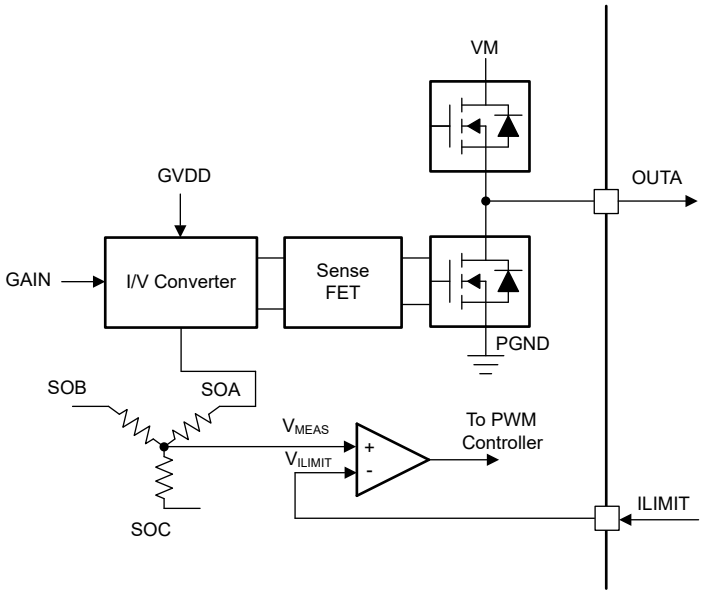


Figure 7-28. Current Limit Implementation

When then the current limit activates, the high-side FET of each half bride is disabled until the rising edge of the PWM of that half bridge as shown in Figure 7-29 . The low-side FETs can operate in brake mode or high-Z mode by configuring the ILIM_MODE bit in the SPI device variant. The low-side FETs operate in Coast (high-Z) mode in the hardware variant.

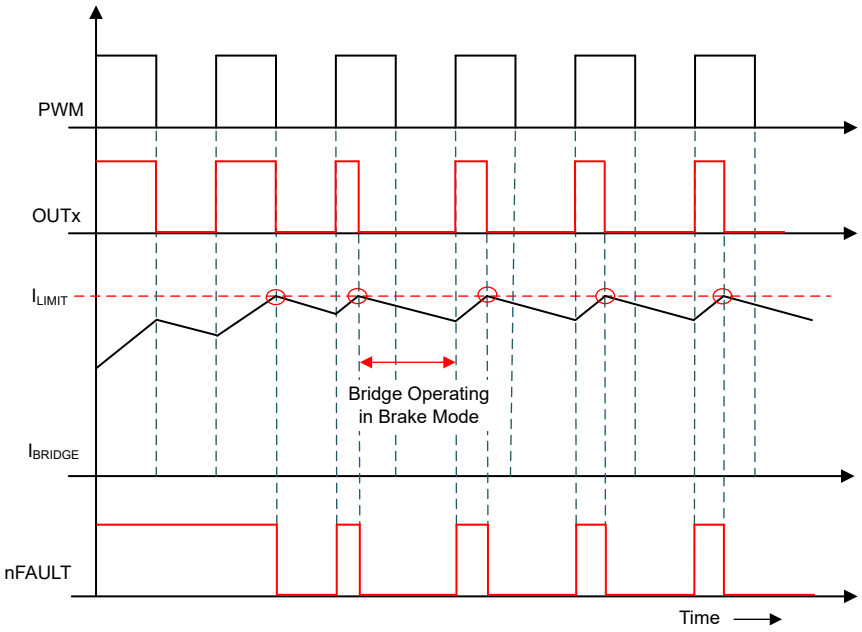


Figure 7-29. Cycle-by-Cycle Current-Limit Operation

When the current limit activates in synchronous rectification mode, the current recirculates through the low-side FETs while the high-side FETs are disabled as shown in Figure 7-30

When the current limit activates in asynchronous rectification mode, the current recirculates through the body diodes of the low-side FETs while the high-side FETs are disabled as shown in Figure 7-31

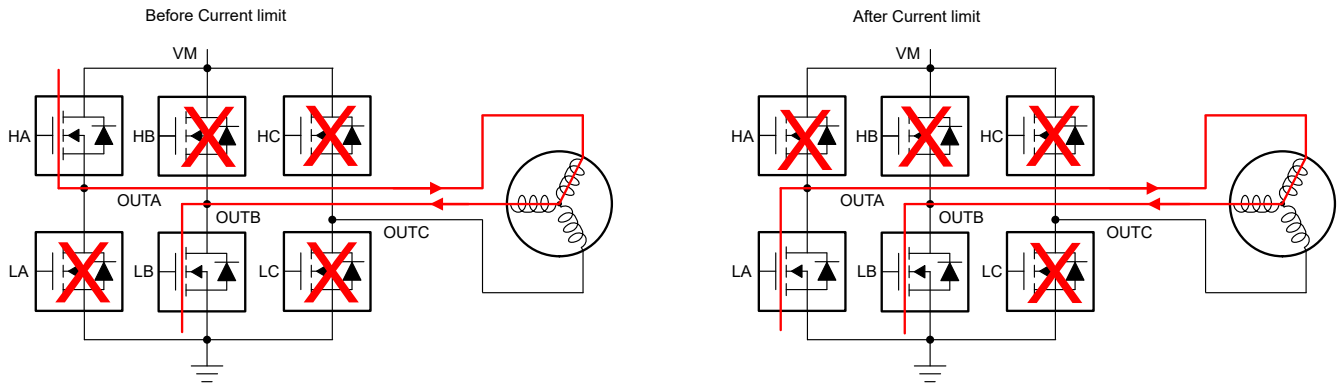


Figure 7-30. Brake State

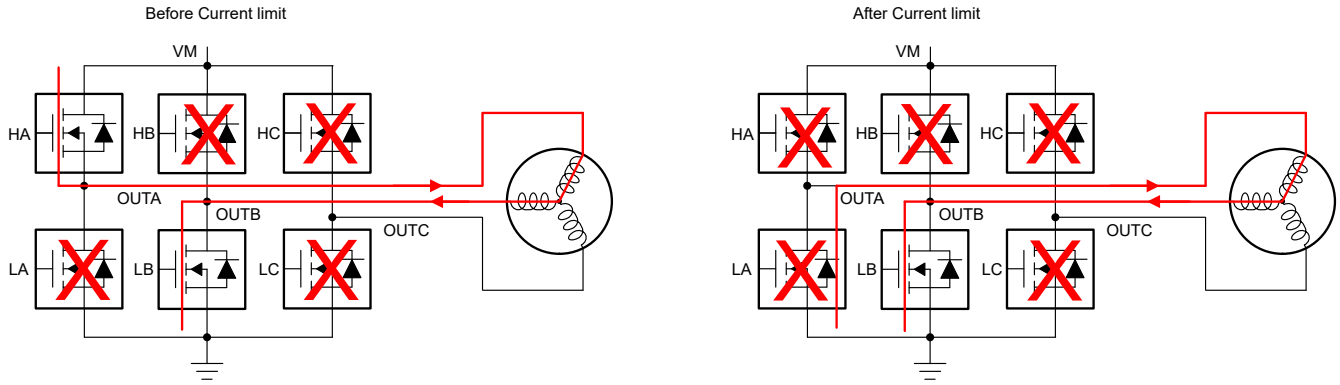


Figure 7-31. Coast State

Note

During the brake operation, a high current flows through the low-side FETs, which ultimately activates the overcurrent protection circuit. In this state, the body diode of the high-side FET conducts and directs brake energy to the VM supply rail.

7.3.12.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, MCT8376Z-Q1 has built in internal PWM clock which is used to turn high-side FET back on once high-side FET is disabled after exceeding I_{LIMIT} threshold. In SPI variant MCT8376Z-Q1, this internal PWM clock can be configured to either 10kHz or 20kHz or 40kHz through PWM_100_DUTY_SEL. In H/W variant MCT8376Z-Q1 PWM internal clock is set to 20kHz. Figure 7-32 shows operation with 100% duty cycle.

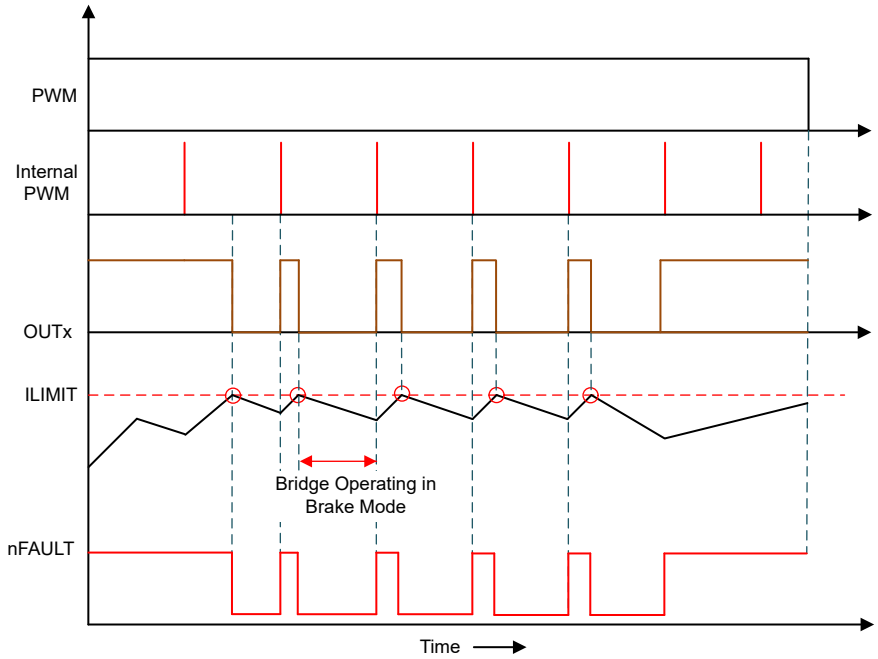


Figure 7-32. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

7.3.13 Hall Comparators (Analog Hall Inputs)

Three comparators are provided to process the raw signals from the Hall-effect sensors to commutate the motor. The Hall comparators sense the zero crossings of the differential inputs and pass the information to digital logic. The Hall comparators have hysteresis, and their detect threshold is centered at 0. The hysteresis is defined as shown in Figure 7-33.

In addition to the hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of t_{HDEG} after sensing a valid transition. Ignoring these transitions for the t_{HDEG} time prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, adding capacitors between the positive and negative inputs of the Hall comparators may be required. The ESD protection circuitry on the Hall inputs implements a diode to the GVDD pin. Because of this diode, the voltage on the Hall inputs should not exceed the GVDD voltage.

Because the GVDD pin is disabled in sleep mode (nSLEEP inactive), the Hall inputs should not be driven by external voltages in sleep mode. If the Hall sensors are powered externally, the supply to the Hall sensors should be disabled if the MCT8376Z-Q1 device is put into sleep mode. In addition, the Hall sensors' power supply should be powered up after enabling the motor otherwise an invalid Hall state may cause a delay in motor operation.

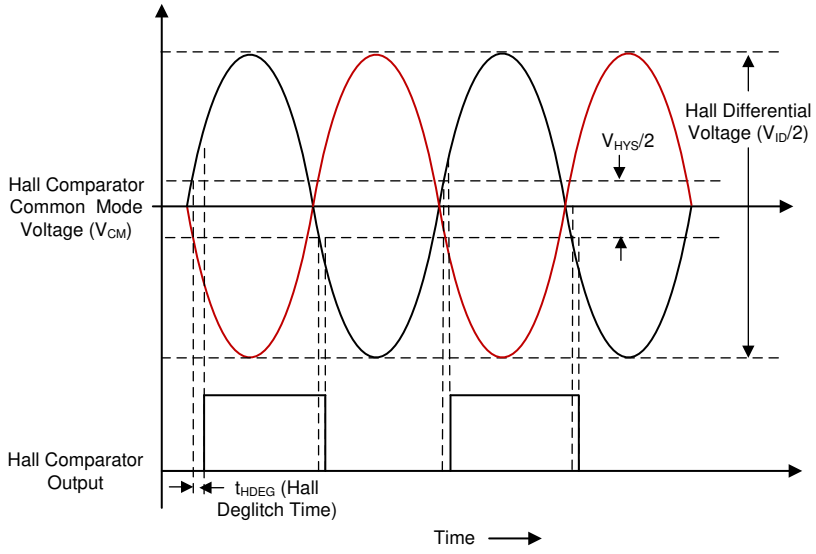


Figure 7-33. Hall Comparators Operation

7.3.14 Advance Angle

The MCT8376Z-Q1 includes device an advance angle feature to advance the commutation by a specified electrical angle based on the voltage on the ADVANCE pin (in H/W device variant) or the ADVANCE bits (in SPI device variant). Figure 7-34 shows the operation of advance angle feature.

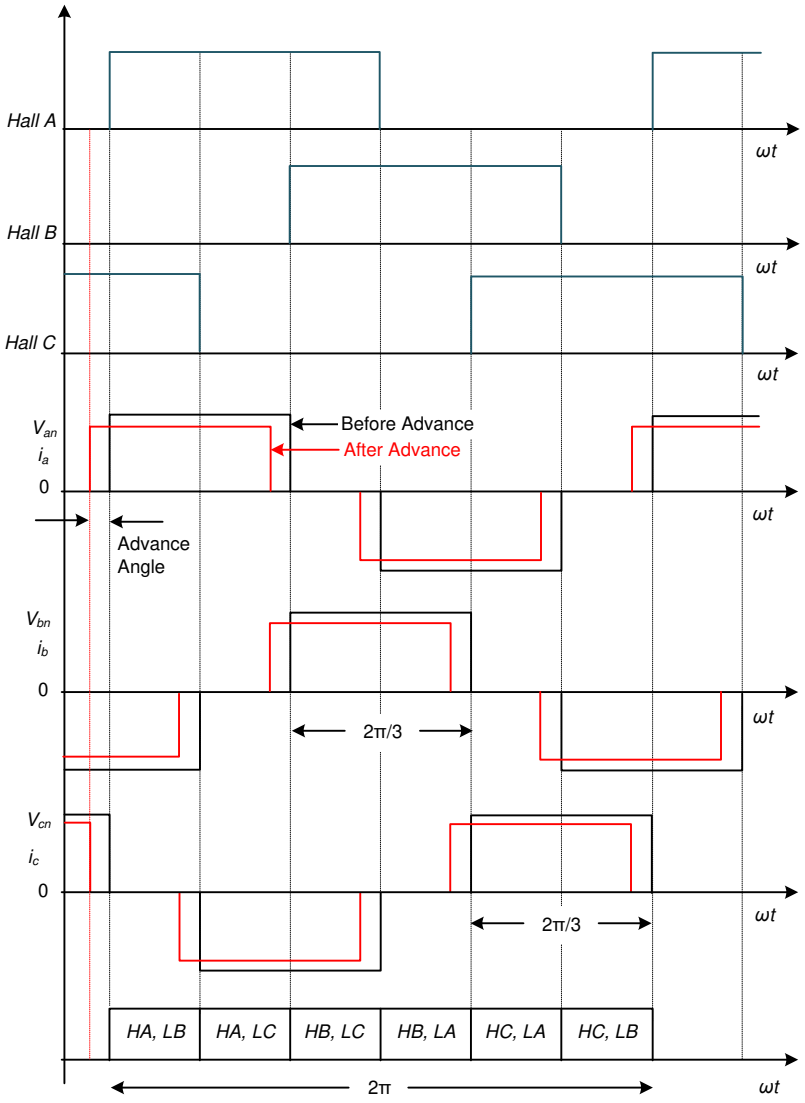


Figure 7-34. Advance Angle

7.3.15 FGOUT Signal

The MCT8376Z-Q1 device also has an open-drain FGOUT signal that can be used for closed-loop speed control of a BLDC motor. This signal includes the information of all three Hall-elements inputs as shown in Section 7.3.15. In the MCT8376ZS-Q1 (SPI variant), FGOUT can be configured to be a different division factor of Hall signals as shown in Section 7.3.15. In the MCT8376ZH-Q1 (Hardware variant), the default mode is FG_MODE = 00b.

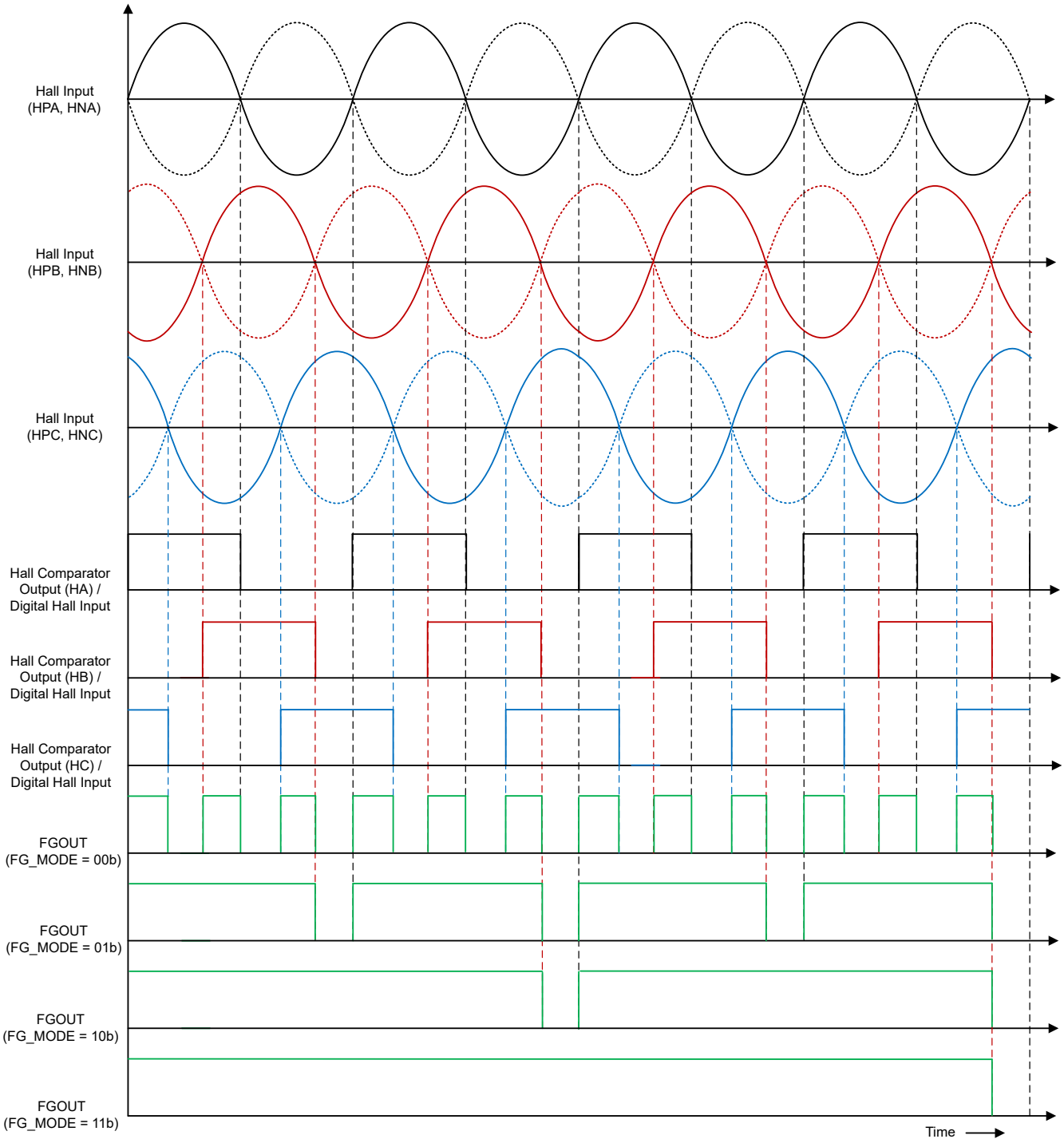


Figure 7-35. FGOUT Signal

7.3.16 Protections

The MCT8376Z-Q1 family of devices is protected against VM undervoltage, charge pump undervoltage, and overcurrent events. Table 7-7 summarizes various faults details.

Table 7-7. Fault Action and Response (SPI Devices)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (RESET)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO\_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
GVDD undervoltage (RESET)	$V_{GVDD} < V_{GVDD\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{GVDD} > V_{GVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
AVDD undervoltage (RESET)	$V_{AVDD} < V_{AVDD\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
OverVoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_MODE = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_MODE = 1b	FAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY} CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 10b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 11b	None	Active	Active	No action
ILIMIT	$V_{ILIMIT} < V_{SO}$	ILIMFLT_MODE = 0b	None	ILIMIT Mode	Active	Automatic: High side on the next rising edge of INHx Low side on the next rising edge of INLx
		ILIMFLT_MODE = 1b	nFAULT	ILIMIT Mode	Active	Automatic: High side on the next rising edge of INHx Low side on the next rising edge of INLx
SPI Error (SPI_FLT)	SCLK, Parity and ADDR fault	SPIFLT_MODE = 0b	None	Active	Active	No action
		SPIFLT_MODE = 1b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
OTP Error (OTP_ERR)	OTP reading is erroneous	—	nFAULT	Hi-Z	Active	Latched: Power Cycle, CLR_FLT
Motor Lock (MTR_LOCK)	No Hall Signals > $t_{MTR\_LOCK\_TDET}$	MTR_LOCK_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Pulse (MTR_LOCK bit)
		MTR_LOCK_MODE = 01b	nFAULT	Hi-Z	Active	Retry: $t_{MTR\_LOCK\_RETRY}$ (MTR_LOCK bit)
		MTR_LOCK_MODE = 10b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (MTR_LOCK bit)
		MTR_LOCK_MODE = 11b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_MODE = 0b	None	Active	Active	No action
		OTW_MODE = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{OTW\_HYS}$ CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (OTSD)	$T_J > T_{TSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{TSD} - T_{TSD\_HYS}$

7.3.16.1 VM Supply Undervoltage Lockout (RESET)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in Figure 7-36. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The

RESET bit is latched high in the device status (DEV_STS) register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

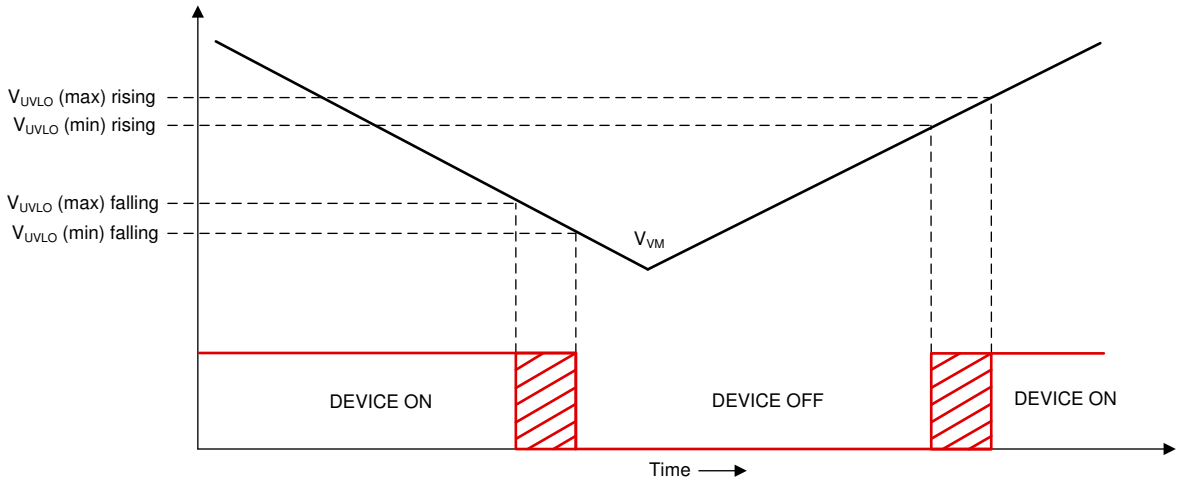


Figure 7-36. VM Supply Undervoltage Lockout

7.3.16.2 AVDD Undervoltage Protection (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed. The RESET bit is latched high in the device status (DEV_STS) register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

7.3.16.3 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on GVDD pin falls lower than the V_{GVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the GVDD undervoltage condition is removed. The RESET bit is latched high in the device status (DEV_STS) register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

7.3.16.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The charge pump undervoltage is reported on FAULT and CPUV bits. FAULT bit will be autocleared when charge pump undervoltage condition is removed. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device varaints.

7.3.16.5 Overvoltage Protections (OV)

If at any time input supply voltage on the VM pins rises higher than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The undervoltage is reported on FAULT and OVP bits. FAULT bit is autocleared when over voltage condition is removed. The OVP bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). Setting the OVP_MODE bit high on the SPI devices enables this protection feature. On hardware interface devices, the OVP protection is disabled.

The OVP threshold is also programmable on the SPI device variant. The OVP threshold can be set to 35V or 65V based on the OVP_SEL bit. In hardware interface device, over voltage protection is disabled.

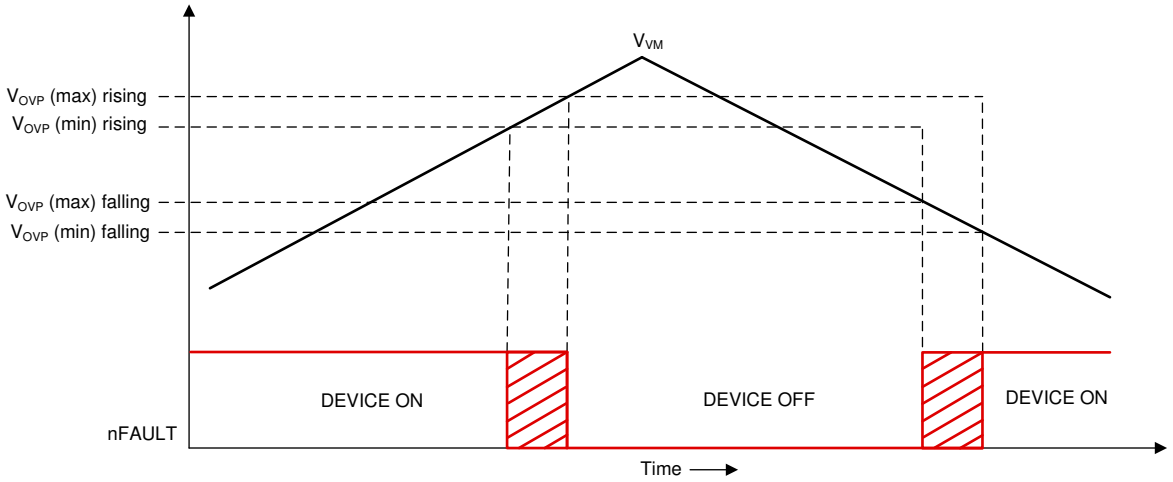


Figure 7-37. Over Voltage Protection

7.3.16.6 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current through a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the I_{OCP} threshold is fixed at 4.5A threshold, the t_{OCP_DEG} is fixed at 1.2µs, and the OCP_MODE is configured for retry mode with 5ms retry time. On SPI devices, the I_{OCP} threshold is set through the OCP_LVL bits, the t_{OCP_DEG} is set through the OCP_DEG bits.

The OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

7.3.16.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

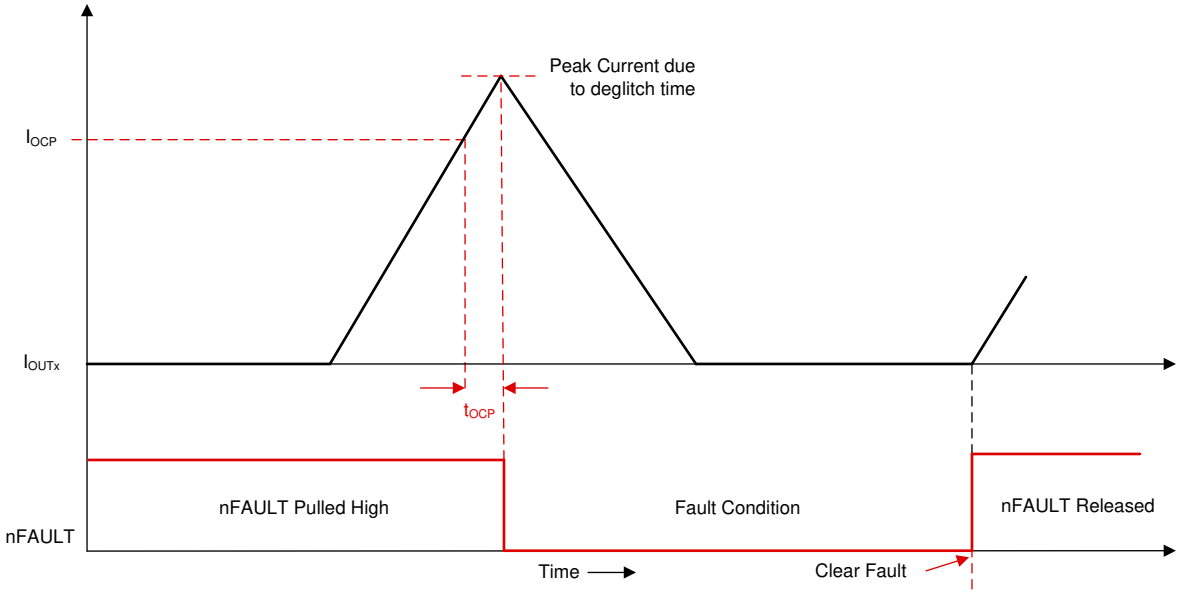


Figure 7-38. Overcurrent Protection - Latched Shutdown Mode

7.3.16.6.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the FAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

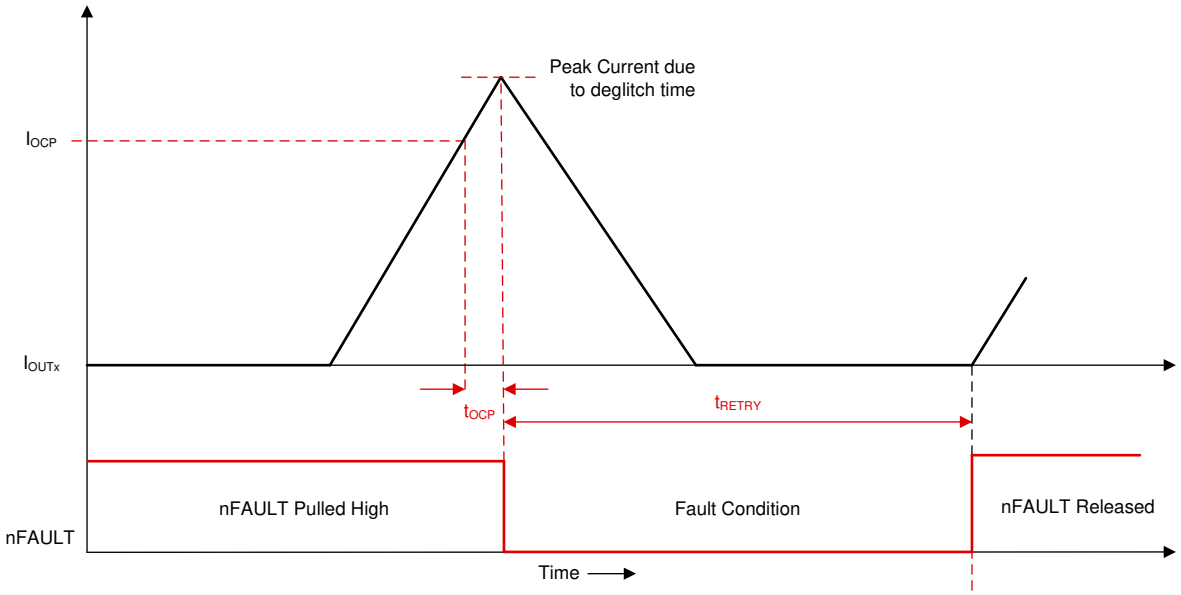


Figure 7-39. Overcurrent Protection - Automatic Retry Mode

7.3.16.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding FET's OCP bits high in the SPI registers. The MCT8376Z-Q1 continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.16.6.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

7.3.16.7 Motor Lock (MTR_LOCK)

During motor is in lock condition the hall signals are not available, so a Motor Lock event is sensed by monitoring the hall signals. If the hall signals are not present for longer than the t_{MTR_LOCK}, a MTR_LCK event is recognized and action is done according to the MTR_LOCK_MODE bits. On hardware interface devices, the t_{MTR_LOCK} threshold is set based on configuration at GAIN_SLEW_tLOCK pin as per Table 7-5, and the MTR_LOCK_MODE is configured for automatic retry with detection time of 500ms or 5s configured through GAIN_SLEW_tLOCK pin, and retry time of 10s. On SPI devices, the t_{MTR_LOCK} threshold is set through the MTR_LOCK_TDET register and the MTR_LOCK_MODE bit can operate in four different modes: MTR_LOCK latched shutdown, MTR_LOCK automatic retry, MTR_LOCK report only, and MTR_LOCK disabled.

7.3.16.7.1 MTR_LOCK Latched Shutdown (MTR_LOCK_MODE = 00b)

After a motor lock event in this mode, all FETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.16.7.2 MTR_LOCK Automatic Retry (MTR_LOCK_MODE = 01b)

After a motor lock event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the $t_{MTR\_LOCK\_RETRY}$ time elapses. The FAULT and MTR_LOCK bits stay latched until the $t_{MTR\_LOCK\_RETRY}$ period expires.

7.3.16.7.3 MTR_LOCK Report Only (MTR_LOCK_MODE= 10b)

No protective action occurs after a MTR_LOCK event in this mode. The motor lock event is reported by driving the nFAULT pin low and latching the FAULT and MTR_LOCK bits high in the SPI registers. The MCT8376Z-Q1 continues to operate as usual. The external controller manages the motor lock condition by acting appropriately. The reporting clears (nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.16.7.4 MTR_LOCK Disabled (MTR_LOCK_MODE = 11b)

No action occurs after a MTR_LOCK event in this mode.

Note

The motor lock detection scheme requires the PWM off-time (tPWM_OFF) to be lower than the motor lock detection time (tMTR_LOCK)

7.3.16.8 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the OT status (OT_STS) register and and OTF bit in the status register (DEV_STS) is set. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_MODE) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}). In hardware variant the over temperature warning is reported on nFAULT pin by default.

7.3.16.9 Thermal Shutdown (OTS)

If the die temperature in the device exceeds the trip point of the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OTSD bit in the OT status (OT_STS) register and OTF bit in the status register (DEV_STS) is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the MCT8376Z-Q1 family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, sense amplifiers are disabled, the charge pump is disabled, the GVDD and AVDD regulators are disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

Note

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin in low does not exceed the t_{SLEEP} or t_{WAKE} time.

7.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, GVDD and AVDD regulator, and SPI bus are active.

7.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the MCT8376Z-Q1 family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the nSLEEP pin on either interface variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence falls with the t_{RST} time window or else the device starts the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

7.4.2 DRVOFF Functionality

MCT8376Z-Q1 has capability to disable predriver and MOSFETs through DRVOFF pin. When DRVOFF pin is pulled high, all six MOSFETs are disabled. If nSLEEP is high when the DRVOFF pin is high, the charge pump, AVDD regulator, GVDD regulator, and SPI bus are active and any driver-related faults such as OCP is inactive. DRVOFF pin independently disables MOSFETs which stops motor commutation irrespective of status of INHx and INLx input pins.

7.5 SPI Communication

7.5.1 Programming

On MCT8376Z-Q1 SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in secondary mode and connects to a controller. The SPI input data (SDI) word consists of a 24-bit word, with one read or write bit, a parity bit, 6-bit address and 15 bits of data with a parity bit. The SPI output consists of 24 bit word, with a 8 bits of status information (STS register) and 16-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin is low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin is pulled high for at least 400ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 24 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 24 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and when the device is enters sleep mode

7.5.1.1 SPI Format

SPI Format - with Parity

The SDI input data word is 24 bits long and consists of the following format:

- 1 read or write bit, W (bit B16)
- 6 address bits, A (bits B22 through B17)
- Parity bit, P (bit B23)
- 15 data bits with 1 parity bit, D (bits B15 through B0)

The SDO output data word is 24 bits long. The most significant bits are status bits and the least significant 16 bits are the data content of the register being accessed.

Table 7-8. SDI Input Data Word Format for SPI

PARITY	ADDRESS						RW	PARITY	DATA													
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
P	A5	A4	A3	A2	A1	A0	W0	P	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-9. SDO Output Data Word Format

STATUS								DATA															
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The details of the bits used in SPI frame format are detailed below.

Read/Write Bit (R/W): R/W (W0) bit set to 0b indicates a SPI write transaction. For a SPI read operation, R/W bit needs to be set to 1b.

Address Bits (A): A SPI secondary device takes a 6-bit register address.

Parity Bit (P): Both header and data fields of a SPI input data frame include a parity bit for single bit error detection - in Table 7-8, B23 is parity bit for the header field, while B15 is the parity bit for the data field. The parity scheme used is even parity - the number of ones in a block of 16-bits (including the parity bit) is even. Data will be written to the internal registers only if the parity check is successful. Parity checks can be enabled or disabled by configuring the SPI_PEN bit of SYS_CTRL register. Parity checks are disabled by default.

Note

Though parity checks are disabled by default, TI recommends enabling parity checks to safeguard against single-bit errors.

8 Register Map

8.1 STATUS Registers

Table 8-1 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. STATUS Registers

Offset	Acronym	Register Name	Section
0h	Device Status Register	Device Status Register	Section 8.1.1
2h	Device Raw Status Register	Device Raw Status Register	Section 8.1.2
4h	Over Temperature Status Register	Over Temperature Status Register	Section 8.1.3
5h	Supply Status Register	Supply Status Register	Section 8.1.4
6h	Driver Status Register	Driver Status Register	Section 8.1.5
7h	System Interface Status Register	System Interface Status Register	Section 8.1.6

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 Device Status Register (Offset = 0h) [Reset = 0280h]

Device Status Register is shown in Table 8-3.

Return to the Summary Table.

Table 8-3. Device Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-11	RESERVED	R-0	0h	Reserved
10	MTR_LOCK	R	0h	Motor Lock Status Bit 0h = Motor Lock condition is not detected 1h = Motor Lock condition is detected
9	DNRDY_STS	R	1h	Device Not Ready Status. Will be cleared automatically after completion of Power Up. 0h = Device is Ready 1h = Device is NOT Ready
8	SYSFLT	R	0h	OTP Read fault occurred. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No OTP read fault is detected 1h = OTP read fault detected
7	RESET	R	1h	Device Reset status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = Cleared 1h = Device has undergone power on reset
6	SPIFLT	R	0h	SPI Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No SPI fault is detected 1h = SPI fault is detected
5	OCP	R	0h	Overcurrent Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
4	RESERVED	R-0	0h	Reserved
3	OVP	R	0h	Over Voltage Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No over voltage condition is detected 1h = Over voltage condition is detected
2	UVP	R	0h	Supply Undervoltage Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No undervoltage voltage condition is detected on CP 1h = Undervoltage voltage condition is detected on CP
1	OTF	R	0h	Overtemperature Fault Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
0	FAULT	R	0h	Device Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No fault condition is detected 1h = Fault condition is detected

8.1.2 Device Raw Status Register (Offset = 2h) [Reset = 0280h]

Device Raw Status Register is shown in Table 8-4.

Return to the Summary Table.

Table 8-4. Device Raw Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved

Table 8-4. Device Raw Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-13	RESERVED	R-0	0h	Reserved
12	DRVOFF_RSTS	R	0h	Status of DRV_OFF pin 0h = DRV_OFF is not active 1h = DRV_OFF is active
11	OTW_RSTS	R	0h	OT Warning Raw Status 0h = OTW not active 1h = OTW is active
10	MTR_LOCK_RSTS	R	0h	Motor Lock Status Bit 0h = Motor Lock condition is not detected 1h = Motor Lock condition is detected
9	DNRDY_RSTS	R	1h	Device Not Ready Status 0h = Device is Ready 1h = Device is NOT Ready
8	SYSFLT_RSTS	R	0h	OTP Read fault occurred. Status remains latched until cleared by write to FLT_CLR 0h = No OTP read fault is detected 1h = OTP read fault detected
7	RESET	R	1h	Device power on status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = Cleared by FW after read 1h = Device has undergone power on reset
6	SPIFLT_RSTS	R	0h	SPI Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No SPI fault is detected 1h = SPI fault is detected
5	OCP_RSTS	R	0h	Overcurrent Fault Raw Status. Status remains latched until completion of Auto Retry or write to FLT_CLR or reset pulse on nSLEEP. 0h = Overcurrent condition is not active 1h = Overcurrent condition is active
4	RESERVED	R-0	0h	Reserved
3	OVP_RSTS	R	0h	Over Voltage Raw Fault Status. 0h = Over Voltage condition is not active. 1h = Over Voltage condition is active.
2	UVP_RSTS	R	0h	CP Undervoltage Raw Fault Status. 0h = Chare Pump Under voltage condition is not active. 1h = Chare Pump Under voltage condition is active.
1	OTF_RSTS	R	0h	Overtemperature Shutdown Raw Fault Status. 0h = Overtemperature shutdown is not active. 1h = Overtemperature shutdown is active.
0	RESERVED	R-0	0h	Reserved

8.1.3 Over Temperature Status Register (Offset = 4h) [Reset = 0000h]

Over Temperature Status Register is shown in Table 8-5.

Return to the Summary Table.

Table 8-5. Over Temperature Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-2	RESERVED	R-0	0h	Reserved
1	OTW	R	0h	Overtemperature Warning Fault status. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected

Table 8-5. Over Temperature Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OTSD	R	0h	Overtemperature Shutdown Fault status. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected

8.1.4 Supply Status Register (Offset = 5h) [Reset = 0000h]

Supply Status Register is shown in Table 8-6.

Return to the Summary Table.

Table 8-6. Supply Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-7	RESERVED	R-0	0h	Reserved
6	VM_OV	R	0h	Vm Over Voltage Fault Status 0h = No Vm over voltage is detected 1h = Vm over voltage is detected
5	RESERVED	R-0	0h	Reserved
4	CP_UV	R	0h	Charge Pump Undervoltage fault status 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
3-0	RESERVED	R-0	0h	Reserved

8.1.5 Driver Status Register (Offset = 6h) [Reset = 0000h]

Driver Status Register is shown in Table 8-7.

Return to the Summary Table.

Table 8-7. Driver Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-7	RESERVED	R-0	0h	Reserved
6	OCPC_HS	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side MOSFET of OUTC 1h = Overcurrent detected on high-side MOSFET of OUTC
5	OCPB_HS	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side MOSFET of OUTB 1h = Overcurrent detected on high-side MOSFET of OUTB
4	OCPA_HS	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side MOSFET of OUTA 1h = Overcurrent detected on high-side MOSFET of OUTA
3	RESERVED	R-0	0h	Reserved
2	OCPC_LS	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side MOSFET of OUTC 1h = Overcurrent detected on low-side MOSFET of OUTC
1	OCPB_LS	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side MOSFET of OUTB 1h = Overcurrent detected on low-side MOSFET of OUTB
0	OCPA_LS	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side MOSFET of OUTA 1h = Overcurrent detected on low-side MOSFET of OUTA

8.1.6 System Interface Status Register (Offset = 7h) [Reset = 0000h]

System Interface Status Register is shown in Table 8-8.

Return to the Summary Table.

Table 8-8. System Interface Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-5	RESERVED	R-0	0h	Reserved
4	OTPLD_ERR	R	0h	OTP CRC error during load 0h = No OTP read error is detected 1h = OTP read error is detected
3	RESERVED	R-0	0h	Reserved
2	SPI_PARITY	R	0h	SPI Parity Error 0h = No SPI Parity Error is detected 1h = SPI Parity Error is detected
1	RESERVED	R-0	0h	Reserved
0	FRM_ERR	R	0h	SPI Frame Error 0h = No SPI Frame Error is detected 1h = SPI Frame Error is detected

8.2 CONTROL Registers

Table 8-9 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in Table 8-9 are considered as reserved locations and the register contents are not to be modified.

Table 8-9. CONTROL Registers

Offset	Acronym	Register Name	Section
10h	Fault Mode Register	Fault Mode Register	Section 8.2.1
13h	Driver Fault Control Register	Driver Fault Control Register	Section 8.2.2
17h	Fault Clear Register	Fault Clear Register	Section 8.2.3
20h	PWM Control Register 1A	PWM Control Register 1A	Section 8.2.4
22h	Predriver control Register	Predriver control Register	Section 8.2.5
23h	CSA Control Register	CSA Control Register	Section 8.2.6
3Fh	System Control Register	System Control Register	Section 8.2.7

Complex bit access types are encoded to fit into small table cells. Table 8-10 shows the codes that are used for access types in this section.

Table 8-10. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 Fault Mode Register (Offset = 10h) [Reset = 2811h]

Fault Mode Register is shown in Table 8-11.

Return to the Summary Table.

Table 8-11. Fault Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	RESERVED	R-0	0h	Reserved
13	ILIMFLT_MODE	R/W	1h	ILIMIT Fault mode 0h = ILIMIT reporting on nFAULT pin is disabled 1h = ILIMIT reporting on nFAULT pin is enabled
12-11	MTR_LOCK_MODE	R/W	1h	Motor Lock Fault mode - Honor OTP even in HW device 0h = Motor lock causes a latched fault 1h = Motor lock causes an automatic retrying fault 2h = Motor lock is report only but no action is taken 3h = Motor lock is not reported and no action is taken
10	RESERVED	R-0	0h	Reserved
9	OVP_MODE	R/W	0h	Over Voltage Protection Fault mode 0h = Over Voltage protection is disabled 1h = Over Voltage protection is enabled
8	RESERVED	R-0	0h	Reserved
7	SPIFLT_MODE	R/W	0h	SPI Fault mode 0h = SPI fault reporting on nFAULT pin is disabled 1h = SPI fault reporting on nFAULT pin is enabled
6	RESERVED	R-0	0h	Reserved
5-4	OCP_MODE	R/W	1h	Overcurrent Protection Fault mode 0h = Over Current causes a latched fault 1h = Over Current causes an automatic retrying fault 2h = Over Current is report only but no action is taken 3h = Over Current is not reported and no action is taken
3-1	RESERVED	R-0	0h	Reserved
0	OTW_MODE	R/W	1h	Overtemperature Warning Fault mode 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled

8.2.2 Driver Fault Control Register (Offset = 13h) [Reset = 1010h]

Driver Fault Control Register is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. Drviver Fault Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	RESERVED	R-0	0h	Reserved
13-12	MTR_LOCK_TDET	R/W	1h	Motor lock detection time settings 0h = 5000ms 1h = 1000ms 2h = 500ms 3h = 250ms
11	RESERVED	R-0	0h	Reserved
10	MTR_LOCK_RETRY	R/W	0h	Motor lock retry time setting 0h = 10s 1h = 2s
9	RESERVED	R-0	0h	Reserved
8	OVP_SEL	R/W	0h	Overvoltage level setting 0h = VM overvoltage level is 65V 1h = VM overvoltage level is 35V
7-6	RESERVED	R-0	0h	Reserved
5-4	OCP_DEG	R/W	1h	OCP Deglitch time 0h = OCP Deglitch time is 0.6µs 1h = OCP Deglitch time is 1.25µs 2h = OCP Deglitch time is 1.6µs 3h = OCP Deglitch time is 2µs
3	RESERVED	R-0	0h	Reserved
2	OCP_TRETRY	R/W	0h	OCP Retry Time 0h = 5ms 1h = 500ms
1	RESERVED	R-0	0h	Reserved
0	OCP_LVL	R/W	0h	OCP Level 0h = 4.5A 1h = 2A

8.2.3 Fault Clear Register (Offset = 17h) [Reset = 0000h]

Fault Clear Register is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. Fault Clear Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-1	RESERVED	R-0	0h	Reserved
0	FLT_CLR	R-0/W1C	0h	Clear latched faults 0h = No clear fault command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.

8.2.4 PWM Control Register 1A (Offset = 20h) [Reset = 0020h]

PWM Control Register 1A is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. PWM Control Register 1A Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-12	ADVANCE_LVL	R/W	0h	Phase Advance Setting 0h = 0° 1h = 4° 2h = 7° 3h = 11° 4h = 15° 5h = 20° 6h = 25° 7h = 30°
11	HALL_HYS	R/W	0h	Hall Comparator Hysteresis setting 0h = 5mV 1h = 50mV
10	DIR	R/W	0h	Direction control. In HW mode, the DIR is taken from Pad. 0h = Motor direction set to clockwise 1h = Motor direction set to Counter clockwise
9-8	FG_MODE	R/W	0h	Electrical Frequency Generation output mode bits 0h = FG frequency is 3x commutation frequency 1h = FG frequency is 1x of commutation frequency 2h = FG frequency is 0.5x of commutation frequency 3h = FG frequency is 0.25x of commutation frequency
7-6	PWM_100_FREQ_SEL	R/W	0h	Frequency of PWM at 100% Duty cycle 0h = 20KHz 1h = 40KHz 2h = 10KHz 3h = None
5	ILIM_MODE	R/W	1h	Current limit recirculation settings 0h = Current recirculation through FETs (Brake mode) 1h = Current recirculation through diodes (coast mode)
4	BRAKE_MODE	R/W	0h	Brake Mode setting 0h = Device operation is braking in Brake mode 1h = Device operation is braking in coast mode.
3	EN_AAR	R/W	0h	Enable AAR where LS FET gets turned off when current goes negative. 0h = Active Demagnetization AAR is Disabled 1h = Active Demagnetization AAR is Enabled
2	EN_ASR	R/W	0h	Enable turning on the HS or LS FET when current flows through the body diode of FET. 0h = Active Demagnetization ASR is Disabled 1h = Active Demagnetization ASR is Enabled
1-0	PWM_MODE	R/W	0h	PWM mode selection 0h = Synchronous rectification with digital Hall 1h = Synchronous rectification with analog Hall 2h = Asynchronous rectification with digital Hall 3h = Asynchronous rectification with analog Hall

8.2.5 Predriver control Register (Offset = 22h) [Reset = 0080h]

Predriver control Register is shown in Table 8-15.

Return to the Summary Table.

Table 8-15. Predriver control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-11	RESERVED	R-0	0h	Reserved
10-8	ILIM_BLANK_SEL	R/W	0h	Current Limit Blanking Time Selection 0h = 5.5us for slew rate of 50 and 1.8us for all other slew rates. 1h = 6.0us for slew rate of 50 and 2.3us for all other slew rates. 2h = 6.5us for slew rate of 50 and 2.8us for all other slew rates. 3h = 7.5us for slew rate of 50 and 3.8us for all other slew rates.
7-4	ADMAG_TMARGIN	R/W	8h	Wait time before determining HiZ. N*4*100ns
3	AD_COMP_TH_HS	R/W	0h	Active demag high side comparator threshold 0h = active demag comparator threshold is 100mA 1h = active demag comparator threshold is 150mA
2	AD_COMP_TH_LS	R/W	0h	Active demag low side comparator threshold 0h = active demag comparator threshold is 100mA 1h = active demag comparator threshold is 150mA
1-0	SLEW_RATE	R/W	0h	Slew rate settings 0h = Slew rate is 1100 V/µs 1h = Slew rate is 500 V/µs 2h = Slew rate is 250 V/µs 3h = Slew rate is 50 V/µs

8.2.6 CSA Control Register (Offset = 23h) [Reset = 0000h]

CSA Control Register is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. CSA Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-2	RESERVED	R-0	0h	Reserved
1-0	CSA_GAIN	R/W	0h	CSA Gain settings 0h = CSA gain is 0.4 V/A 1h = CSA gain is 1.0 V/A 2h = CSA gain is 2.5 V/A 3h = CSA gain is 5.0 V/A

8.2.7 System Control Register (Offset = 3Fh) [Reset = 0008h]

System Control Register is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. System Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-12	WRITE_KEY	R-0/W	0h	0x5 Write Key Specific to this register.
11	SDO_VSEL	R/W	0h	SDO Output Voltage Select 0h = AVDD 1h = GVDD
10	SDO_ODEN	R/W	0h	SDO in Open Drain Mode 0h = SDO in Push Pull Mode 1h = SDO in Open Drain Mode
9-8	RESERVED	R-0	0h	Reserved
7	REG_LOCK	R/W	0h	Register Lock Bit 0h = Registers Unlocked 1h = Registers Locked
6	SPI_PEN	R/W	0h	Parity Enable for SPI 0h = Parity Disabled 1h = Parity Enabled
5-4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2-0	RESERVED	R-0	0h	Reserved

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The MCT8376Z-Q1 can be used to drive Brushless-DC motors. A primary application schematic is shown in Figure 9-1 Figure 9-2.

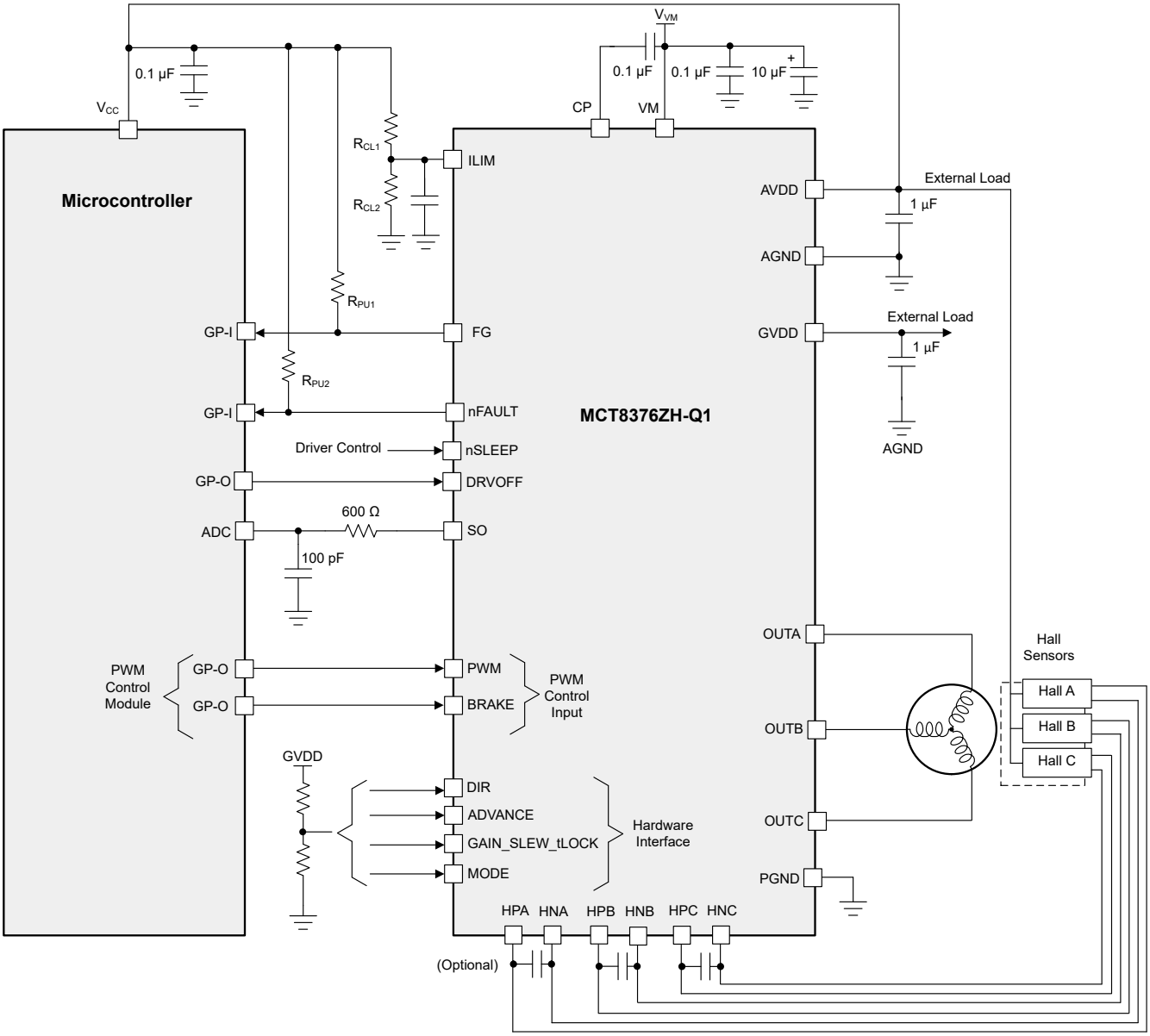


Figure 9-1. Primary Application Schematics for MCT8376ZH-Q1 (hardware variant)

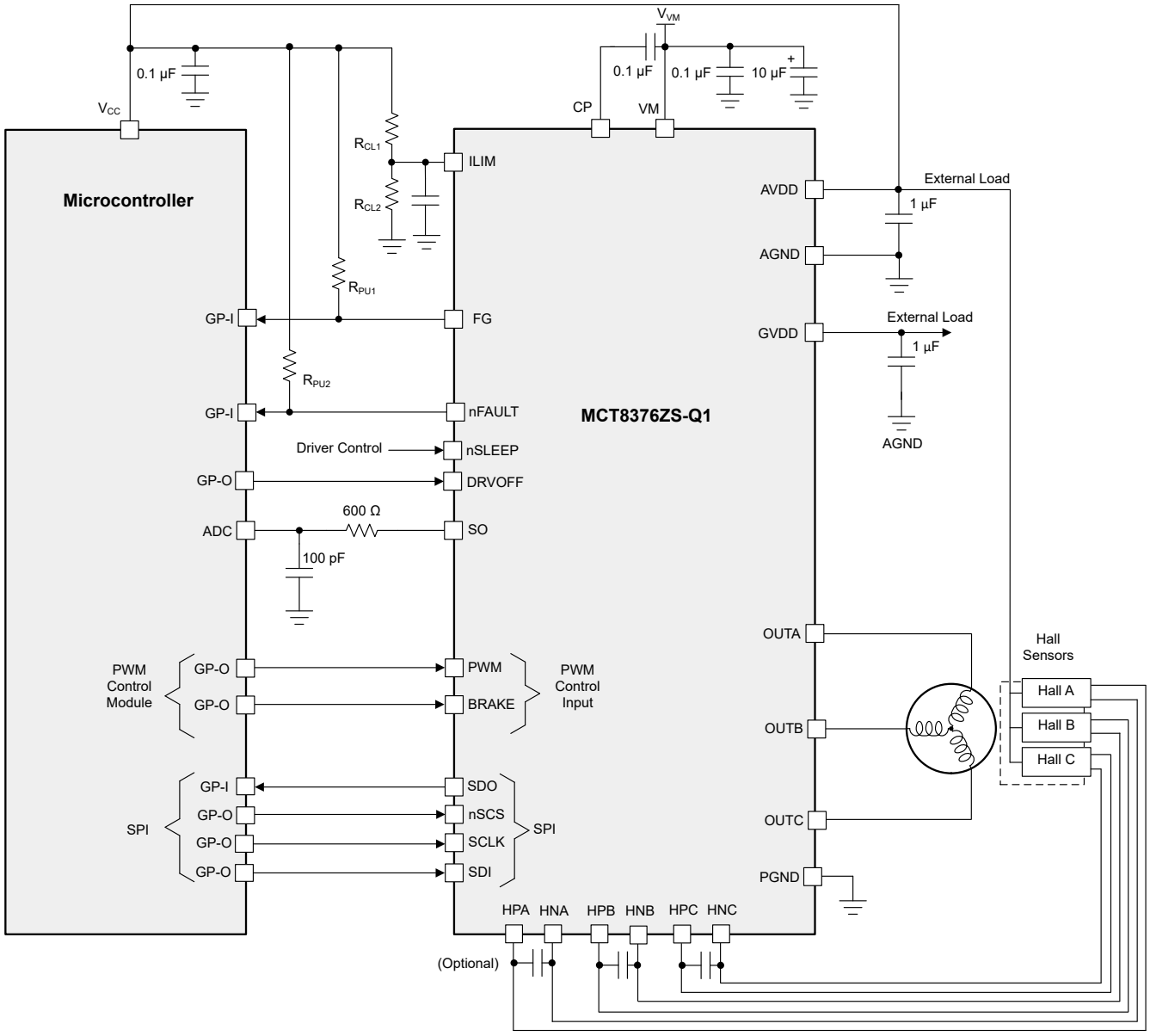


Figure 9-2. Primary Application Schematics for MCT8376ZS-Q1 (SPI variant)

9.2 Hall Sensor Configuration and Connection

The combinations of Hall sensor connections in this section are common connections.

9.2.1 Typical Configuration

The Hall sensor inputs on the MCT8376Z-Q1 device can interface with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal. To use this type of sensor, the AVDD regulator can be used to power the Hall sensor. Figure 9-3 shows the connections.

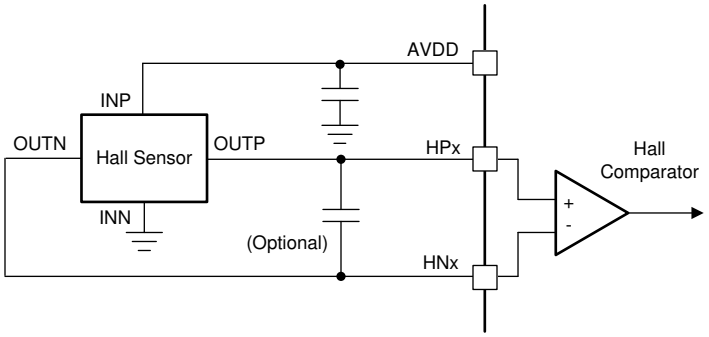


Figure 9-3. Typical Hall Sensor Configuration

Because the amplitude of the Hall-sensor output signal is very low, capacitors are often placed across the Hall inputs to help reject noise coupled from the motor. Capacitors with a value of 1 nF to 100 nF are typically used.

9.2.2 Open Drain Configuration

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the MCT8376Z-Q1 device, with the addition of a few resistors as shown in Figure 9-4.

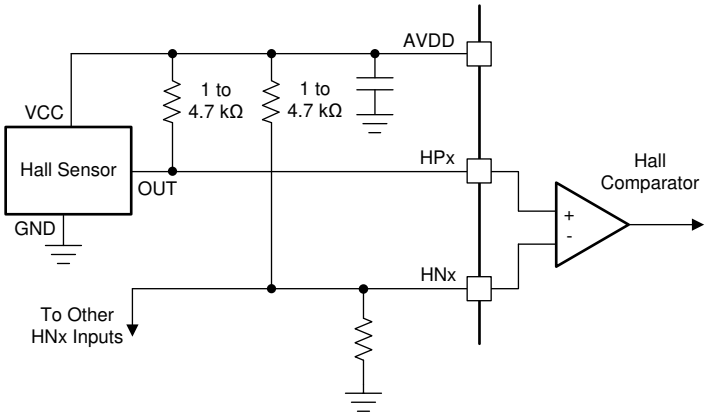


Figure 9-4. Open-Drain Hall Sensor Configuration

The negative (HNx) inputs are biased to AVDD / 2 by a pair of resistors between the AVDD pin and ground. For open-collector Hall sensors, an additional pullup resistor to the VREG pin is required on the positive (HPx) input. Again, the AVDD output can usually be used to supply power to the Hall sensors.

9.2.3 Series Configuration

Hall elements are also connected in series or parallel depending upon the Hall sensor current/voltage requirement. Figure 9-5 shows the series connection of Hall sensors powered via the MCT8376Z-Q1 internal LDO (AVDD). This configuration is used if the current requirement per Hall sensor is high (>10 mA)

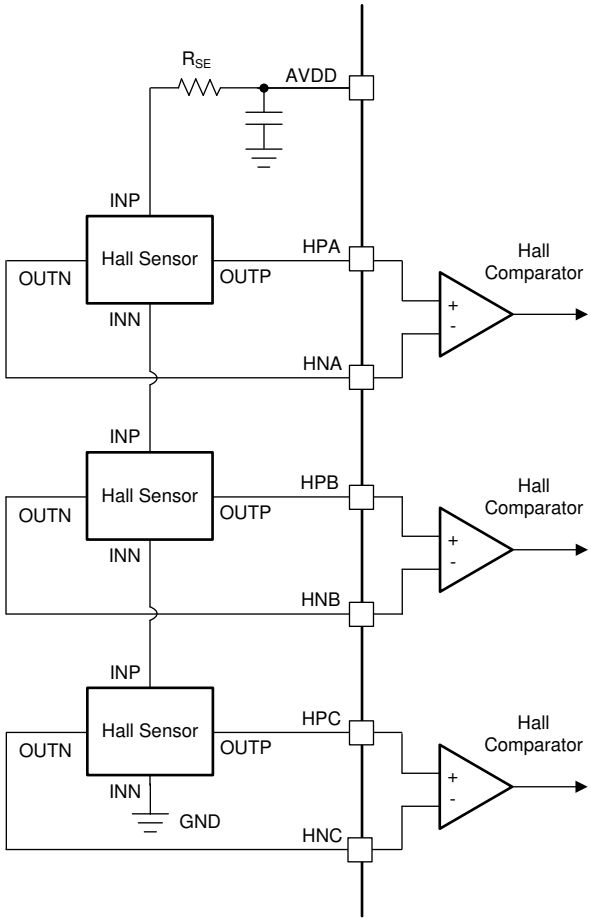


Figure 9-5. Hall Sensor Connected in Series Configuration

9.2.4 Parallel Configuration

Figure 9-6 shows the parallel connection of Hall sensors which is powered by the AVDD. This configuration can be used if the current requirement per Hall sensor is low (<10 mA).

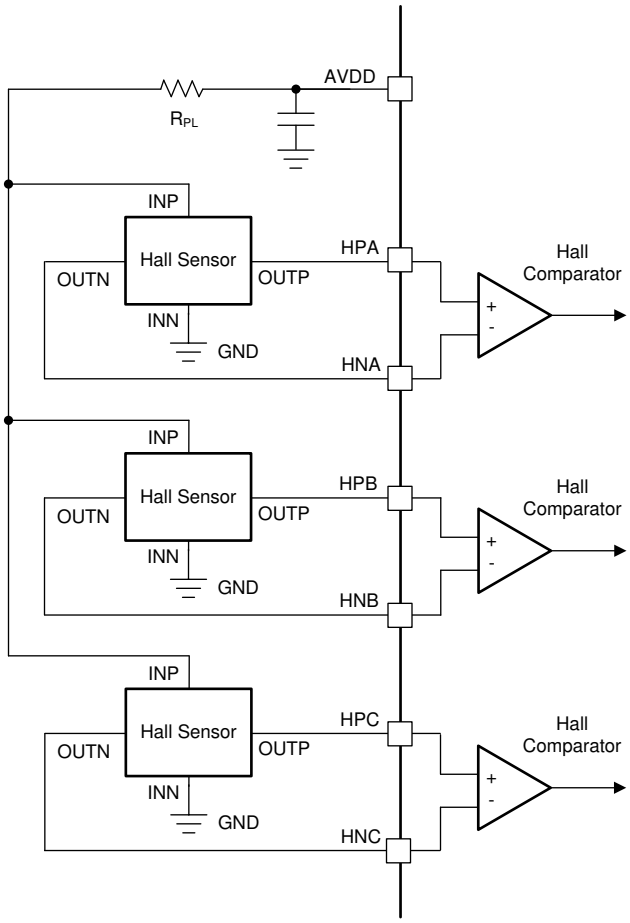


Figure 9-6. Hall Sensors Connected in Parallel Configuration

9.3 Power Supply Recommendations

9.3.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

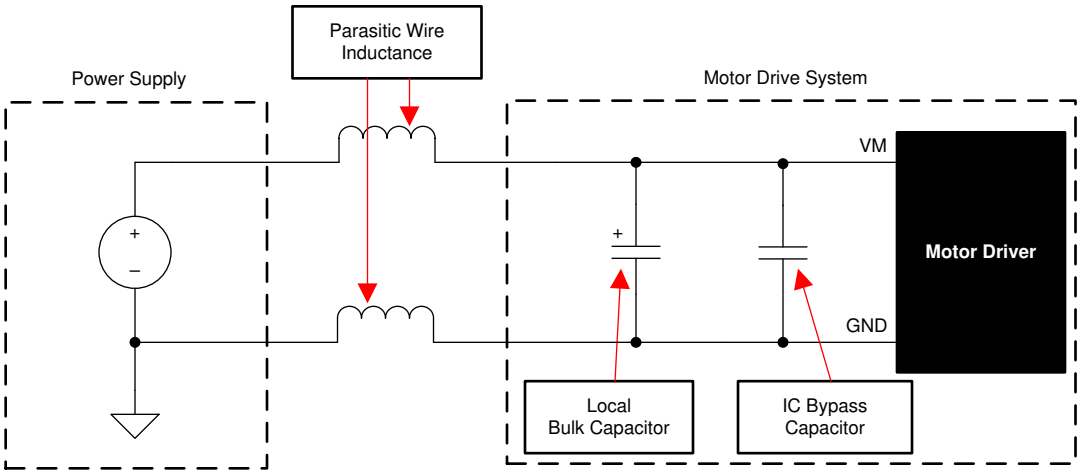


Figure 9-7. Example Setup of Motor Drive System With External Power Supply

Make the voltage rating for bulk capacitors higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

9.4 Layout

9.4.1 Layout Guidelines

The bulk capacitor is placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths is as wide as possible, and numerous vias are used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the charge pump, GVDD and AVDD capacitors are ceramic and placed closely to device pins.

The high-current device outputs use wide metal traces.

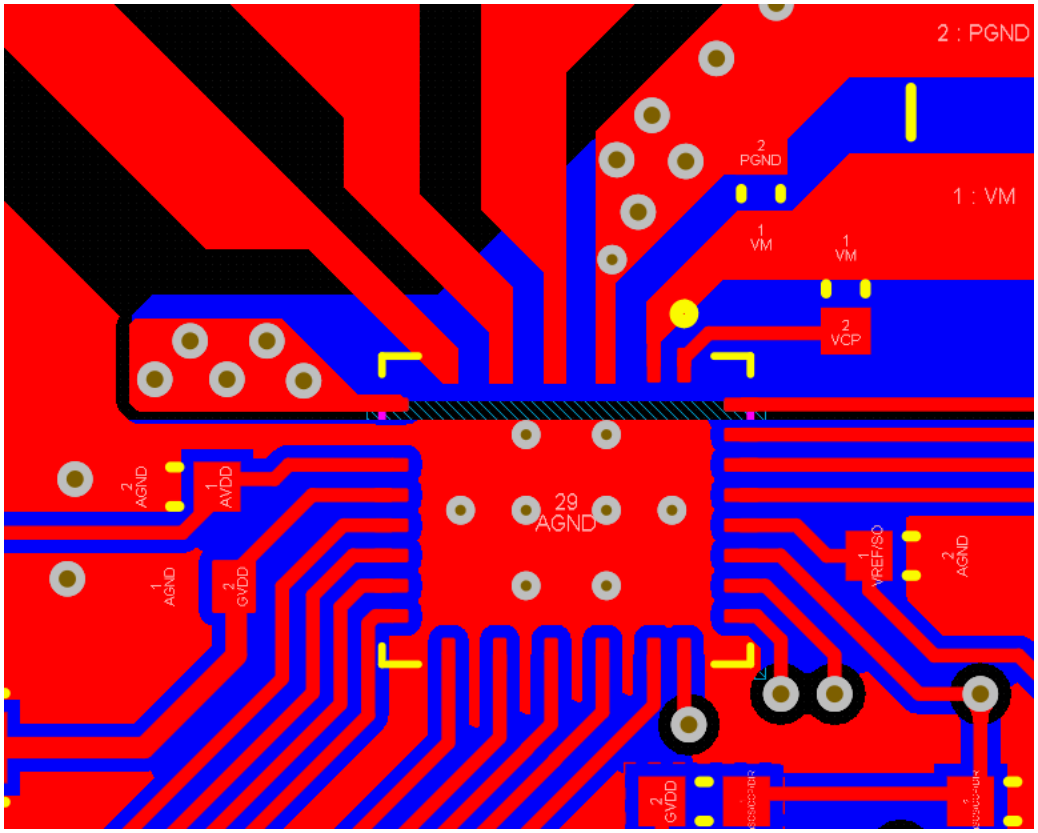
To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding are partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Verify grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad are soldered to the PCB top-layer ground plane. Multiple vias are used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

9.4.2 Layout Example

Recommended Layout Example for VQFN Package



9.4.3 Thermal Considerations

The MCT8376Z-Q1 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heat sinking, or too high an ambient temperature.

9.4.3.1 Power Dissipation

The power loss in MCT8376Z-Q1 include standby power losses, LDO power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in MCT8376Z-Q1. At start-up and fault conditions, the output current is much higher than normal current; remember to take these peak currents and the duration of the currents into consideration. The total device dissipation is the power dissipated in each of the three half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that RDS,ON increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

10 Device and Documentation Support

10.1 Documentation Support

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MCT8376Z0HQNLGRQ1	Active	Production	VQFN (NLG) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M8376HQ
MCT8376Z0SQNLGRQ1	Active	Production	VQFN (NLG) | 28	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M8376SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

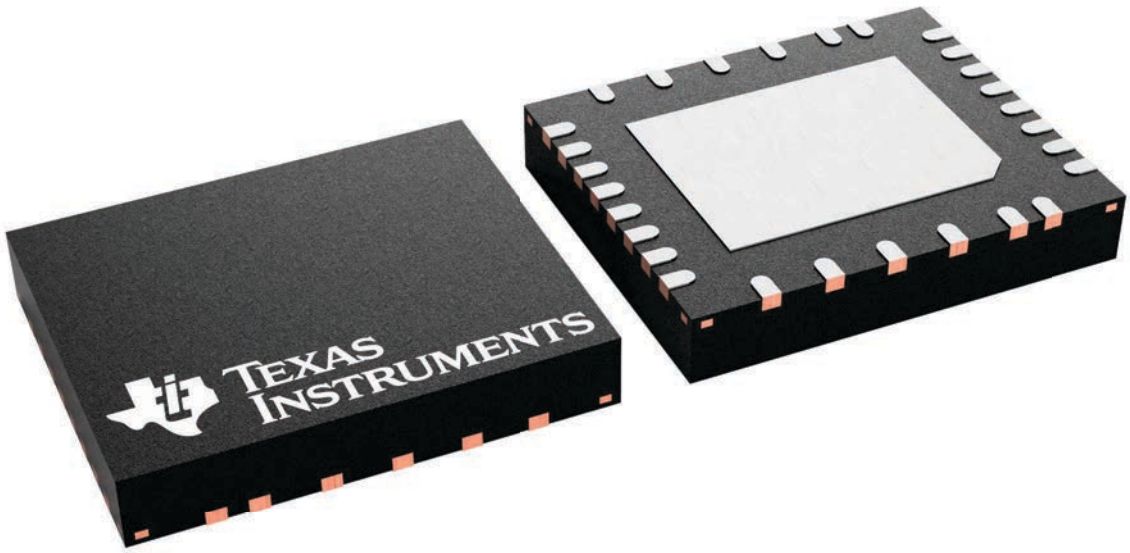
NLG 28

VQFN - 1 mm max height

5 x 6, 0.5 mm pitch

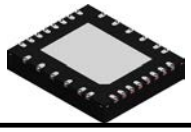
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230518/A

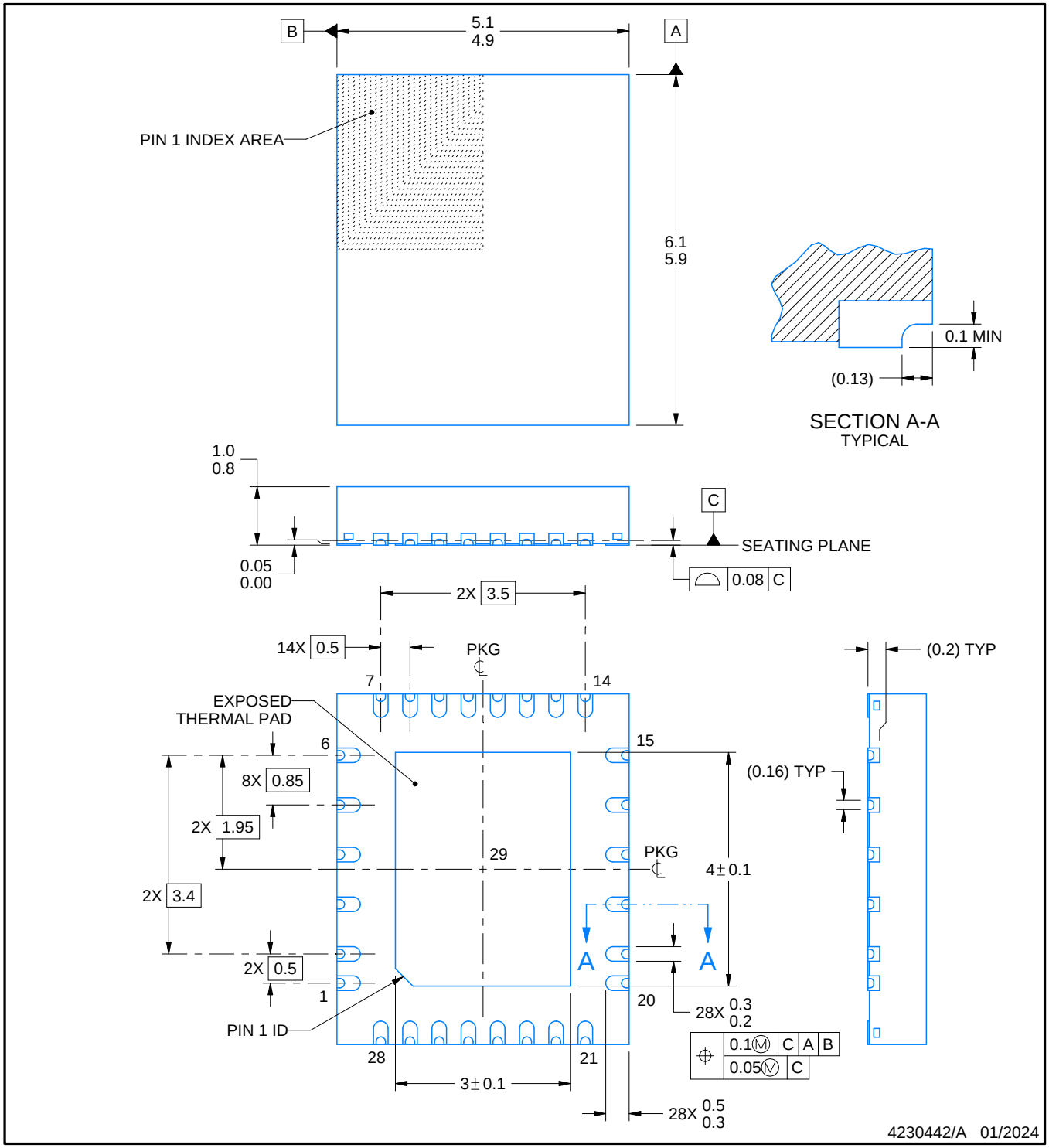
NLG0028A



PACKAGE OUTLINE

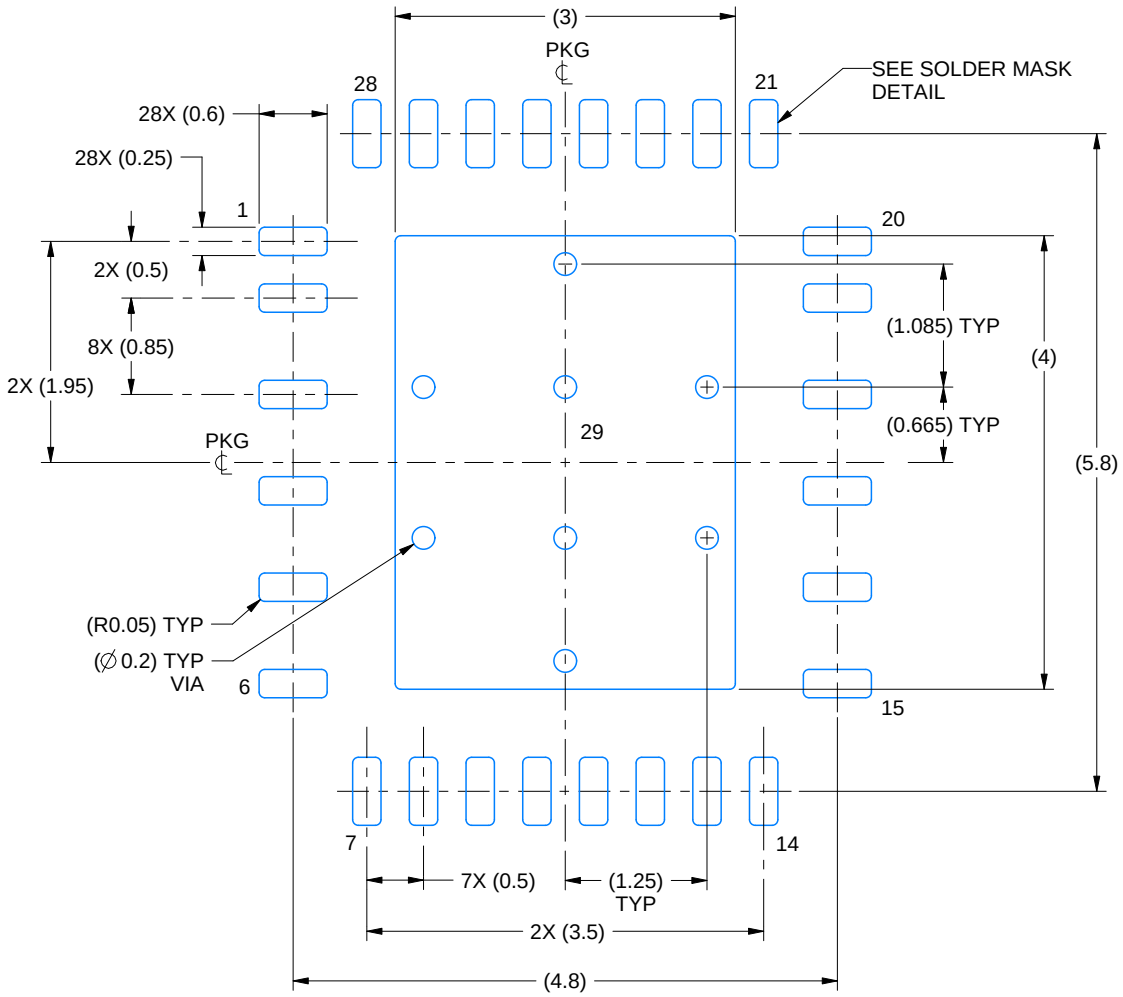
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

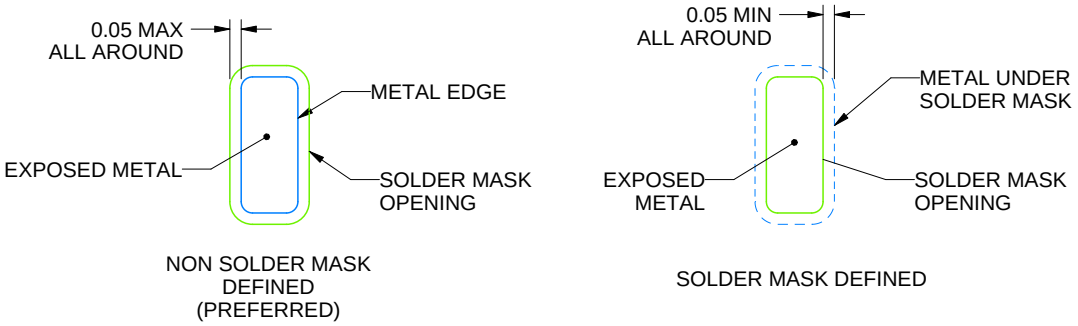


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

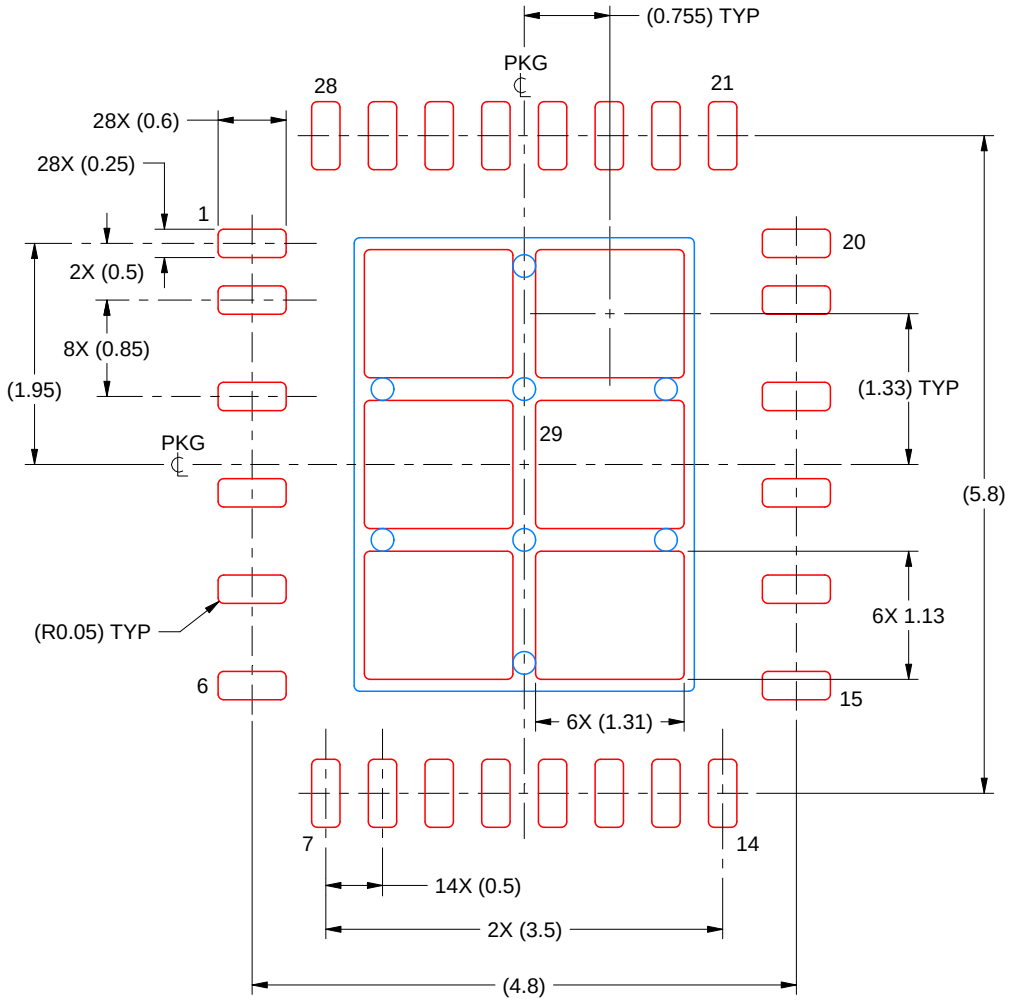
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

NLG0028A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 29
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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