



LPV511 Micropower, Rail-to-Rail Input and Output Operational Amplifier

1 Features

- Wide Supply Voltage Range: 2.7 V to 12 V
- Slew Rate: 7.7 V/ms
- Supply Current: 880 nA
- Output Short-Circuit Current: 1.35 mA
- Rail-to-Rail Input
- Rail-to-Rail Output: 100 mV from Rails
- Bandwidth ($C_L = 50$ pF, $R_L = 1$ M Ω): 27 kHz
- Unity Gain Stable

2 Applications

- Battery Powered Systems
- Security Systems
- Micropower Thermostats
- Solar Powered Systems
- Portable Instrumentation
- Micropower Filters
- Remote Sensor Amplifiers

3 Description

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7 V to 12 V with ensured specifications at 3 V, 5 V, and 12 V. The ultra-low power LPV511 exhibits an excellent speed to power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz. These specifications make the LPV511 an ideal choice for battery-powered systems that require long life through low supply current, such as instrumentation, sensor conditioning and battery current monitoring.

The LPV511 has an input range that includes both supply rails for ground and high-side battery sensing applications. The LPV511 output swings within 100 mV of either rail to maximize the signal's dynamic range in low supply applications. In addition, the output is capable of sourcing 650 μ A of current when powered by a 12-V battery.

The LPV511 is fabricated on TI's advanced VIP50C process.

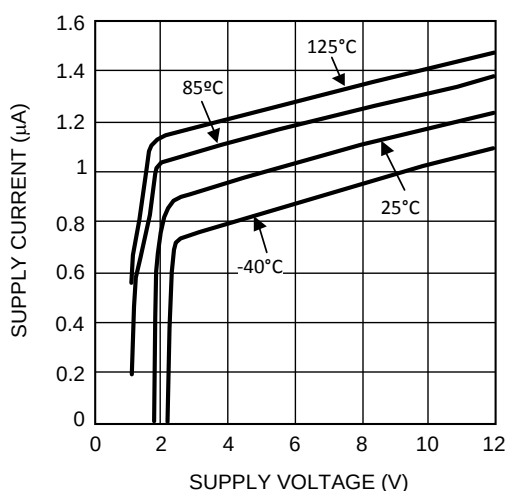
The LPV511 is available in the space-saving SC70 package, which makes it ideal for portable electronics with area-constrained PC boards.

Device Information⁽¹⁾

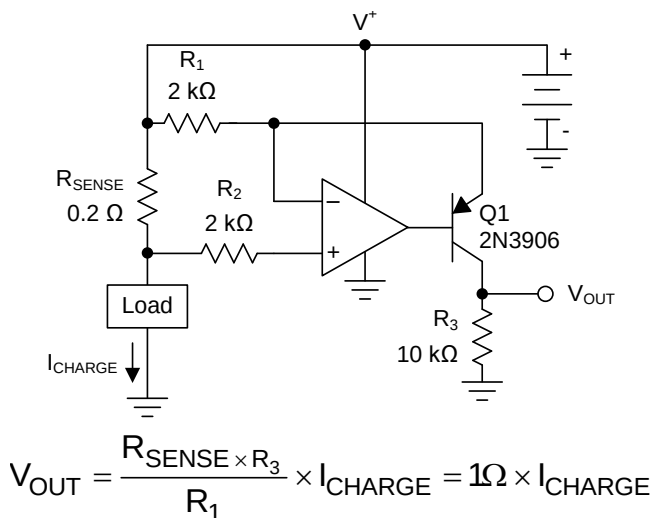
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LPV511	SC70 (5)	2.00 mm $\times$ 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Supply Current



High-Side Battery Current Sensor



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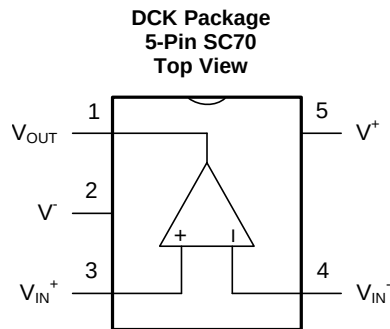
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D	Page
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Added Thermal Information table	4

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{OUT}	O	Output
2	V^{-}	P	Negative supply voltage
3	V_{IN}^{+}	I	Noninverting input
4	V_{IN}^{-}	I	Inverting input
5	V^{+}	P	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
V _{IN} Differential		2.1	V
Supply voltage (V ⁺ - V ⁻)		13.2	V
Voltage at input and output pins	V ⁺ + 0.3	V ⁻ - 0.3	V
Short-circuit duration	See ⁽³⁾		
Junction temperature, T _J ⁽⁴⁾		150	°C
Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Output short-circuit duration is infinite for V⁺ < 6 V at room temperature and below. For V⁺ > 6 V, allowable short-circuit duration is 1.5 ms.
- (4) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾⁽²⁾	±2000	V
	Machine model (MM) ⁽³⁾	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Human Body Model: 1.5 kΩ in series with 100 pF.
- (3) Machine Model: 0 Ω in series with 200 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature ⁽¹⁾	-40	85	°C
Supply voltage (V ⁺ - V ⁻)	2.7	12	V

- (1) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LPV511	UNIT
		DCK (SC70)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	278	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	105.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics: 3 V

Unless otherwise specified, all limits are specified for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\text{ k}\Omega$ to $V^+/2$.⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_{OS}	Input offset voltage	$T_J = 25^\circ\text{C}$			± 0.2	± 3	mV
		$T_J = -40^\circ\text{C}$ to 85°C				± 3.8	
TC V_{OS}	Input offset voltage drift ⁽⁴⁾	$T_J = 25^\circ\text{C}$			± 0.3		$\mu\text{V}/^\circ\text{C}$
		$T_J = -40^\circ\text{C}$ to 85°C				± 15	
I_B	Input bias current ⁽⁵⁾	$V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	-1000	-320		pA
			$T_J = -40^\circ\text{C}$ to 85°C	-1600			
		$V_{CM} = 2.5\text{ V}$	$T_J = 25^\circ\text{C}$		110	800	
			$T_J = -40^\circ\text{C}$ to 85°C			1900	
I_{OS}	Input offset current				± 10		pA
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 1.5 V	$T_J = 25^\circ\text{C}$	77	100		dB
			$T_J = -40^\circ\text{C}$ to 85°C	70			
		V_{CM} Stepped from 2.4 V to 3 V	$T_J = 25^\circ\text{C}$	75	115		
			$T_J = -40^\circ\text{C}$ to 85°C	68			
		V_{CM} Stepped from 0.5 V to 2.5 V	$T_J = 25^\circ\text{C}$	60	80		
			$T_J = -40^\circ\text{C}$ to 85°C	56			
PSRR	Power supply rejection ratio	$V^+ = 2.7\text{ V}$ to 5 V , $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	72	114		dB
			$T_J = -40^\circ\text{C}$ to 85°C	68			
		$V^+ = 3\text{ V}$ to 5 V , $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	76	115		
			$T_J = -40^\circ\text{C}$ to 85°C	72			
		$V^+ = 5\text{ V}$ to 12 V , $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	84	117		
			$T_J = -40^\circ\text{C}$ to 85°C	80			
CMVR	Input common-mode voltage	CMRR $\geq 50\text{ dB}$	$T_J = 25^\circ\text{C}$	-0.1		3.1	V
			$T_J = -40^\circ\text{C}$ to 85°C	0		3	
A_{VOL}	Large signal voltage gain	Sinking, $V_O = 2.5\text{ V}$	$T_J = 25^\circ\text{C}$	75	105		dB
			$T_J = -40^\circ\text{C}$ to 85°C	70			
		Sourcing, $V_O = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	75	105		
			$T_J = -40^\circ\text{C}$ to 85°C	70			
V_O	Output swing high	$V_{ID} = 100\text{ mV}$	$T_J = 25^\circ\text{C}$	2.85	2.9		V
			$T_J = -40^\circ\text{C}$ to 85°C	2.8			
	Output swing low	$V_{ID} = -100\text{ mV}$	$T_J = 25^\circ\text{C}$		100	150	
			$T_J = -40^\circ\text{C}$ to 85°C			200	
I_{SC}	Output short circuit current ⁽⁶⁾	Sourcing $V_{ID} = 100\text{ mV}$			-500	-225	μA
		Sinking $V_{ID} = -100\text{ mV}$		225	1350		
I_S	Supply current	$T_J = 25^\circ\text{C}$			0.88	1.2	μA
		$T_J = -40^\circ\text{C}$ to 85°C				1.5	
SR	Slew rate ⁽⁷⁾	$A_V = 1$, V_O ramps from 0.5 V to 2.5 V	$T_J = 25^\circ\text{C}$	5.25	7.7		V/ms
			$T_J = -40^\circ\text{C}$ to 85°C	3.10			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm at the time of characterization.

(4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

(5) Positive current corresponds to current flowing into the device.

(6) The Short-Circuit Test is a momentary test. See Note 3 in [Absolute Maximum Ratings](#).

(7) Slew rate is the average of the rising and falling slew rates.

Electrical Characteristics: 3 V (continued)

Unless otherwise specified, all limits are specified for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\text{ k}\Omega$ to $V^+/2$.⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
GBW	Gain bandwidth product	$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$	27		kHz
	Phase margin	$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$	53		°
e_n	Input-referred voltage noise	$f = 100\text{ Hz}$	320		nV/ $\sqrt{\text{Hz}}$
i_n	Input-referred current noise	$f = 10\text{ Hz}$	0.02		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	0.01		

6.6 Electrical Characteristics: 5 V

Unless otherwise specified, all limits are specified for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\text{ k}\Omega$ to $V^+/2$.⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_{OS}	Input offset voltage	$T_J = 25^\circ\text{C}$	± 0.2	± 3	mV
		$T_J = -40^\circ\text{C}$ to 85°C		± 3.8	
TC V_{OS}	Input offset voltage drift ⁽⁴⁾	$T_J = 25^\circ\text{C}$	± 0.3		$\mu\text{V}/^\circ\text{C}$
		$T_J = -40^\circ\text{C}$ to 85°C		± 15	
I_B	Input bias current ⁽⁵⁾	$V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	-1000	pA
			$T_J = -40^\circ\text{C}$ to 85°C	-1600	
		$V_{CM} = 4.5\text{ V}$	$T_J = 25^\circ\text{C}$	110	
			$T_J = -40^\circ\text{C}$ to 85°C	800	
I_{OS}	Input offset current		± 10		pA
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 2.5 V	$T_J = 25^\circ\text{C}$	80	dB
			$T_J = -40^\circ\text{C}$ to 85°C	115	
		V_{CM} Stepped from 4.4 to 5 V	$T_J = 25^\circ\text{C}$	75	
			$T_J = -40^\circ\text{C}$ to 85°C	107	
		V_{CM} Stepped from 0.5 to 4.5 V	$T_J = 25^\circ\text{C}$	65	
			$T_J = -40^\circ\text{C}$ to 85°C	87	
PSRR	Power supply rejection ratio	$V^+ = 2.7\text{ V}$ to 5 V , $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	72	dB
			$T_J = -40^\circ\text{C}$ to 85°C	114	
		$V^+ = 3\text{ V}$ to 5 V , $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	68	
			$T_J = -40^\circ\text{C}$ to 85°C	115	
		$V^+ = 5\text{ V}$ to 12 V , $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	76	
			$T_J = -40^\circ\text{C}$ to 85°C	117	
CMVR	Input common-mode voltage	CMRR $\geq 50\text{ dB}$	$T_J = 25^\circ\text{C}$	-0.1	V
			$T_J = -40^\circ\text{C}$ to 85°C	5.1	
A_{VOL}	Large signal voltage gain	Sinking, $V_O = 4.5\text{ V}$	$T_J = 25^\circ\text{C}$	0	dB
			$T_J = -40^\circ\text{C}$ to 85°C	5	
		Sourcing, $V_O = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	78	
			$T_J = -40^\circ\text{C}$ to 85°C	110	

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
- (3) Typical values represent the most likely parametric norm at the time of characterization.
- (4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
- (5) Positive current corresponds to current flowing into the device.

Electrical Characteristics: 5 V (continued)

Unless otherwise specified, all limits are specified for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\text{ k}\Omega$ to $V^+/2$.⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_O	Output swing high	$V_{ID} = 100\text{ mV}$	$T_J = 25^\circ\text{C}$	4.8	4.89		V
			$T_J = -40^\circ\text{C}$ to 85°C	4.75			
	Output swing low	$V_{ID} = -100\text{ mV}$	$T_J = 25^\circ\text{C}$		110	200	mV
			$T_J = -40^\circ\text{C}$ to 85°C			250	
I_{SC}	Output short circuit current ⁽⁶⁾	Sourcing to V^- $V_{ID} = 100\text{ mV}$			-550	-225	μA
		Sinking to V^+ $V_{ID} = -100\text{ mV}$		225	1350		
I_S	Supply current	$T_J = 25^\circ\text{C}$			0.97	1.2	μA
		$T_J = -40^\circ\text{C}$ to 85°C				1.5	
SR	Slew rate ⁽⁷⁾	$A_V = 1$, V_O ramps from 0.5 V to 4.5 V	$T_J = 25^\circ\text{C}$	5.25	7.5		V/ms
			$T_J = -40^\circ\text{C}$ to 85°C	3.1			
GBW	Gain bandwidth product	$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$			27		kHz
	Phase margin	$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$			53		°
e_n	Input-referred voltage noise	$f = 100\text{ Hz}$			320		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input-referred current noise	$f = 10\text{ Hz}$			0.02		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			0.01		

(6) The Short-Circuit Test is a momentary test. See Note 3 in [Absolute Maximum Ratings](#).

(7) Slew rate is the average of the rising and falling slew rates.

6.7 Electrical Characteristics: 12 V

Unless otherwise specified, all limits are specified for $T_J = 25^\circ\text{C}$, $V^+ = 12\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\text{ k}\Omega$ to $V^+/2$.⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_{OS}	Input offset voltage	$T_J = 25^\circ\text{C}$			± 0.2	± 3	mV
		$T_J = -40^\circ\text{C}$ to 85°C				± 3.8	
TC V_{OS}	Input offset voltage drift ⁽⁴⁾	$T_J = 25^\circ\text{C}$			± 0.3		$\mu\text{V}/^\circ\text{C}$
		$T_J = -40^\circ\text{C}$ to 85°C				± 15	
I_B	Input bias current ⁽⁵⁾	$V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	-1000	-320		pA
			$T_J = -40^\circ\text{C}$ to 85°C	-1600			
		$V_{CM} = 11.5\text{ V}$	$T_J = 25^\circ\text{C}$		110	800	
			$T_J = -40^\circ\text{C}$ to 85°C			1900	
I_{OS}	Input offset current				± 10		pA
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 6 V	$T_J = 25^\circ\text{C}$	75	115		dB
			$T_J = -40^\circ\text{C}$ to 85°C	70			
		V_{CM} Stepped from 11.4 V to 12 V	$T_J = 25^\circ\text{C}$	75	110		
			$T_J = -40^\circ\text{C}$ to 85°C	68			
		V_{CM} Stepped from 0.5 V to 11.5 V	$T_J = 25^\circ\text{C}$	70	97		
			$T_J = -40^\circ\text{C}$ to 85°C	65			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm at the time of characterization.

(4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

(5) Positive current corresponds to current flowing into the device.

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Electrical Characteristics: 12 V (continued)

Unless otherwise specified, all limits are specified for $T_J = 25^\circ\text{C}$, $V^+ = 12\text{ V}$, $V^- = 0\text{ V}$, $V_{CM} = V_O = V^+/2$, and $R_L = 100\text{ k}\Omega$ to $V^+/2$.⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
PSRR	Power supply rejection ratio	$V^+ = 2.7\text{ V to }5\text{ V}$, $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	72	114	
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	68		
		$V^+ = 3\text{ V to }5\text{ V}$, $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	76	115	
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	72		
		$V^+ = 5\text{ V to }12\text{ V}$, $V_{CM} = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	84	117	
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	80		
CMVR	Input common-mode voltage	CMRR $\geq 50\text{ dB}$	$T_J = 25^\circ\text{C}$	-0.1	12.1	V
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	0	12	
A _{VOL}	Large signal voltage gain	Sinking, $V_O = 0.5\text{ V}$	$T_J = 25^\circ\text{C}$	89	110	dB
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	84		
		Sourcing, $V_O = 11.5\text{ V}$	$T_J = 25^\circ\text{C}$	89	110	
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	84		
V _O	Output swing high	$V_{ID} = 100\text{ mV}$	$T_J = 25^\circ\text{C}$	11.8	11.85	V
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	11.72		
	Output swing low	$V_{ID} = -100\text{ mV}$	$T_J = 25^\circ\text{C}$		150	mV
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$		280	
I _{SC}	Output short circuit current ⁽⁶⁾	Sourcing $V_{ID} = 100\text{ mV}$		-650	-200	μA
		Sinking $V_{ID} = -100\text{ mV}$	200	1300		
I _S	Supply current	$T_J = 25^\circ\text{C}$		1.2	1.75	μA
		$T_J = -40^\circ\text{C to }85^\circ\text{C}$			2.5	
SR	Slew rate ⁽⁷⁾	$A_V = 1$, V_O ramped from 1 V to 11 V		5.25	7	V/ms
				3.1		
GBW	Gain bandwidth product	$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$		25		kHz
	Phase margin	$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$		52		°
e _n	Input-referred voltage noise	$f = 100\text{ Hz}$		320		nV/ $\sqrt{\text{Hz}}$
i _n	Input-referred current noise	$f = 10\text{ Hz}$		0.02		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.01		

(6) The Short-Circuit Test is a momentary test. See Note 3 in [Absolute Maximum Ratings](#).

(7) Slew rate is the average of the rising and falling slew rates.

6.8 Typical Characteristics

At $T_j = 25^\circ\text{C}$, unless otherwise specified.

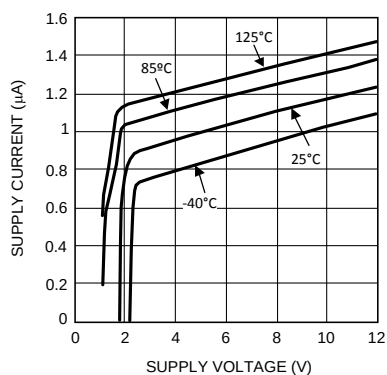


Figure 1. Supply Current vs Supply Voltage

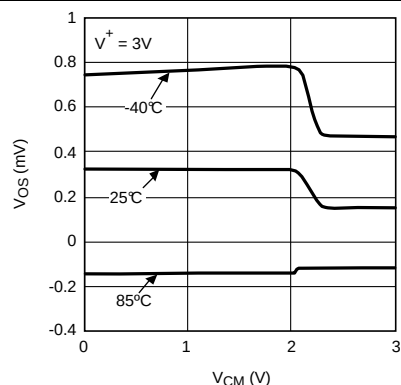


Figure 2. Input Offset Voltage vs Input Common Mode

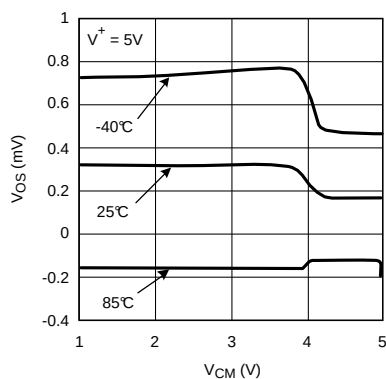


Figure 3. Input Offset Voltage vs Input Common Mode

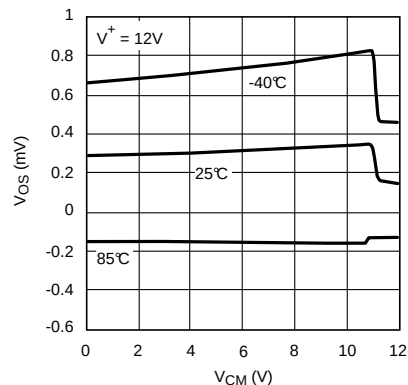


Figure 4. Input Offset Voltage vs Input Common Mode

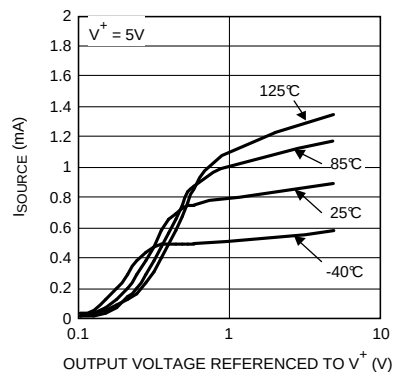


Figure 5. Sourcing Current vs Output Voltage

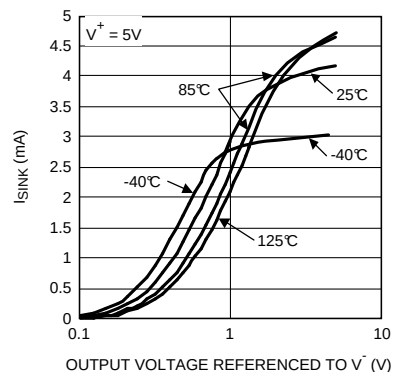


Figure 6. Sinking Current vs Output Voltage

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, unless otherwise specified.

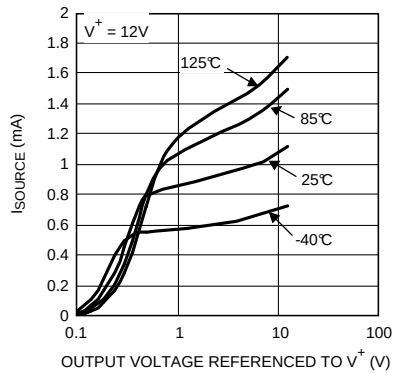


Figure 7. Sourcing Current vs Output Voltage

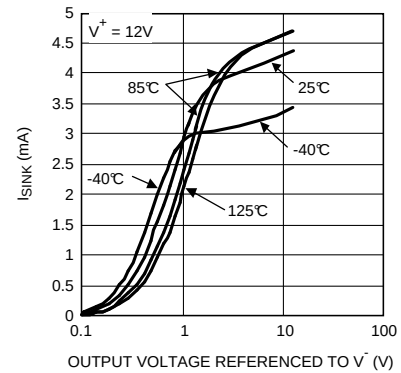


Figure 8. Sinking Current vs Output Voltage

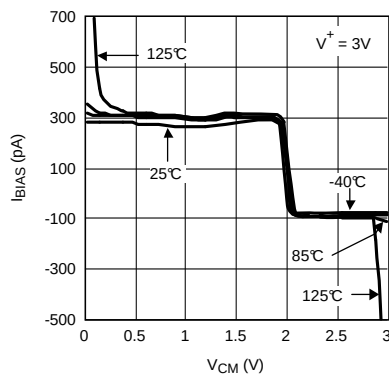


Figure 9. Input Bias Current vs Common Mode Voltage

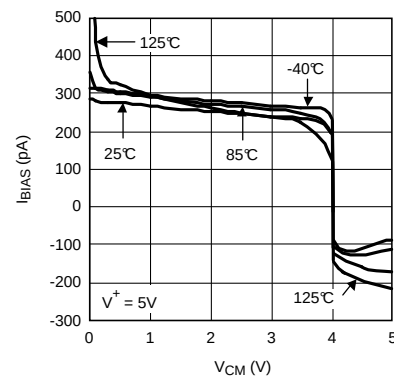


Figure 10. Input Bias Current vs Common Mode Voltage

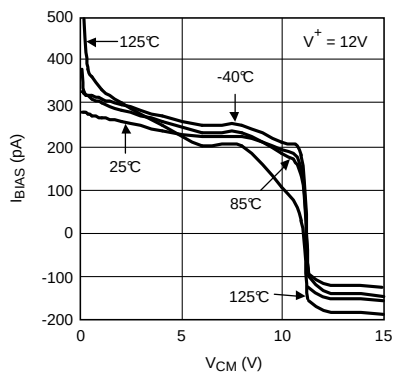


Figure 11. Input Bias Current vs Common Mode Voltage

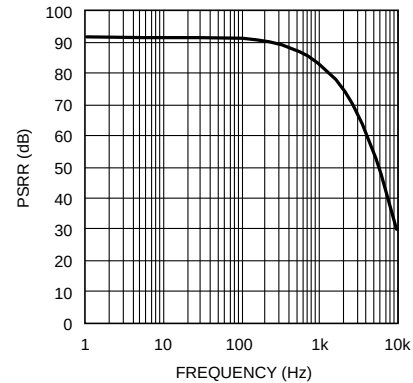


Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, unless otherwise specified.

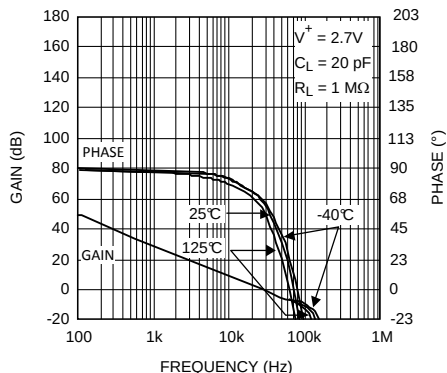


Figure 13. Frequency Response vs Temperature

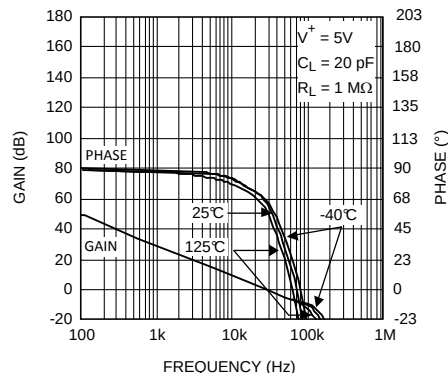


Figure 14. Frequency Response vs Temperature

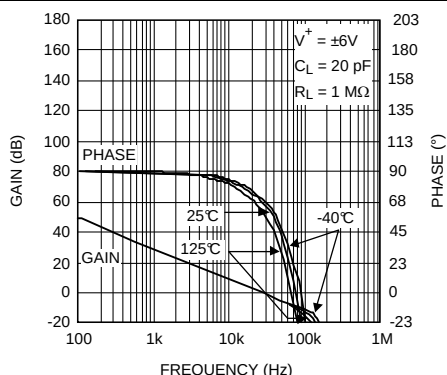


Figure 15. Frequency Response vs Temperature

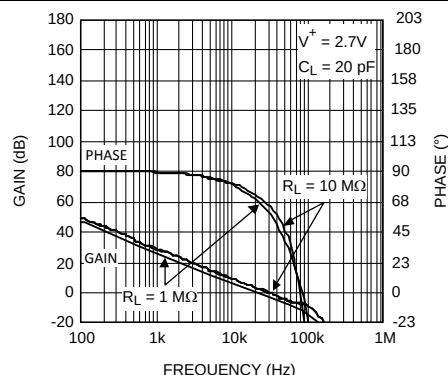


Figure 16. Frequency Response vs R_L

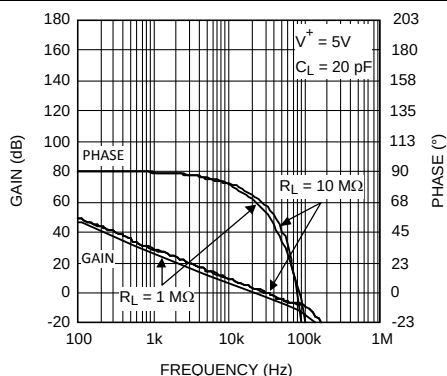


Figure 17. Frequency Response vs R_L

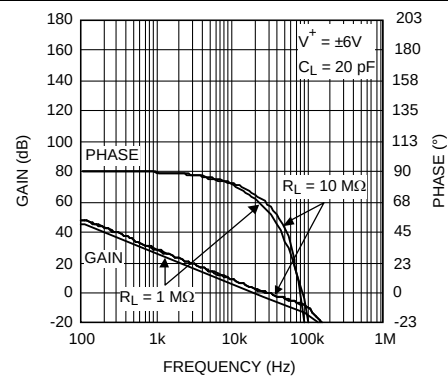


Figure 18. Frequency Response vs R_L

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, unless otherwise specified.

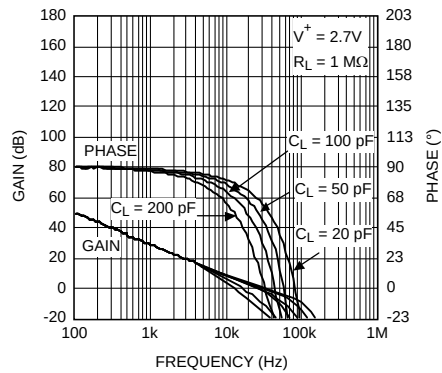


Figure 19. Frequency Response vs C_L

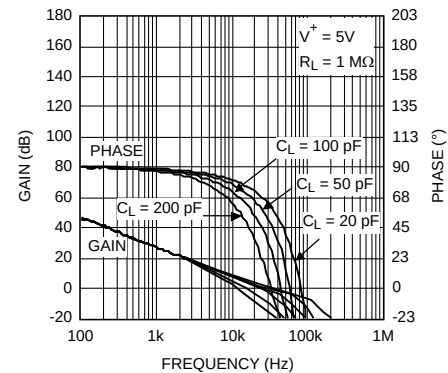


Figure 20. Frequency Response vs C_L

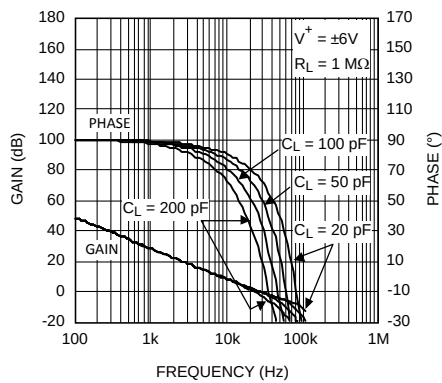


Figure 21. Frequency Response vs C_L

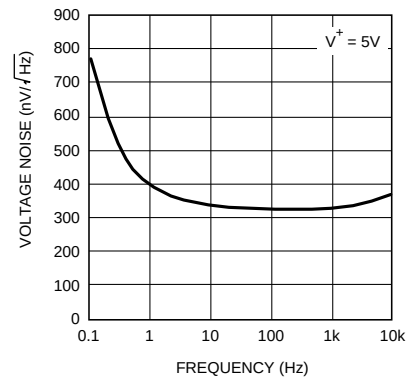


Figure 22. Voltage Noise vs Frequency

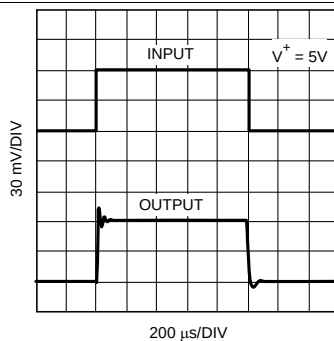


Figure 23. Noninverting Small-Signal Pulse Response

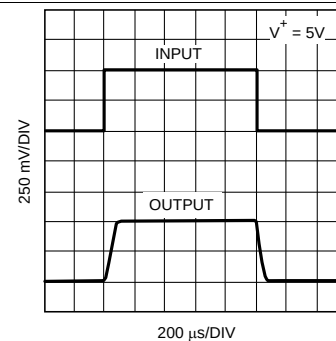


Figure 24. Noninverting Large-Signal Pulse Response

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, unless otherwise specified.

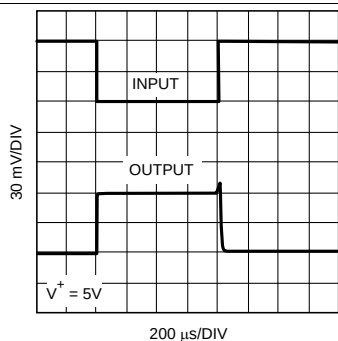


Figure 25. Inverting Small-Signal Pulse Response

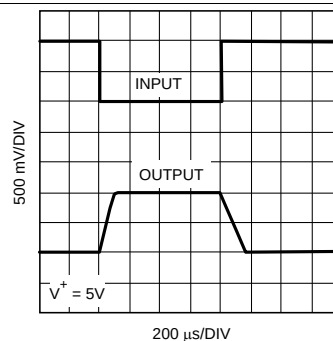


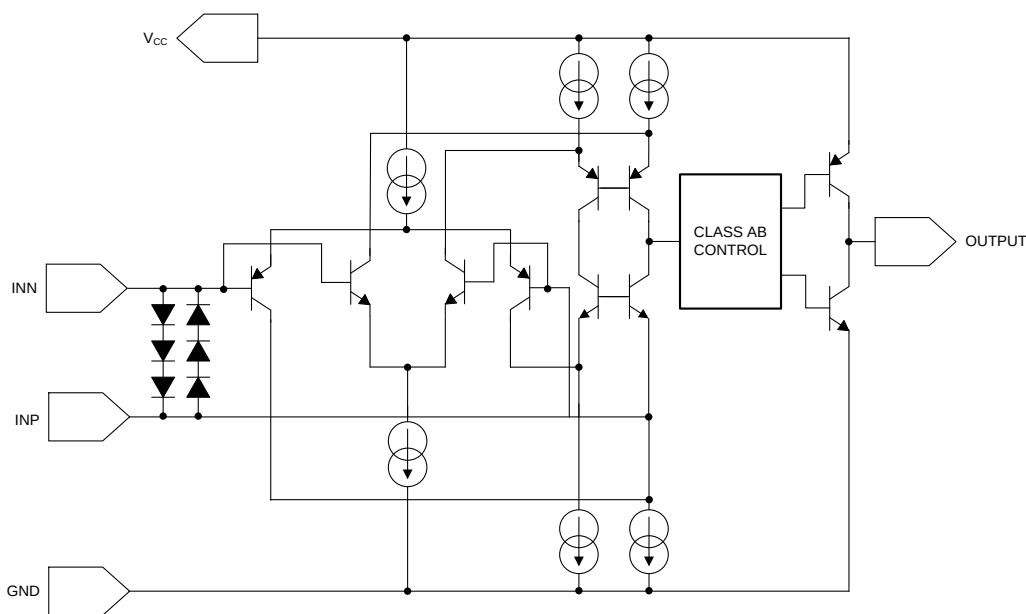
Figure 26. Inverting Large-Signal Pulse Response

7 Detailed Description

7.1 Overview

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7 V to 12 V with ensured specifications at 3 V, 5 V, and 12 V. The LPV511 exhibits an excellent speed-to-power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz.

7.2 Functional Block Diagram



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7.3 Feature Description

The LPV511 has a rail-to-rail input which provides more flexibility for the system designer. As can be seen from [Functional Block Diagram](#), rail-to-rail input is achieved by using in parallel, one PNP differential pair and one NPN differential pair. When the common mode input voltage (V_{CM}) is near V^+ , the NPN pair is on and the PNP pair is off. When V_{CM} is near V^- , the NPN pair is off and the PNP pair is on. When V_{CM} is between V^+ and V^- , internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

7.4 Device Functional Modes

7.4.1 Input Stage

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LPV511 becomes a function of V_{CM} . V_{OS} has a crossover point at 1 V below V^+ . See the V_{OS} vs V_{CM} curve in [Typical Characteristics](#). Caution must be taken in situations where the input signal amplitude is comparable to the V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The input bias current, I_B will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in V_{CM} across the differential pair transition region.

Differential input voltage is the difference in voltage between the noninverting (+) input and the inverting input (–) of the op amp. Due to the three series diodes across the two inputs, the absolute maximum differential input voltage is ± 2.1 V. This may not be a problem to most conventional op amp designs; however, designers **must avoid using the LPV511 as a comparator**.

Device Functional Modes (continued)

7.4.2 Output Stage

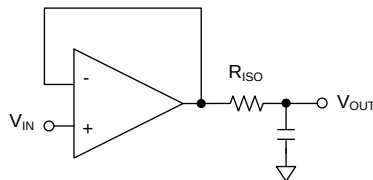
The LPV511 output voltage swing 100 mV from rails at 3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV511 maximum output voltage swing defines the maximum swing possible under a particular output load. The LPV511 output swings 110 mV from the rail at 5-V supply with an output load of 100 k Ω .

7.4.3 Driving Capacitive Load

The LPV511 is internally compensated for stable unity gain operation, with a 27-kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of the op amp. When the output is required to drive a large capacitive load, greater than 100 pF, a small series resistor at the output of the amplifier improves the phase margin (see [Figure 27](#)).

In [Figure 27](#), the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO} . The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. But the DC accuracy is degraded when the R_{ISO} gets bigger. If there were a load resistor in [Figure 27](#), the output voltage would be divided by R_{ISO} and the load resistor.



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Figure 27. Resistive Isolation of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

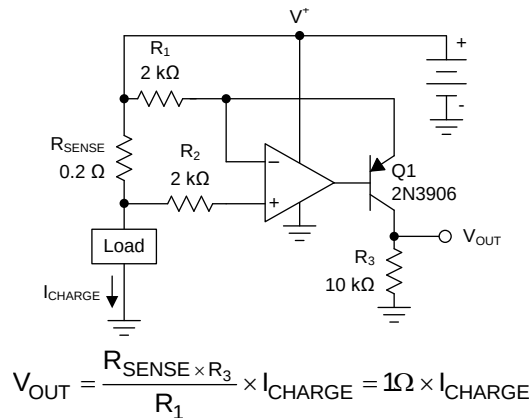
8.1 Application Information

The LPV511 is fabricated with Texas Instrument's state-of-the-art VIP50C process.

8.2 Typical Applications

8.2.1 Battery Current Sensing

The rail-to-rail common mode input range and the very low quiescent current make the LPV511 ideal to use in high-side and low-side battery current sensing applications. The high-side current sensing circuit in [Figure 28](#) is commonly used in a battery charger to monitor the charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly.



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Figure 28. High Side Current Sensing

8.2.1.1 Design Requirements

The high-side current-sensing circuit ([Figure 28](#)) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LPV511 is ideal for this application because its common-mode input range extends up to the positive supply.

8.2.1.2 Detailed Design Procedure

As seen in [Figure 28](#), the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE} . The voltage at the negative sense point will now be less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LPV511 cause little voltage drop through R_2 , so the negative input of the LPV511 amplifier is at essentially the same potential as the negative sense input.

The LPV511 will detect this voltage error between its inputs and servo the transistor base to conduct more current through $Q1$, increasing the voltage drop across R_1 until the LPV511 inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE} .

I_G , a current proportional to I_{CHARGE} , will flow according to the following relation to:

$$I_G = V_{SENSE} / R_1 = (R_{SENSE} \times I_{CHARGE}) / R_1 \quad (1)$$

Typical Applications (continued)

I_G also flows through the gain resistor R_3 developing a voltage drop equal to:

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3 \quad (2)$$

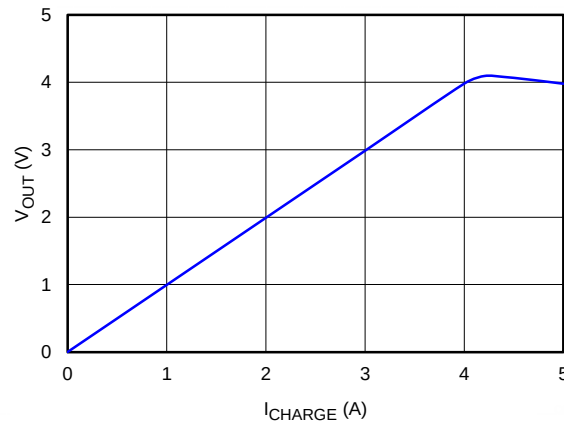
$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$

where

$$G = R_3 / R_1 \quad (3)$$

8.2.1.3 Application Curve

Figure 29 shows the results of the example current sense circuit.



The error after 4 V where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

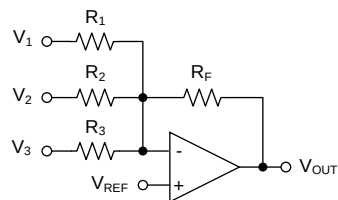
Figure 29. Current Sense Amplifier Results

8.2.2 Summing Amplifier

The LPV511 operational amplifier is a perfect fit in a summing amplifier circuit because of the rail-to-rail input and output and the sub-micro Amp quiescent current. In this configuration, the amplifier outputs the sum of the three input voltages.

Equation 4 shows the ratio of the sum and the output voltage is defined using feedback and input resistors.

$$V_{OUT} = R_F \left(\frac{V_{REF} - V_1}{R_1} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3} \right) + V_{REF} \quad (4)$$



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Figure 30. Summing Amplifier Circuit

8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

The LPV80x is specified for operation from 1.6 V to 5.5 V (± 0.8 V to ± 2.75 V) over a -40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Electrical Characteristics: 3 V](#).

CAUTION

Supply voltages larger than 13.2 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^{+} and V^{-} supply leads. For dual supplies, place one capacitor between V^{+} and ground, and one capacitor between V^{-} and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

- The V^{+} pin should be bypassed to ground with a low-ESR capacitor.
- The optimum placement is closest to the V^{+} and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between V^{+} and ground.
- The ground pin should be connected to the PCB ground plane at the pin of the device.
- The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

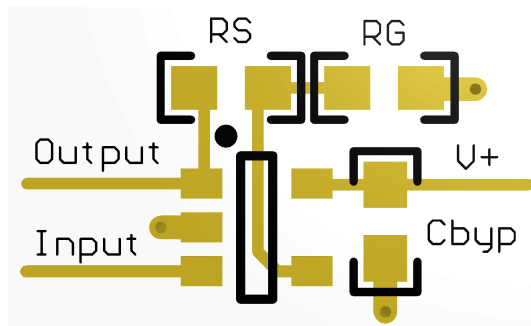


Figure 31. SOT-23 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LPV511 PSICE Model, <http://www.ti.com/lit/zip/snom023>

TINA-TI SPICE-Based Analog Simulation Program, <http://www.ti.com/tool/tina-ti>

DIP Adapter Evaluation Module, <http://www.ti.com/tool/dip-adapter-evm>

TI Universal Operational Amplifier Evaluation Module, <http://www.ti.com/tool/opampevm>

TI Filterpro Software, <http://www.ti.com/tool/filterpro>

11.2 Documentation Support

11.2.1 Related Documentation

- *Handbook of Operational Amplifier Applications* (SBOA092)
- *Compensate Transimpedance Amplifiers Intuitively* (SBOA055)
- *Circuit Board Layout Techniques* (SLOA089)
- *AN-1803 Design Considerations for a Transimpedance Amplifier* (SNOA515)

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LPV511MG/NOPB	Active	Production	SC70 (DCK) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91
LPV511MG/NOPB.A	Active	Production	SC70 (DCK) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91
LPV511MGX/NOPB	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91
LPV511MGX/NOPB.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

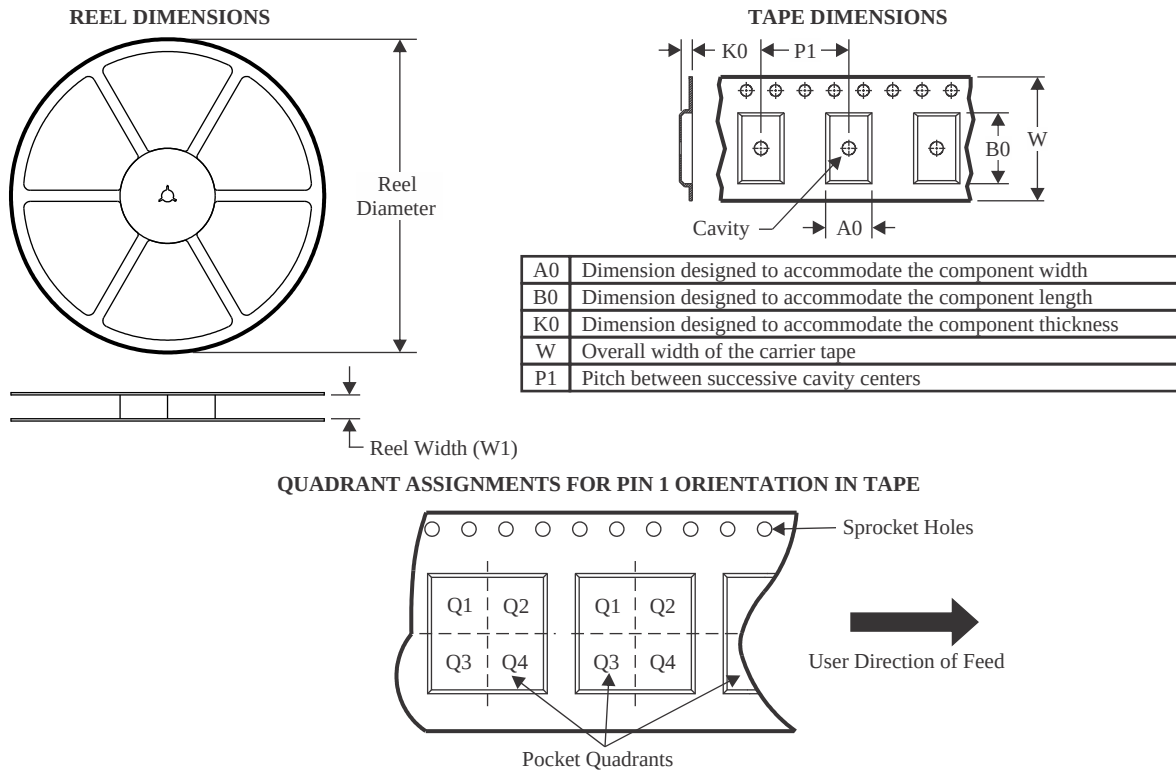
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

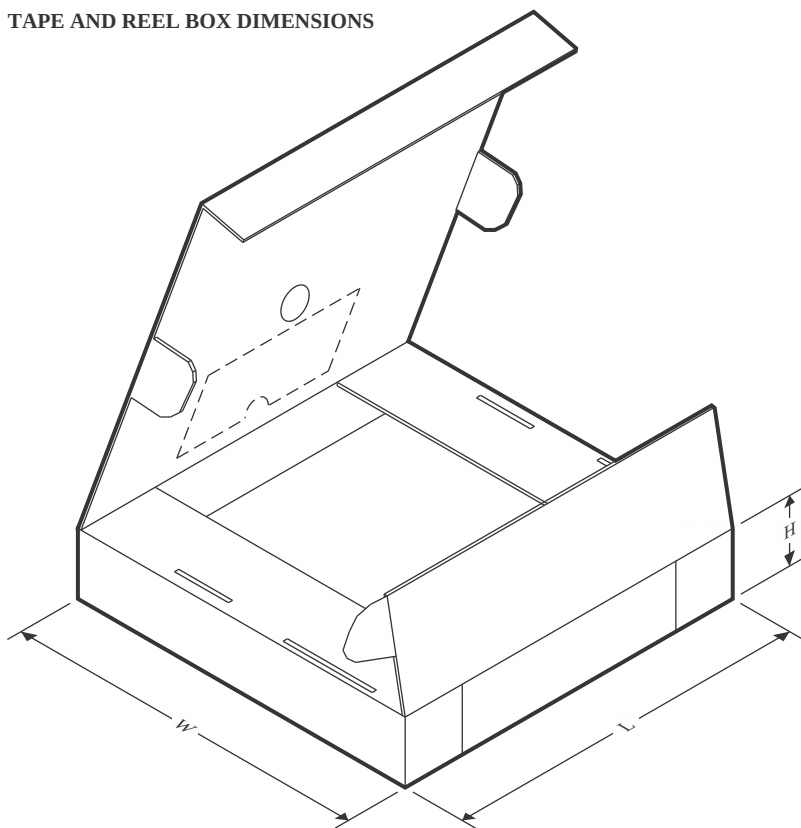
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV511MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV511MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV511MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LPV511MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0



SOT - 1.1 max height

Technical drawing of a mechanical part showing three views: front, side, and top.

Front View:

- Overall dimensions: 2.4 x 1.8
- Mounting holes: 1.4 x 1.1
- Central feature: 1.3 x 1.3
- Pin 1 Index Area: Indicated by a dashed line and a callout.
- NOTE 4: (0.15) and (0.1)
- Surface finish: 0.15 (dashed line)
- Feature 1: 1.3 x 0.65
- Feature 2: 1.3 x 0.65
- Feature 3: 1.3 x 0.65
- Feature 4: 1.3 x 0.65
- Feature 5: 1.3 x 0.65

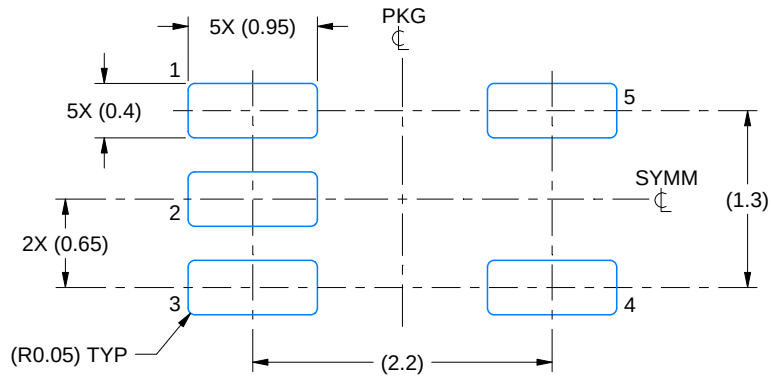
Side View:

- Overall dimensions: 1.1 MAX x 2.15
- Feature 1: 1.1 MAX
- Feature 2: 0.1 C
- Feature 3: 0.1 C
- Feature 4: 0.1 C
- Feature 5: 0.1 C
- Feature 6: 0.1 C
- Feature 7: 0.1 C
- Feature 8: 0.1 C
- Feature 9: 0.1 C
- Feature 10: 0.1 C
- Feature 11: 0.1 C
- Feature 12: 0.1 C
- Feature 13: 0.1 C
- Feature 14: 0.1 C
- Feature 15: 0.1 C
- Feature 16: 0.1 C
- Feature 17: 0.1 C
- Feature 18: 0.1 C
- Feature 19: 0.1 C
- Feature 20: 0.1 C
- Feature 21: 0.1 C
- Feature 22: 0.1 C
- Feature 23: 0.1 C
- Feature 24: 0.1 C
- Feature 25: 0.1 C
- Feature 26: 0.1 C
- Feature 27: 0.1 C
- Feature 28: 0.1 C
- Feature 29: 0.1 C
- Feature 30: 0.1 C
- Feature 31: 0.1 C
- Feature 32: 0.1 C
- Feature 33: 0.1 C
- Feature 34: 0.1 C
- Feature 35: 0.1 C
- Feature 36: 0.1 C
- Feature 37: 0.1 C
- Feature 38: 0.1 C
- Feature 39: 0.1 C
- Feature 40: 0.1 C
- Feature 41: 0.1 C
- Feature 42: 0.1 C
- Feature 43: 0.1 C
- Feature 44: 0.1 C
- Feature 45: 0.1 C
- Feature 46: 0.1 C
- Feature 47: 0.1 C
- Feature 48: 0.1 C
- Feature 49: 0.1 C
- Feature 50: 0.1 C
- Feature 51: 0.1 C
- Feature 52: 0.1 C
- Feature 53: 0.1 C
- Feature 54: 0.1 C
- Feature 55: 0.1 C
- Feature 56: 0.1 C
- Feature 57: 0.1 C
- Feature 58: 0.1 C
- Feature 59: 0.1 C
- Feature 60: 0.1 C
- Feature 61: 0.1 C
- Feature 62: 0.1 C
- Feature 63: 0.1 C
- Feature 64: 0.1 C
- Feature 65: 0.1 C
- Feature 66: 0.1 C
- Feature 67: 0.1 C
- Feature 68: 0.1 C
- Feature 69: 0.1 C
- Feature 70: 0.1 C
- Feature 71: 0.1 C
- Feature 72: 0.1 C
- Feature 73: 0.1 C
- Feature 74: 0.1 C
- Feature 75: 0.1 C
- Feature 76: 0.1 C
- Feature 77: 0.1 C
- Feature 78: 0.1 C
- Feature 79: 0.1 C
- Feature 80: 0.1 C
- Feature 81: 0.1 C
- Feature 82: 0.1 C
- Feature 83: 0.1 C
- Feature 84: 0.1 C
- Feature 85: 0.1 C
- Feature 86: 0.1 C
- Feature 87: 0.1 C
- Feature 88: 0.1 C
- Feature 89: 0.1 C
- Feature 90: 0.1 C
- Feature 91: 0.1 C
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- Feature 93: 0.1 C
- Feature 94: 0.1 C
- Feature 95: 0.1 C
- Feature 96: 0.1 C
- Feature 97: 0.1 C
- Feature 98: 0.1 C
- Feature 99: 0.1 C
- Feature 100: 0.1 C

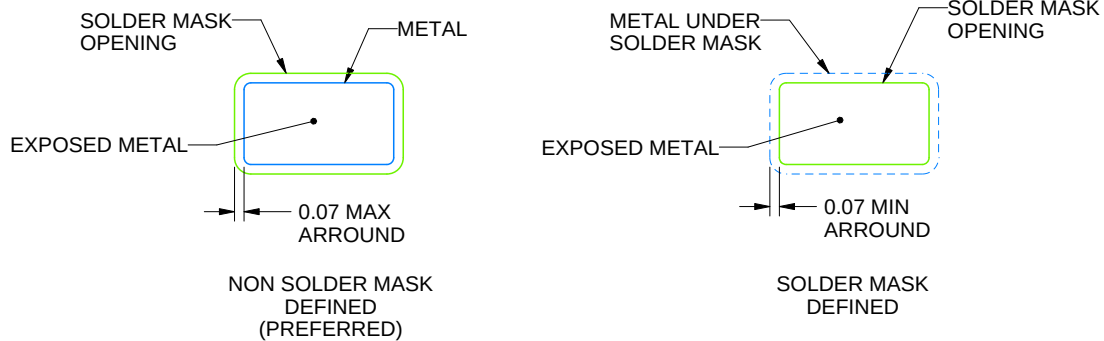
Top View:

- Overall dimensions: 0.9 x 0.1
- Feature 1: 0.9
- Feature 2: 0.1
- Feature 3: 0.1
- Feature 4: 0.1
- Feature 5: 0.1
- Feature 6: 0.1
- Feature 7: 0.1
- Feature 8: 0.1
- Feature 9: 0.1
- Feature 10: 0.1
- Feature 11: 0.1
- Feature 12: 0.1
- Feature 13: 0.1
- Feature 14: 0.1
- Feature 15: 0.1
- Feature 16: 0.1
- Feature 17: 0.1
- Feature 18: 0.1
- Feature 19: 0.1
- Feature 20: 0.1
- Feature 21: 0.1
- Feature 22: 0.1
- Feature 23: 0.1
- Feature 24: 0.1
- Feature 25: 0.1
- Feature 26: 0.1
- Feature 27: 0.1
- Feature 28: 0.1
- Feature 29: 0.1
- Feature 30: 0.1
- Feature 31: 0.1
- Feature 32: 0.1
- Feature 33: 0.1
- Feature 34: 0.1
- Feature 35: 0.1
- Feature 36: 0.1
- Feature 37: 0.1
- Feature 38: 0.1
- Feature 39: 0.1
- Feature 40: 0.1
- Feature 41: 0.1
- Feature 42: 0.1
- Feature 43: 0.1
- Feature 44: 0.1
- Feature 45: 0.1
- Feature 46: 0.1
- Feature 47: 0.1
- Feature 48: 0.1
- Feature 49: 0.1
- Feature 50: 0.1
- Feature 51: 0.1
- Feature 52: 0.1
- Feature 53: 0.1
- Feature 54: 0.1
- Feature 55: 0.1
- Feature 56: 0.1
- Feature 57: 0.1
- Feature 58: 0.1
- Feature 59: 0.1
- Feature 60: 0.1
- Feature 61: 0.1
- Feature 62: 0.1
- Feature 63: 0.1
- Feature 64: 0.1
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- Feature 66: 0.1
- Feature 67: 0.1
- Feature 68: 0.1
- Feature 69: 0.1
- Feature 70: 0.1
- Feature 71: 0.1
- Feature 72: 0.1
- Feature 73: 0.1
- Feature 74: 0.1
- Feature 75: 0.1
- Feature 76: 0.1
- Feature 77: 0.1
- Feature 78: 0.1
- Feature 79: 0.1
- Feature 80: 0.1
- Feature 81: 0.1
- Feature 82: 0.1
- Feature 83: 0.1
- Feature 84: 0.1
- Feature 85: 0.1
- Feature 86: 0.1
- Feature 87: 0.1
- Feature 88: 0.1
- Feature 89: 0.1
- Feature 90: 0.1
- Feature 91: 0.1
- Feature 92: 0.1
- Feature 93: 0.1
- Feature 94: 0.1
- Feature 95: 0.1
- Feature 96: 0.1
- Feature 97: 0.1
- Feature 98: 0.1
- Feature 99: 0.1
- Feature 100: 0.1

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

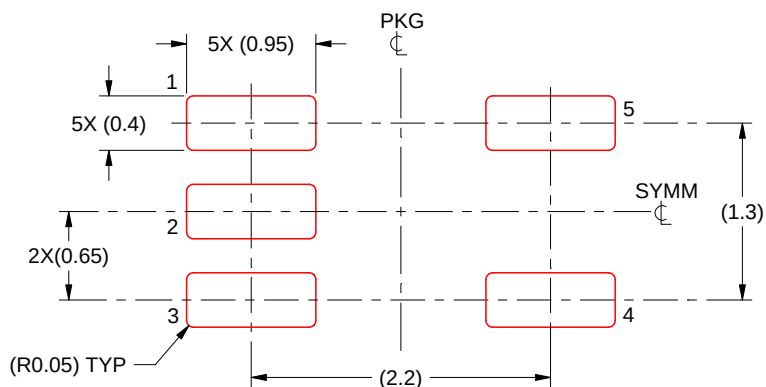


SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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