LPV321-N Single, LPV358-N Dual, and LPV324-N Quad General-Purpose, Low Voltage, Low Power, Rail-to-Rail Output Operational Amplifiers

1 Features

- Specified 2.7-V and 5-V Performance
- No Crossover Distortion
- Space-Saving Package
  - 5-Pin SC70 2 × 2.1 × 1 mm
- Industrial Temperature Range: −40°C to 85°C
- Gain-Bandwidth Product: 152 kHz
- Low Supply Current
  - LPV321-N: 9 µA
  - LPV358-N: 15 µA
  - LPV324-N: 28 µA
- Rail-to-Rail Output Swing at 100 kΩ Load:
  - $V^+ - 3.5$ mV
  - $V^- + 90$ mV
- V_{CM}, −0.2 V to $V^+ - 0.8$ V

2 Applications

- Active Filters
- General-Purpose Low Voltage Applications
- General-Purpose Portable Devices

3 Description

The LPV3xx-N are low power (9-µA per channel at 5 V) versions of the LMV3xx op amps. This is another addition to the LMV family of commodity op amps.

The LPV3xx-N are the most cost effective solutions for the applications where low voltage, low power operation, space saving and low price are needed. The LPV3xx-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratio, achieving 152 kHz of bandwidth with a supply current of only 9 µA.

The LPV321-N is available in space saving 5-Pin SC70, which is approximately half the size of 5-Pin SOT-23. The small package saves space on PC boards, and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

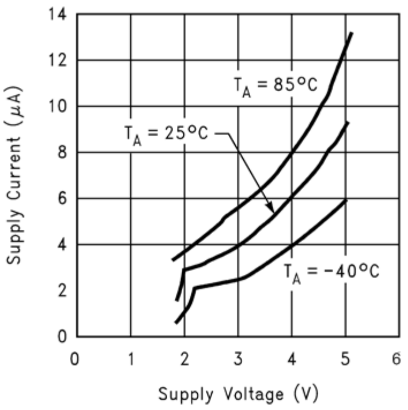
The chips are built with Texas Instruments's advanced submicron silicon-gate BiCMOS process. The LPV3xx-N have bipolar input and output stages for improved noise performance and higher output current drive.

Device Information(1)

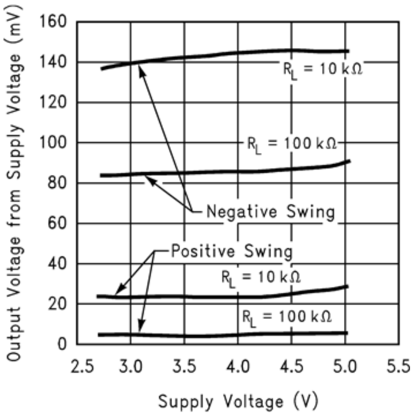
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LPV321-N	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
LPV358-N	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LPV324-N	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Micropower Supply Current



Rail-to-Rail Output Swing



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4 Revision History

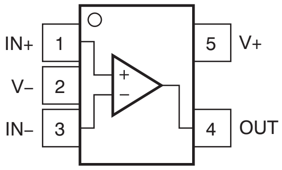
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Soldering temperature (235°C maximum)	4
• Changed Thermal Resistance, $R_{\theta JA}$, values From: 478 To: 296.7 (SC70), From: 265 To: 206.6 (SOT-23), From: 190 To: 130.1 (8-Pin SOIC), From: 235 To: 187.5 (VSSOP), From: 145 To: 103.9 (14-Pin SOIC), From: 155 To: 132.7 (TSSOP)	4

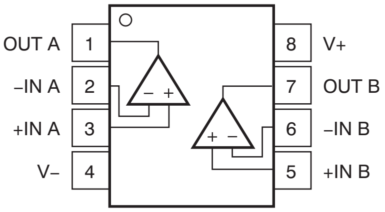
Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1

5 Pin Configuration and Functions

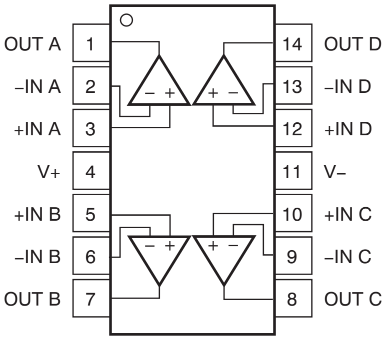
DBV or DCK Package
5-Pin SC70 or SOT-23
Top View



D or DGK Package
8-Pin SOIC or VSSOP
Top View



D or PW Package
14-Pin SOIC or TSSOP
Top View



Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	SC70 or SOT-23	SOIC or VSSOP	SOIC or TSSOP		
+IN	1	—	—	I	Noninverting input
IN A+	—	3	3	I	Noninverting input, channel A
IN B+	—	5	5	I	Noninverting input, channel B
IN C+	—	—	10	I	Noninverting input, channel C
IN D+	—	—	12	I	Noninverting input, channel D
–IN	3	—	—	I	Inverting input
IN A–	—	2	2	I	Inverting input, channel A
IN B–	—	6	6	I	Inverting input, channel B
IN C–	—	—	9	I	Inverting input, channel C
IN D–	—	—	13	I	Inverting input, channel D
OUTPUT	4	—	—	O	Output
OUT A	—	1	1	O	Output, channel A
OUT B	—	7	7	O	Output, channel B
OUT C	—	—	8	O	Output, channel C
OUT D	—	—	14	O	Output, channel D
V+	5	8	4	P	Positive (highest) power supply
V–	2	4	11	P	Negative (lowest) power supply

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Differential input voltage	±Supply voltage		
Supply voltage ($V^+ – V^-$)		5.5	V
Output short circuit to V^+	See (2)		
Output short circuit to V^-	See (3)		
Junction temperature, $T_{J(MAX)}$ (4)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Shorting output to V^+ will adversely affect reliability.
(3) Shorting output to V^- will adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$ and $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
LPV321-N in DBV and DCK Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V
		Machine model	±100	
LPV358-N in D and DGK Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V
		Machine model	±100	
LPV324-N in D and PW Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Machine model	±100	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.7	5	V
Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		LPV321-N		LPV358-N		LPV324-N		UNIT
		DBV (SOT-23)	DCK (SC70)	DGK (VSSOP)	D (SOIC)	D (SOIC)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.6	296.7	187.5	130.1	103.9	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	167.2	128.1	77.7	74.3	61.6	59.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.5	74.3	108	70.7	58.4	75.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	50.2	6.5	15.2	23.1	21.2	10.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.1	73.6	106.5	70.2	58.1	74.58	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics – 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input offset voltage			1.2	7	mV
TCV_{OS}	Input offset voltage average drift			2		µV/°C
I_B	Input bias current			1.7	50	nA
I_{OS}	Input offset current			0.6	40	nA
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 1.7 V	50	70		dB
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	50	65		dB
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB	0	−0.2		V
				1.9	1.7	
V_O	Output swing	R_L = 100 kΩ to 1.35 V	V^+ − 100	V^+ − 3		mV
				80	180	
I_S	Supply current	LPV321-N		4	8	µA
		LPV358-N, both amplifiers		8	16	
		LPV324-N, all four amplifiers		16	24	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.6 AC Electrical Characteristics – 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
GBWP	Gain-bandwidth product	C_L = 22 pF		112		kHz
Φ_m	Phase margin			97		°
G_m	Gain margin			35		dB
e_n	Input-referred voltage noise	f = 1 kHz		178		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.5		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.7 DC Electrical Characteristics – 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input offset voltage	T_J = 25°C		1.5	7	mV
		T_J = –40°C to 85°C			10	
TCV_{OS}	Input offset voltage average drift			2		µV/°C
I_B	Input bias current	T_J = 25°C		2	50	nA
		T_J = –40°C to 85°C			60	
I_{OS}	Input offset current	T_J = 25°C		0.6	40	nA
		T_J = –40°C to 85°C			50	
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 4 V	50	71		dB
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	50	65		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

DC Electrical Characteristics – 5 V (continued)

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB		0	−0.2		V
					4.2	4	
A_V	Large signal voltage gain(3)	R_L = 100 kΩ	T_J = 25°C	15	100		V/mV
			T_J = –40°C to 85°C	10			
V_O	Output swing	Sourcing R_L = 100 kΩ to 2.5 V	T_J = 25°C	V^+ −100	V^+ −3.5		mV
			T_J = –40°C to 85°C	V^+ −200			
		Sinking R_L = 100 kΩ to 2.5 V	T_J = 25°C		90	180	
			T_J = –40°C to 85°C			220	
I_O	Output short circuit current sourcing	LPV3xx-N, V_O = 0 V		2	16		mA
	Output short circuit current sinking	LPV321-N, V_O = 5 V		20	60		
		LPV324-N and LPV358-N, V_O = 5 V		11	16		
I_S	Supply current	LPV321-N	T_J = 25°C		9	12	µA
			T_J = –40°C to 85°C			15	
		LPV358-N, Both amplifiers	T_J = 25°C		15	20	
			T_J = –40°C to 85°C			24	
		LPV324-N, All four amplifiers	T_J = 25°C		28	42	
			T_J = –40°C to 85°C			46	

(3) R_L is connected to V^-. The output voltage is 0.5 V ≤ V_O ≤ 4.5 V.

6.8 AC Electrical Characteristics – 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2 V, V_O = V^+/2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SR	Slew rate(3)			0.1		V/µs
GBWP	Gain-bandwidth product	C_L = 22 pF		152		kHz
Φ_m	Phase margin			87		°
G_m	Gain margin			19		dB
e_n	Input-referred voltage noise	f = 1 kHz		146		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.3		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

6.9 Typical Characteristics

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

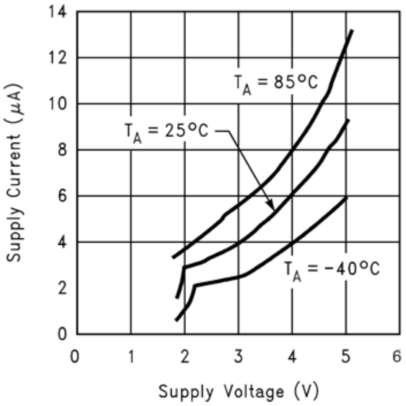


Figure 1. Supply Current vs Supply Voltage (LPV321-N)

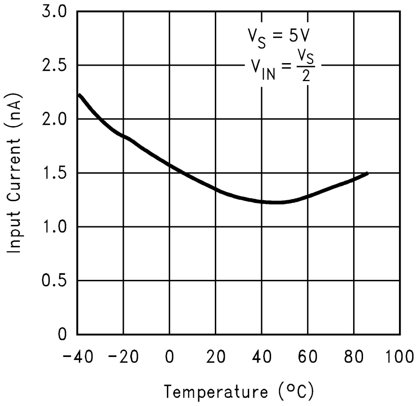


Figure 2. Input Current vs Temperature

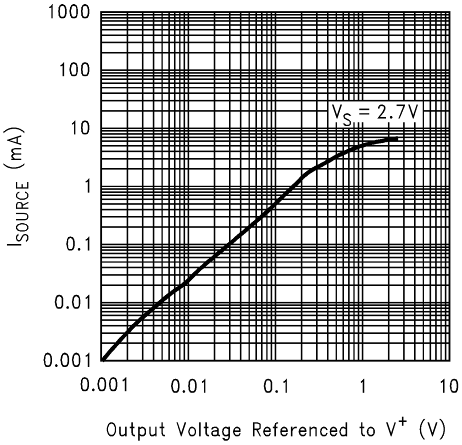


Figure 3. Sourcing Current vs Output Voltage

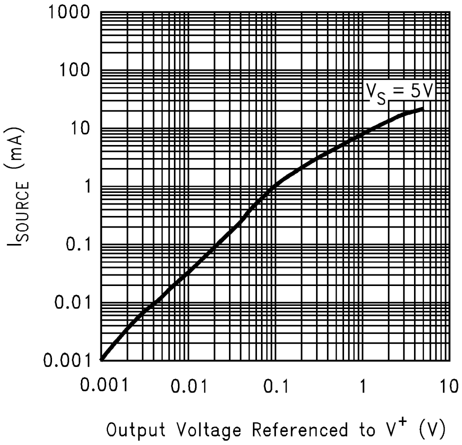


Figure 4. Sourcing Current vs Output Voltage

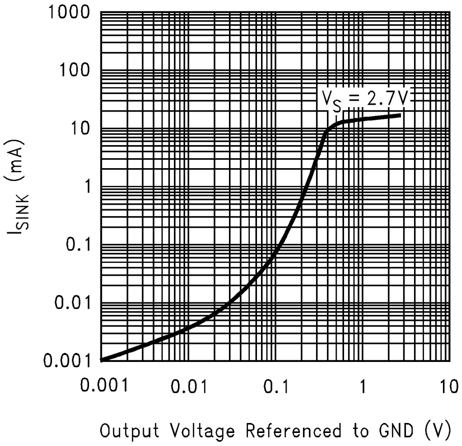


Figure 5. Sinking Current vs Output Voltage

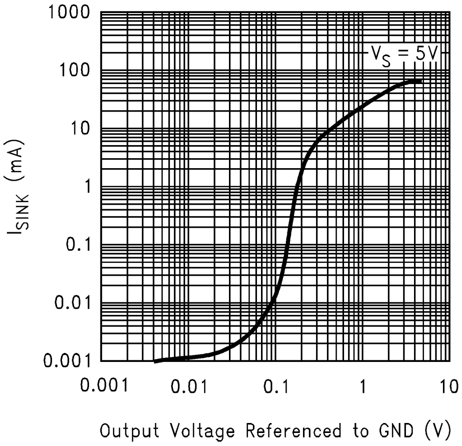


Figure 6. Sinking Current vs Output Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

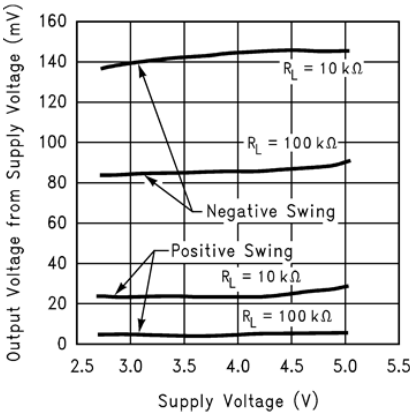


Figure 7. Output Voltage Swing vs Supply Voltage

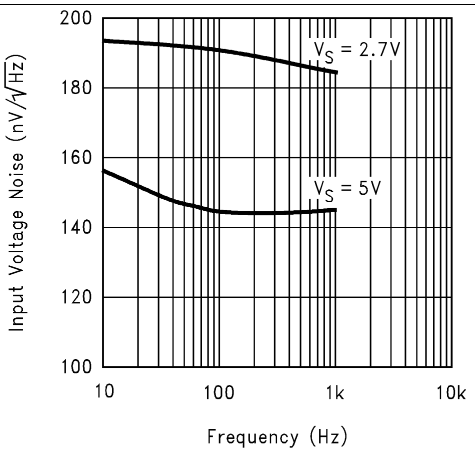


Figure 8. Input Voltage Noise vs Frequency

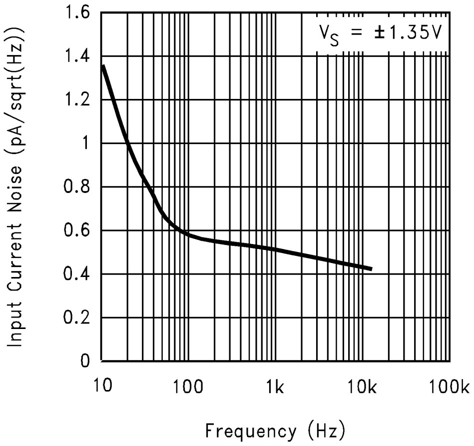


Figure 9. Input Current Noise vs Frequency

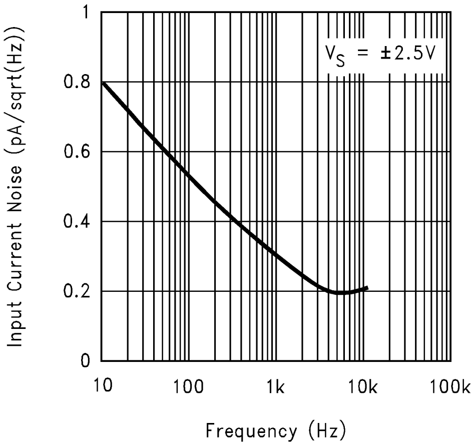


Figure 10. Input Current Noise vs Frequency

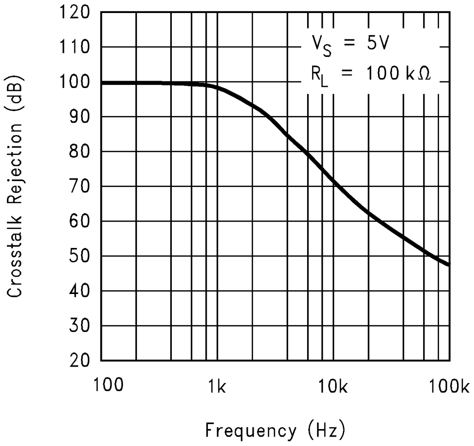


Figure 11. Crosstalk Rejection vs Frequency

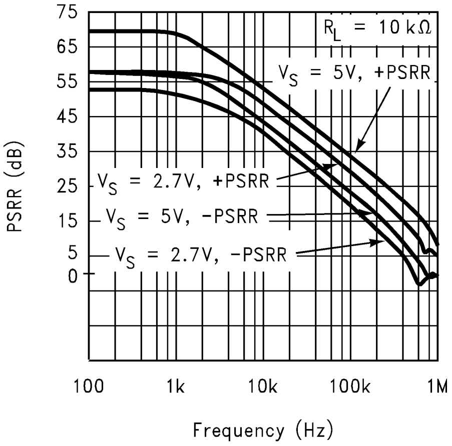


Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

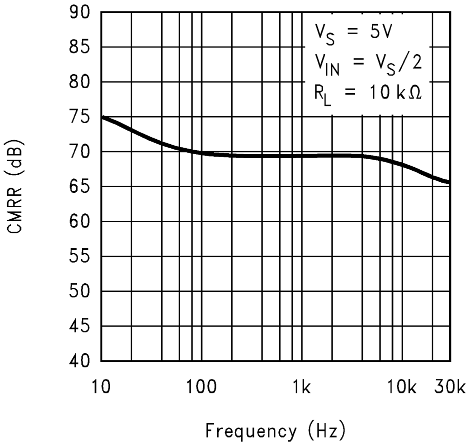


Figure 13. CMRR vs Frequency

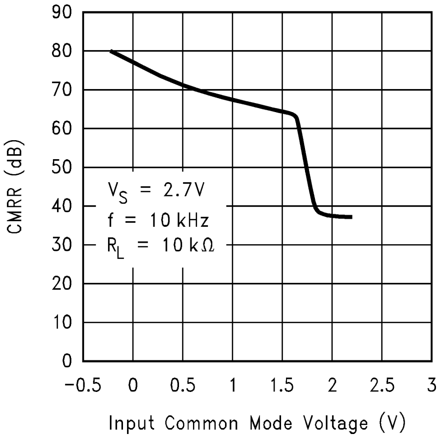


Figure 14. CMRR vs Input Common Mode Voltage

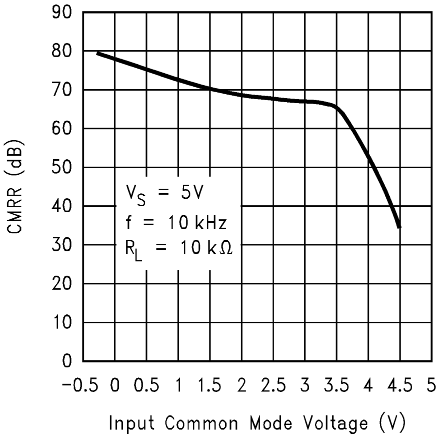


Figure 15. CMRR vs Input Common Mode Voltage

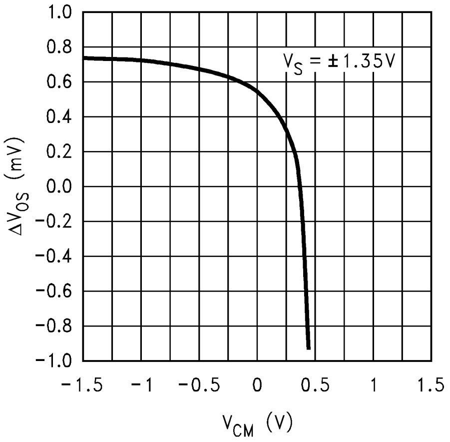


Figure 16. ΔV_{OS} vs V_{CM}

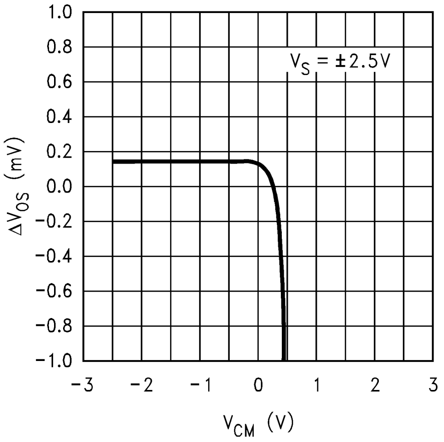


Figure 17. ΔV_{OS} vs V_{CM}

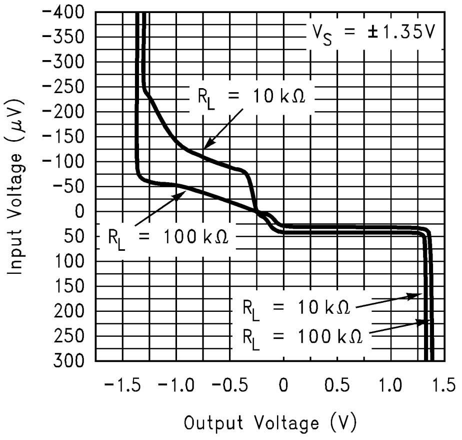


Figure 18. Input Voltage vs Output Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

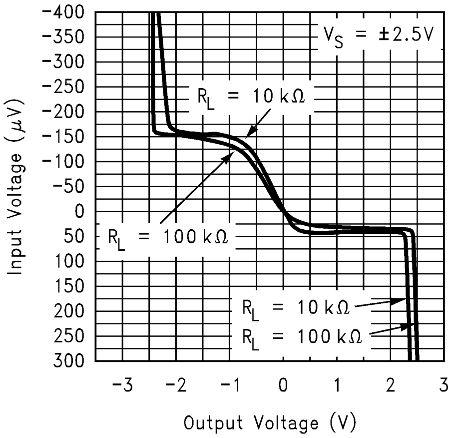


Figure 19. Input Voltage vs Output Voltage

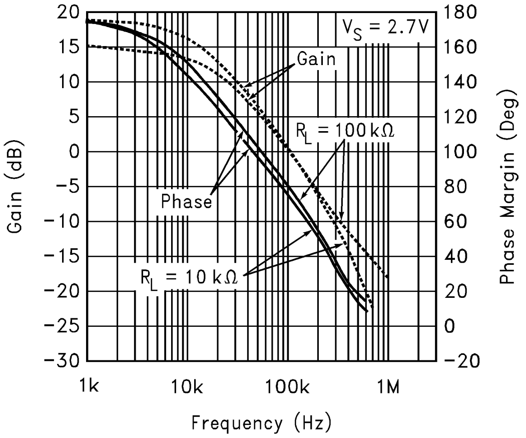


Figure 20. Open-Loop Frequency Response

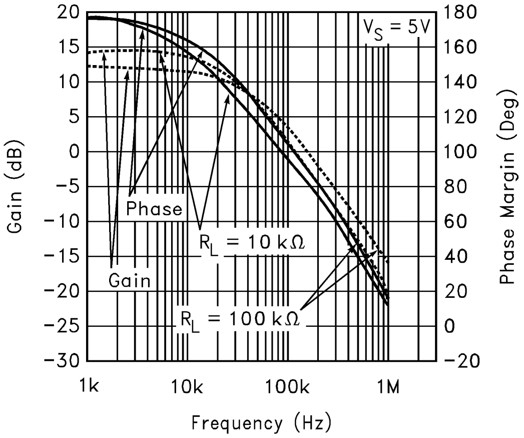


Figure 21. Open-Loop Frequency Response

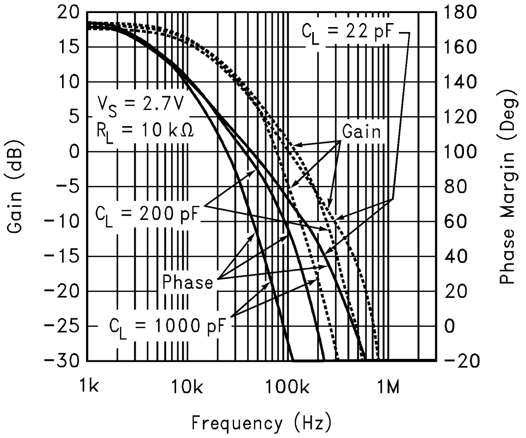


Figure 22. Gain and Phase vs Capacitive Load

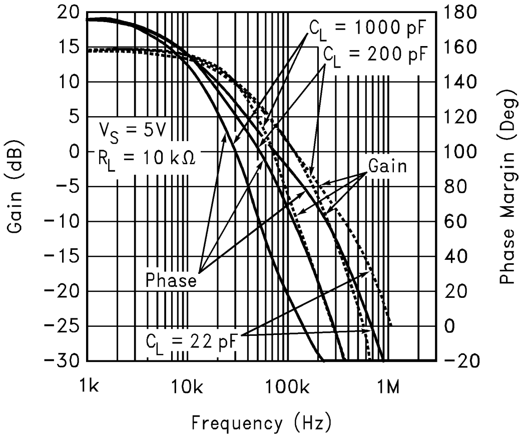


Figure 23. Gain and Phase vs Capacitive Load

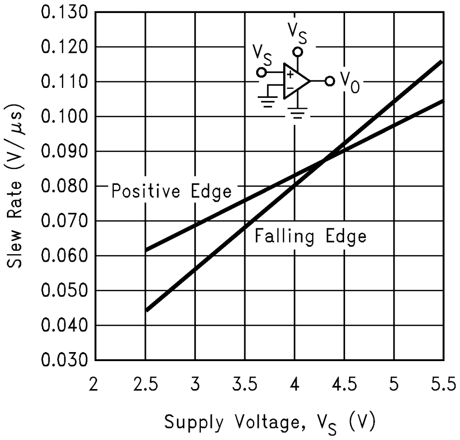


Figure 24. Slew Rate vs Supply Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

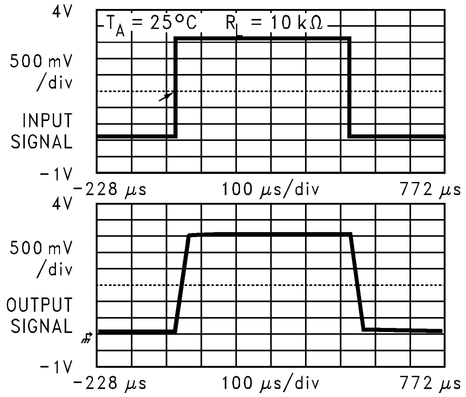


Figure 25. Noninverting Large Signal Pulse Response

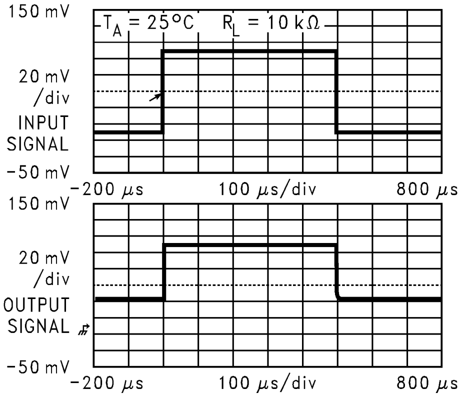


Figure 26. Noninverting Small Signal Pulse Response

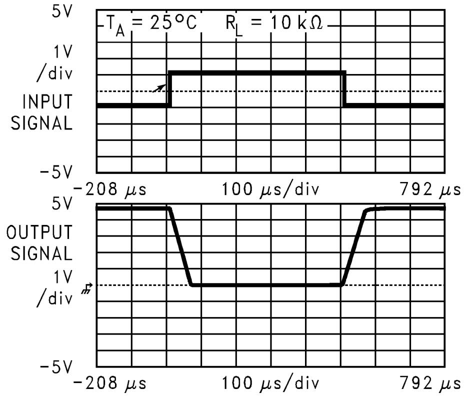


Figure 27. Inverting Large Signal Pulse Response

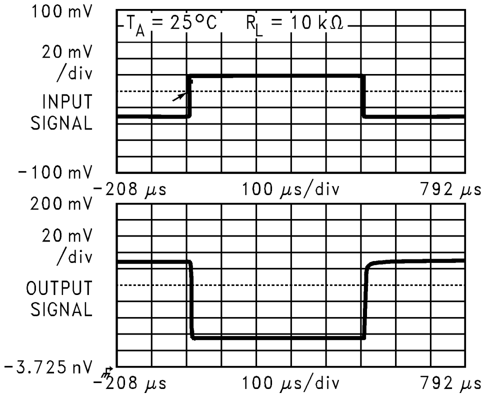


Figure 28. Inverting Small Signal Pulse Response

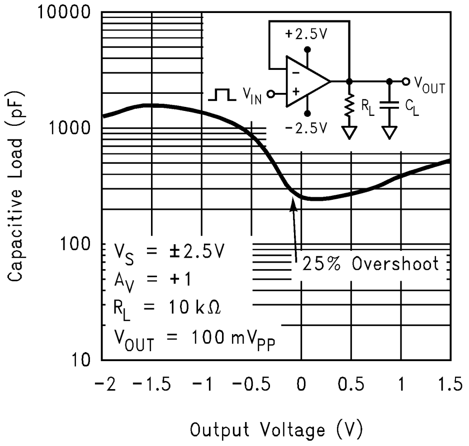


Figure 29. Stability vs Capacitive Load

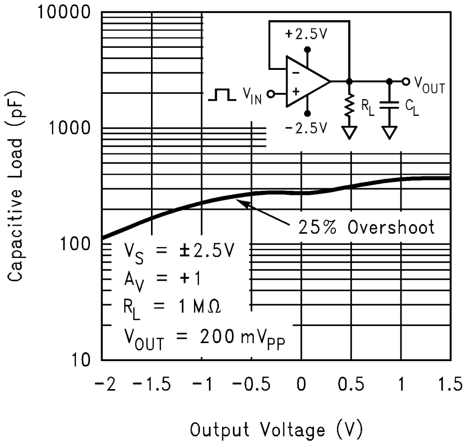


Figure 30. Stability vs Capacitive Load

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

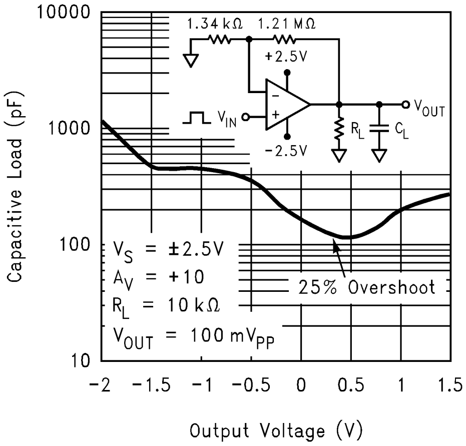


Figure 31. Stability vs Capacitive Load

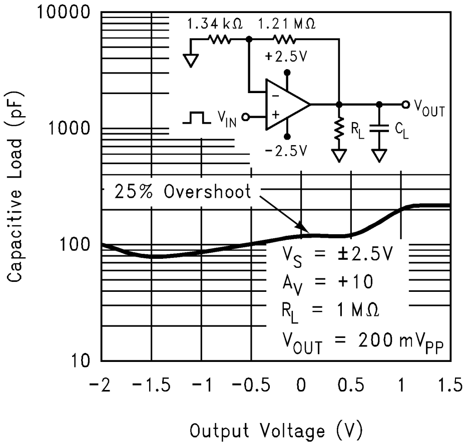


Figure 32. Stability vs Capacitive Load

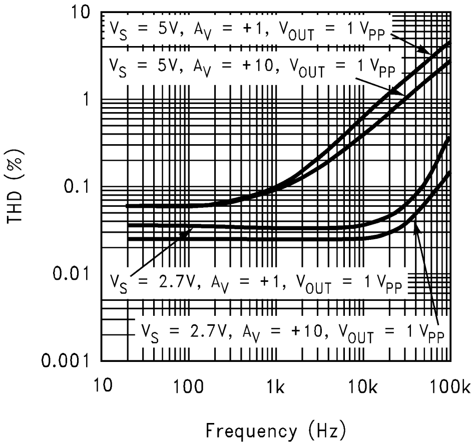


Figure 33. THD vs Frequency

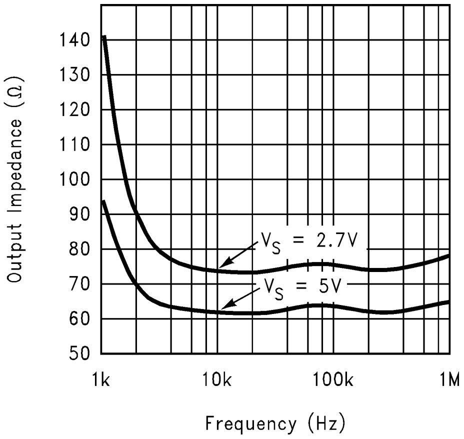


Figure 34. Open-Loop Output Impedance vs Frequency

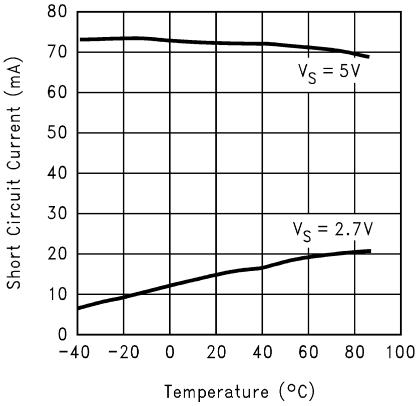


Figure 35. Short Circuit Current vs Temperature (Sinking)

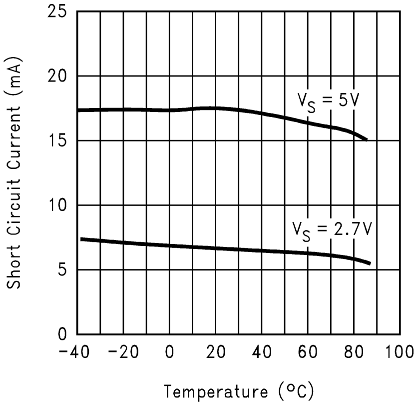


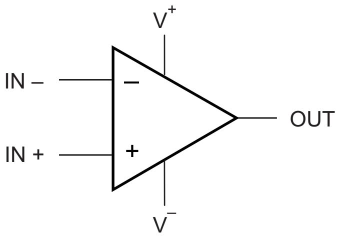
Figure 36. Short Circuit Current vs Temperature (Sourcing)

7 Detailed Description

7.1 Overview

The LPV321-N, LPV358-N, and LPV324-N devices are micropower (10-µA) versions of the popular LMV3xx-N. The LPV321-N is the single-channel version. The LPV358-N is the dual, and the LPV324-N is the quad. The LPV32x-N are the most cost effective solution for applications where low power and low voltage operation, space efficiency, and low-price are important. The LPV3x-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 152 kHz of bandwidth and 0.1-V/µs slew rate with 10 mA of supply current.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Size

The small footprints of the LPV3xx-N packages save space on printed circuit boards, and enable the design of smaller electronic products (such as cellular phones, pagers, or other portable systems). The low profile of the LPV3xx-N make them possible to use in PCMCIA type III cards.

7.3.2 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LPV3xx-N can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

7.3.3 Simplified Board Layout

These products help avoid using long printed-circuit traces in the PCB. This means no additional components, such as capacitors and resistors, are needed to filter out unwanted signals due to the interference between the long printed-circuit traces.

7.3.4 Low Supply Current

These devices help maximize battery life. They are ideal for battery powered systems.

7.3.5 Low Supply Voltage

TI provides ensured performance at 2.7 V and 5 V. These specifications ensure operation throughout the battery lifetime.

7.3.6 Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low-supply voltages.

Feature Description (continued)

7.3.7 Input Includes Ground

Allows direct sensing near GND in single supply operation.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

7.4 Device Functional Modes

The LPV3xx-N can be operated as a single-supply or a dual-supply operational amplifier depending on the application.

7.4.1 Capacitive Load Tolerance

The LPV3xx-N can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in Figure 37 can be used.

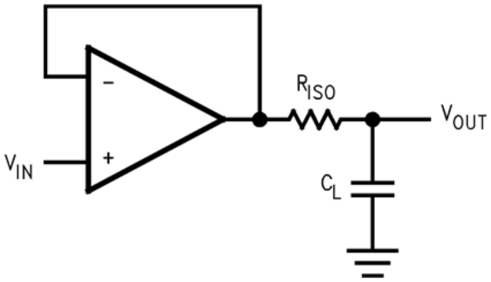


Figure 37. Indirectly Driving A Capacitive Load Using Resistive Isolation

In Figure 37, the isolation resistor (R_{ISO}) and the load capacitor (C_L) form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} is. Figure 38 is an output waveform of Figure 37 using 100 kΩ for R_{ISO} and 1000 pF for C_L.

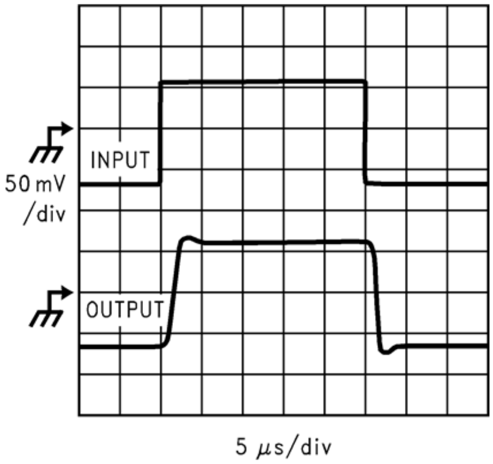


Figure 38. Pulse Response of the LPV324 Circuit in Figure 37

Device Functional Modes (continued)

The circuit in Figure 39 is an improvement to the one in Figure 37 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 37, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 39, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Caution is needed in choosing the value of R_F due to the input bias current of the LPV3xx-N. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn slows down the pulse response.

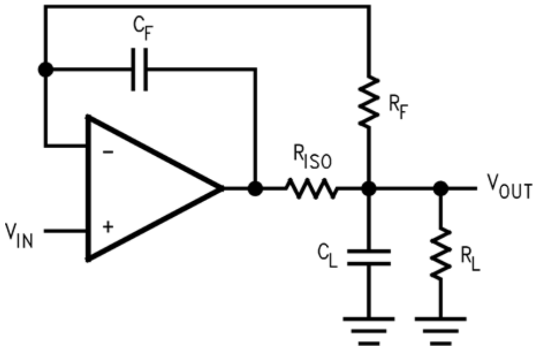


Figure 39. Indirectly Driving A Capacitive Load With DC Accuracy

7.4.2 Input Bias Current Cancellation

The LPV3xx-N family has a bipolar input stage. The typical input bias current of LPV3xx-N is 1.5 nA with 5-V supply. Thus a 100-kΩ input resistor causes 0.15 mV of error voltage. By balancing the resistor values at both inverting and noninverting inputs, the error caused by the amplifier's input bias current is reduced. The circuit in Figure 40 shows how to cancel the error caused by input bias current.

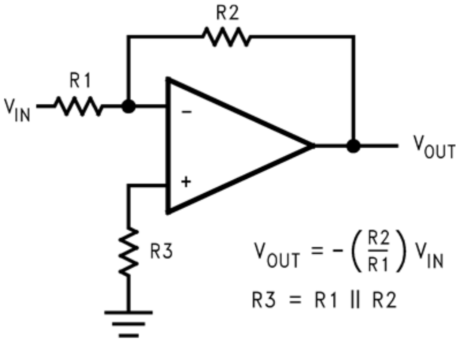


Figure 40. Cancelling the Error Caused by Input Bias Current

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV3xx-N family of amplifiers is specified for operation from 2.7 V to 5 V (±1.35 V to ±2.5 V). Many of the specifications apply from –40°C to 125°C. They provide ground-sensing inputs as well as rail-to-rail output swing. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.2 Typical Applications

8.2.1 Simple Low-Pass Active Filter

A simple low-pass filter is shown in Figure 41.

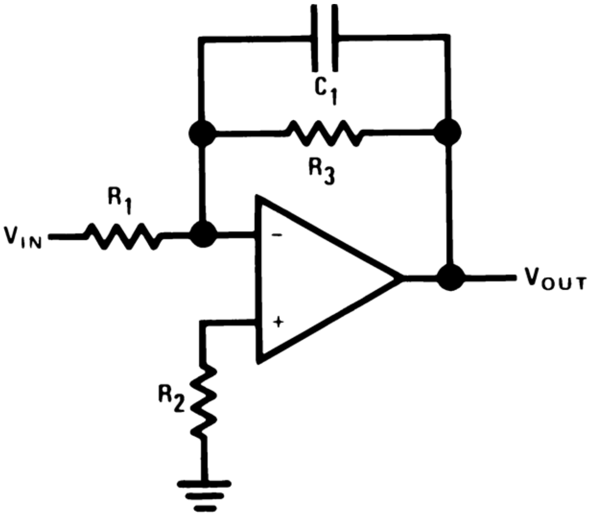


Figure 41. Simple Low-Pass Active Filter Schematic

8.2.1.1 Design Requirements

The low-pass filter is shown in Figure 41 passes low frequencies and attenuate frequencies above corner frequency (fc) at a roll-off rate of 20 dB/Decade.

8.2.1.2 Detailed Design Procedure

The low-frequency gain ($\omega \rightarrow o$) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a −20 dB/decade roll-off after its corner frequency fc. R_2 must be chosen equal to the parallel combination of R_1 and R_3 to minimize errors due to bais current. The frequency response of the filter is shown in Figure 42.

$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \parallel R_3 \tag{1}$$

Typical Applications (continued)

Note that the single op amp active filters are used in to the applications that require low quality factor, Q (≤ 10), low frequency (≤ 5 kHz), and low gain (≤ 10), or a small value for the product of gain times Q (≤ 100). The op amp must have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp must have a slew rate that meets the requirements in Equation 2.

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{V}/\mu\text{sec}$$

where

- ω_H is the highest frequency of interest
- V_{OPP} is the output peak-to-peak voltage (2)

8.2.1.3 Application Curve

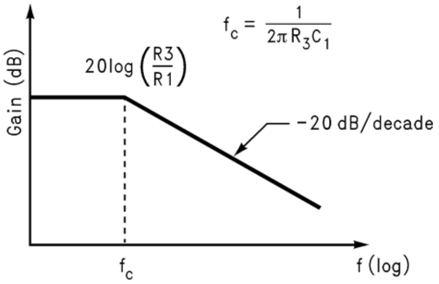


Figure 42. Frequency Response of Simple Low-pass Active Filter

8.2.2 Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier in making a differential to single-ended conversion or in rejecting a common mode signal.

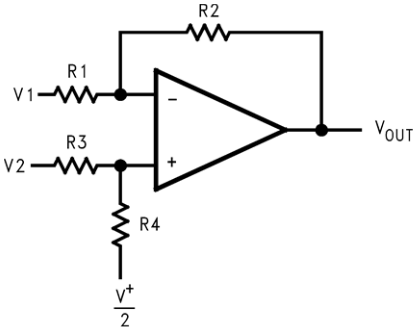


Figure 43. Difference Amplifier Schematic

$$V_{OUT} = \left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1+R2}{R3+R4}\right)\frac{R3}{R1} \times \frac{V^+}{2}$$

for R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}(V_2 - V1) + \frac{V^+}{2} \quad (3)$$

8.2.3 Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistor R_1, R_2, R_3, and R_4. To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

Typical Applications (continued)

8.2.3.1 Three Operating Amplifier Instrumentation

The quad LPV324 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 44

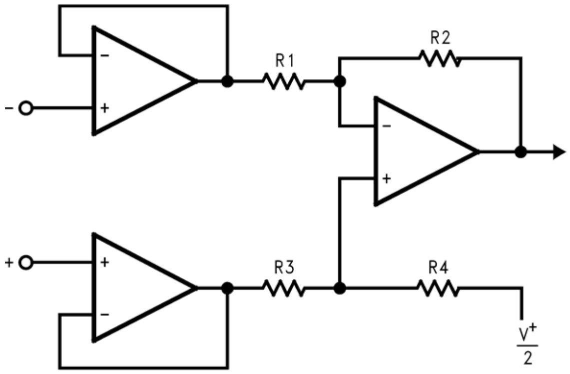


Figure 44. Three-op-amp Instrumentation Amplifier Schematic

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1. R_3 should equal R_1 and R_4 equal R_2. Matching of R_3 to R_1 and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 Slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum.

8.2.3.2 Two Operating Amplifier Instrumentation

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 45). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should equal to R_1 and R_3 must equal R_2.

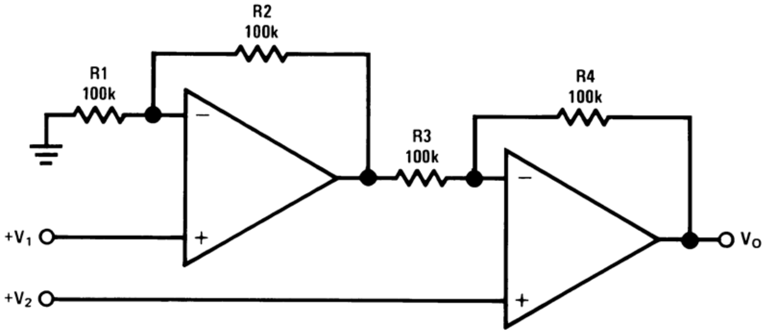


Figure 45. Two-op-amp Instrumentation Amplifier Schematic

$$V_O = \left(1 + \frac{R4}{R3}\right)(V_2 - V_1), \text{where } R1 = R4 \text{ and } R2 = R3$$

$$\text{As shown}: V_O = 2(V_2 - V_1) \quad (4)$$

8.2.3.3 Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-common voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency in Equation 5.

$$fc = 1/2\pi R_1 C_1 \quad (5)$$

Typical Applications (continued)

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

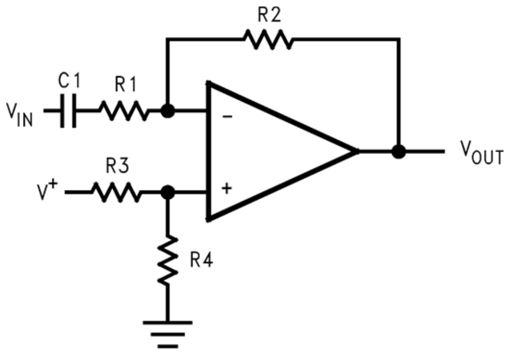


Figure 46. Single-Supply Inverting Amplifier

$$V_{OUT} = -\frac{R2}{R1} V_{IN} \tag{6}$$

9 Power Supply Recommendations

The LPV3xx-N is specified for operation from 2.7 V to 5.5 V; many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Figure 47.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

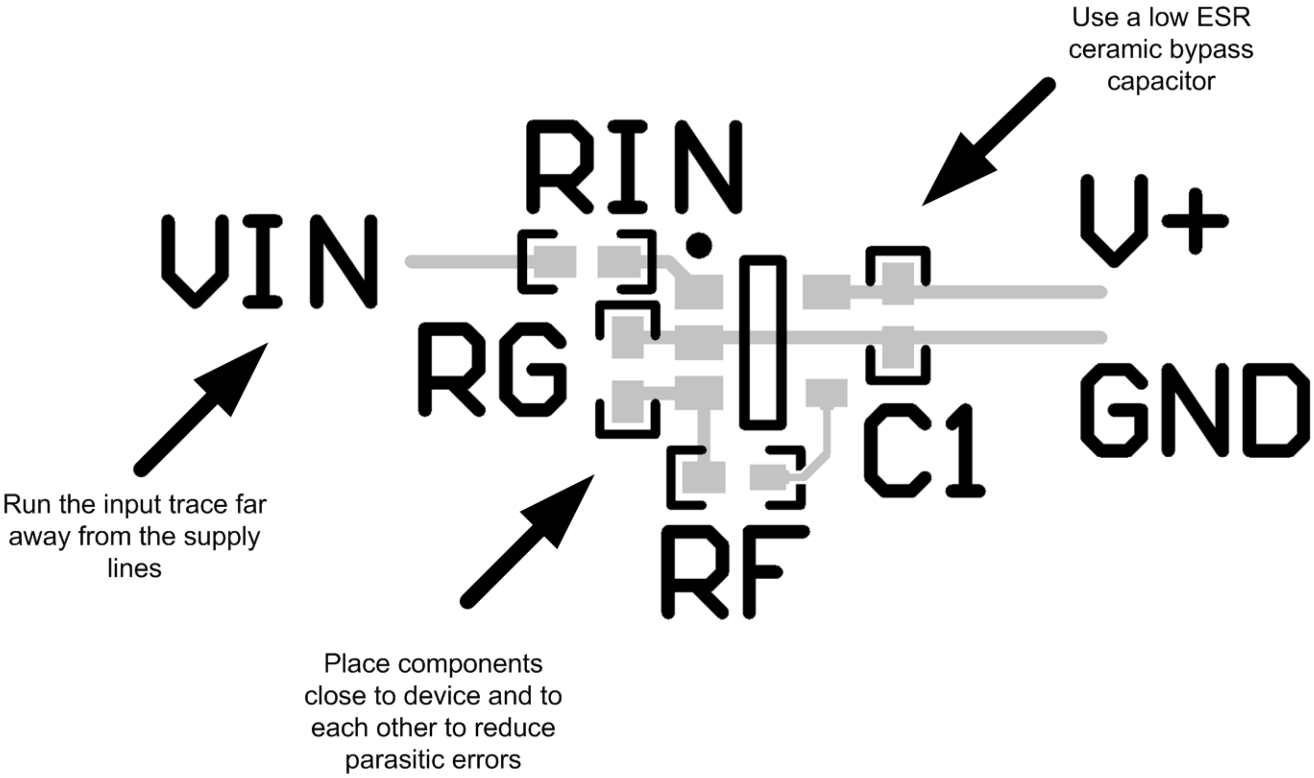


Figure 47. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- LPV321-N PSPICE Model (SNOM026)
- LPV358-N PSPICE Model (SNOM022)
- LPV324-N PSPICE Model (SNOM027)
- TINA-TI SPICE-Based Analog Simulation Program
- DIP Adapter Evaluation Module
- TI Universal Operational Amplifier Evaluation Module
- TI Filterpro Software

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Handbook of Operational Amplifier Applications* (SBOA092)
- *Compensate Transimpedance Amplifiers Intuitively* (SBOA055)
- *Circuit Board Layout Techniques* (SLOA089)
- *AN-1803 Design Considerations for a Transimpedance Amplifier* (SNOA515)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LPV321-N	Click here	Click here	Click here	Click here	Click here
LPV324-N	Click here	Click here	Click here	Click here	Click here
LPV358-N	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LPV321M5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A27A
LPV321M5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A27A
LPV321M5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A27A
LPV321M5X/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A27A
LPV321M7/NOPB	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A19
LPV321M7/NOPB.A	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A19
LPV321M7X/NOPB	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A19
LPV321M7X/NOPB.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A19
LPV324M/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324M
LPV324M/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324M
LPV324MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT
LPV324MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT
LPV324MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT
LPV324MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT
LPV324MX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324M
LPV324MX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV324M
LPV358M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M
LPV358M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M
LPV358MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	P358
LPV358MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	P358
LPV358MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	P358
LPV358MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	P358
LPV358MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 85	P358
LPV358MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LPV358MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

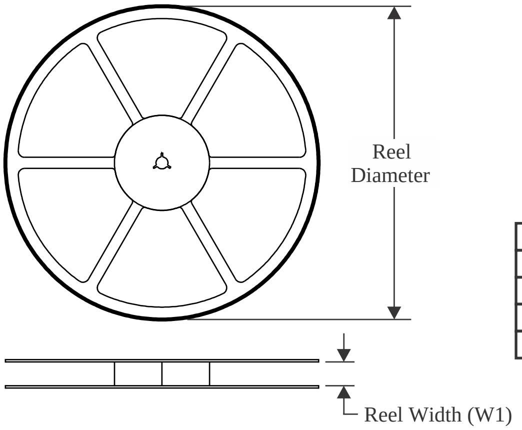
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

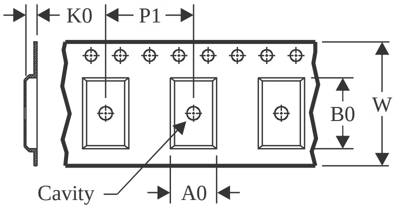
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

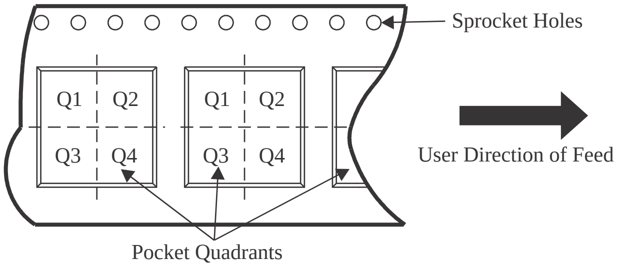


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

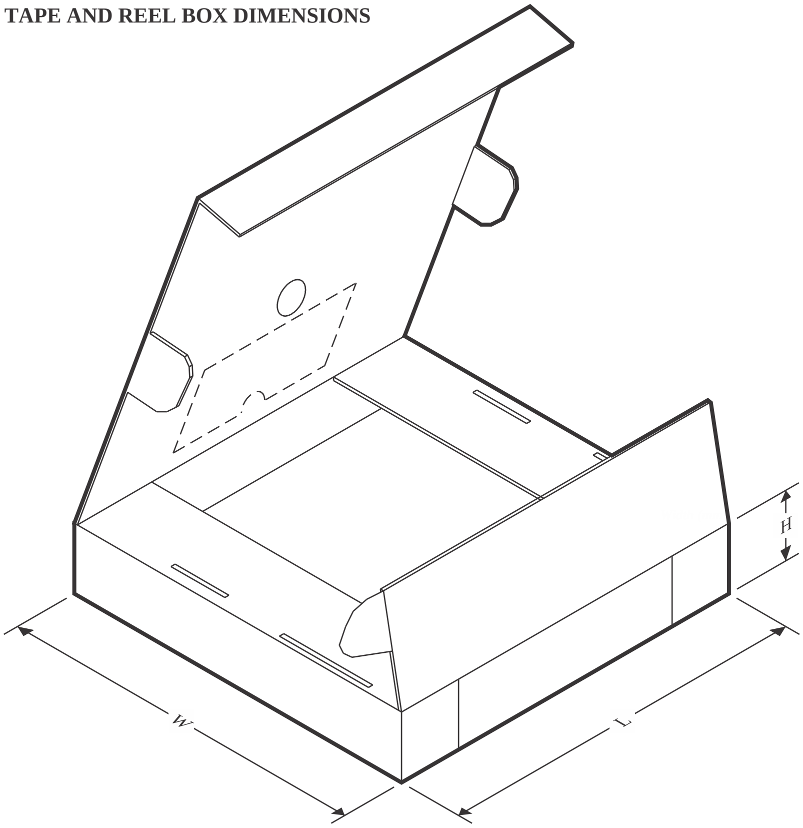
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV321M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LPV324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPV358MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

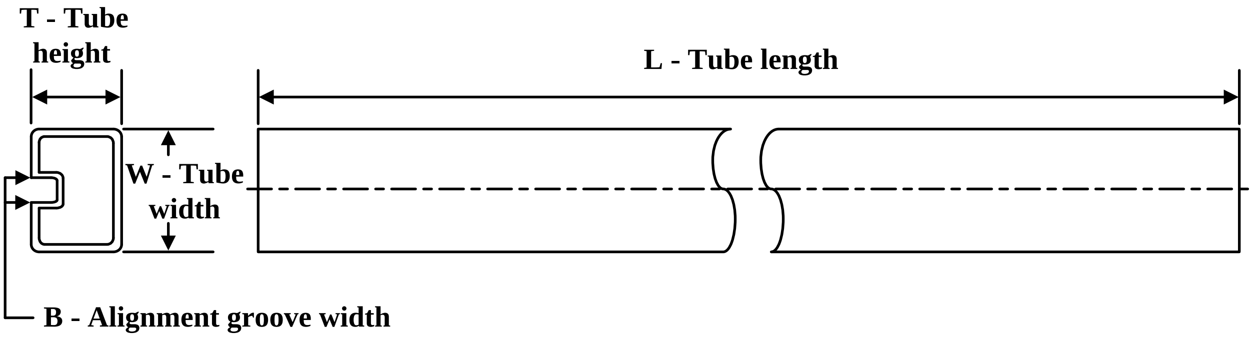
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

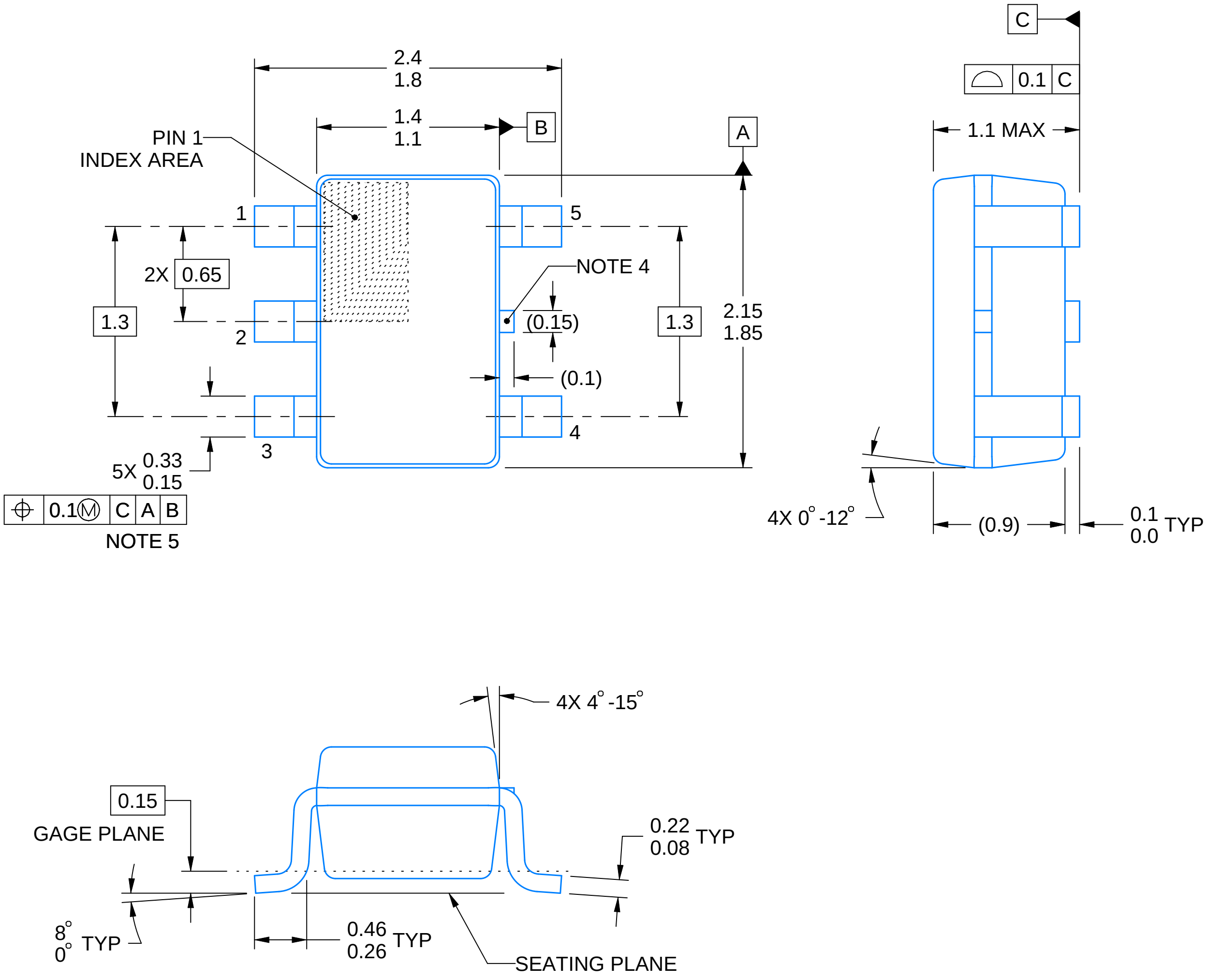
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV321M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LPV321M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LPV321M7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LPV321M7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LPV324MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LPV324MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LPV358MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LPV358MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LPV358MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

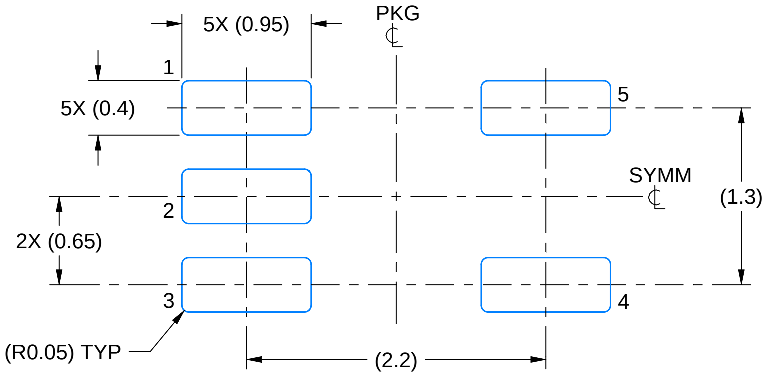
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LPV324M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LPV324M/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
LPV324MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LPV324MT/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06
LPV358M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LPV358M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05



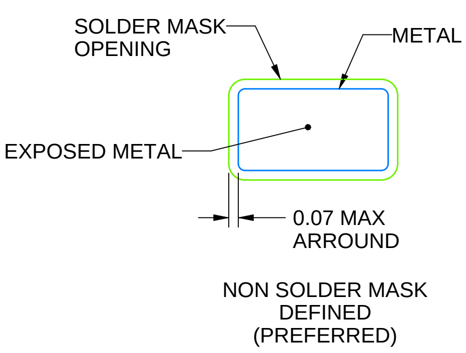
4214834/G 11/2024

NOTES:

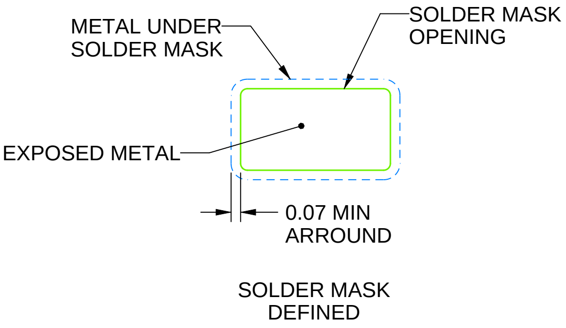
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

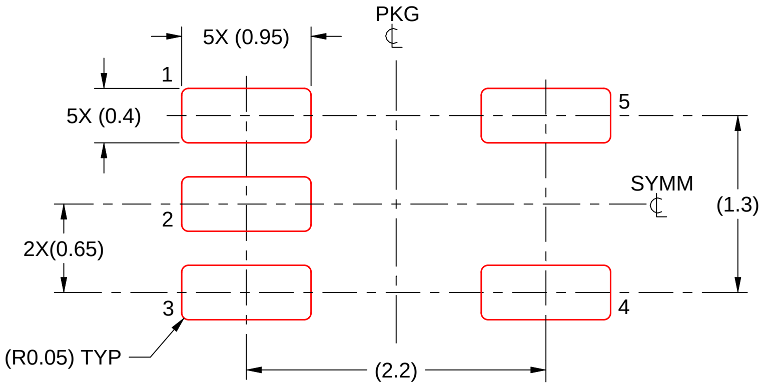


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

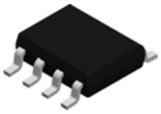
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

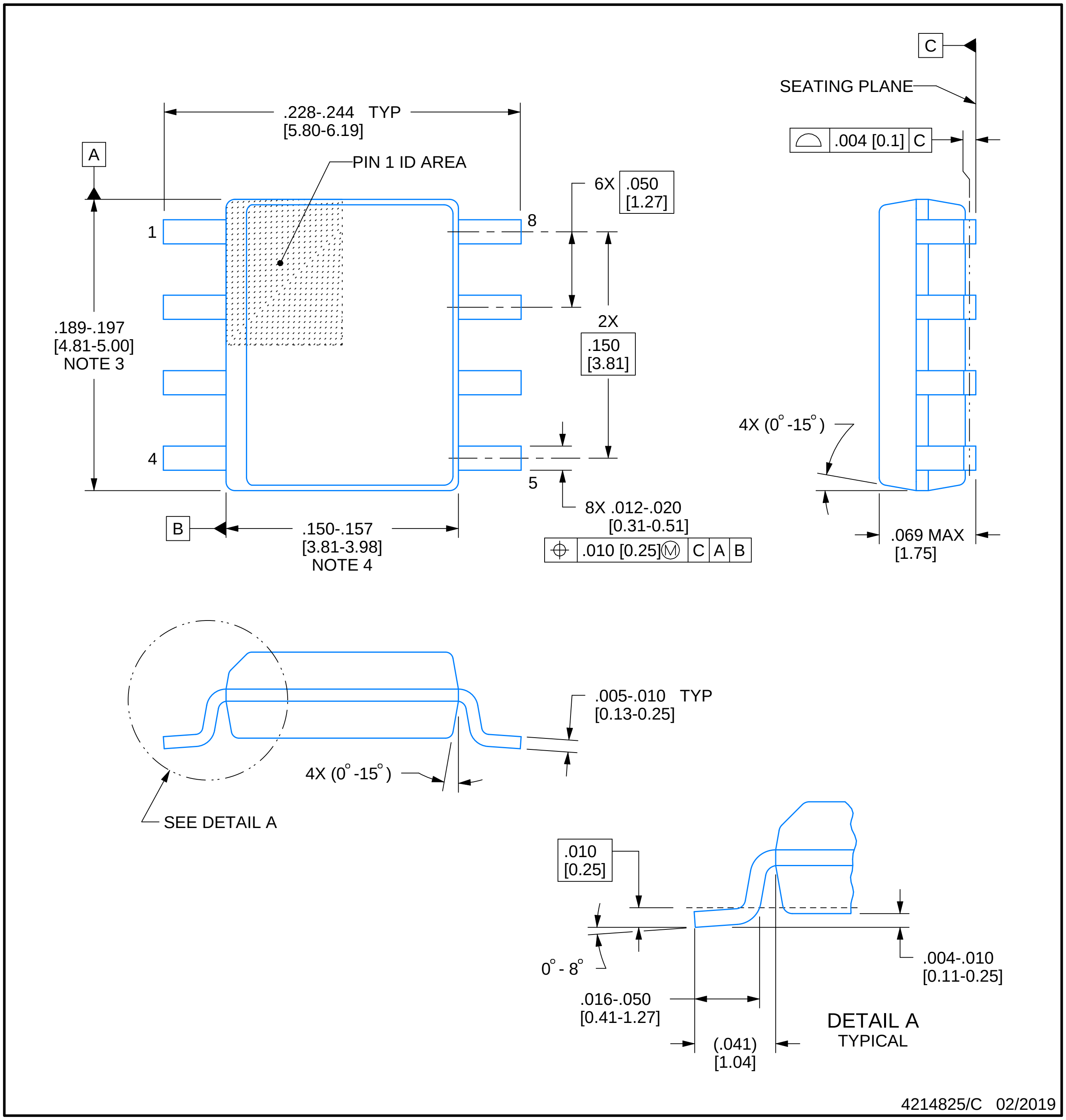


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

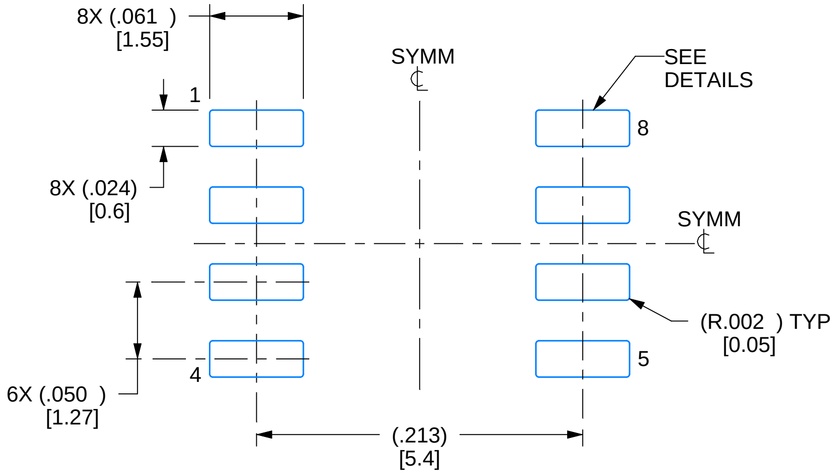
SMALL OUTLINE INTEGRATED CIRCUIT



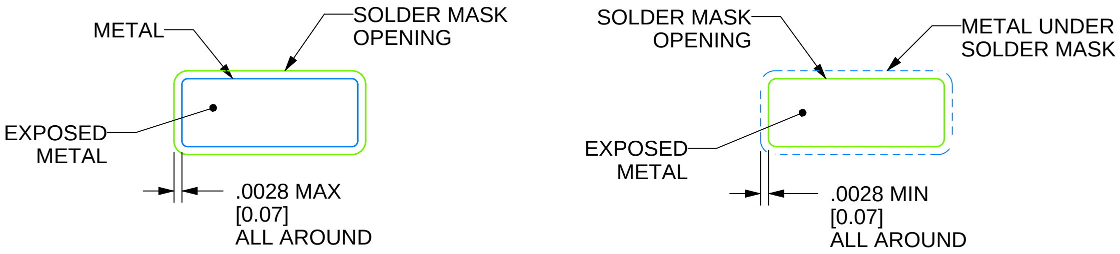
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



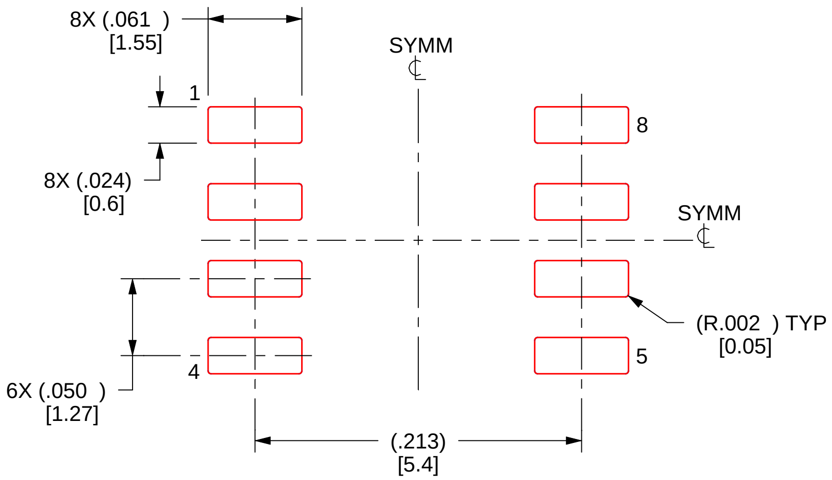
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

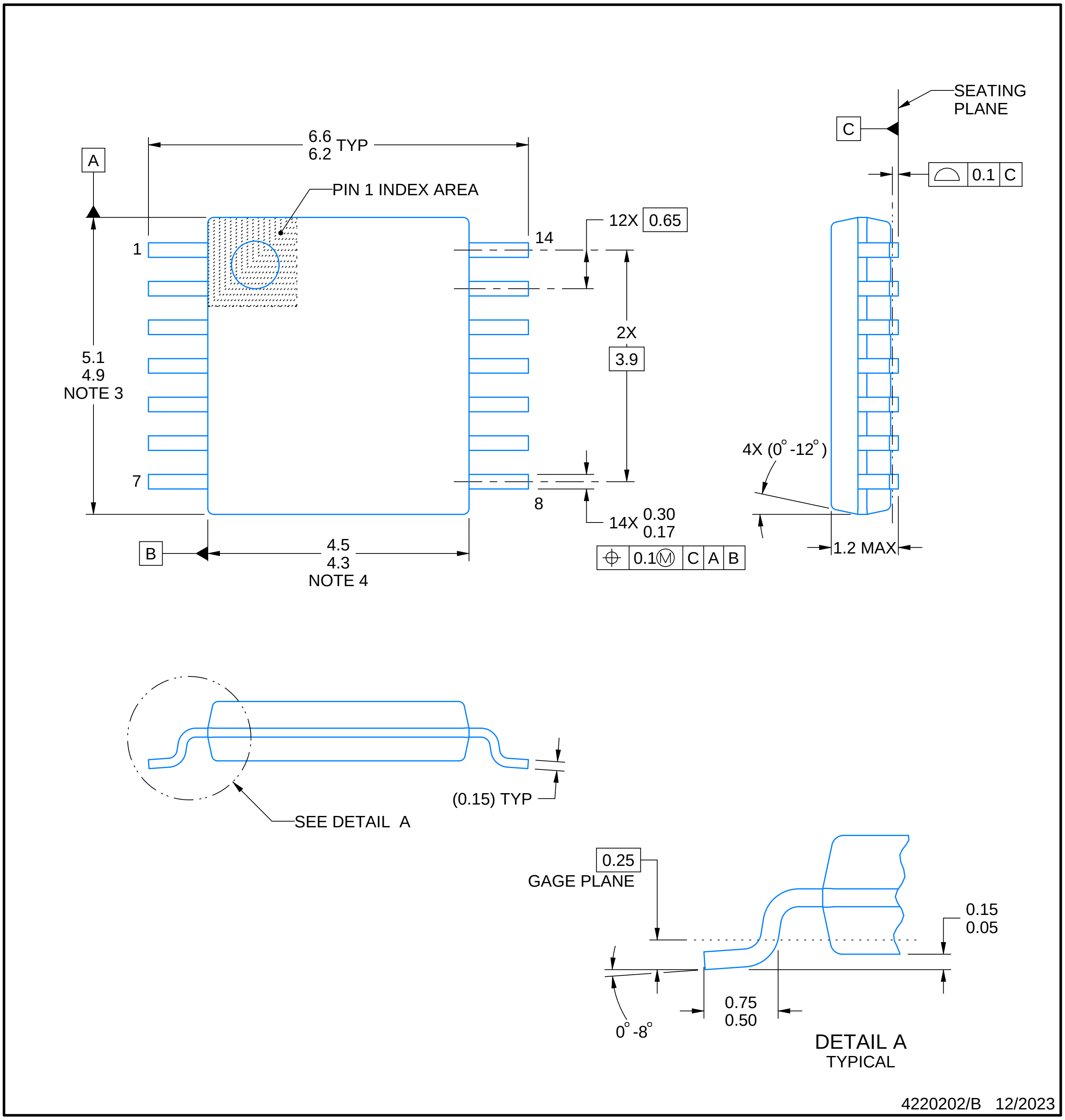
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

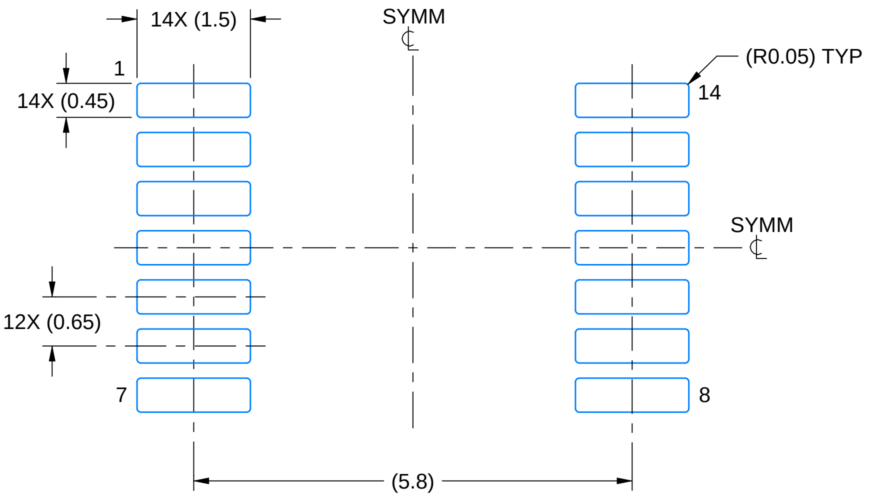
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

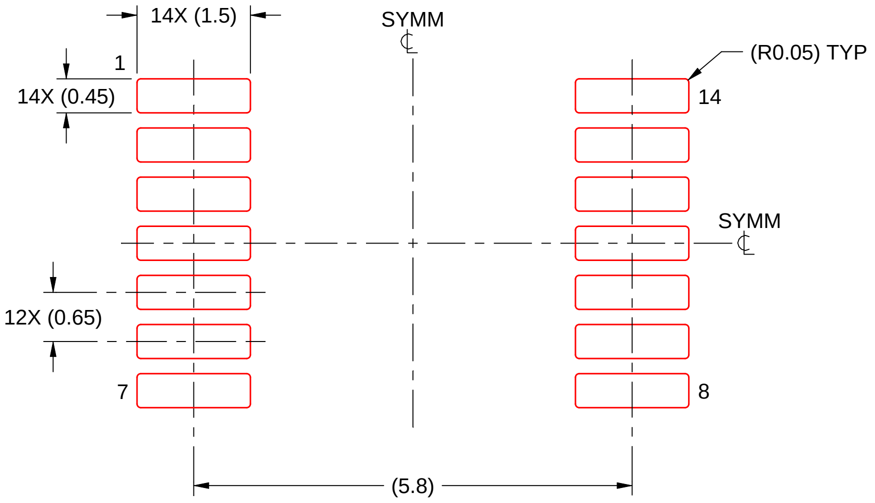
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

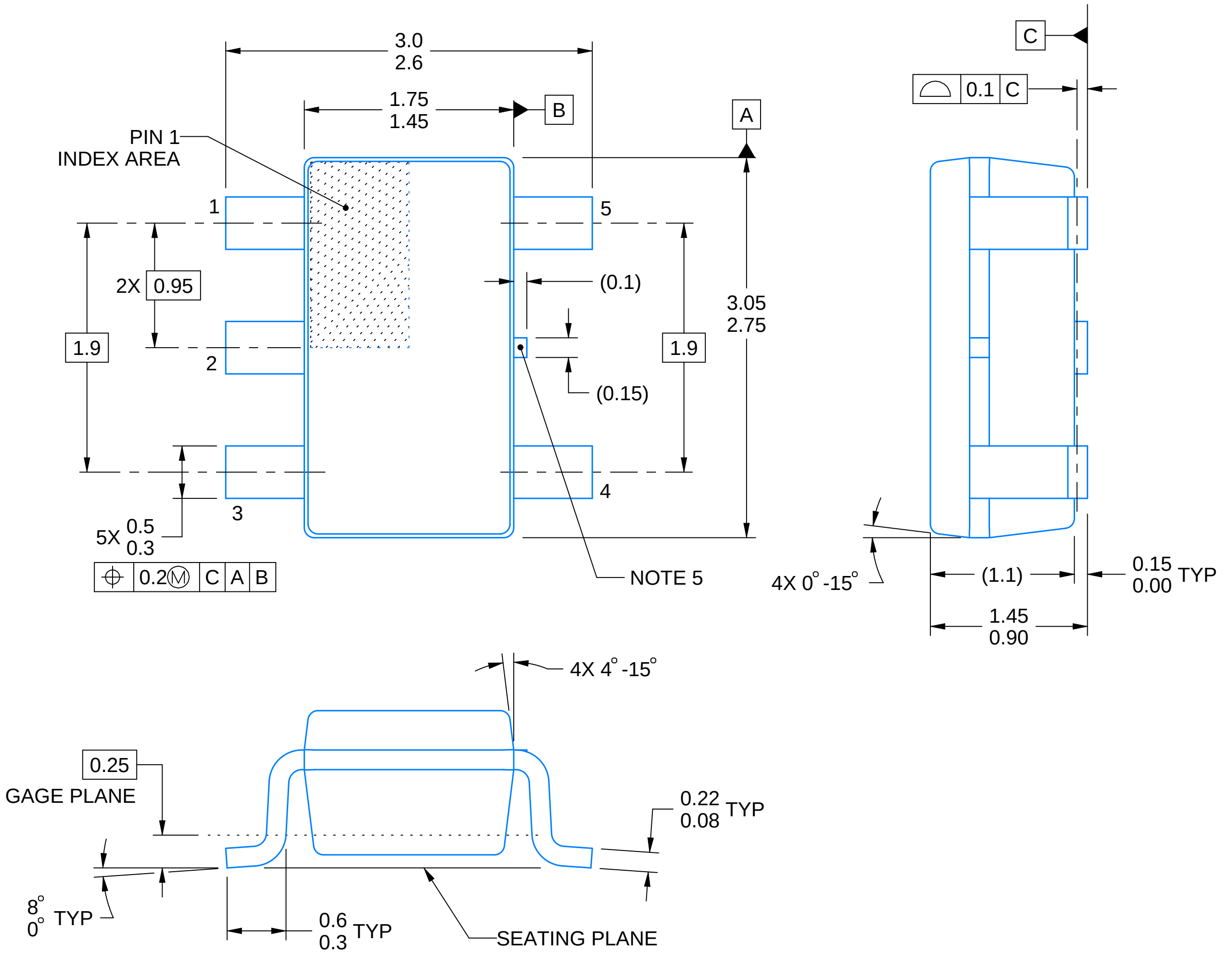
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

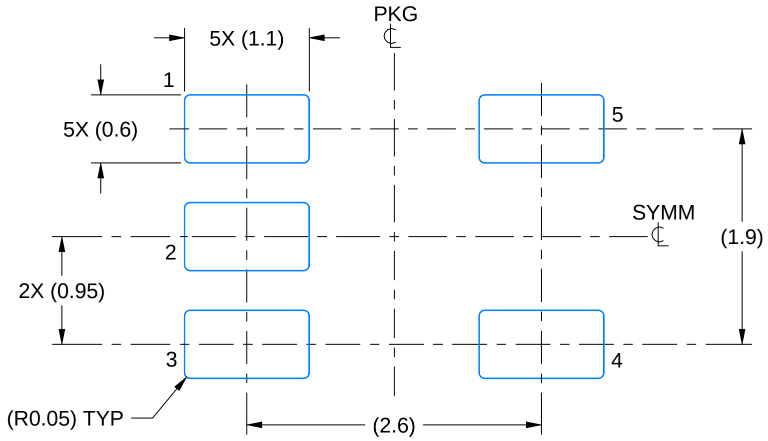
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



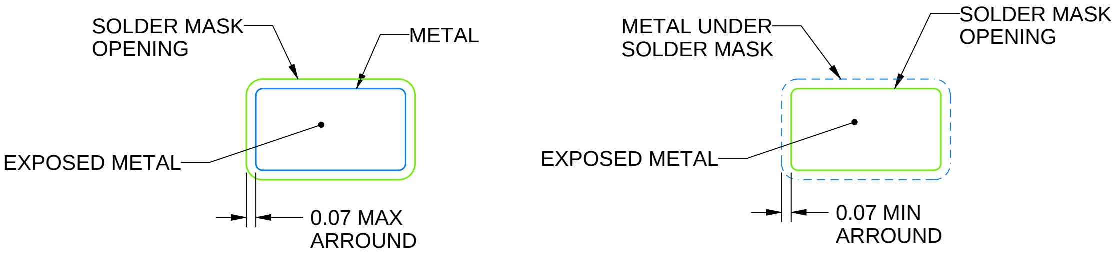
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



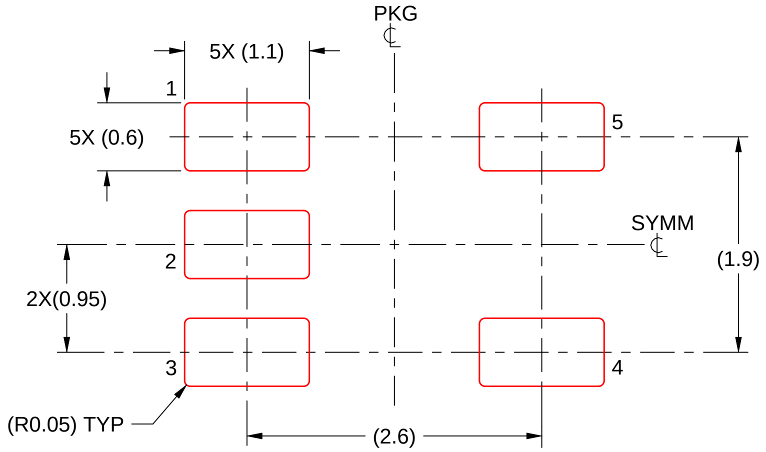
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

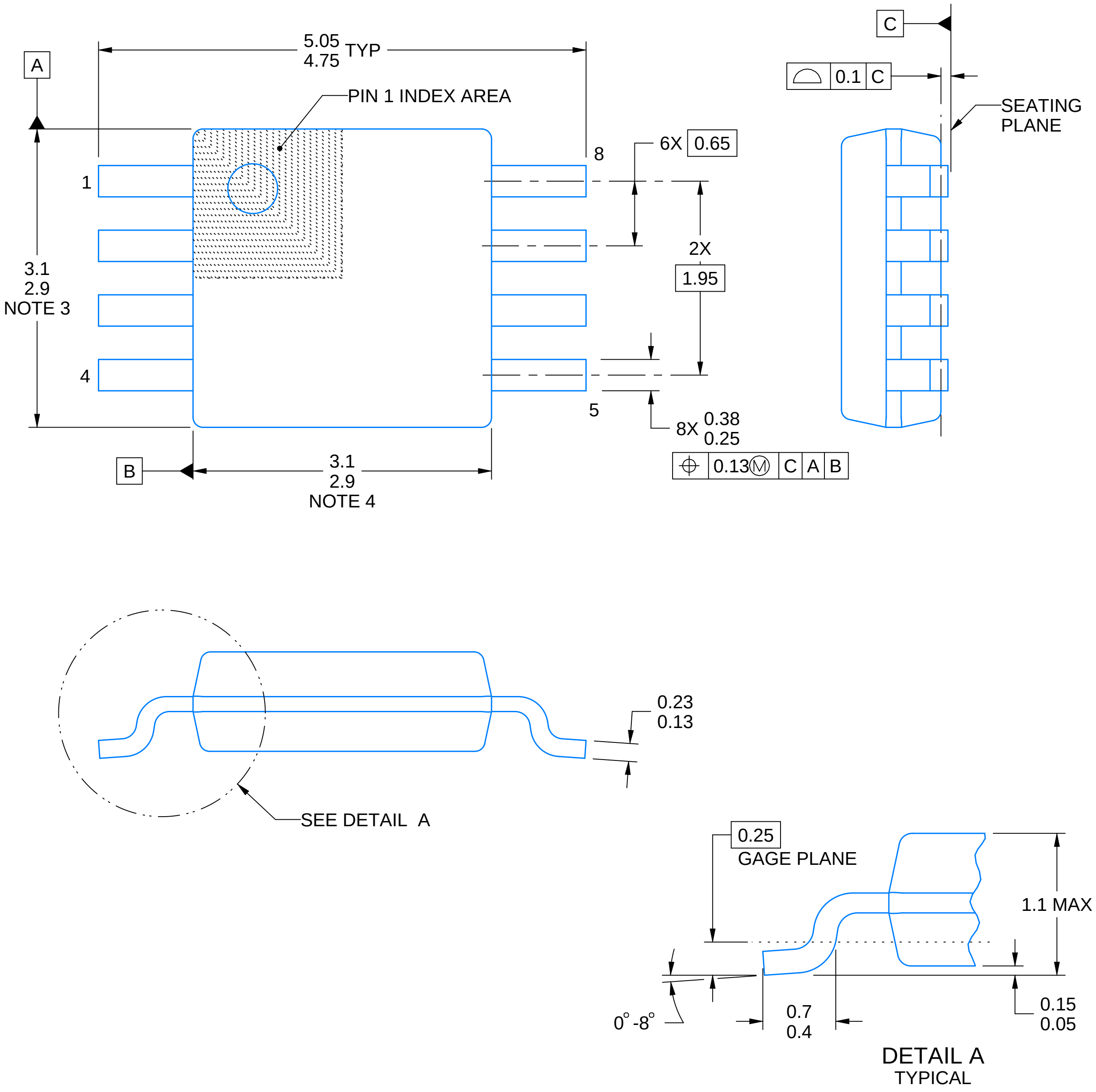
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

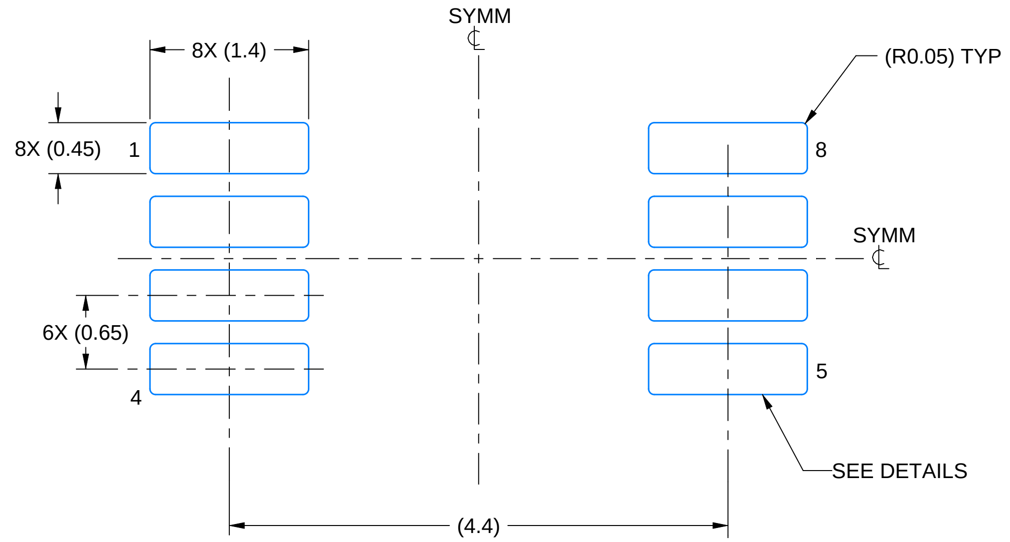


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

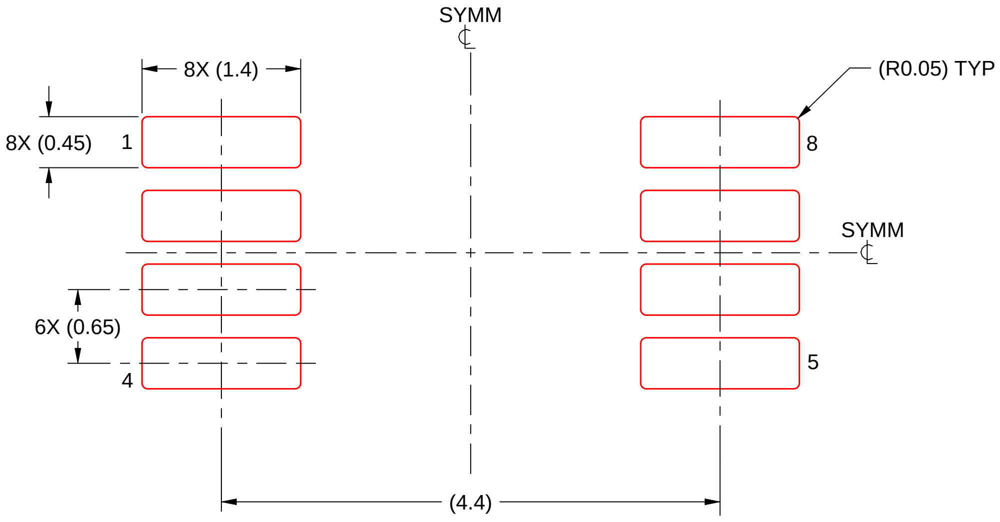
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

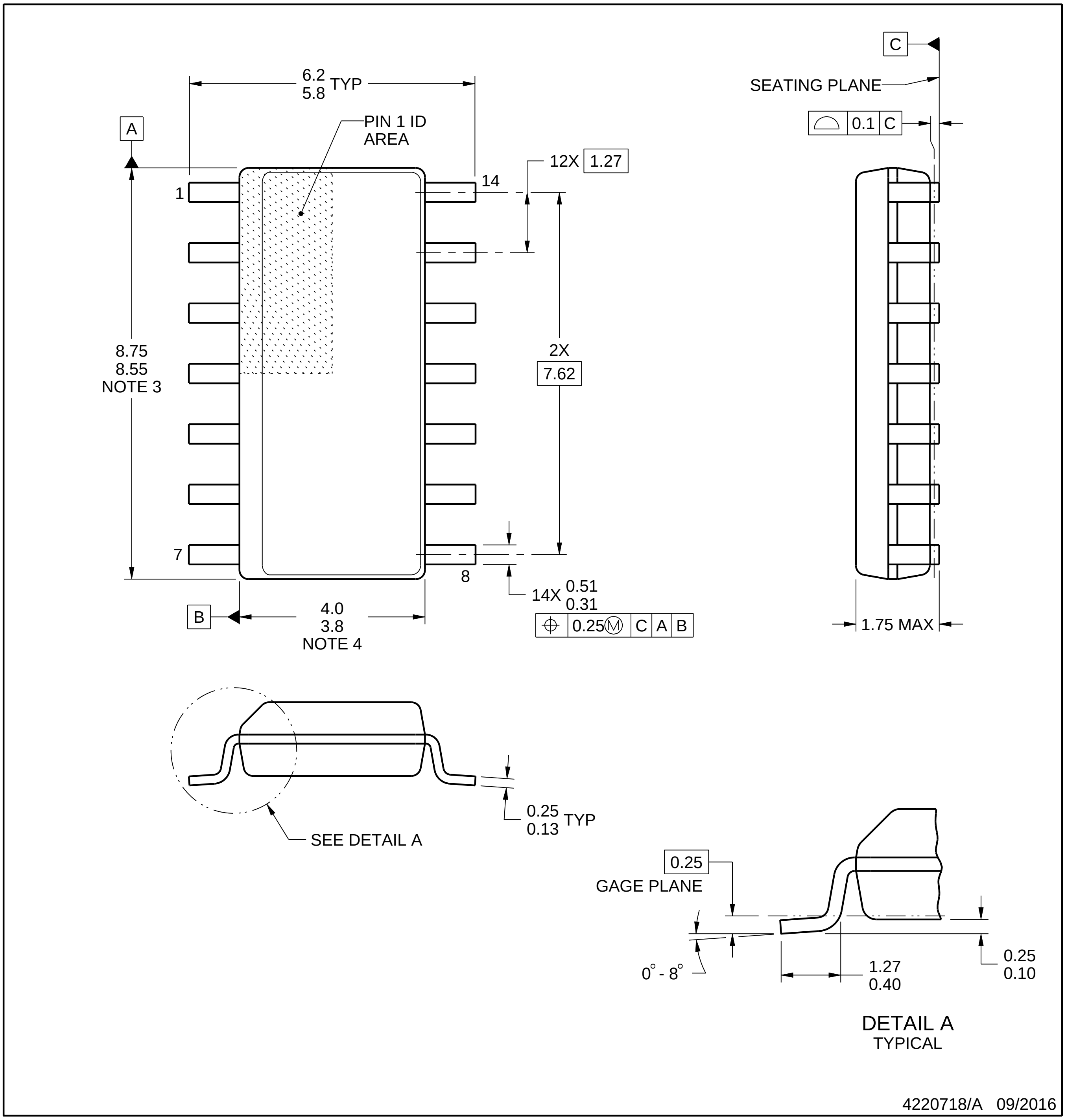
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A

SOIC - 1.75 mm max height

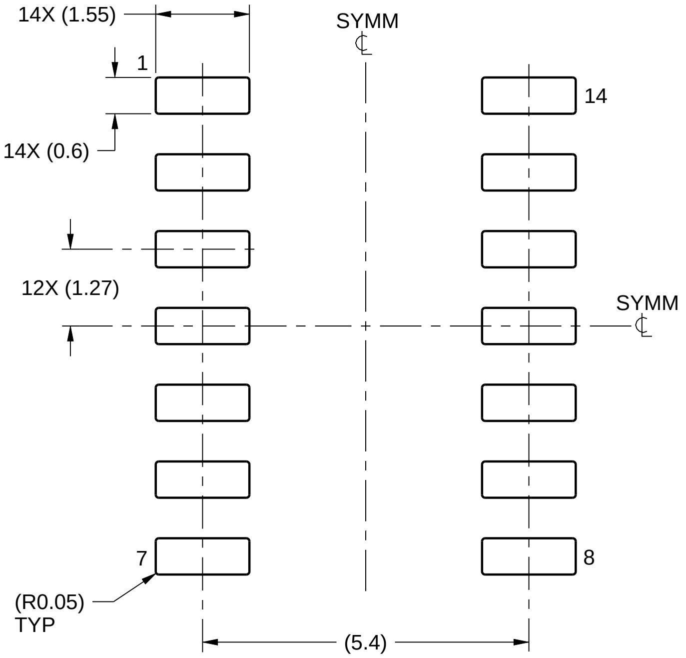
SMALL OUTLINE INTEGRATED CIRCUIT



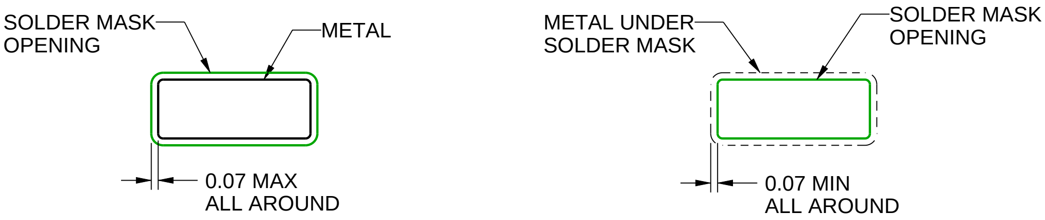
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:8X



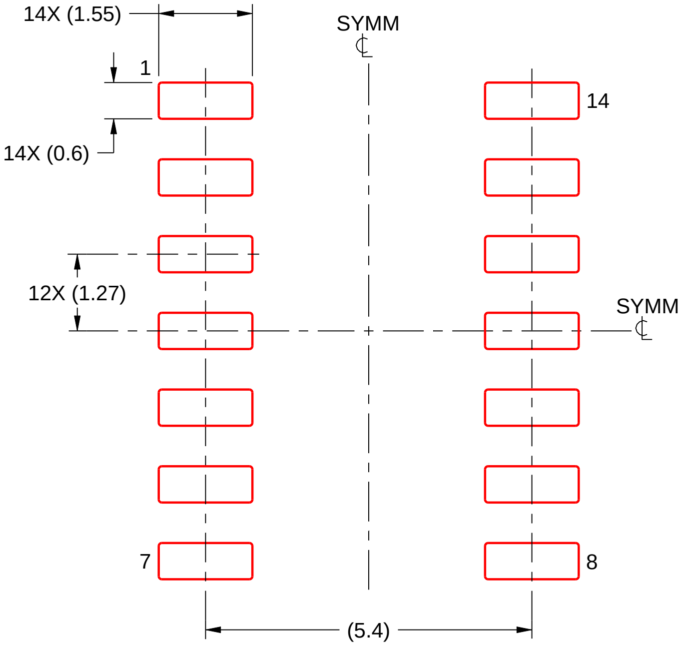
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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