

# LP38512-ADJ 1.5A Fast-Transient Response Adjustable Low-Dropout Linear Voltage Regulator

Check for Samples: [LP38512-ADJ](#)

## FEATURES

- 2.25V to 5.5V Input Voltage Range
- Adjustable Output Voltage Range of 0.5V to 4.5V
- 1.5A Output Load Current
- $\pm 2.0\%$  Accuracy over Line, Load, and Full-Temperature Range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Stable with Tiny 10  $\mu\text{F}$  Ceramic Capacitors
- Enable Pin
- Typically Less than 1 $\mu\text{A}$  of Ground Pin Current in when Enable Pin is Low
- 25dB of PSRR at 100 kHz
- Over-Temperature and Over-Current Protection
- 8-Pin SO PowerPad and 5-Pin PFM Surface Mount Packages

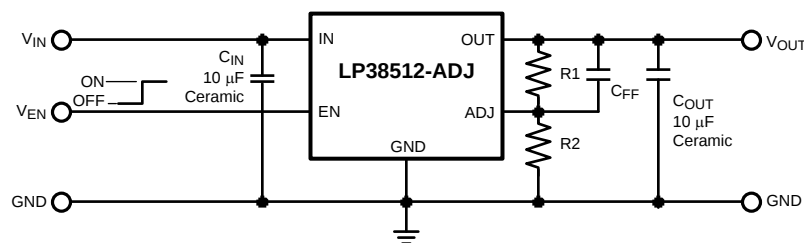
## APPLICATIONS

- Digital Core ASICs, FPGAs, and DSPs
- Servers
- Routers and Switches
- Base Stations
- Storage Area Networks
- DDR2 Memory

## DESCRIPTION

The LP38512-ADJ Fast-Transient Response Low-Dropout Voltage Regulator offers the highest-performance in meeting AC and DC accuracy requirements for powering Digital Cores. The LP38512-ADJ uses a proprietary control loop that enables extremely fast response to change in line conditions and load demands. Output Voltage DC accuracy is specified at 2.5% over line, load and full temperature range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The LP38512-ADJ is designed for inputs from the 2.5V, 3.3V, and 5.0V rail, is stable with 10  $\mu\text{F}$  ceramic capacitors, and has an adjustable output voltage. The LP38512-ADJ provides excellent transient performance to meet the demand of high performance digital core ASICs, DSPs, and FPGAs found in highly-intensive applications such as servers, routers/switches, and base stations.

## Typical Application Circuit



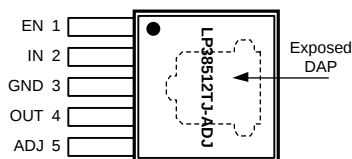
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

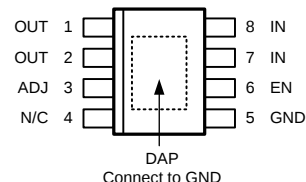
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2013, Texas Instruments Incorporated

## Connection Diagram



**Figure 1. 5-Pin PFM, Top View**  
See NDQ0005A Package



**Figure 2. 8-Pin SO PowerPad, Top View**  
See DDA0008A Package

### PIN DESCRIPTIONS FOR PFM PACKAGE

| Pin # | Pin Name | Function                                                                                                                                                                                                                                                                                                                          |
|-------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | EN       | Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.                                                                                                                                                                       |
| 2     | IN       | Input Supply Pin                                                                                                                                                                                                                                                                                                                  |
| 3     | GND      | Ground                                                                                                                                                                                                                                                                                                                            |
| 4     | OUT      | Regulated Output Voltage Pin                                                                                                                                                                                                                                                                                                      |
| 5     | ADJ      | The feedback to the internal Error Amplifier to set the output voltage                                                                                                                                                                                                                                                            |
| DAP   | DAP      | The PFM DAP is used as a thermal connection to remove heat from the device to an external heat-sink in the form of the copper area on the printed circuit board. The DAP is physically connected to backside of the die, but is not internally connected to device ground. The DAP should be soldered to the Ground Plane copper. |

### PIN DESCRIPTIONS FOR SO PowerPad PACKAGE

| Pin # | Pin Name | Function                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2  | OUT      | Regulated Output Voltage Pin. Pins share current and must be connected together.                                                                                                                                                                                                                                                                     |
| 3     | ADJ      | The feedback to the internal Error Amplifier to set the output voltage                                                                                                                                                                                                                                                                               |
| 4     | N/C      | No internal connection.                                                                                                                                                                                                                                                                                                                              |
| 5     | GND      | Ground                                                                                                                                                                                                                                                                                                                                               |
| 6     | EN       | Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.                                                                                                                                                                                          |
| 7, 8  | IN       | Input Supply Pin. Pins share current and must be connected together.                                                                                                                                                                                                                                                                                 |
| DAP   | DAP      | The SO PowerPad DAP connection is used as a thermal connection to remove heat from the device to an external heat-sink in the form of the copper area on the printed circuit board. The DAP is physically connected to backside of the die, but is not internally connected to device ground. The DAP should be soldered to the Ground Plane copper. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)</sup>

|                                      |             |                    |
|--------------------------------------|-------------|--------------------|
| Storage Temperature Range            |             | -65°C to +150°C    |
| Soldering Temperature <sup>(2)</sup> | PFM         | 260°C, 10s         |
|                                      | SO PowerPad | 260°C, 10s         |
| ESD Rating <sup>(3)</sup>            |             | ±2 kV              |
| Power Dissipation <sup>(4)</sup>     |             | Internally Limited |
| Input Pin Voltage (Survival)         |             | -0.3V to +6.0V     |
| Enable Pin Voltage (Survival)        |             | -0.3V to +6.0V     |
| Output Pin Voltage (Survival)        |             | -0.3V to +6.0V     |
| ADJ Pin Voltage (Survival)           |             | -0.3V to +6.0V     |
| I <sub>OUT</sub> (Survival)          |             | Internally Limited |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
- (2) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperatures and times are for Sn-Pb (STD) only.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22-A114.
- (4) Device operation must be evaluated, and derated as needed, based on ambient temperature (T<sub>A</sub>), power dissipation (P<sub>D</sub>), maximum allowable operating junction temperature (T<sub>J(MAX)</sub>), and package thermal resistance (θ<sub>JA</sub>). The typical θ<sub>JA</sub> ratings given are worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See [POWER DISSIPATION/HEAT-SINKING](#) for details.

## Operating Ratings<sup>(1)</sup>

|                                       |                        |
|---------------------------------------|------------------------|
| Input Supply Voltage, V <sub>IN</sub> | 2.25V to 5.5V          |
| Output Voltage, V <sub>OUT</sub>      | V <sub>ADJ</sub> to 5V |
| Enable Input Voltage, V <sub>EN</sub> | 0.0V to 5.5V           |
| Output Current (DC)                   | 1 mA to 1.5A           |
| Junction Temperature <sup>(2)</sup>   | -40°C to +125°C        |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
- (2) Device operation must be evaluated, and derated as needed, based on ambient temperature (T<sub>A</sub>), power dissipation (P<sub>D</sub>), maximum allowable operating junction temperature (T<sub>J(MAX)</sub>), and package thermal resistance (θ<sub>JA</sub>). The typical θ<sub>JA</sub> ratings given are worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See [POWER DISSIPATION/HEAT-SINKING](#) for details.

## Electrical Characteristics

Unless otherwise specified: V<sub>IN</sub> = 2.50V, V<sub>OUT</sub> = V<sub>ADJ</sub>, I<sub>OUT</sub> = 10 mA, C<sub>IN</sub> = 10 μF, C<sub>OUT</sub> = 10 μF, V<sub>EN</sub> = 2.0V. Limits in standard type are for T<sub>J</sub> = 25°C only; limits in **boldface type** apply over the junction temperature (T<sub>J</sub>) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25°C, and are provided for reference purposes only.

| Symbol                               | Parameter                                          | Conditions                                                        | Min                   | Typ                 | Max                   | Units |
|--------------------------------------|----------------------------------------------------|-------------------------------------------------------------------|-----------------------|---------------------|-----------------------|-------|
| V <sub>ADJ</sub>                     | V <sub>ADJ</sub> Accuracy <sup>(1)</sup>           | 2.25V ≤ V <sub>IN</sub> ≤ 5.5V<br>10 mA ≤ I <sub>OUT</sub> ≤ 1.5A | 495.0<br><b>490.0</b> | 500.                | 505.0<br><b>510.0</b> | mV    |
| I <sub>ADJ</sub>                     | ADJ Pin Bias Current                               | 2.25V ≤ V <sub>IN</sub> ≤ 5.5V                                    | -                     | 1                   | -                     | nA    |
| ΔV <sub>ADJ</sub> /ΔV <sub>IN</sub>  | V <sub>ADJ</sub> Line Regulation <sup>(2)(1)</sup> | 2.25V ≤ V <sub>IN</sub> ≤ 5.5V                                    | -                     | 0.03<br><b>0.06</b> | -                     | %/V   |
| ΔV <sub>ADJ</sub> /ΔI <sub>OUT</sub> | V <sub>ADJ</sub> Load Regulation <sup>(3)(1)</sup> | 10 mA ≤ I <sub>OUT</sub> ≤ 1.5A                                   | -                     | 0.10<br><b>0.20</b> | -                     | %/A   |
| V <sub>DO</sub>                      | Dropout Voltage <sup>(4)</sup>                     | I <sub>OUT</sub> = 1.5A                                           | -                     | -                   | <b>300</b>            | mV    |

- (1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
- (2) Line regulation is defined as the change in V<sub>ADJ</sub> from the nominal value due to change in the voltage at the input.
- (3) Load regulation is defined as the change in V<sub>ADJ</sub> from the nominal value due to change in the load current at the output.
- (4) Dropout voltage (V<sub>DO</sub>) is typically defined as the input to output voltage differential (V<sub>IN</sub> - V<sub>OUT</sub>) where the input voltage is low enough to cause the output voltage to drop 2%. For the LP38512-ADJ, the minimum operating voltage of 2.25V is the limiting factor when the programed output voltage is less than typically 1.80V.

## Electrical Characteristics (continued)

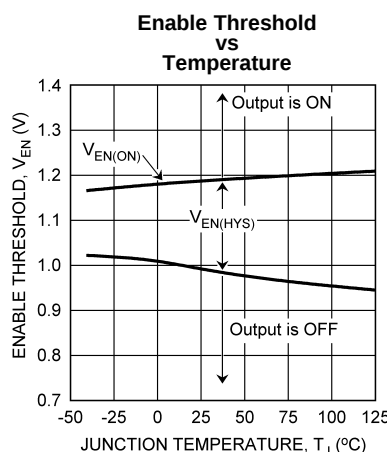
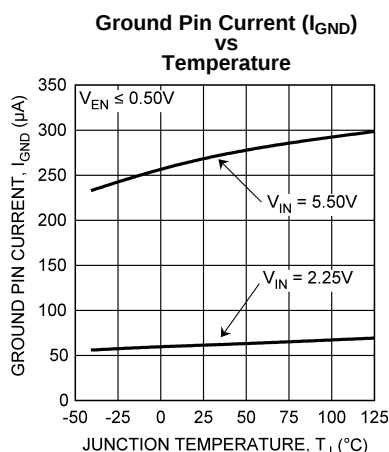
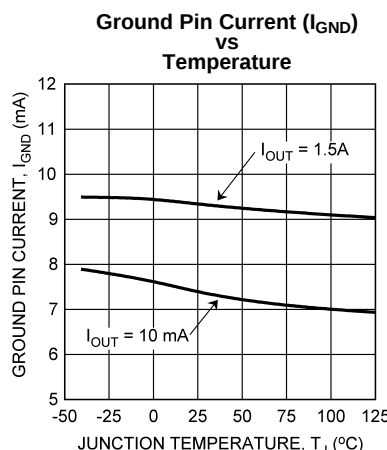
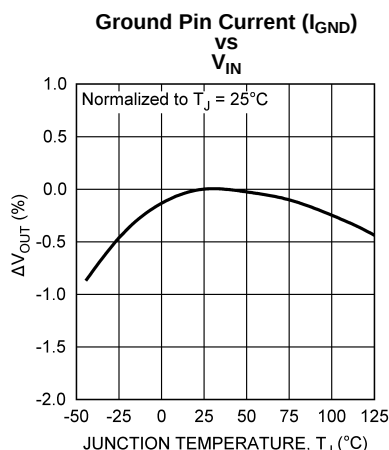
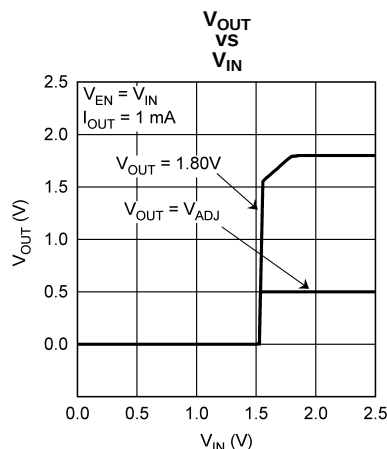
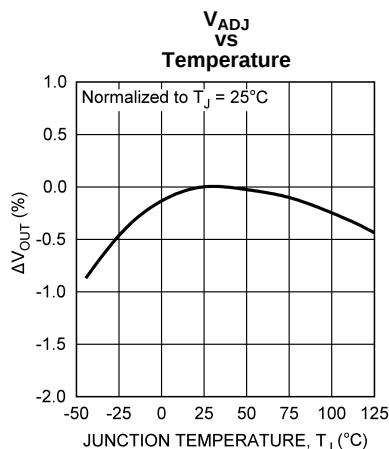
Unless otherwise specified:  $V_{IN} = 2.50V$ ,  $V_{OUT} = V_{ADJ}$ ,  $I_{OUT} = 10\text{ mA}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $V_{EN} = 2.0V$ . Limits in standard type are for  $T_J = 25^\circ\text{C}$  only; limits in **boldface type** apply over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only.

| Symbol                  | Parameter                                             | Conditions                                                                                          | Min          | Typ  | Max          | Units             |
|-------------------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------|--------------|------|--------------|-------------------|
| I <sub>GND</sub>        | Ground Pin Current, Output Enabled                    | I <sub>OUT</sub> = 10 mA                                                                            | -            | 10   | 12<br>15     | mA                |
|                         |                                                       | I <sub>OUT</sub> = 1.5A                                                                             | -            | 10   | 12<br>14     |                   |
|                         | Ground Pin Current, Output Disabled                   | V <sub>EN</sub> = 0.50V                                                                             | -            | 60   | 100<br>110   | μA                |
| I <sub>SC</sub>         | Short Circuit Current                                 | V <sub>OUT</sub> = 0V                                                                               | -            | 2.8  | -            | A                 |
| Enable Input            |                                                       |                                                                                                     |              |      |              |                   |
| V <sub>EN(ON)</sub>     | Enable ON Voltage Threshold                           | V <sub>EN</sub> rising from < V <sub>EN(OFF)</sub> until V <sub>OUT</sub> = ON                      | 0.90<br>0.80 | 1.20 | 1.50<br>1.60 | V                 |
| V <sub>EN(OFF)</sub>    | Enable OFF Voltage Threshold                          | V <sub>EN</sub> falling from > V <sub>EN(ON)</sub> until V <sub>OUT</sub> = OFF                     | 0.60<br>0.50 | 1.00 | 1.40<br>1.50 | V                 |
| V <sub>EN(HYS)</sub>    | Enable Voltage Hysteresis                             | V <sub>EN(ON)</sub> - V <sub>EN(OFF)</sub>                                                          | -            | 200  | -            | mV                |
| I <sub>EN</sub>         | Enable Pin Current                                    | V <sub>EN</sub> = V <sub>IN</sub>                                                                   | -            | 1    | -            | nA                |
|                         |                                                       | V <sub>EN</sub> = 0V                                                                                | -            | -1   | -            |                   |
| t <sub>d(OFF)</sub>     | Turn-off delay                                        | Time from V <sub>EN</sub> < V <sub>EN(TH)</sub> to V <sub>OUT</sub> = OFF, I <sub>LOAD</sub> = 1.5A | -            | 5    | -            | μs                |
| t <sub>d(ON)</sub>      | Turn-on delay                                         | Time from V <sub>EN</sub> > V <sub>EN(TH)</sub> to V <sub>OUT</sub> = ON, I <sub>LOAD</sub> = 1.5A  | -            | 5    | -            |                   |
| AC Parameters           |                                                       |                                                                                                     |              |      |              |                   |
| PSRR                    | Ripple Rejection                                      | V <sub>IN</sub> = 2.5V<br>f = 120Hz                                                                 | -            | 73   | -            | dB                |
|                         |                                                       | V <sub>IN</sub> = 2.5V<br>f = 1 kHz                                                                 | -            | 70   | -            |                   |
| ρ <sub>n(f)</sub>       | Output Noise Density                                  | f = 120Hz                                                                                           | -            | 0.4  | -            | μV/√Hz            |
| e <sub>n</sub>          | Output Noise Voltage                                  | BW = 10Hz - 100kHz                                                                                  | -            | 25   | -            | μV <sub>RMS</sub> |
| Thermal Characteristics |                                                       |                                                                                                     |              |      |              |                   |
| T <sub>SD</sub>         | Thermal Shutdown                                      | T <sub>J</sub> rising                                                                               | -            | 165  | -            | °C                |
| ΔT <sub>SD</sub>        | Thermal Shutdown Hysteresis                           | T <sub>J</sub> falling from T <sub>SD</sub>                                                         | -            | 10   | -            |                   |
| θ <sub>J-A</sub>        | Thermal Resistance Junction to Ambient <sup>(5)</sup> | SO PowerPad                                                                                         | -            | 168  | -            | °C/W              |
|                         |                                                       | PFM                                                                                                 | -            | 67   | -            |                   |
| θ <sub>J-C</sub>        | Thermal Resistance Junction to Case                   | SO PowerPad                                                                                         | -            | 11   | -            | °C/W              |
|                         |                                                       | PFM                                                                                                 | -            | 3    | -            |                   |

- (5) Device operation must be evaluated, and derated as needed, based on ambient temperature ( $T_A$ ), power dissipation ( $P_D$ ), maximum allowable operating junction temperature ( $T_{J(MAX)}$ ), and package thermal resistance ( $\theta_{JA}$ ). The typical  $\theta_{JA}$  ratings given are worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See [POWER DISSIPATION/HEAT-SINKING](#) for details.

## Typical Performance Characteristics

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 2.50\text{V}$ ,  $V_{OUT} = V_{ADJ}$ ,  $V_{EN} = 2.0\text{V}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $I_{OUT} = 10\ \text{mA}$ .



## Typical Performance Characteristics (continued)

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 2.50\text{V}$ ,  $V_{OUT} = V_{ADJ}$ ,  $V_{EN} = 2.0\text{V}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $I_{OUT} = 10\ \text{mA}$ .

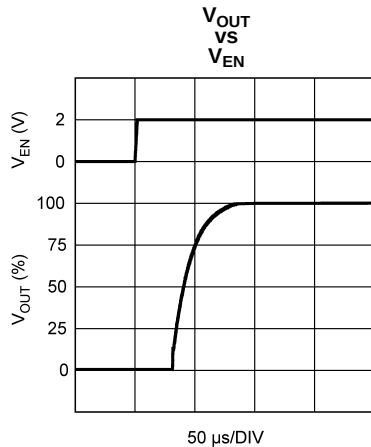


Figure 9.

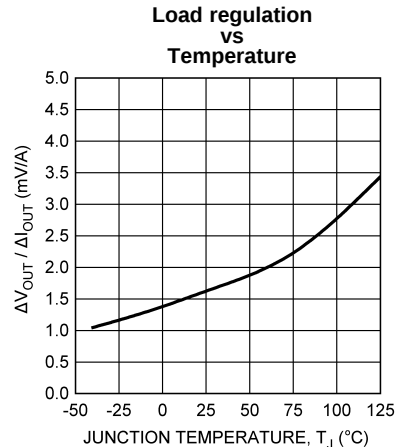


Figure 10.

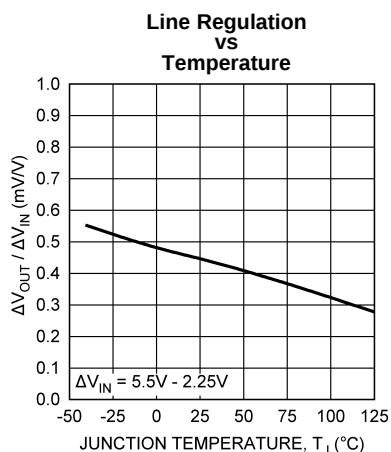


Figure 11.

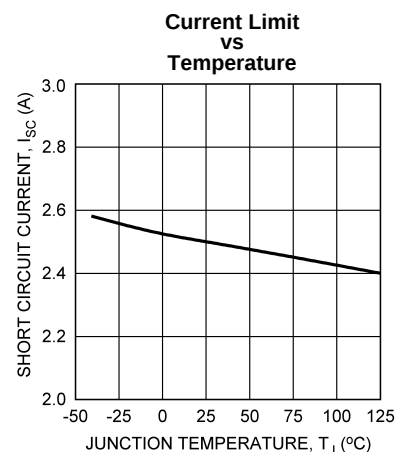


Figure 12.

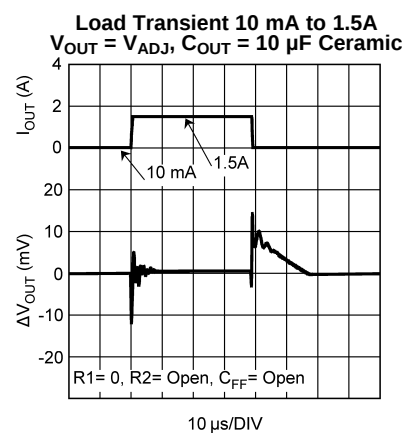


Figure 13.

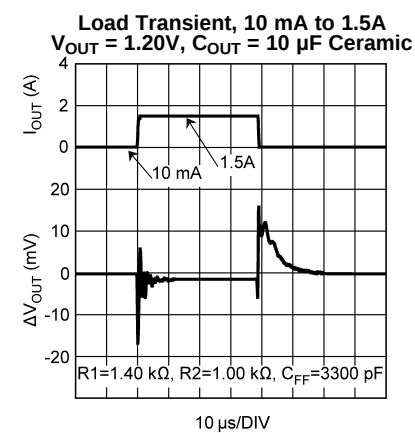


Figure 14.

## Typical Performance Characteristics (continued)

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 2.50\text{V}$ ,  $V_{OUT} = V_{ADJ}$ ,  $V_{EN} = 2.0\text{V}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $I_{OUT} = 10\text{ mA}$ .

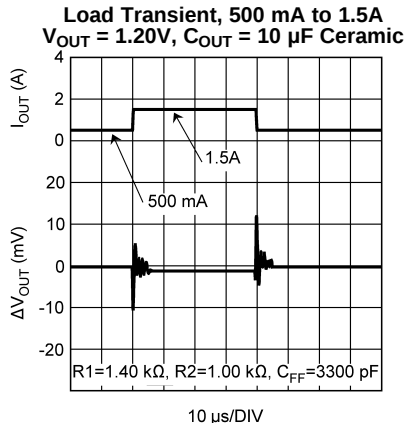


Figure 15.

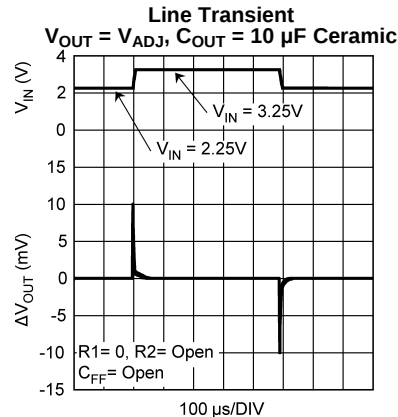


Figure 16.

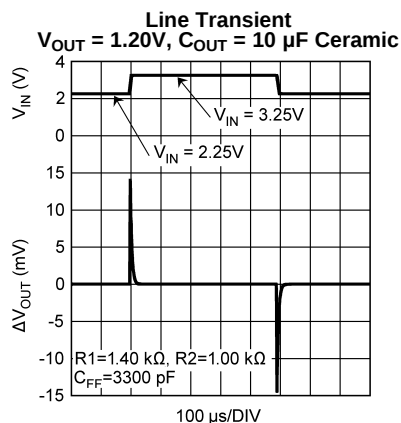


Figure 17.

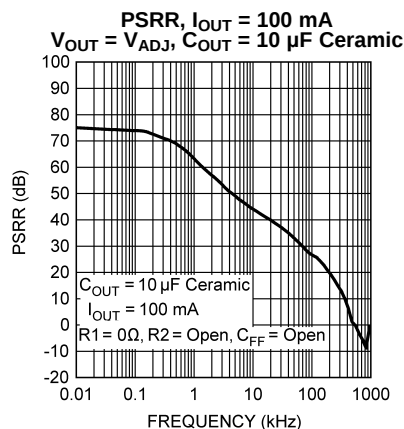


Figure 18.

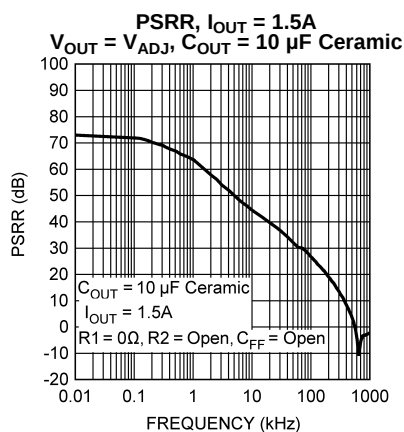


Figure 19.

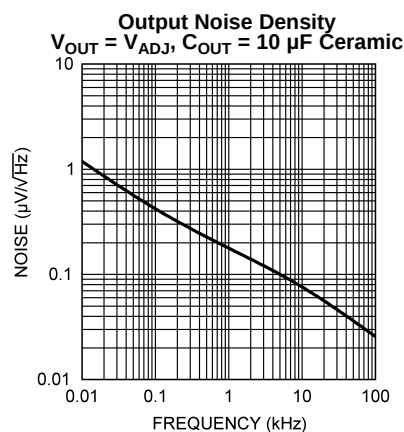
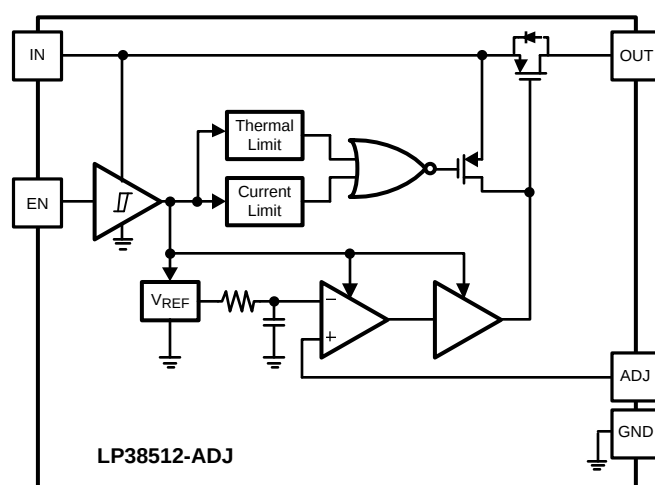


Figure 20.

## Block Diagram



## APPLICATION INFORMATION

### EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

#### Input Capacitor

A ceramic input capacitor of at least 10  $\mu\text{F}$  is required. For general usage across all load currents and operating conditions, a 10  $\mu\text{F}$  ceramic input capacitor will provide satisfactory performance.

#### Output Capacitor

A ceramic capacitor with a minimum value of 10  $\mu\text{F}$  is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pin using traces which have no other currents flowing through them. As long as the minimum of 10  $\mu\text{F}$  ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within  $\pm 20\%$  of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drop severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

### REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when  $V_{\text{IN}}$  is abruptly taken low and  $C_{\text{OUT}}$  continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

While  $V_{\text{IN}}$  is high enough to keep the control circuitry alive, and the Enable pin is above the  $V_{\text{EN(ON)}}$  threshold, the control circuitry will attempt to regulate the output voltage. Since the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full on condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the  $R_{\text{DS(ON)}}$  of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000  $\mu\text{F}$  in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable is low this condition will be prevented.

The internal PFET pass element in the LP38512-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output voltage to input voltage differential is more than 500 mV (typical) the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

### SHORT-CIRCUIT PROTECTION

The LP38512-ADJ is short circuit protected, and in the event of a peak over-current condition the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the [POWER DISSIPATION/HEAT-SINKING](#) section for power dissipation calculations.

## SETTING THE OUTPUT VOLTAGE

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + (R1/R2)) \quad (1)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of  $V_{ADJ}$  is specified, the final value of  $V_{OUT}$  is not. The use of low quality resistors for R1 and R2 can easily produce a  $V_{OUT}$  value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 1.00 kΩ. This is to reduce the possibility of any internal parasitic capacitances on the ADJ pin from creating an undesirable phase shift that may interfere with device stability.

$$( (R1 \times R2) / (R1 + R2) ) \leq 1.00 \text{ k}\Omega \quad (2)$$

## FEED FORWARD CAPACITOR, $C_{FF}$

When using a ceramic capacitor for  $C_{OUT}$ , the typical ESR value will be too small to provide any meaningful positive phase compensation,  $F_Z$ , to offset the internal negative phase shifts in the gain loop.

$$F_Z = 1 / (2 \times \pi \times C_{OUT} \times \text{ESR}) \quad (3)$$

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor,  $C_{FF}$ , in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (4)$$

For optimum load transient response select  $C_{FF}$  so the zero frequency,  $F_Z$ , falls between 20 kHz and 40 kHz.

$$C_{FF} = 1 / (2 \times \pi \times R1 \times F_Z) \quad (5)$$

The phase lead provided by  $C_{FF}$  diminishes as the DC gain approaches unity, or  $V_{OUT}$  approaches  $V_{ADJ}$ . This is because  $C_{FF}$  also forms a pole with a frequency of:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times (R1 \parallel R2)) \quad (6)$$

It's important to note that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero move closer together. The phase lead provided from  $C_{FF}$  diminishes quickly as the output voltage is reduced, and has no effect when  $V_{OUT} = V_{ADJ}$ . For this reason, relying on this compensation technique alone is adequate only for higher output voltages.

**Table 1** lists some suggested, best fit, standard  $\pm 1\%$  resistor values for R1 and R2, and a standard  $\pm 10\%$  capacitor values for  $C_{FF}$ , for a range of  $V_{OUT}$  values. Other values of R1, R2, and  $C_{FF}$  are available that will give similar results.

**Table 1.**

| $V_{OUT}$ | $R_1$   | $R_2$   | $C_{FF}$ | $F_Z$    |
|-----------|---------|---------|----------|----------|
| 0.80V     | 1.07 kΩ | 1.78 kΩ | 4700 pF  | 31.6 kHz |
| 1.00V     | 1.00 kΩ | 1.00 kΩ | 4700 pF  | 33.8 kHz |
| 1.20V     | 1.40 kΩ | 1.00 kΩ | 3300 pF  | 34.4 kHz |
| 1.50V     | 2.00 kΩ | 1.00 kΩ | 2700 pF  | 29.5 kHz |
| 1.80V     | 2.94 kΩ | 1.13 kΩ | 1500 pF  | 36.1kHz  |
| 2.00V     | 1.02 kΩ | 340Ω    | 4700 pF  | 33.2 kHz |
| 2.50V     | 1.02 kΩ | 255Ω    | 4700 pF  | 33.2 kHz |
| 3.00V     | 1.00 kΩ | 200Ω    | 4700 pF  | 33.8 kHz |
| 3.30V     | 2.00 kΩ | 357Ω    | 2700 pF  | 29.5 kHz |

Please refer to Application Note *AN-1378 Method For Calculating Output Voltage Tolerances in Adjustable Regulators* ([SNVA112](#)) for additional information on how resistor tolerances affect the calculated  $V_{OUT}$  value.

## ENABLE OPERATION

The Enable ON threshold is typically 1.2V, and the OFF threshold is typically 1.0V. To ensure reliable operation the Enable pin voltage must rise above the maximum  $V_{EN(ON)}$  threshold and must fall below the minimum  $V_{EN(OFF)}$  threshold. The Enable threshold has typically 200mV of hysteresis to improve noise immunity.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the Enable pin is driven from a single ended device (such as the collector of a discrete transistor) a pull-up resistor to  $V_{IN}$ , or a pull-down resistor to ground, will be required for proper operation. A 1 k $\Omega$  to 100 k $\Omega$  resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the pin should be connected directly to the adjacent  $V_{IN}$  pin.

## POWER DISSIPATION/HEAT-SINKING

A heat-sink may be required depending on the maximum power dissipation ( $P_{D(MAX)}$ ), maximum ambient temperature ( $T_{A(MAX)}$ ) of the application, and the thermal resistance ( $\theta_{JA}$ ) of the package. Under all possible conditions, the junction temperature ( $T_J$ ) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + (V_{IN}) \times I_{GND} \quad (7)$$

where  $I_{GND}$  is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise ( $\Delta T_J$ ) depends on the maximum expected ambient temperature ( $T_{A(MAX)}$ ) of the application, and the maximum allowable junction temperature ( $T_{J(MAX)}$ ):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (8)$$

The maximum allowable value for junction to ambient Thermal Resistance,  $\theta_{JA}$ , can be calculated using the formula:

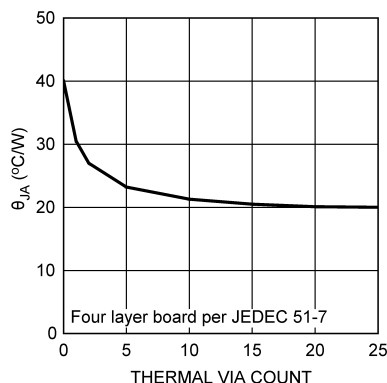
$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (9)$$

LP38512-ADJ is available in PFM and SO PowerPad surface mount packages. For a comparison of the PFM package to the standard TO-263 package see Application Note *AN-1797 PFM Package* ([SNVA328](#)). The  $\theta_{JA}$  thermal resistance depends on amount of copper area, or heat sink, attached to the DAP, and on air flow. See Application Note *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* ([SNVA183](#)) for guidelines.

### Heat-Sinking the PFM Package

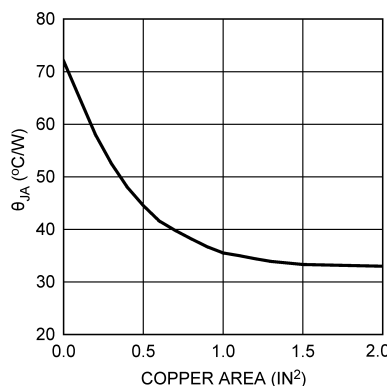
The DAP of the PFM package is soldered to the copper plane for heat sinking. The PFM package has a  $\theta_{JA}$  rating of 67°C/W, and a  $\theta_{JC}$  rating of 2°C/W. The  $\theta_{JA}$  rating of 67°C/W includes the device DAP soldered to an area of 0.055 square inches (0.22 in x 0.25 in) of 1 ounce copper on a two sided PCB, with no airflow. See JEDEC standard EIA/JESD51-3 for more information.

**Figure 21** shows a curve for the  $\theta_{JA}$  of PFM package for different thermal via counts under the exposed DAP, using a four layer PCB for heat sinking. The thermal vias connect the copper area directly under the exposed DAP to the first internal copper plane only. See JEDEC standards EIA/JESD51-5 and EIA/JESD51-7 for more information.



**Figure 21.  $\theta_{JA}$  vs Thermal Via Count for the PFM Package on 4-Layer PCB**

Figure 22 shows the thermal performance when the Thin TO-263 is mounted to a two layer PCB where the copper area is predominately directly under the exposed DAP. As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement.

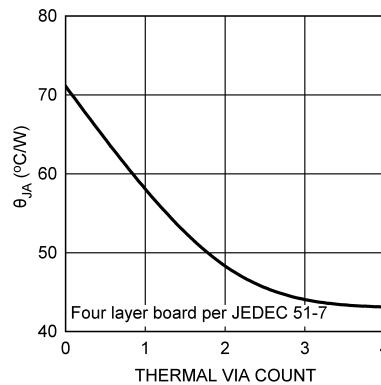


**Figure 22.  $\theta_{JA}$  vs Copper Area for the PFM Package**

### Heat-Sinking The SO PowerPad Package

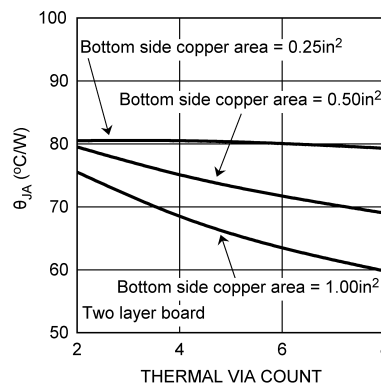
The DAP of the SO PowerPad package is soldered to the copper plane for heat sinking. The LP38512MR package has a  $\theta_{JA}$  rating of 168°C/W, and a  $\theta_{JC}$  rating of 11°C/W. The  $\theta_{JA}$  rating of 168°C/W includes the device DAP soldered to an area of 0.008 square inches (0.09 in x 0.09 in) of 1 ounce copper on a two sided PCB, with no airflow. See JEDEC standard EIA/JESD51-3 for more information.

Figure 23 shows a curve for different thermal via counts under the exposed DAP, using a four layer PCB for heat sinking. The thermal vias connect the copper area directly under the exposed DAP to the first internal copper plane only. See JEDEC standards EIA/JESD51-5 and EIA/JESD51-7 for more information.



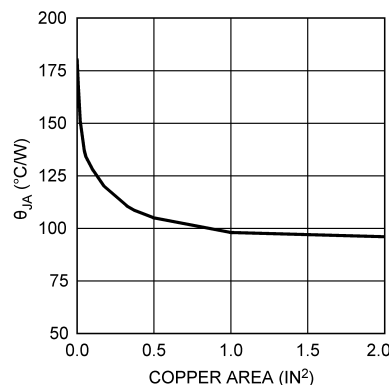
**Figure 23.  $\theta_{JA}$  vs Thermal Via Count for the SO PowerPad Package on 2-Layer PCB with Copper Area on Bottom-Side**

Figure 24 shows thermal performance for a two layer board using thermal vias to a copper area on the bottom of the PCB. The copper area on the top of the PCB, which is soldered to the exposed DAP, is 0.10in x 0.20in, which is approximately the same dimensions as the body of the SO PowerPad package. The copper area on the bottom of the PCB is a square area and is centered directly under the SO PowerPad package.



**Figure 24.  $\theta_{JA}$  vs Thermal Via Count for the SO PowerPad Package on 2-Layer PCB with Copper Area on Bottom-Side**

Figure 25 shows thermal performance for a two layer board with the DAP soldered to copper area on the of the PCB only. Increasing the copper area soldered to the DAP to 1 square inch of 1 ounce copper, using a dog-bone type layout, will produce a typical  $\theta_{JA}$  rating of 98°C/W.



**Figure 25.  $\theta_{JA}$  vs Copper Area for the SO PowerPad Package on 2-Layer PCB with Copper Area on Top-Side**



## REVISION HISTORY

### Changes from Revision C (April 2013) to Revision D

### Page

- Changed layout of National Data Sheet to TI format ..... [13](#)

## PACKAGING INFORMATION

| Orderable part number               | Status<br>(1) | Material type<br>(2) | Package   Pins        | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------------|---------------|----------------------|-----------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LP38512MR-ADJ/NOPB</a>  | Active        | Production           | SO PowerPAD (DDA)   8 | 95   TUBE             | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | L38512-ADJ          |
| LP38512MR-ADJ/NOPB.A                | Active        | Production           | SO PowerPAD (DDA)   8 | 95   TUBE             | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | L38512-ADJ          |
| LP38512MRX-ADJ/NO.A                 | Active        | Production           | SO PowerPAD (DDA)   8 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | L38512-ADJ          |
| <a href="#">LP38512MRX-ADJ/NOPB</a> | Active        | Production           | SO PowerPAD (DDA)   8 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | L38512-ADJ          |
| <a href="#">LP38512TJ-ADJ/NOPB</a>  | Active        | Production           | TO-263 (NDQ)   5      | 1000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LP38512TJ-ADJ       |
| LP38512TJ-ADJ/NOPB.A                | Active        | Production           | TO-263 (NDQ)   5      | 1000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LP38512TJ-ADJ       |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device              | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP38512MRX-ADJ/NOPB | SO PowerPAD  | DDA             | 8    | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| LP38512TJ-ADJ/NOPB  | TO-263       | NDQ             | 5    | 1000 | 330.0              | 24.4               | 10.6    | 15.4    | 2.45    | 12.0    | 24.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device              | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP38512MRX-ADJ/NOPB | SO PowerPAD  | DDA             | 8    | 2500 | 356.0       | 356.0      | 36.0        |
| LP38512TJ-ADJ/NOPB  | TO-263       | NDQ             | 5    | 1000 | 367.0       | 367.0      | 35.0        |

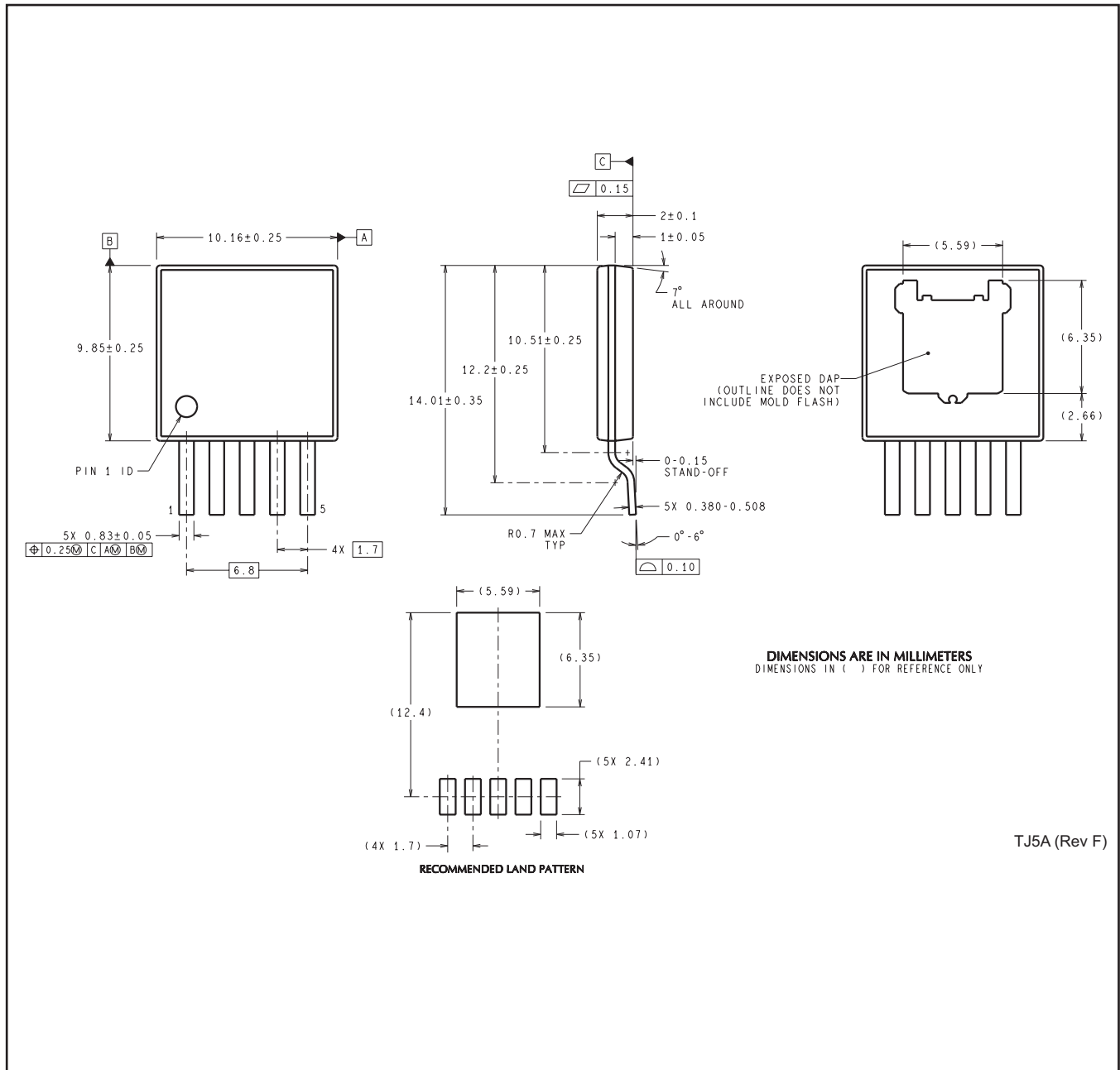
## TUBE

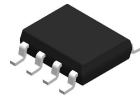


\*All dimensions are nominal

| Device               | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LP38512MR-ADJ/NOPB   | DDA          | HSOIC        | 8    | 95  | 495    | 8      | 4064   | 3.05   |
| LP38512MR-ADJ/NOPB.A | DDA          | HSOIC        | 8    | 95  | 495    | 8      | 4064   | 3.05   |

NDQ0005A

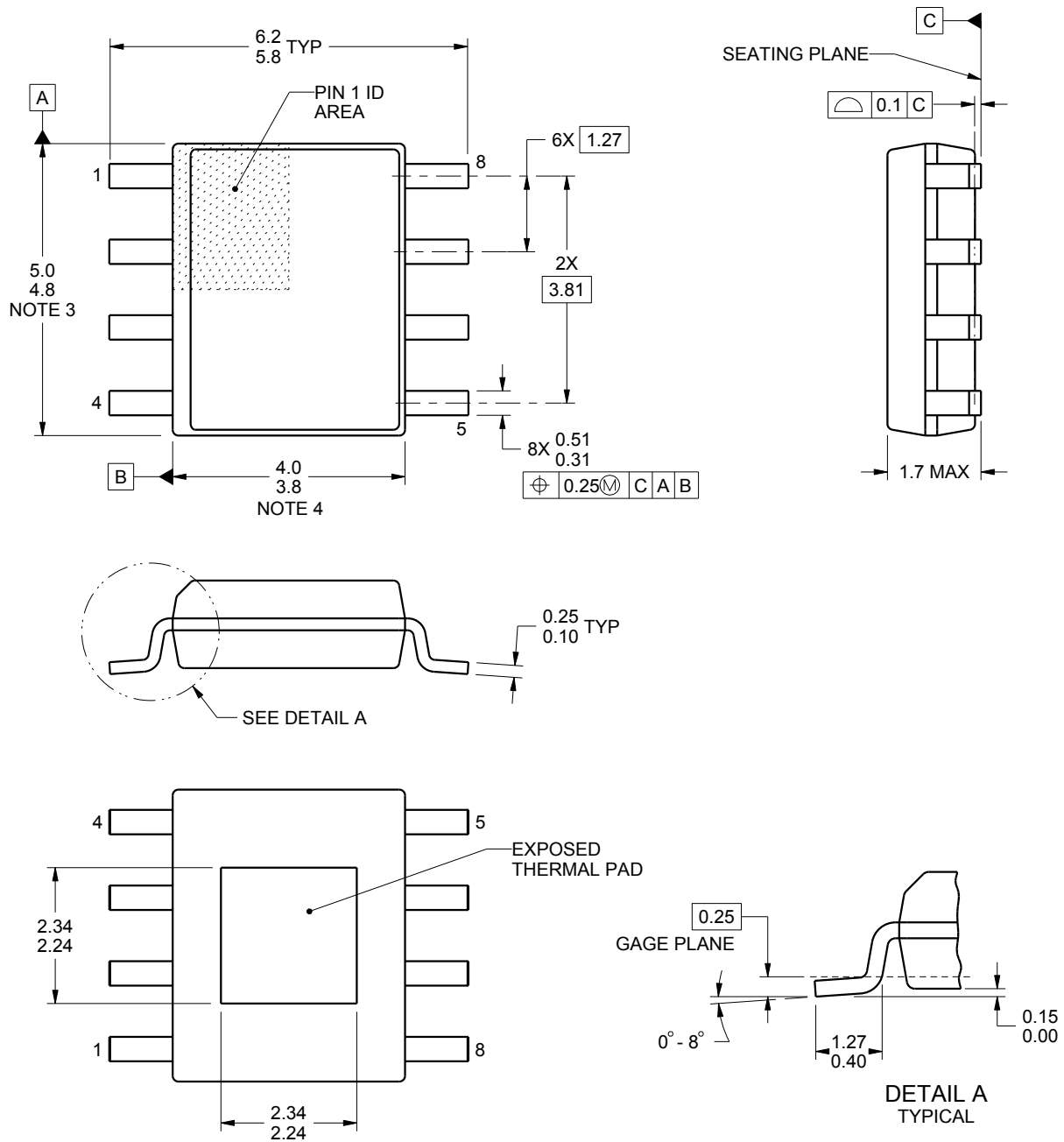


**DDA0008A**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4218825/A 05/2016

PowerPAD is a trademark of Texas Instruments.

**NOTES:**

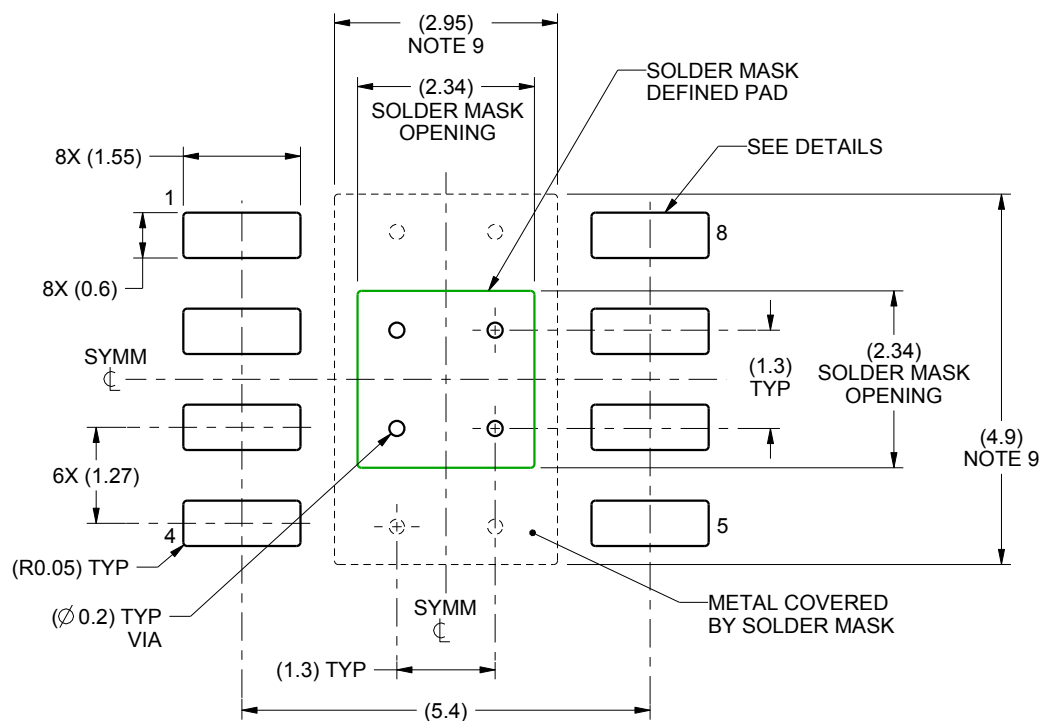
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

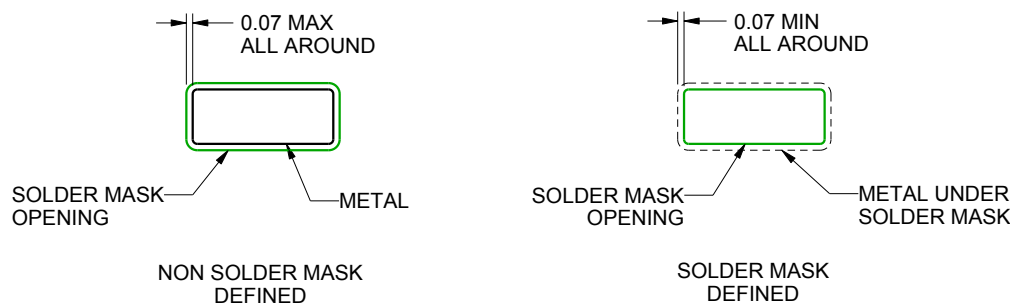
DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

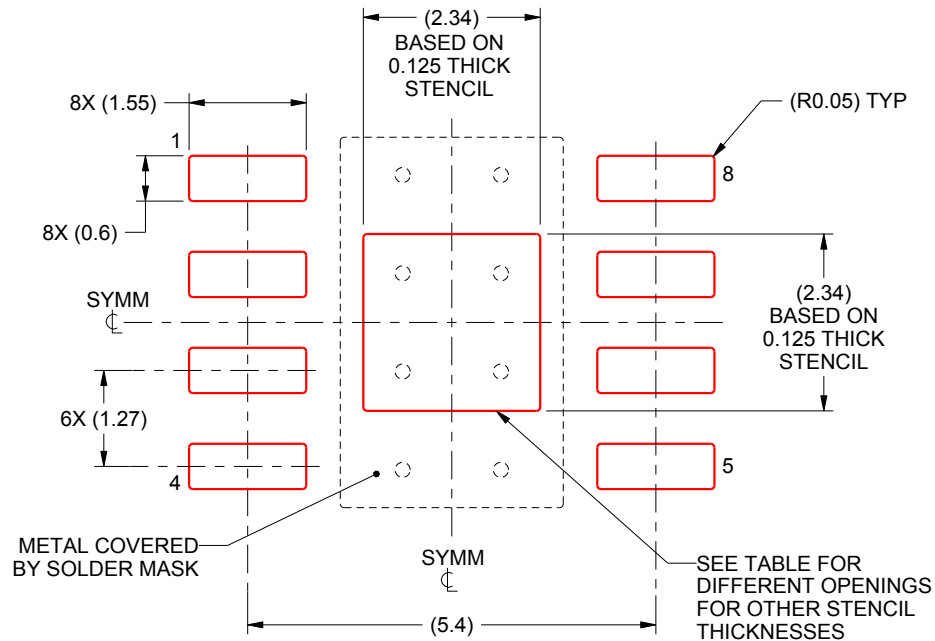
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 2.62 X 2.62            |
| 0.125             | 2.34 X 2.34 (SHOWN)    |
| 0.150             | 2.14 X 2.14            |
| 0.175             | 1.98 X 1.98            |

4218825/A 05/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated