

## LP2997 DDR-II Termination Regulator

Check for Samples: [LP2997](#)

### FEATURES

- Source and Sink Current
- Low Output Voltage Offset
- No External Resistors Required
- Linear Topology
- Suspend to Ram (STR) Functionality
- Low External Component Count
- Thermal Shutdown
- Available in SOIC-8, SO PowerPAD-8 Packages

### APPLICATIONS

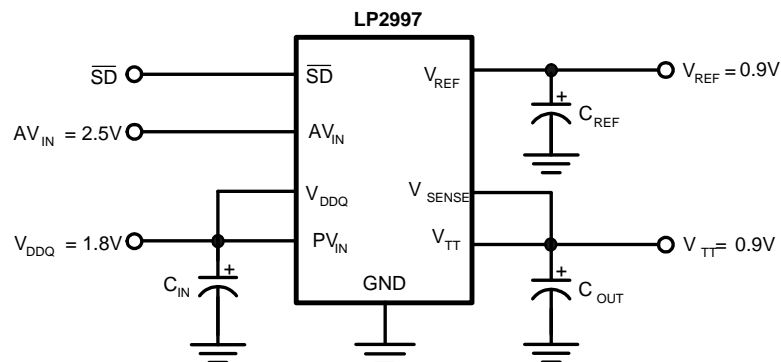
- DDR-II Termination Voltage
- SSTL-18 Termination

### DESCRIPTION

The LP2997 linear regulator is designed to meet the JEDEC SSTL-18 specifications for termination of DDR-II memory. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 500mA continuous current and transient peaks up to 900mA in the application as required for DDR-II SDRAM termination. The LP2997 also incorporates a  $V_{SENSE}$  pin to provide superior load regulation and a  $V_{REF}$  output as a reference for the chipset and DIMMs.

An additional feature found on the LP2997 is an active low shutdown ( $\overline{SD}$ ) pin that provides Suspend To RAM (STR) functionality. When  $\overline{SD}$  is pulled low the  $V_{TT}$  output will tri-state providing a high impedance output, but,  $V_{REF}$  will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

### Typical Application Circuit



**Figure 1. Typical Application Circuit**



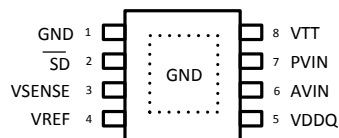
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

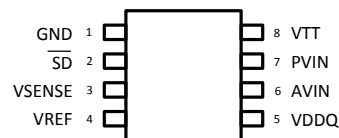
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

## Connection Diagram



**Figure 2. SO PowerPAD-8 Layout**  
See Package Number DDA (R-PDSO-G8)



**Figure 3. SOIC-8 Layout**  
See Package Number D0008A

## PIN DESCRIPTIONS

SOIC-8 Pin or SO PowerPAD-8 Pin	Name	Function
1	GND	Ground
2	$\overline{\text{SD}}$	Shutdown
3	VSENSE	Feedback pin for regulating $V_{\text{TT}}$ .
4	VREF	Buffered internal reference voltage of $V_{\text{DDQ}}/2$
5	VDDQ	Input for internal reference equal to $V_{\text{DDQ}}/2$
6	AVIN	Analog input pin
7	PVIN	Power input pin
8	VTT	Output voltage for connection to termination resistors
	EP	Exposed pad thermal connection Connect to Ground



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

AVIN to GND	–0.3V to +6V
PVIN to GND	–0.3V to AVIN
VDDQ <sup>(3)</sup>	–0.3V to +6V
Storage Temp. Range	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
SOIC-8 Thermal Resistance ( $\theta_{\text{JA}}$ )	151°C/W
SO PowerPAD-8 Thermal Resistance ( $\theta_{\text{JA}}$ )	43°C/W
Minimum ESD Rating <sup>(4)</sup>	1kV

- (1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specific specifications and test conditions see Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) VDDQ voltage must be less than  $2 \times (\text{AVIN} - 1)$  or 6V, whichever is smaller.
- (4) The human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin.

## Operating Range

Junction Temp. Range <sup>(1)</sup>	0°C to +125°C
AVIN to GND	2.2V to 5.5V

- (1) At elevated temperatures, devices must be derated based on thermal resistance. The device in the SOIC-8 package must be derated at  $\theta_{\text{JA}} = 151.2^\circ \text{C/W}$  junction to ambient with no heat sink.

## Electrical Characteristics

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$  and limits in **boldface type** apply over the full **Operating Temperature Range** ( $T_J = 0^\circ\text{C}$  to  $+125^\circ\text{C}$ )<sup>(1)</sup>. Unless otherwise specified,  $AVIN = 2.5\text{V}$ ,  $PVIN = 1.8\text{V}$ ,  $VDDQ = 1.8\text{V}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{REF}$	$V_{REF}$ Voltage	$PVIN = VDDQ = 1.7\text{V}$ $PVIN = VDDQ = 1.8\text{V}$ $PVIN = VDDQ = 1.9\text{V}$	<b>0.837</b> <b>0.887</b> <b>0.936</b>	0.860 0.910 0.959	<b>0.887</b> <b>0.937</b> <b>0.986</b>	V
$Z_{VREF}$	$V_{REF}$ Output Impedance	$I_{REF} = -30$ to $+30\ \mu\text{A}$		2.5		k $\Omega$
$V_{TT}$	$V_{TT}$ Output Voltage	$I_{OUT} = 0\text{A}$ $PVIN = VDDQ = 1.7\text{V}$ $PVIN = VDDQ = 1.8\text{V}$ $PVIN = VDDQ = 1.9\text{V}$	<b>0.822</b> <b>0.874</b> <b>0.923</b>	0.856 0.908 0.957	<b>0.887</b> <b>0.939</b> <b>0.988</b>	V
		$I_{OUT} = \pm 0.5\text{A}$ <sup>(2)</sup> $PVIN = VDDQ = 1.7\text{V}$ $PVIN = VDDQ = 1.8\text{V}$ $PVIN = VDDQ = 1.9\text{V}$	<b>0.828</b> <b>0.878</b> <b>0.928</b>	0.856 0.908 0.957	<b>0.890</b> <b>0.940</b> <b>0.990</b>	
$V_{OS_{TT}/V_{TT}}$	$V_{TT}$ Output Voltage Offset ( $V_{REF} - V_{TT}$ )	$I_{OUT} = 0\text{A}$ $I_{OUT} = -0.5\text{A}$ $I_{OUT} = +0.5\text{A}$	<b>-25</b> <b>-25</b> <b>-25</b>	0 0 0	<b>25</b> <b>25</b> <b>25</b>	mV
$I_Q$	Quiescent Current <sup>(3)</sup>	$I_{OUT} = 0\text{A}$ <sup>(3)</sup>		320	<b>500</b>	$\mu\text{A}$
$Z_{VDDQ}$	$VDDQ$ Input Impedance			100		k $\Omega$
$I_{SD}$	Quiescent Current in Shutdown <sup>(3)</sup>	$SD = 0\text{V}$		115	<b>150</b>	$\mu\text{A}$
$I_{Q\_SD}$	Shutdown Leakage Current	$SD = 0\text{V}$		2	<b>5</b>	$\mu\text{A}$
$V_{IH}$	Minimum Shutdown High Level		<b>1.9</b>			V
$V_{IL}$	Maximum Shutdown Low Level				<b>0.8</b>	V
$I_{SENSE}$	$V_{SENSE}$ Input Current			13		nA
$T_{SD}$	Thermal Shutdown	See <sup>(4)</sup>		165		Celsius
$T_{SD\_HYS}$	Thermal Shutdown Hysteresis			10		Celsius

(1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).

(2)  $V_{TT}$  load regulation is tested by using a 10 ms current pulse and measuring  $V_{TT}$ .

(3) Quiescent current defined as the current flow into  $AVIN$ .

(4) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{J(MAX)}$ , the junction to ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

## Typical Performance Characteristics

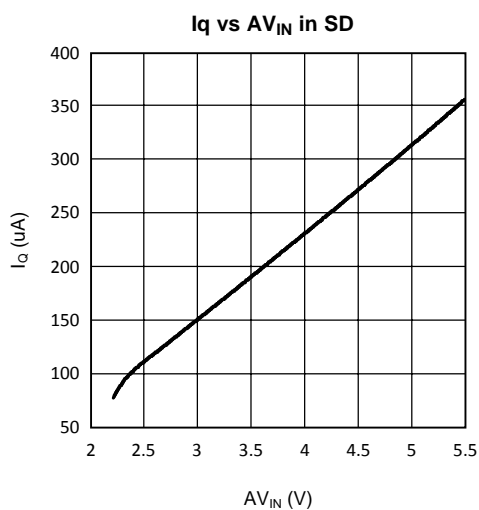


Figure 4.

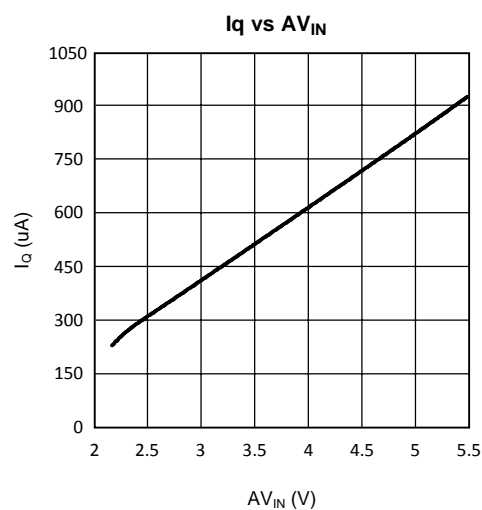


Figure 5.

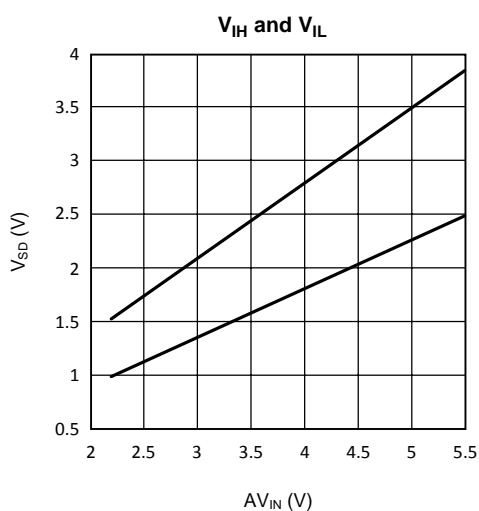


Figure 6.

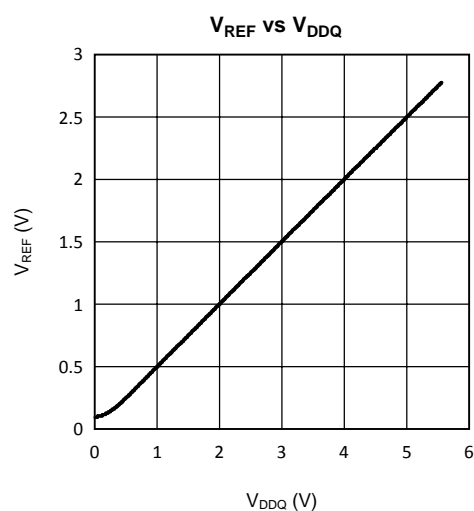


Figure 7.

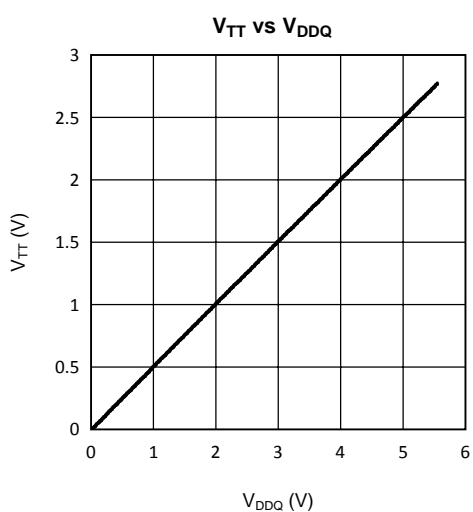


Figure 8.

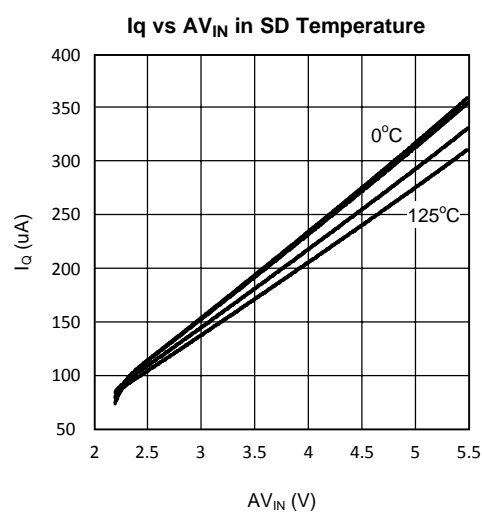


Figure 9.

## Typical Performance Characteristics (continued)

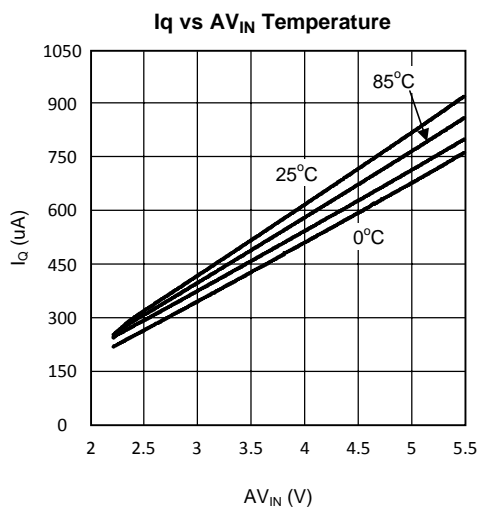


Figure 10.

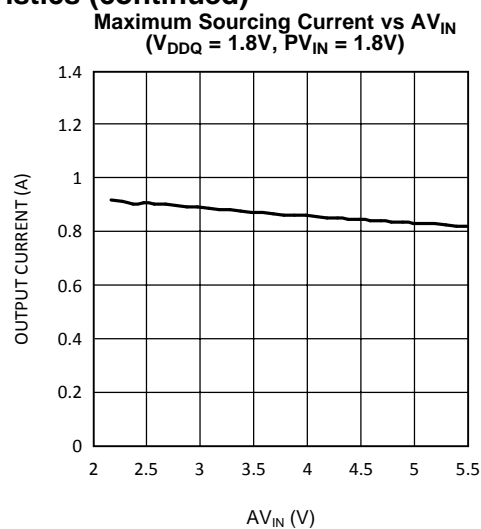


Figure 11.

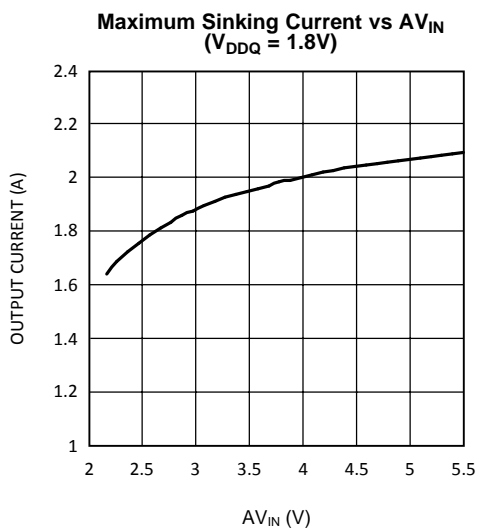
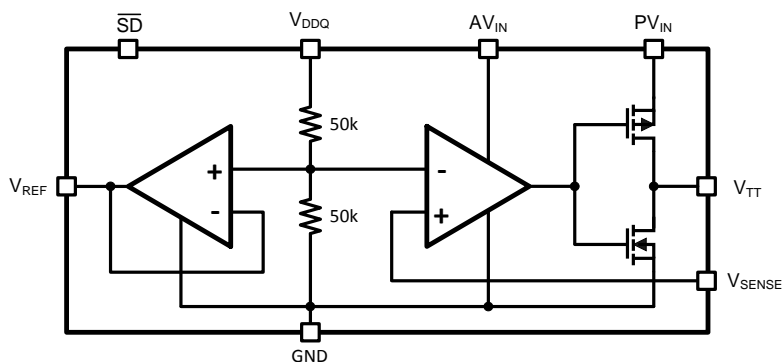


Figure 12.

## Block Diagram



## DESCRIPTION

The LP2997 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-18. The output,  $V_{TT}$  is capable of sinking and sourcing current while regulating the output voltage equal to  $V_{DDQ} / 2$ . The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2997 also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2997 to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII).

## Pin Descriptions

**AVIN AND PVIN** AVIN and PVIN are the input supply pins for the LP2997. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create  $V_{TT}$ . These pins have the capability to work off separate supplies, under the condition that AVIN is always greater than or equal to PVIN. For SSTL-18 applications, it is recommended to connect PVIN to the 1.8V rail used for the memory core and AVIN to a rail within its operating range of 2.2V to 5.5V (typically a 2.5V supply). PVIN should always be used with either a 1.8V or 2.5V rail. This prevents the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown then the part will enter a shutdown state identical to the manual shutdown where  $V_{TT}$  is tri-stated and  $V_{REF}$  remains active. A lower rail such as 1.5V can be used but it will reduce the maximum output current, therefore it is not recommended for most termination schemes.

**VDDQ** VDDQ is the input used to create the internal reference voltage for regulating  $V_{TT}$ . The reference voltage is generated from a resistor divider of two internal 50k $\Omega$  resistors. This ensures that  $V_{TT}$  will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 1.8V rail at the DIMM instead of PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-18 applications VDDQ will be a 1.8V signal, which will create a 0.9V termination voltage at  $V_{TT}$  (See Electrical Characteristics Table for exact values of  $V_{TT}$  over temperature).

**VSENSE** The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to  $V_{TT}$  in a long plane. If the output voltage was regulated only at the output of the LP2997 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The  $V_{SENSE}$  pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the  $V_{SENSE}$  pin must still be connected to  $V_{TT}$ . Care should be taken when a long  $V_{SENSE}$  trace is implemented in close proximity to the memory. Noise pickup in the  $V_{SENSE}$  trace can cause problems with precise regulation of  $V_{TT}$ . A small 0.1 $\mu$ F ceramic capacitor placed next to the  $V_{SENSE}$  pin can help filter any high frequency signals and preventing errors.

**SHUTDOWN** The LP2997 contains an active low shutdown pin that can be used for suspend to RAM functionality. In this condition the  $V_{TT}$  output will tri-state while the  $V_{REF}$  output remains active providing a constant reference signal for the memory and chipset. During shutdown  $V_{TT}$  should not be exposed to voltages that exceed PVIN. With the shutdown pin asserted low the quiescent current of the LP2997 will drop, however, VDDQ will always maintain its constant impedance of 100k $\Omega$  for generating the internal reference. Therefore, to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section. The shutdown pin also has an internal pull-up current; therefore, to turn the part on the shutdown pin can either be connected to AVIN or left open

**VREF**  $V_{REF}$  provides the buffered output of the internal reference voltage  $V_{DDQ} / 2$ . This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from  $V_{REF}$ . For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1  $\mu$ F to 0.01  $\mu$ F is recommended. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

**VTT**  $V_{TT}$  is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to  $V_{DDQ} / 2$ . The LP2997 is designed to handle continuous currents of up to  $\pm 0.5$ A with excellent load regulation. If a transient is expected to last above the maximum continuous current rating for a significant amount of time, then the bulk output capacitor should be sized large enough to prevent an excessive voltage drop. If the LP2997 is to operate in elevated temperatures for long durations care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal de-rating should always be used. (Please refer to the Thermal Dissipation section) If the junction temperature exceeds the thermal shutdown point then  $V_{TT}$  will tri-state until the part returns below the temperature hysteresis trip-point

## COMPONENT SELECTIONS

### INPUT CAPACITOR

The LP2997 does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 22  $\mu$ F. Ceramic capacitors can also be used. A value in the range of 10  $\mu$ F with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2997 is placed close to the bulk capacitance from the output of the 1.8V DC-DC converter. For the AVIN pin, a small 0.1 $\mu$ F ceramic capacitor is sufficient to prevent excessive noise from coupling into the device.

## OUTPUT CAPACITOR

The LP2997 has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of  $V_{TT}$ . As a general recommendation the output capacitor should be sized above 100  $\mu\text{F}$  with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

**AL** - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (100 kHz) should be used for the LP2997. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

**Ceramic** - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100  $\mu\text{F}$  range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 m $\Omega$ ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

**Hybrid** - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitors.

## Thermal Dissipation

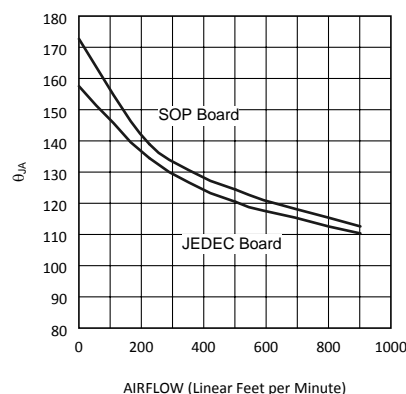
Since the LP2997 is a linear regulator any current flow from  $V_{TT}$  will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise ( $T_{Rmax}$ ) can be calculated given the maximum ambient temperature ( $T_{Amax}$ ) of the application and the maximum allowable junction temperature ( $T_{Jmax}$ ).

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (1)$$

From this equation, the maximum power dissipation ( $P_{Dmax}$ ) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA} \quad (2)$$

The  $\theta_{JA}$  of the LP2997 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the  $\theta_{JA}$  of the SOIC-8 is 163°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. [Figure 13](#) shows how the  $\theta_{JA}$  varies with airflow for the two boards mentioned.



**Figure 13.  $\theta_{JA}$  vs Airflow (SOIC-8)**

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the  $\theta_{JA}$  further than the nominal values shown in [Figure 13](#).

Optimizing the  $\theta_{JA}$  and placing the LP2997 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at  $V_{TT}$ , either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT} \quad (3)$$

Where,

$$P_{AVIN} = I_{AVIN} \times V_{AVIN} \quad (4)$$

$$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ}^2 \times R_{VDDQ} \quad (5)$$

To calculate the maximum power dissipation at  $V_{TT}$  both conditions at  $V_{TT}$  need to be examined, sinking and sourcing current. Although only one equation will add into the total,  $V_{TT}$  cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \text{ (Sinking) or} \quad (6)$$

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD} \text{ (Sourcing)} \quad (7)$$

The power dissipation of the LP2997 can also be calculated during the shutdown state. During this condition the output  $V_{TT}$  will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ} \quad (8)$$

$$P_{AVIN} = I_{AVIN} \times V_{AVIN} \quad (9)$$

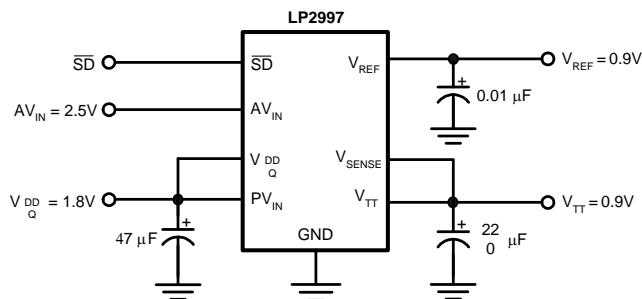
$$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ}^2 \times R_{VDDQ} \quad (10)$$

## Typical Application Circuits

Several different application circuits have been shown to illustrate some of the options that are possible in configuring the LP2997. Graphs of the individual circuit performance can be found in the [Typical Performance Characteristics](#) section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

[Figure 14](#) shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 2.5V, 3.3V or 5V rail.

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where  $V_{TT}$  is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. The bulk output capacitors should be situated at both ends of the  $V_{TT}$  plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.



**Figure 14. Recommended DDR-II Termination**



## PCB Layout Considerations

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2.  $V_{SENSE}$  should be connected to the  $V_{TT}$  termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3.  $V_{DDQ}$  can be connected remotely to the  $V_{DDQ}$  rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the  $V_{SENSE}$  trace to avoid noise pickup from switching I/O signals. A 0.1 $\mu$ F ceramic capacitor located close to the  $V_{SENSE}$  can also be used to filter any unwanted high frequency signal. This can be an issue especially if long  $V_{SENSE}$  traces are used.
6.  $V_{REF}$  should be bypassed with a 0.01  $\mu$ F or 0.1  $\mu$ F ceramic capacitor for improved performance. This capacitor should be located as close as possible to the  $V_{REF}$  pin.

## REVISION HISTORY

### Changes from Revision E (April 2013) to Revision F

### Page

- Changed layout of National Data Sheet to TI format ..... [9](#)

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LP2997M/NOPB</a>	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 125	L2997 M
LP2997M/NOPB.A	Active	Production	SOIC (D)   8	95   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 125	L2997 M
<a href="#">LP2997MR/NOPB</a>	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	NIPDAU   SN	Level-3-260C-168 HR	0 to 125	(L2997, LP2997) MR
LP2997MR/NOPB.A	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 125	(L2997, LP2997) MR
<a href="#">LP2997MRX/NOPB</a>	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU   SN	Level-3-260C-168 HR	0 to 125	(L2997, LP2997) MR
LP2997MRX/NOPB.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 125	(L2997, LP2997) MR
LP2997MRX/NOPBG4	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 125	LP2997 MR
LP2997MRX/NOPBG4.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 125	LP2997 MR
<a href="#">LP2997MX/NOPB</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	L2997 M
LP2997MX/NOPB.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 125	L2997 M

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2997MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LP2997MRX/NOPBG4	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LP2997MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

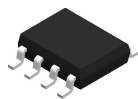
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2997MRX/NOPB	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
LP2997MRX/NOPBG4	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
LP2997MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

## TUBE



\*All dimensions are nominal

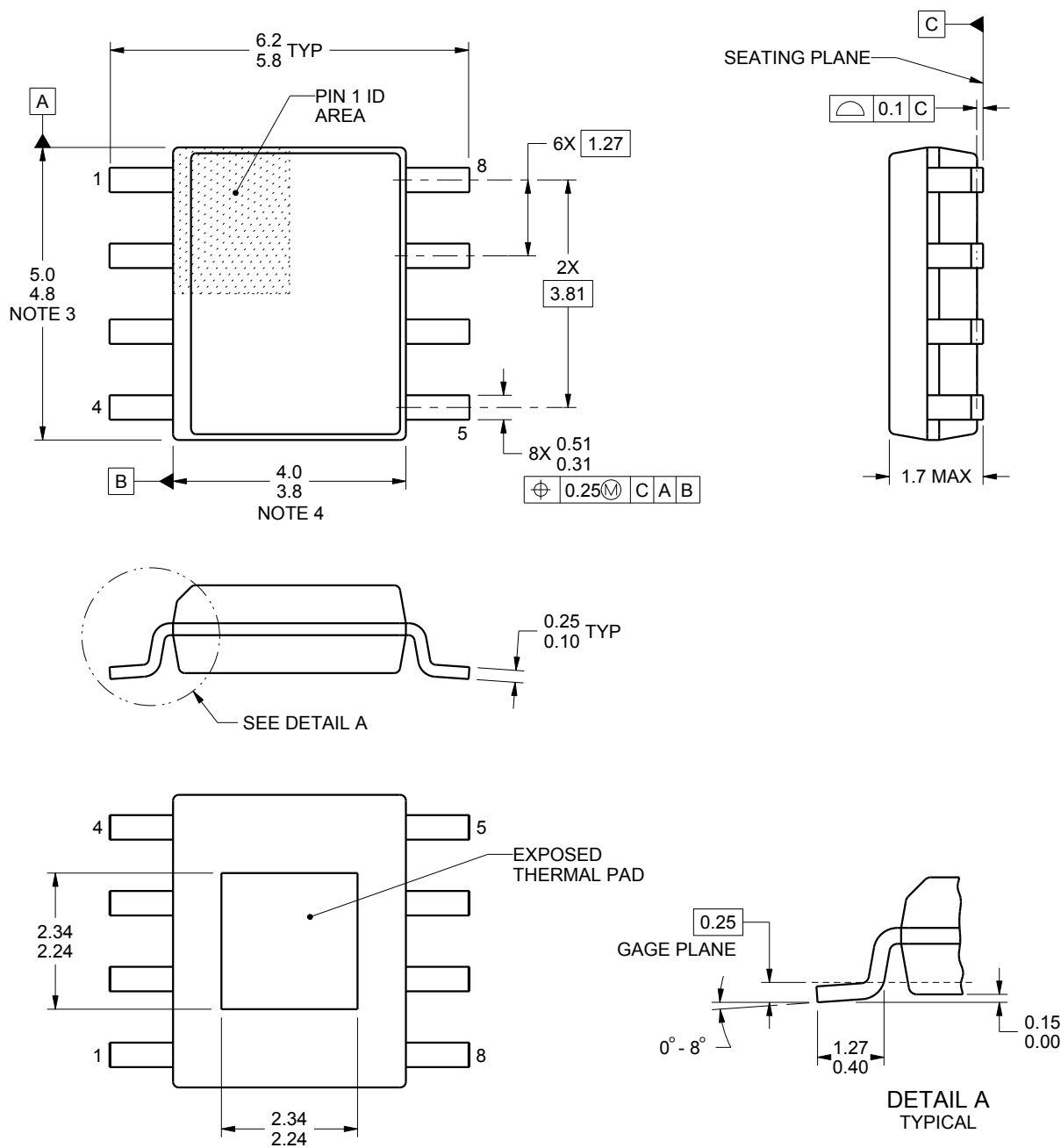
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LP2997M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2997M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LP2997MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP2997MR/NOPB	DDA	HSOIC	8	95	507.79	8	630	4.32
LP2997MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP2997MR/NOPB.A	DDA	HSOIC	8	95	507.79	8	630	4.32
LP2997MR/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05
LP2997MR/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05

**DDA0008A**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4218825/A 05/2016

PowerPAD is a trademark of Texas Instruments.

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

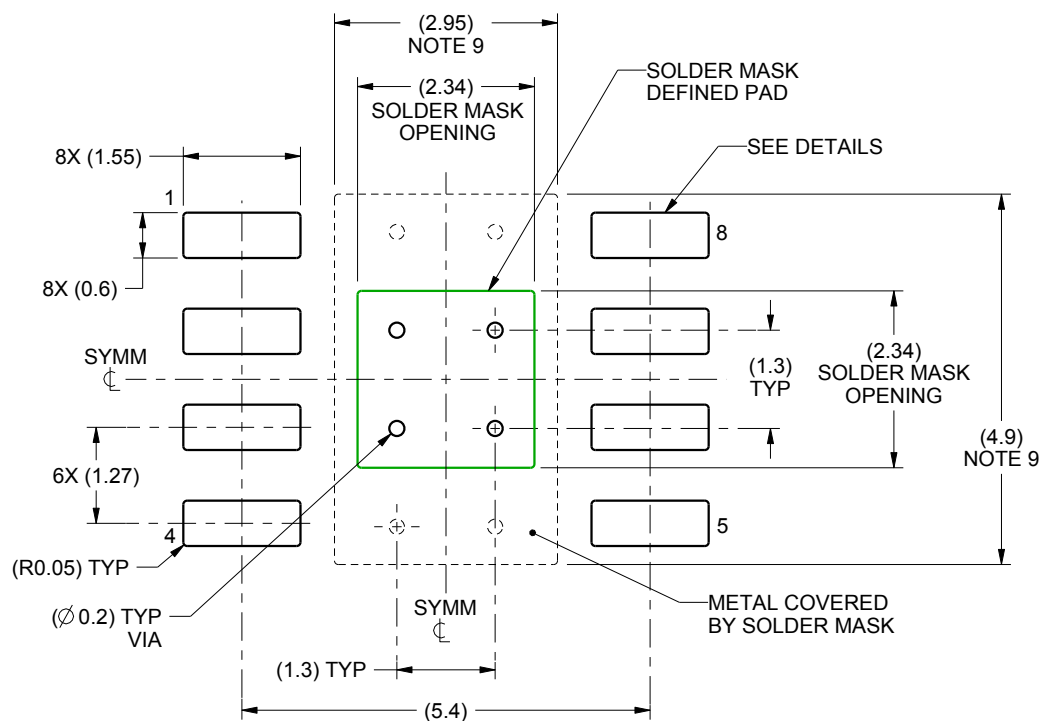


# EXAMPLE BOARD LAYOUT

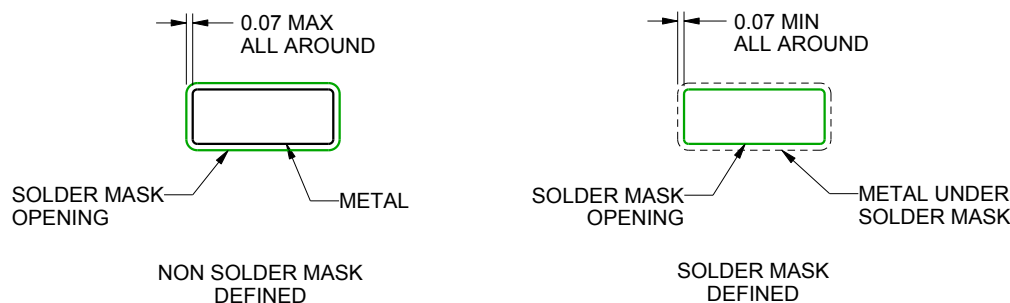
DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

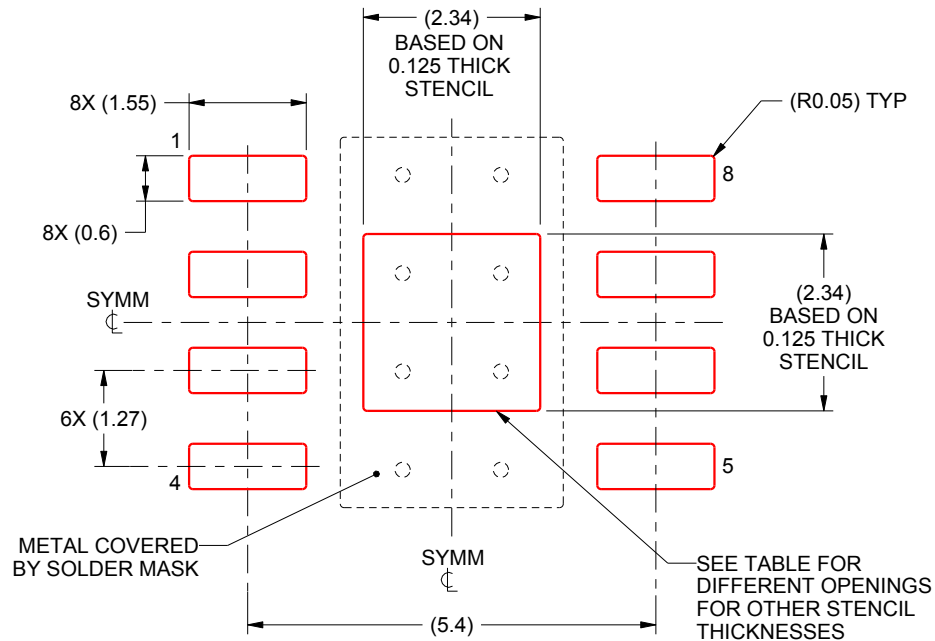
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



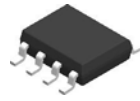
**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

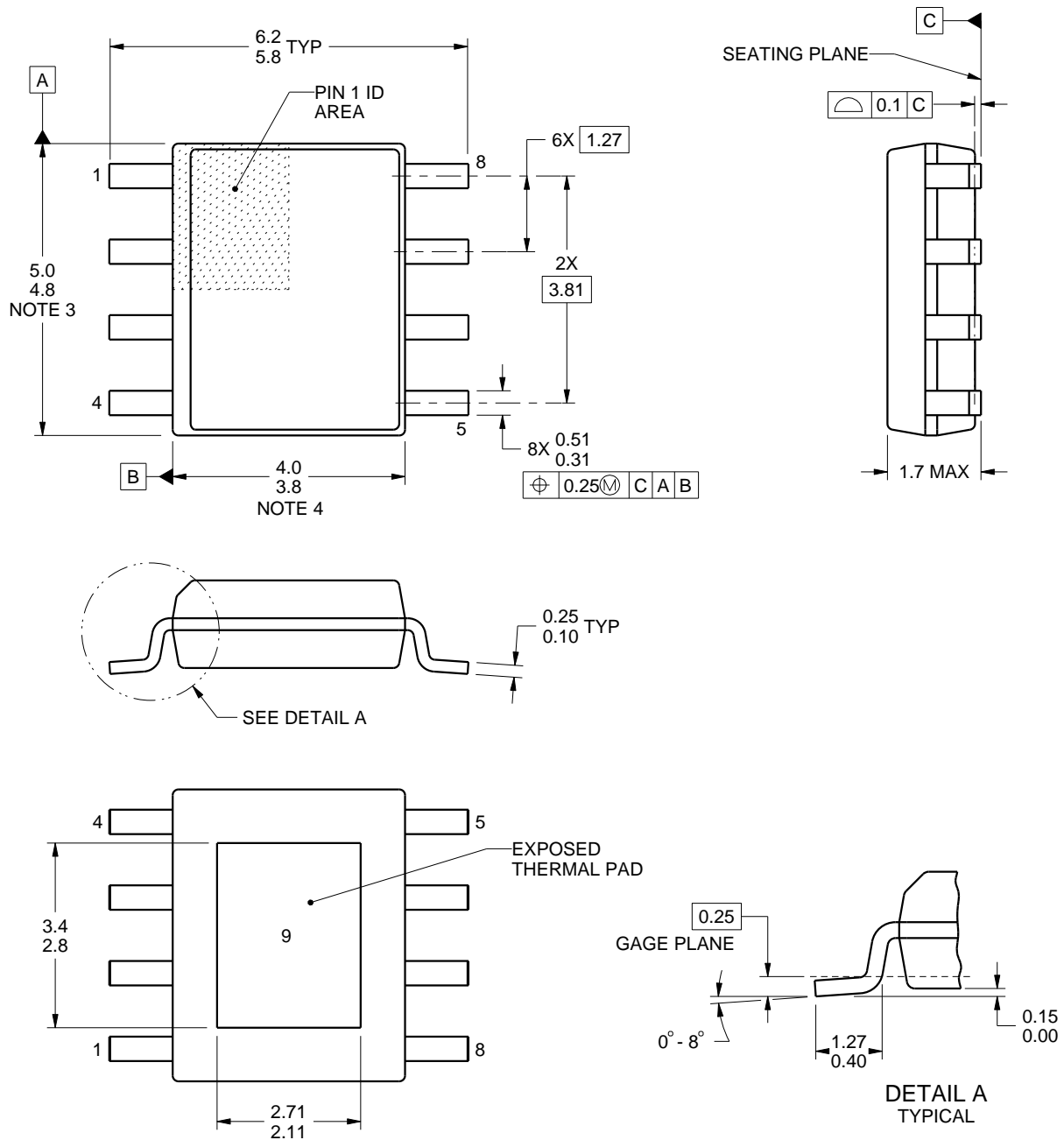
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**DDA0008B**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

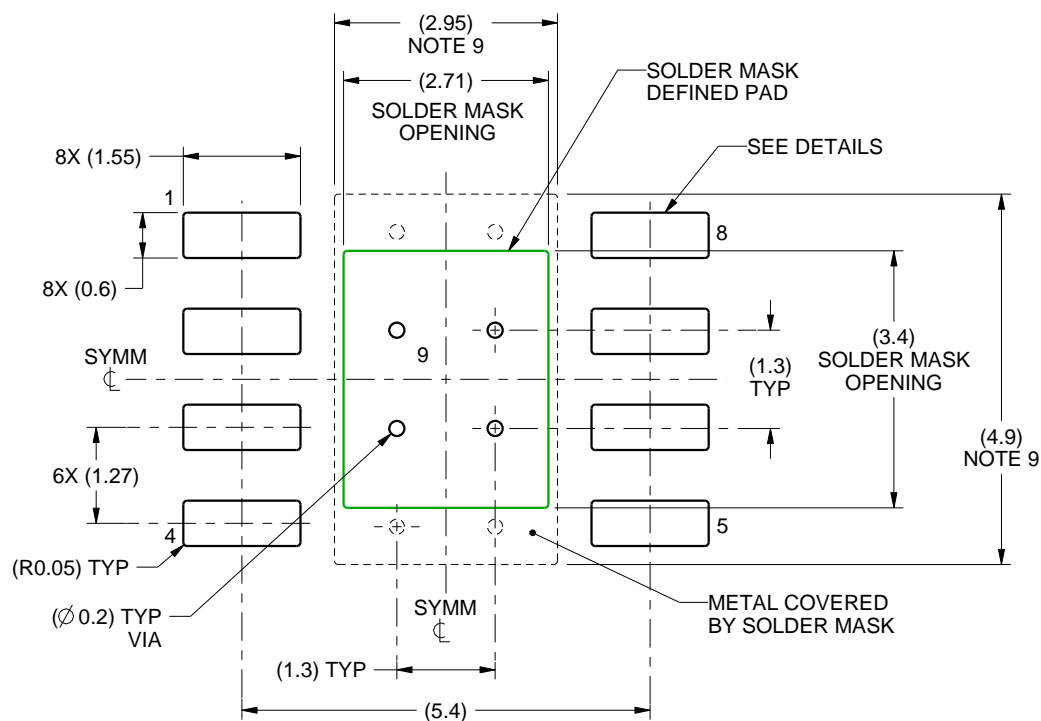
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

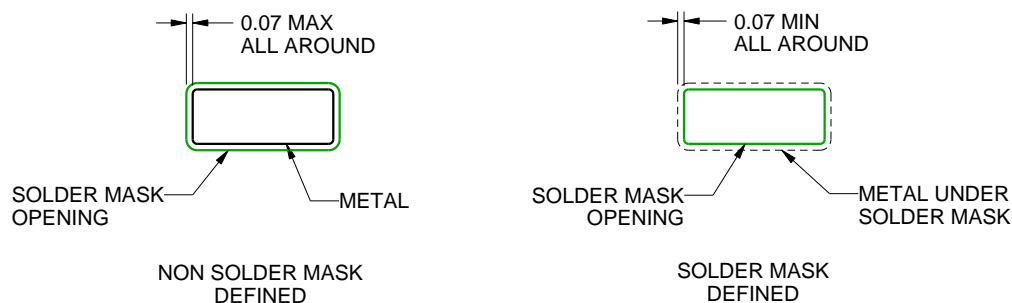
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

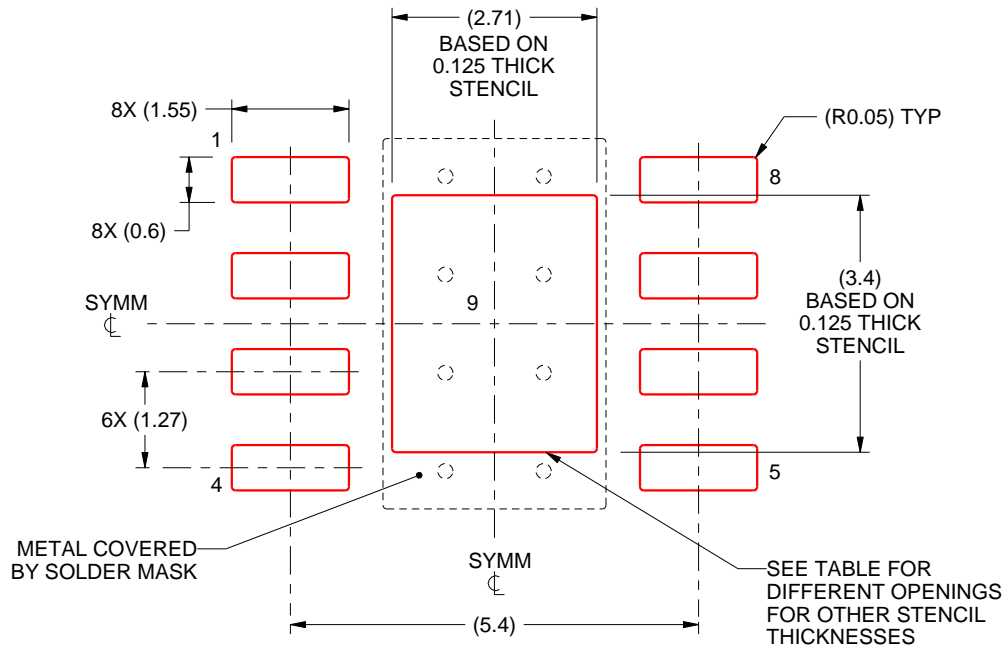
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

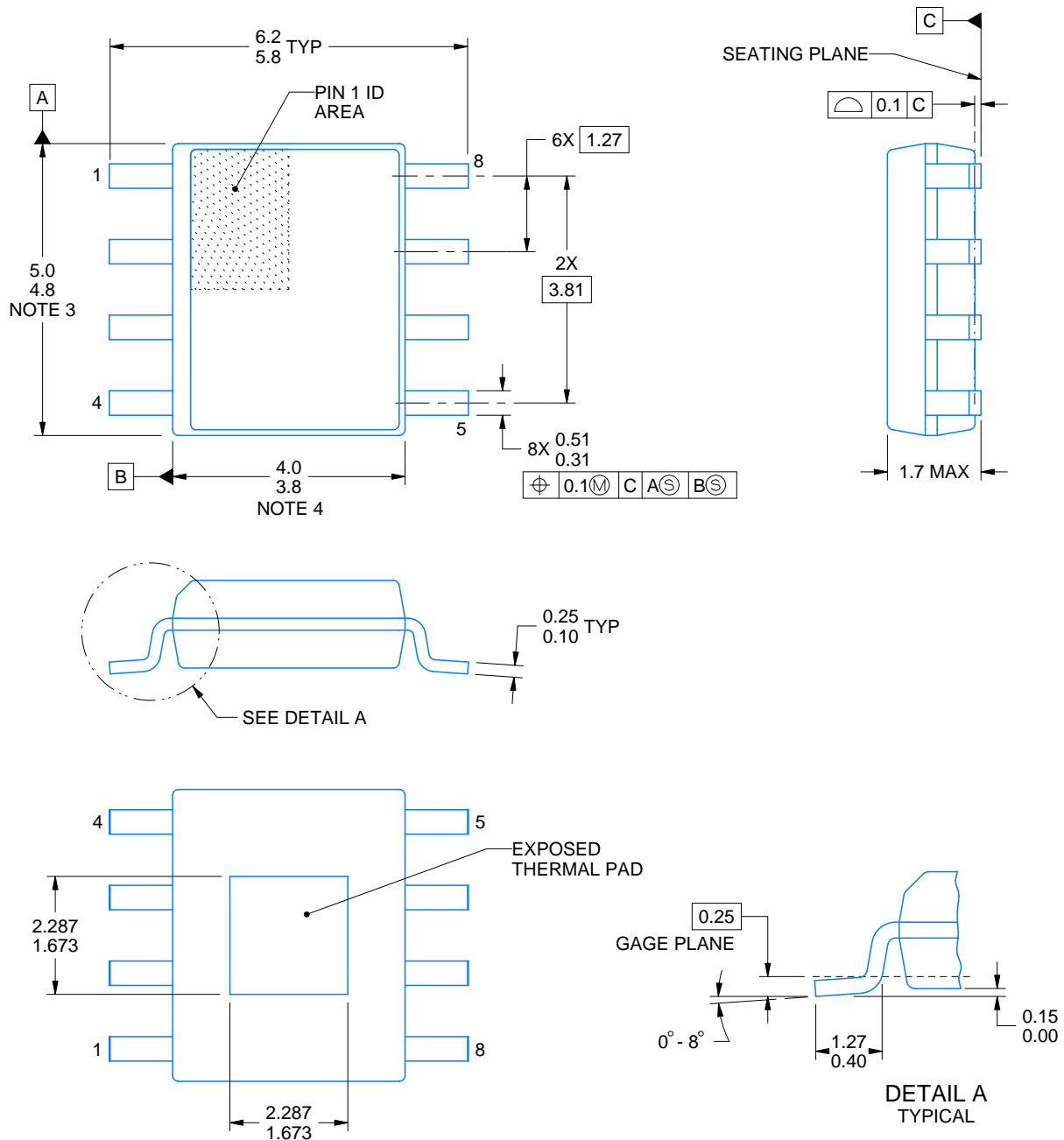
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**DDA0008D**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4218820/A 12/2022

PowerPAD is a trademark of Texas Instruments.

**NOTES:**

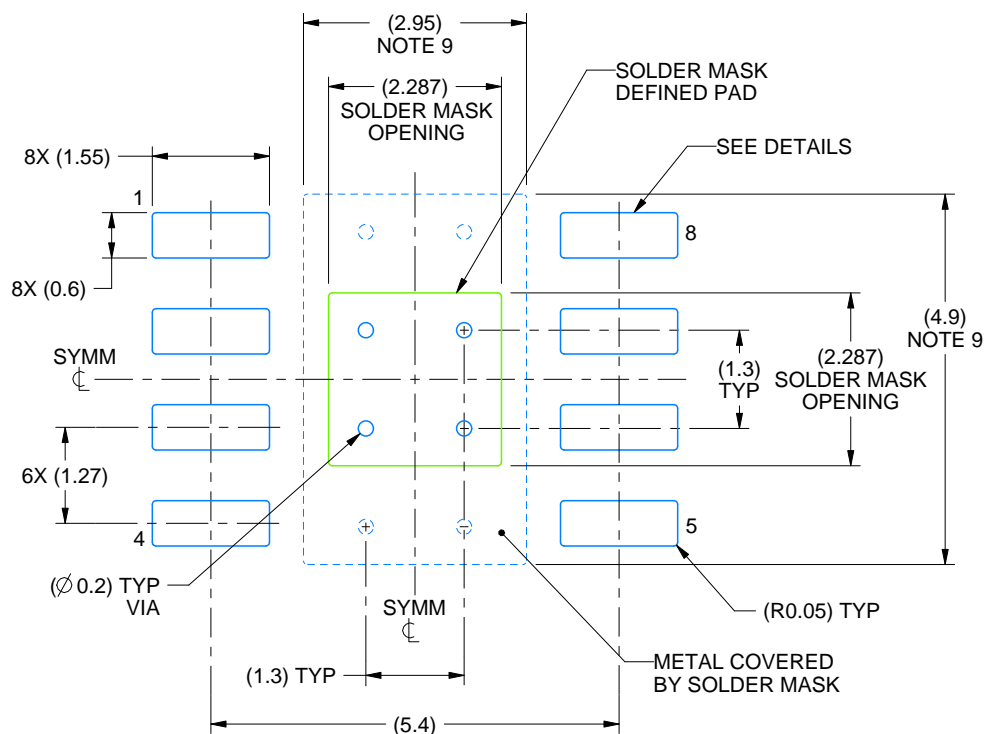
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

# EXAMPLE BOARD LAYOUT

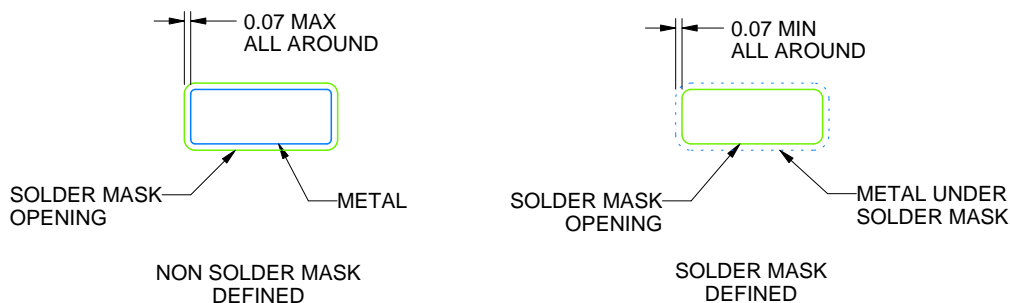
DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS

4218820/A 12/2022

NOTES: (continued)

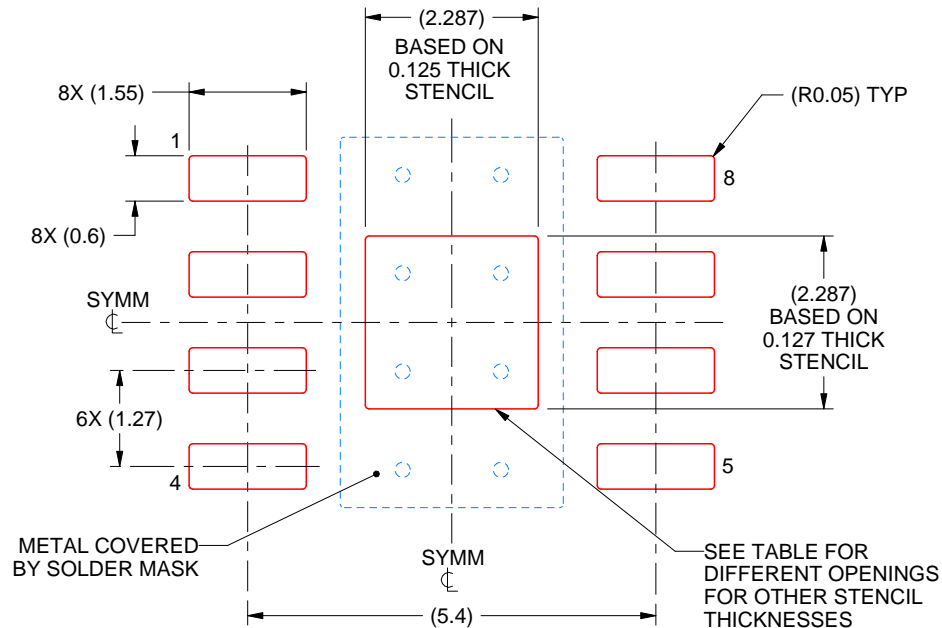
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

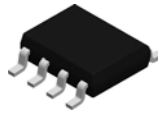
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

4218820/A 12/2022

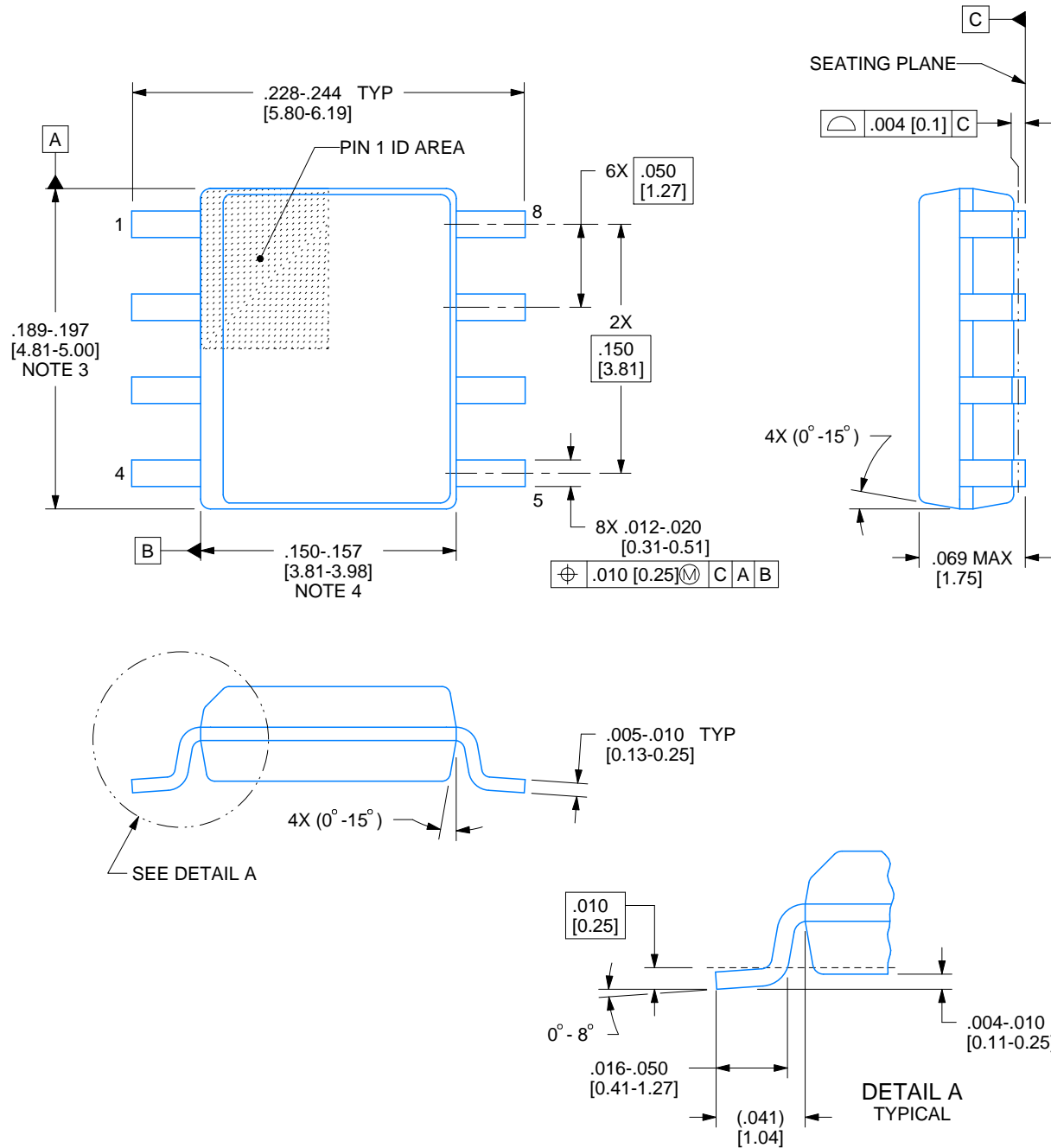
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



**D0008A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

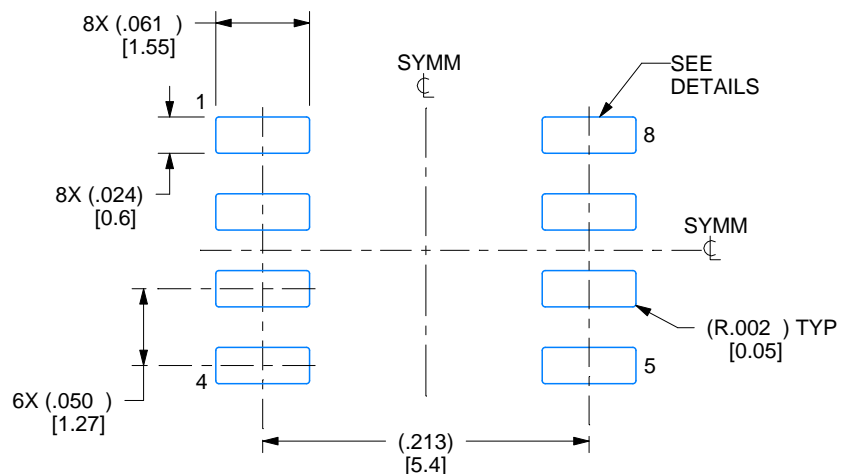
**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

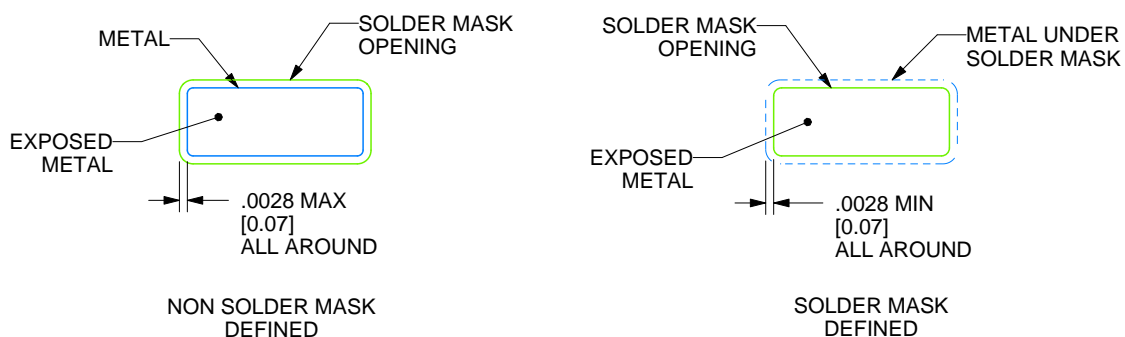
**D0008A**

## SOIC - 1.75 mm max height

## SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

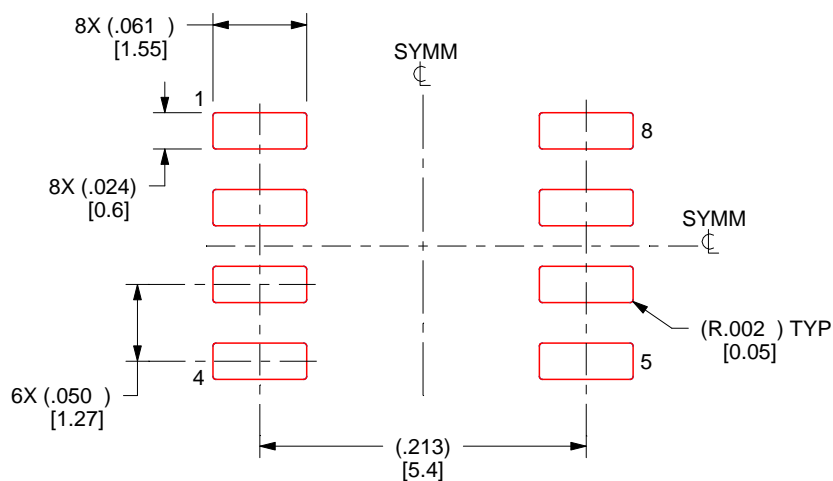
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated