TEXAS INSTRUMENTS

LP358, LP2904

SLOS475A – AUGUST 2005 – REVISED MAY 2017

Ultra-Low Power Dual Operational Amplifiers

1 Features

- Low Supply Current: 54 μA (Typical)
- Low Offset Voltage: 2 mV (Typical)
- Low Input Bias Current: 2 nA (Typical)
- Input Common-Mode to GND
- Wide Supply Voltage: 3 V < V_{CC} < 32 V
- Pin Compatible With LM358 and LM2904

2 Applications

- LCD Displays
- Portable Instrumentation
- Sensor and Metering Equipment
- Consumer Electronics (MP3 Players, Toys)
- Power Supplies

3 Description

The LP358 and LP2904 devices are dual low-power operational amplifiers especially suited for battery-operated applications. Good input specifications and wide supply-voltage range still are achieved despite the ultra-low supply current. Single-supply operation is achieved with an input common-mode range that includes GND.
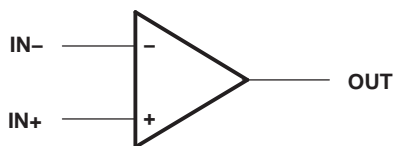
The LP358 and LP2904 devices are ideal in applications where wide supply voltages and low power are more important than speed and bandwidth. These applications include portable instrumentation, LCD displays, consumer electronics (MP3 players, toys, and so forth), and power supplies.
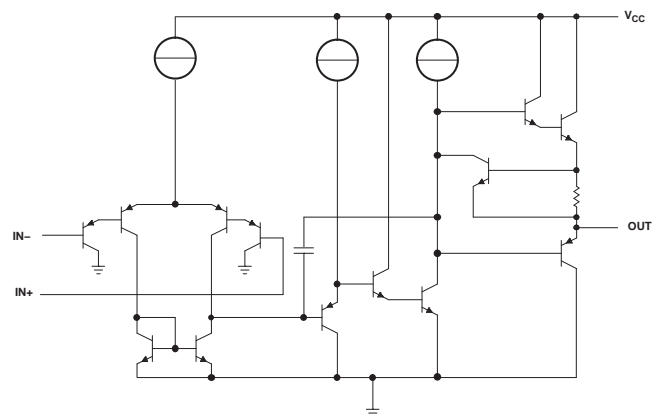
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2904	SOIC (8)	4.90 × 3.91
LP358		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Amplifier)

Schematic (Each Amplifier)

Table of Contents

4 Revision History

5 Pin Configuration and Functions

D, DGK Package
8-Pin SOIC
Top View

```
          ┌───────────────┐
          │   ○           │
1OUT ─────┤ 1          8  ├───── VCC
1IN─ ─────┤ 2          7  ├───── 2OUT
1IN+ ─────┤ 3          6  ├───── 2IN─
GND  ─────┤ 4          5  ├───── 2IN+
          └───────────────┘
```

Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	4	—	Ground or negative power supply
1IN+	3	I	Channel 1 noninverting input
1IN–	2	I	Channel 1 inverting input
1OUT	1	O	Channel 1 output
2IN+	5	I	Channel 2 noninverting input
2IN–	6	I	Channel 2 inverting input
2OUT	7	O	Channel 2 output
V_{CC}	8	—	Positive power supply

Product Folder Links: *LP358 LP2904*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		±16 or 32	V
V_{ID}	Differential input voltage[3]		±32	V
V_I	Input voltage (either input)	−0.3	32	V
	Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, V_{CC} ≤ 15 V[4]	Unlimited		
	Operating virtual temperature, T_J		150	°C
	Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+, with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	32	V
V_{CM}	Common-mode voltage		0	V_{CC} − 1.5 V	V
T_A	Operating free-air temperature	LP358	0	70	°C
		LP2904	−40	85	

6.4 Thermal Information

	THERMAL METRIC[1]	LP358 D, DGK (SOIC) 8 PINS	LP2904 D, DGK (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2][3]	118.8	118.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.7	71.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	68.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.3	23.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.7	67.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} − T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics: LP358

T_A = 25°C, V_{CC} = 5 V, V_{IC} = V_{CC} / 2, R_L = 100 kΩ to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1] [2]		MIN	TYP [3]	MAX	UNIT
V_{IO}	Input offset voltage	T_A = 25°C			2	4	mV
		T_A = Full range				9	
I_{IB}	Input bias current	T_A = 25°C			2	10	nA
		T_A = Full range				20	
I_{IO}	Input offset current	T_A = 25°C			0.2	2	nA
		T_A = Full range				4	
A_V	Large-signal voltage gain	R_L = 10 kΩ to GND, V_{CC} = 30 V	T_A = 25°C	50	100		V/mV
			T_A = Full range	40			
CMRR	Common-mode rejection ratio	V_{CC} = 30 V, V_{IC} = 0 V to V_{CC} – 1.5 V	T_A = 25°C	80	90		dB
			T_A = Full range	75			
k_{VSR}	Power-supply rejection ratio	V_{CC} = 5 V to 30 V	T_A = 25°C	80	90		V
			T_A = Full range	75			
I_{CC}	Supply current	R_L = ∞	T_A = 25°C		54	75	µA
			T_A = Full range			125	
V_{OH}	Output voltage swing (high)	I_L = 0.35 mA to GND V_{IC} = 0 V	T_A = 25°C	3.4	3.6		V
			T_A = Full range	V_{CC} – 1.9			
V_{OL}	Output voltage swing (low)	I_L = 0.35 mA from V_{CC} V_{IC} = 0 V	T_A = 25°C	0.82	0.7		V
			T_A = Full range	1			
I_O	Output source current	V_O = 3 V, V_{ID} = 1 V	T_A = 25°C	7	10		mA
			T_A = Full range	4			
I_O	Output sink current	V_O = 1.5 V, V_{ID} = –1 V	T_A = 25°C	4	5		mA
			T_A = Full range	3			
		V_O = 1.5 V, V_{ID} = –1 V, V_{IC} = 0 V	T_A = 25°C	2	4		
			T_A = Full range	1			
$I_{OS,GND}$	Output short to GND	V_{ID} = 1 V	T_A = 25°C		20	35	mA
			T_A = Full range			40	
$I_{OS,VCC}$	Output short to V_{CC} [4]	V_{ID} = –1 V	T_A = 25°C		15	30	mA
			T_A = Full range			45	
$αV_{IO}$	Input offset voltage drift		T_A = 25°C		10		µV/°C
$αI_{IO}$	Input offset current drift		T_A = 25°C		10		pA/°C

(1)   For full-range temperature limits: V_{CC} = 3 V to 32 V, V_{ICR} = 0 V to V_{CC} – 1.5 V (unless otherwise noted)
(2)   Full range is 0°C to 70°C for LP358.
(3)   All typical values are at T_A = 25°C.
(4)   Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.6 Electrical Characteristics: LP2904

T_A = 25°C, V_{CC} = 5 V, V_{IC} = V_{CC} / 2, R_L = 100 kΩ to GND (unless otherwise noted)

	PARAMETER	TEST CONDITIONS [1] [2]		MIN	TYP [3]	MAX	UNIT
V_{IO}	Input offset voltage	T_A = 25°C			2	4	mV
		T_A = Full range				10	
I_{IB}	Input bias current	T_A = 25°C			2	20	nA
		T_A = Full range				40	
I_{IO}	Input offset current	T_A = 25°C			0.5	4	nA
		T_A = Full range				8	
A_V	Large-signal voltage gain	R_L = 10 kΩ to GND, V_{CC} = 30 V	T_A = 25°C	40	70		V/mV
			T_A = Full range	30			
CMRR	Common-mode rejection ratio	V_{CC} = 30 V, V_{IC} = 0 V to V_{CC} − 1.5 V	T_A = 25°C	80	90		dB
			T_A = Full range	75			
k_{VSR}	Power-supply rejection ratio	V_{CC} = 5 V to 30 V	T_A = 25°C	80	90		V
			T_A = Full range	75			
I_{CC}	Supply current	R_L = ∞	T_A = 25°C		54	75	µA
			T_A = Full range			138	
V_{OH}	Output voltage swing (high)	I_L = 0.35 mA to GND, V_{IC} = 0 V	T_A = 25°C	3.4	3.6		V
			T_A = Full range	V_{CC} − 1.9			
V_{OL}	Output voltage swing (low)	I_L = 0.35 mA from V_{CC}, V_{IC} = 0 V	T_A = 25°C	0.82	0.7		V
			T_A = Full range	1			
I_O	Output source current	V_O = 3 V, V_{ID} = 1 V	T_A = 25°C	7	10		mA
			T_A = Full range	4			
I_O	Output sink current	V_O = 1.5 V, V_{ID} = −1 V	T_A = 25°C	4	5		mA
			T_A = Full range	3			
		V_O = 1.5 V, V_{ID} = −1 V, V_{IC} = 0 V	T_A = 25°C	2	4		
			T_A = Full range	1			
$I_{OS,GND}$	Output short to GND	V_{ID} = 1 V	T_A = 25°C		20	35	mA
			T_A = Full range			40	
$I_{OS,VCC}$	Output short to V_{CC} [4]	V_{ID} = −1 V	T_A = 25°C		15	30	mA
			T_A = Full range			45	
αV_{IO}	Input offset voltage drift		T_A = 25°C		10		µV/°C
αI_{IO}	Input offset current drift		T_A = 25°C		10		pA/°C

(1) For full-range temperature limits: V_{CC} = 3 V to 32 V, V_{ICR} = 0 V to V_{CC} − 1.5 V (unless otherwise noted)
(2) Full range is −40°C to +85°C for LP2904.
(3) All typical values are at T_A = 25°C.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.7 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
GBW	Gain bandwidth product		100		kHz
SR	Slew rate		50		V/ms

7 Typical Characteristics

See *Recommended Operating Conditions* for device temperature limits.
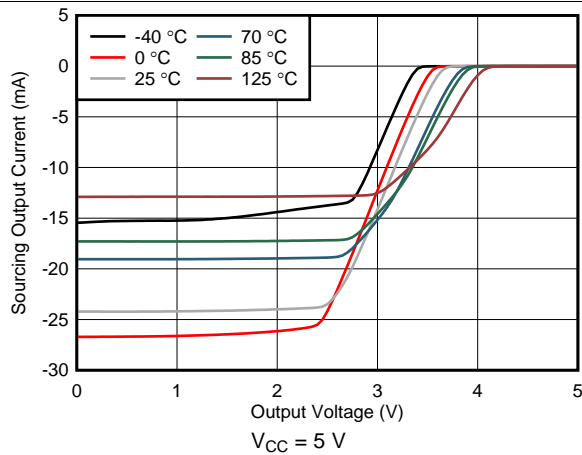
Figure 1. Sourcing Output Current vs Output Voltage
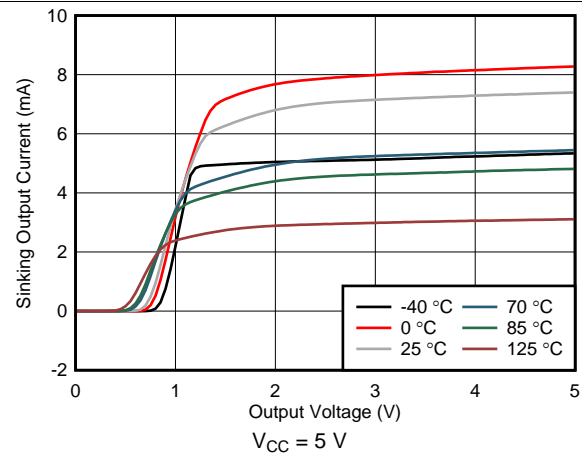
Figure 2. Sinking Output Current vs Output Voltage
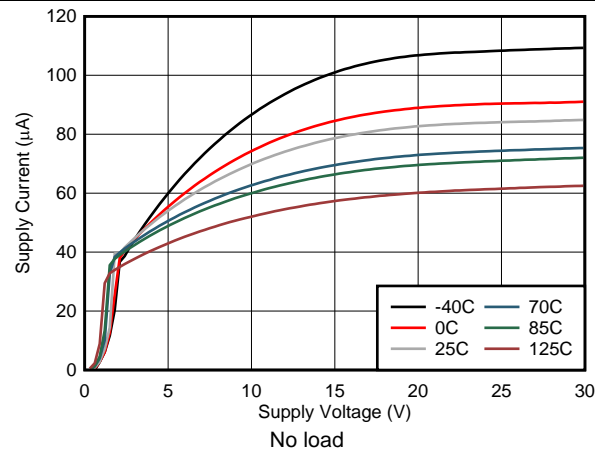
Figure 3. Supply Current vs Supply Voltage

8 Detailed Description

8.1 Overview

The LP358 and LP2904 devices consist of two independent, low-power, unity-gain, stable operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible. The input voltage range includes ground and extends up to $V_{CC} - 1.5$ V. The output cannot drive to either rail, however, loads terminated to ground can support V_{OL} as low as ground. Loads to V_{CC} can support V_{OH} as high as V_{CC}.

8.2 Functional Block Diagram
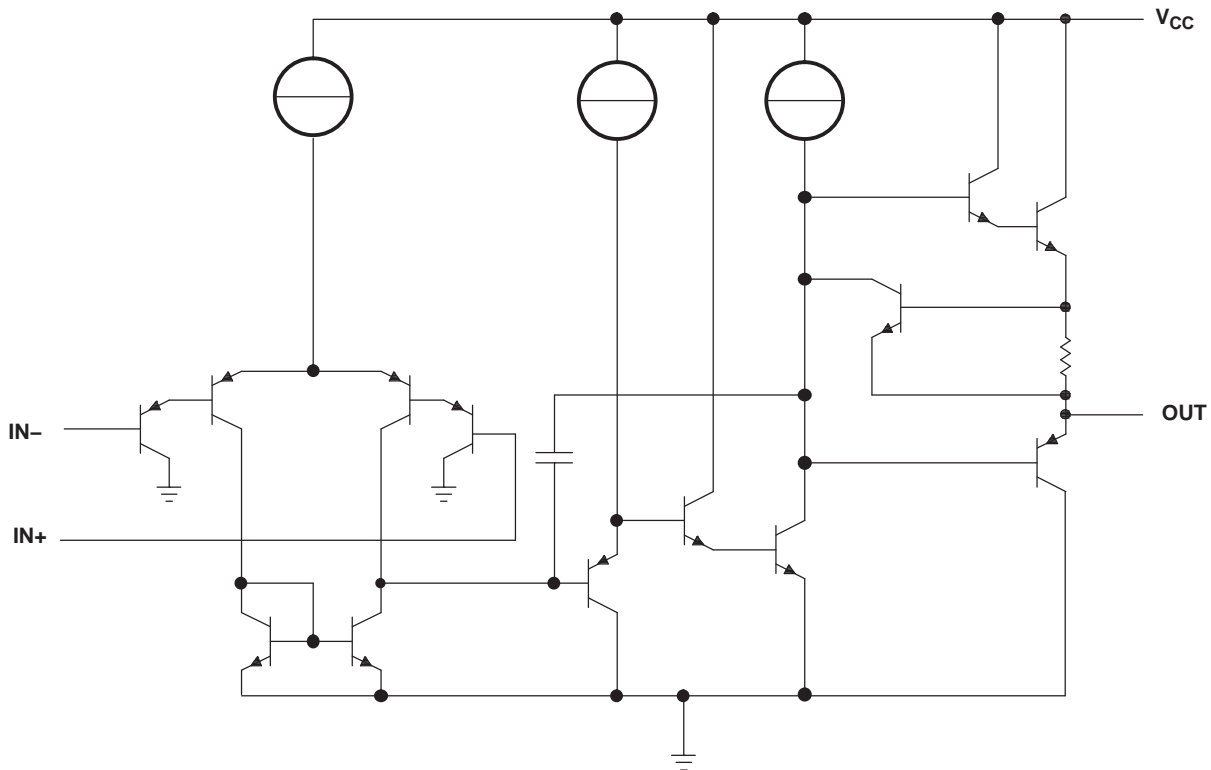
8.3 Feature Description

8.3.1 Power Efficient Output Stage

Darlington source driver and emitter follower sink driver will pass bias current through the load to keep device quiescent current independent of load current.

8.3.2 Input Common-Mode Range

The valid common-mode range is from device ground to $V_{CC} - 1.5$ V. Inputs may exceed V_{CC} up to the maximum V_{CC} without device damage. At least one input must be in the valid input common-mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than –0.3 V then input current must be limited to 1 mA and output phase is undefined.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

> **NOTE**
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP358 and LP2904 operational amplifiers are useful in a wide range of signal conditioning applications due to the wide V_{CC} range. Inputs can be powered before V_{CC} for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier also makes negative voltages positive.
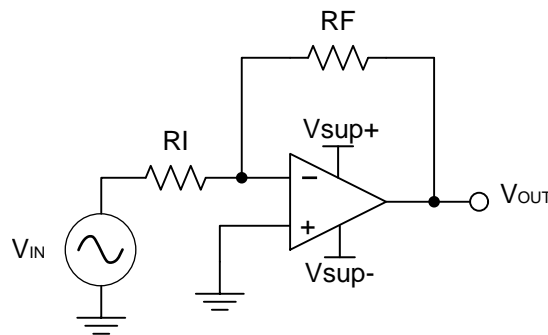
Copyright © 2016, Texas Instruments Incorporated

Figure 4. Application Schematic

9.2.1 Design Requirements

The supply voltage must be selected such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2.

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, select a value for RI or RF. Selecting a value in the kΩ range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. This example uses 10 kΩ for RI, so 36 kΩ is used for RF; this is determined by Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

Typical Application (continued)

9.2.3 Application Curves
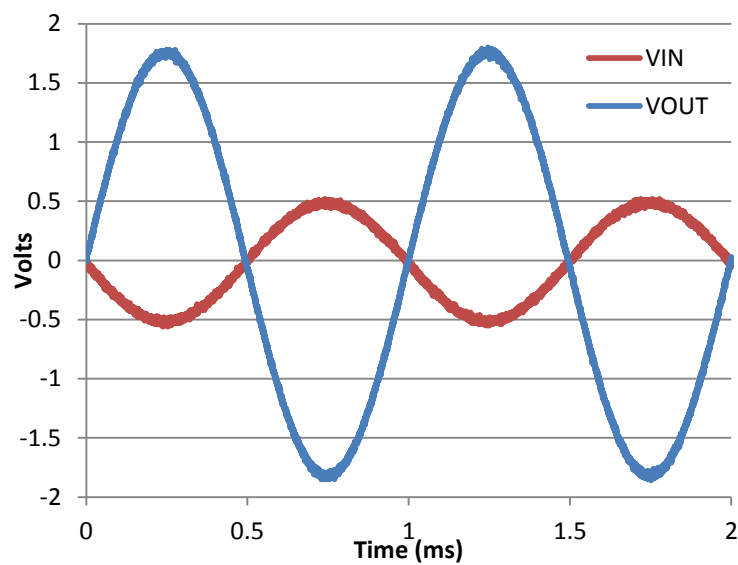
Figure 5. Input and Output Voltages of the Inverting Amplifier

Product Folder Links: *LP358 LP2904*

10   Power Supply Recommendations

> **CAUTION**
>
> Supply voltages larger than 32 V can permanently damage the device (see *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example
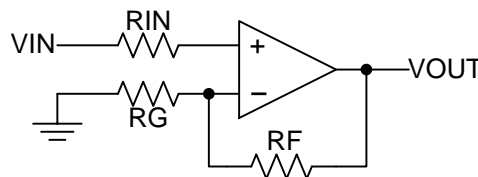
Figure 6. Operational Amplifier Schematic for Noninverting Configuration
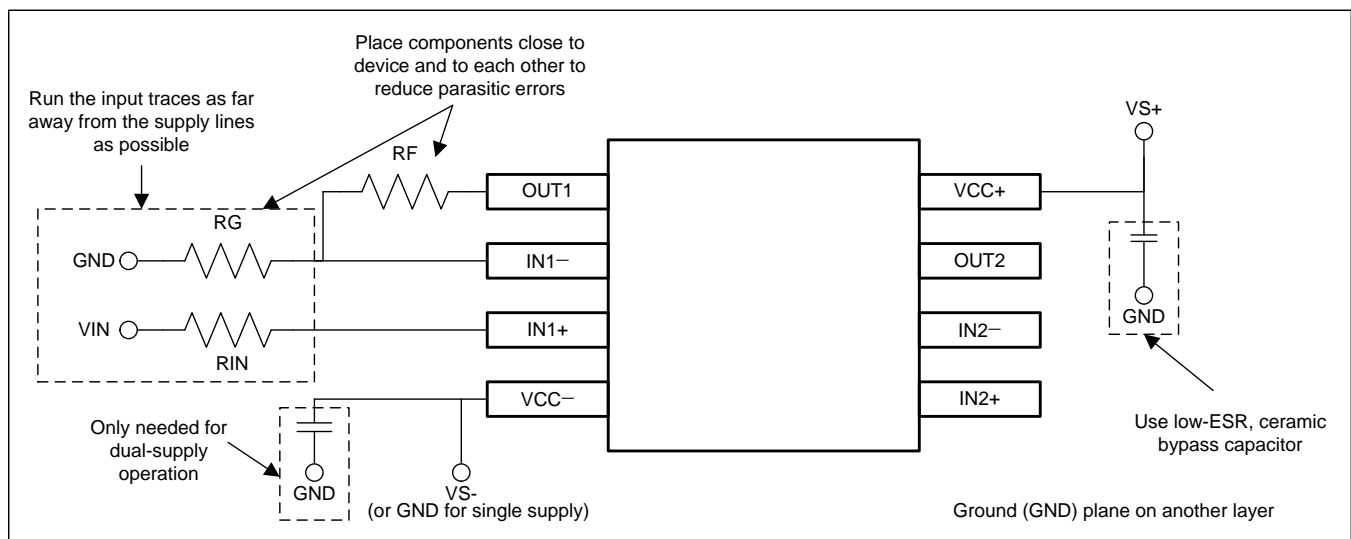
Figure 7. Operational Amplifier Board Layout for Noninverting Configuration

Product Folder Links: *LP358 LP2904*

12   Device and Documentation Support

12.1   Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP358	Click here	Click here	Click here	Click here	Click here
LP2904	Click here	Click here	Click here	Click here	Click here

12.2   Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3   Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4   Trademarks

E2E is a trademark of Texas Instruments.

12.5   Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6   Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2904D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LP2904
LP2904DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2904
LP2904DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2904
LP358D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LP358
LP358DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP358
LP358DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LP358

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2904DR	SOIC	D	8	2500	353.0	353.0	32.0
LP358DR	SOIC	D	8	2500	353.0	353.0	32.0

.228-.244 TYP
[5.80-6.19]

A

PIN 1 ID AREA

6X .050
[1.27]

1

8

2X

.189-.197
[4.81-5.00]
NOTE 3

.150
[3.81]

4

5

8X .012-.020
[0.31-0.51]

B

.150-.157
[3.81-3.98]
NOTE 4

⊕ .010 [0.25] Ⓜ C A B

C

SEATING PLANE

△ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM

4

5

6X (.050)
[1.27]

(R.002) TYP
[0.05]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

6X (.050)
[1.27]

4

SYMM
₵

SYMM
₵

8

5

(R.002) TYP
[0.05]

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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