具有 17V 最大输入电压的 LMZ21700 650mA 微型模块

1 特性

- 集成电感
- 微型 3.5mm × 3.5mm × 1.75mm 封装
- 35 mm² Solution Size (Single Sided)
- –40°C 至 125°C 结温范围
- 可调输出电压
- 集成补偿
- 可调软启动功能
- 启动至预偏置负载
- 电源正常状态和使能引脚
- 节能模式无缝转换
- 输出电流高达 650 mA
- 输入电压范围为 3V 至 17V
- 输出电压范围为 0.9V 到 6V
- 效率高达 95 %
- 1.5µA 关断电流
- 17µA 静态电流
- 使用 LMZ21700 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 3.3V、5V 或 12V 输入电压的负载点转换
- 空间受限型 应用
- 低压降稳压器 (LDO) 替代产品

3 说明

LMZ21700 微型模块是易于使用的降压直流/直流解决方案，可在空间受限的应用中驱动高达 650mA 的 负载。仅需一个输入电容器、一个输出电容器、一个软启动电容器和两个电阻器即可完成基本操作。

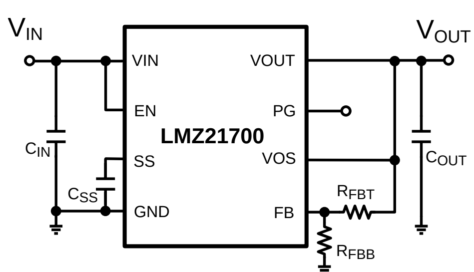
典型应用快速 链接：V_{OUT} = 1.2 V、V_{OUT} = 1.8 V、V_{OUT} = 2.5 V、V_{OUT} = 3.3 V、V_{OUT} = 5.0 V

器件信息(1)

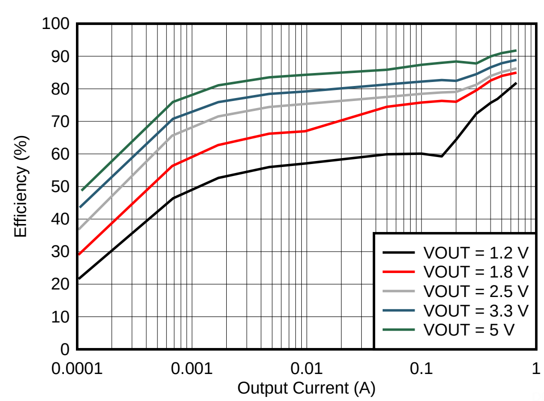
器件型号	封装	封装尺寸（标称值）
LMZ21700	µSIP (8)	3.50mm x 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



V_{IN} = 12V 时的效率



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (November 2014) to Revision D — **Page**

- 删除了 Simple Switcher 品牌；添加了 TI 参考设计顶部导航图标、Webench 链接和 T&R 内容 1

Changes from Revision B (October 2014) to Revision C — **Page**

- 已更改 将“产品概述”更改成了“生产数据” 1
- Changed to Final Limits 5

Changes from Revision A (October 2013) to Revision B — **Page**

- 已添加 *添加了“器件信息”表和“处理额定值”表、“特性 说明”、“应用和实施”、“布局”、“器件和文档支持”以及“机械、封装和可订购信息”，将一些曲线移到了“应用曲线”中* 1
- 已将数据表更改为最新 TI 标准 1

Changes from Original (August 2012) to Revision A — **Page**

- 已更改 说明 1

5 Pin Configuration and Functions

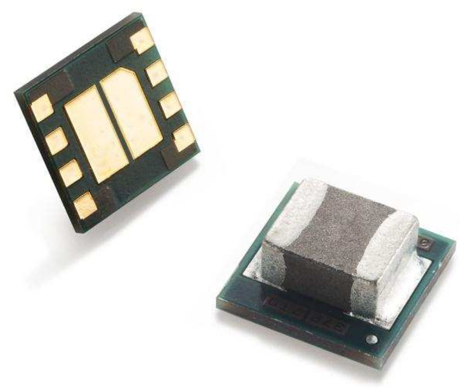


Figure 1. LMZ21700 in the SIL0008E Package

SIL0008E
8-Pin
Top View

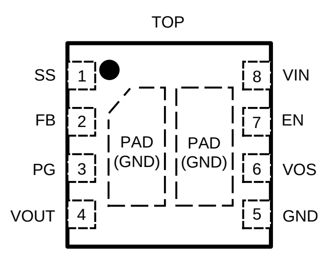


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	1	I	Soft-start pin. An external capacitor connected to this pin sets the internal voltage reference ramp time. It can be used for tracking and sequencing.
FB	2	I	Voltage feedback. Connect resistive voltage divider to this pin to set the output voltage.
PG	3	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor; goes low impedance when EN is low)
VOUT	4	O	Output Voltage. Connected to one terminal of the integrated inductor. Connect output filter capacitor between VOUT and PGND.
GND	5	I	Ground for the power MOSFETs and gate-drive circuitry.
VOS	6	I	Output voltage sense pin and connection for the control loop circuitry.
EN	7	I	Enable input (High = enabled, Low = disabled). Internal pull down resistor keeps logic level low if pin is left floating
VIN	8	I	Supply voltage for control circuitry and power stage.
PAD			Electrically connected to GND. Must be soldered to a ground copper plane to achieve appropriate power dissipation and mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN	−0.3	20	V
EN, SS	−0.3	VIN +0.3 V w/ 20 V max	V
FB, PG, VOS	−0.3	7	V
PG sink current		10	mA
Junction Temperature (T_{J-MAX})	−40	125	°C
Maximum Lead Temperature		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	−500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Voltage Range	3	17	V
Output Voltage Range	0.9	6.0	V
Recommended Load Current	0	650	mA
Junction Temperature (T_J)	−40	125	°C

(1) Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see the Electrical Characteristics section.

6.4 Thermal Information

THERMAL METRIC(1)		LMZ21700	UNIT
		SIL0008E	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	42.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	9.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance (θ_{JA}) is based on 4 layer board thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standards JESD51-1 to JESD51-11. θ_{JA} varies with PCB copper area, power dissipation, and airflow.

6.5 Electrical Characteristics(1)

Limits apply over the recommended operating junction temperature (T_J) range of -40 °C to +125 °C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS						
I_Q	Operating quiescent current	EN = high, I_{OUT}= 0 mA, T_J = -40°C to 85°C device not switching		17	25	µA
		EN = high, I_{OUT}= 0 mA, T_J = -40°C to 125°C device not switching		17	28	µA
I_{SD}	Shutdown current	EN = low, T_J = -40 °C to 85 °C		1.5	4	µA
		EN = low, T_J = -40 °C to 125 °C		1.5	5	µA
VIN_{UVLO}	Input under voltage lock out rising threshold		2.8	2.9	3	V
$VIN_{UVLO-HYS}$	Input under voltage lock out hysteresis		0.125	0.180	0.260	V
T_{SD}	Thermal shutdown	Rising Threshold		160		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis			30		°C
CONTROL						
$V_{IH, ENABLE}$	Enable logic HIGH voltage		0.9			V
$V_{IL, ENABLE}$	Enable logic LOW voltage				0.3	V
I_{LKG}	Input leakage current	EN = VIN or GND		0.01	1	µA
V_{TH_PG}	Power Good threshold voltage	Rising (% V_{OUT})	92 %	95 %	98 %	
		Falling (% V_{OUT})	87 %	90 %	93 %	
V_{OL_PG}	Power Good output low voltage	I_{PG} = -2 mA		0.07	0.3	V
I_{LKG_PG}	Power Good leakage current	V_{PG} = 1.8 V		1	400	nA
I_{SS}	Softstart Pin source current		2.2	2.5	2.8	µA
POWER STAGE						
$R_{DS(ON)}$	High-Side MOSFET ON Resistance	V_{IN} ≥ 6 V		82		mΩ
		V_{IN} = 3 V		120		
	Low-Side MOSFET ON Resistance	V_{IN} ≥ 6 V		40		mΩ
		V_{IN} = 3 V		50		
L	Integrated power inductor value			2.2		µH
DCR	Integrated power inductor DC resistance			92		mΩ
I_{CL-HS}	High-Side MOSFET Current Limit	T_A = 25 °C	1.2	1.5	1.9	A
I_{CL-LS}	Low-Side MOSFET Current Limit	T_A = 25 °C		0.9		A
I_{CL-DC}	Output (DC) current limit	V_{OUT} = 5.0 V, T_A = 85 °C		0.95		A
OUTPUT						
V_{REF}	Internal reference voltage		0.7869	0.803	0.8191	V
I_{FB}	Feedback pin leakage current	V_{FB} = 0.8V		1	100	nA
V_{OUT}	Light load initial voltage accuracy	Power save mode, C_{OUT} = 22 µF, T_A= -40 °C to 85 °C, 1% FB Resistors	-2.3 %		2.8 %	
V_{OUT}	Load regulation	V_{OUT} = 3.3 V PWM mode operation		0.05 %		/ A

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

Electrical Characteristics[1] (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40 °C to +125 °C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OUT}	Line regulation	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 650 mA PWM mode operation		0.02 %		/ V
SYSTEM CHARACTERISTICS						
η	Full Load Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 650 mA		88 %		
	Light Load Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 1 mA		72 %		

6.6 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25 °C

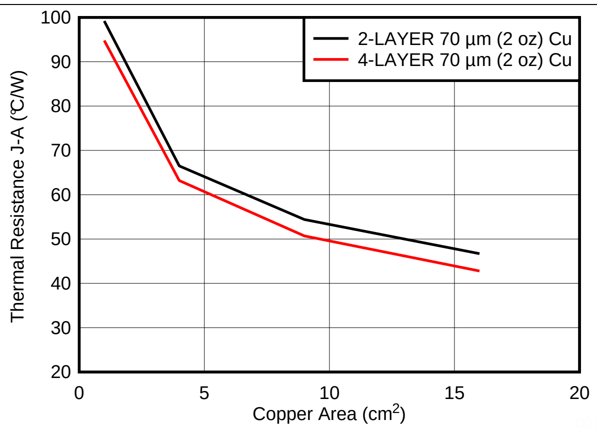
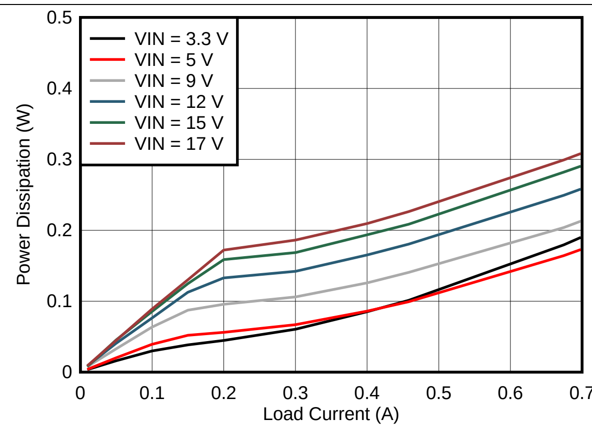
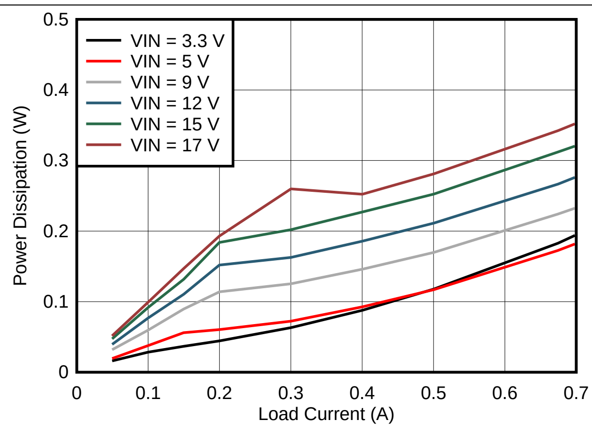


Figure 2. Package Thermal Resistance vs. Board Copper Area, No Air Flow



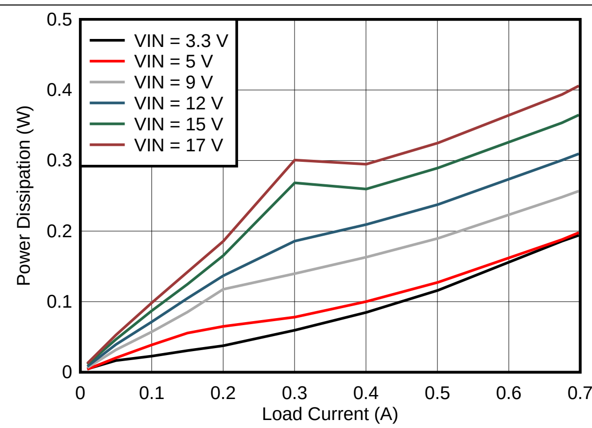
V_{OUT} = 1.2 V T_A = 85 ºC

Figure 3. Power Dissipation



V_{OUT} = 1.8 V T_A = 85 ºC

Figure 4. Power Dissipation

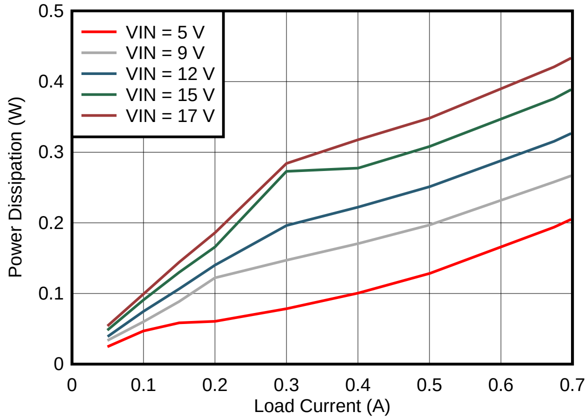


V_{OUT} = 2.5 V T_A = 85 ºC

Figure 5. Power Dissipation

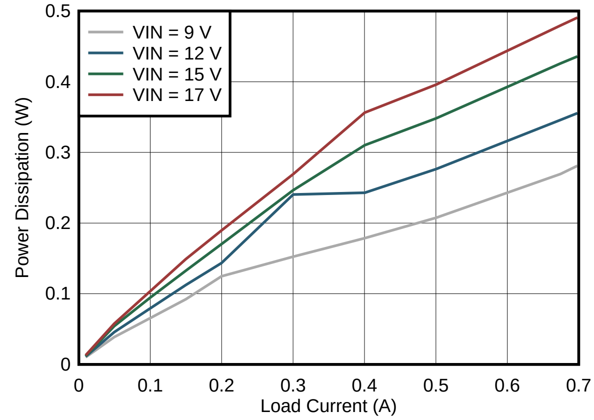
Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25 °C



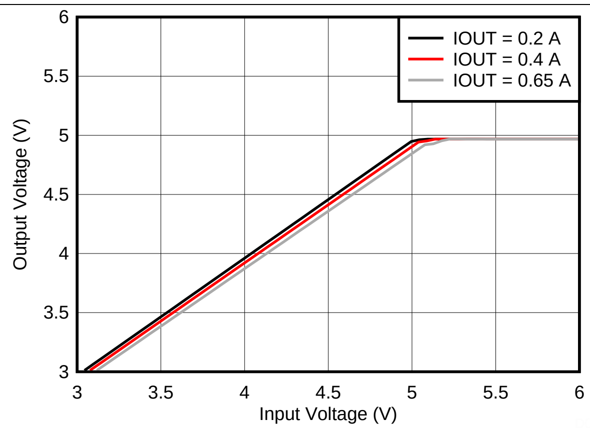
V_{OUT} = 3.3 V T_A = 85 ºC

Figure 6. Power Dissipation



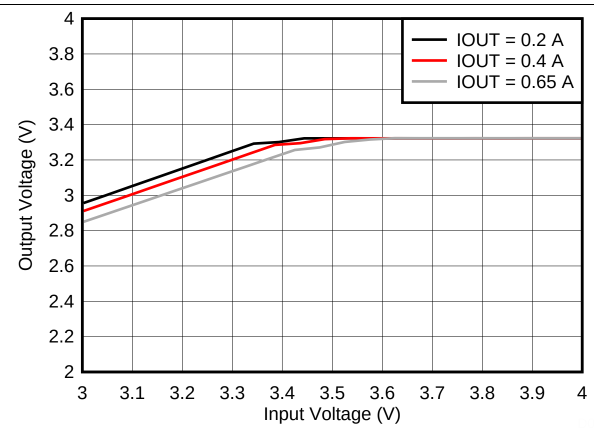
V_{OUT} = 5.0 V T_A = 85 ºC

Figure 7. Power Dissipation



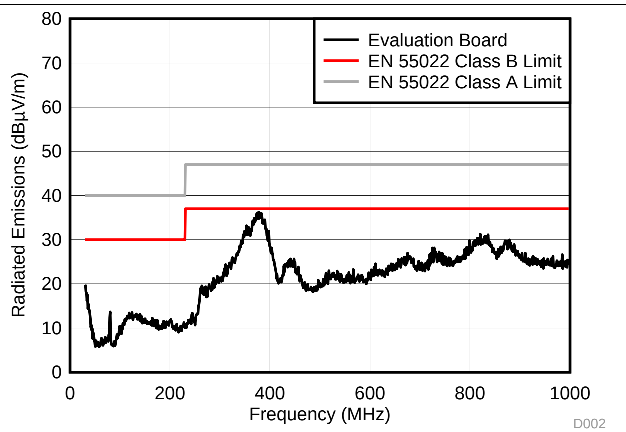
V_{OUT} = 5.0 V T_A = 85 ºC

Figure 8. Dropout



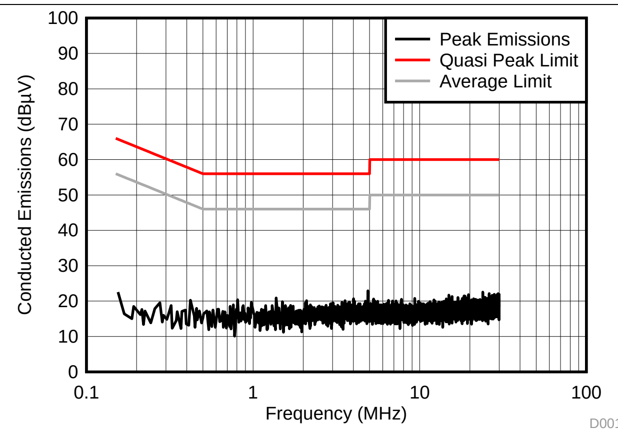
V_{OUT} = 3.3 V T_A = 85 ºC

Figure 9. Dropout



V_{IN}= 12 V V_{OUT} = 3.3 V I_{OUT} = 650 mA

Figure 10. Radiated EMI on EVM



V_{IN}= 12 V V_{OUT} = 3.3 V I_{OUT} = 650 mA

Lf = 2.2 µH Cf = 1.0 µF

Figure 11. Conducted EMI on EVM

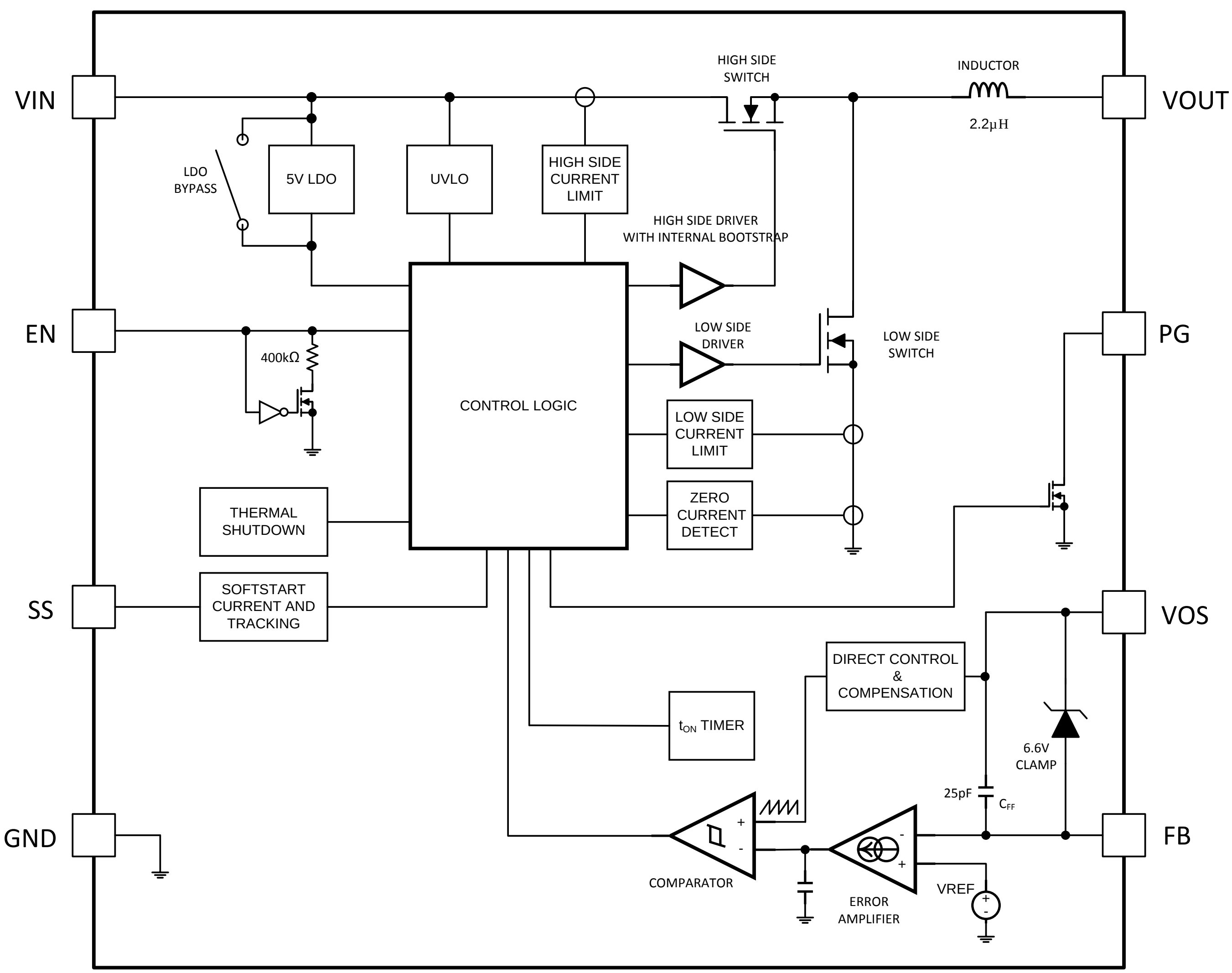
7 Detailed Description

7.1 Overview

The LMZ21700 SIMPLE SWITCHER® Nano Module is an easy-to-use step-down DC-DC solution capable of driving up to 650 mA load in space-constrained applications. Only an input capacitor, an output capacitor, a softstart capacitor, and two resistors are required for basic operation. The Nano Module comes in 8-pin DFN footprint package with an integrated inductor. The LMZ21700 architecture is based on DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode). This architecture combines the fast transient response and stability of hysteretic type converters along with the accurate DC output regulation of voltage mode and current mode regulators.

The LMZ21700 architecture uses Pulse Width Modulation (PWM) mode for medium and heavy load requirements and Power Save Mode (PSM) at light loads for high efficiency. In PWM mode the switching frequency is controlled over the input voltage range. The value depends on the output voltage setting and is typically reduced at low output voltages to achieve higher efficiency. In PSM the switching frequency decreases linearly with the load current. Since the architecture of the device supports both operation modes (PWM and PSM) in a single circuit building block, the transition between the modes of operation is seamless with minimal effect on the output voltage.

7.2 Functional Block Diagram



7.3 Package Construction

In order to achieve a small solution size the LMZ21700 Nano Module comes in an innovative MicroSiP™ package. The construction consists of a synchronous buck converter IC embedded inside an FR-4 laminate substrate, with a power inductor mounted on top of the substrate material. See Figure 12 and Figure 13 below. The bottom (landing pads) of the package resemble a typical 8-pin DFN package. See the Mechanical drawings at the end of the datasheet for details on the recommended landing pattern and solder paste stencil information.

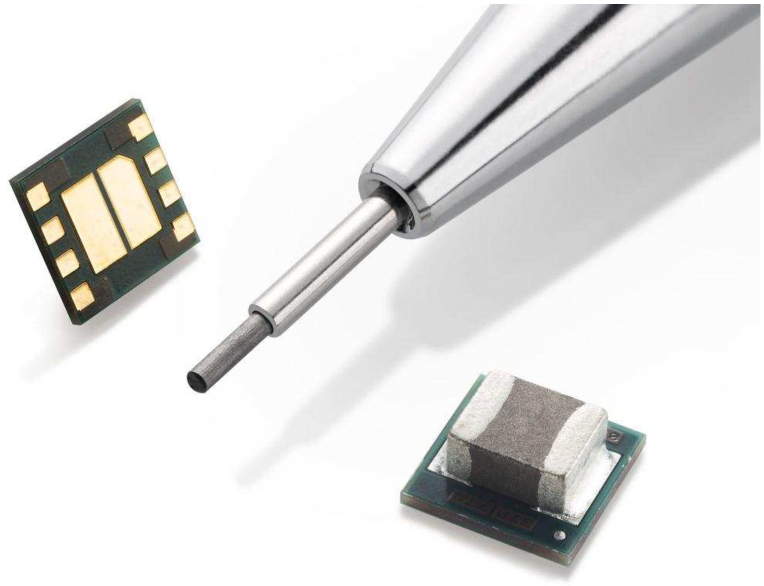


Figure 12. LMZ21700 in the SIL0008E Package

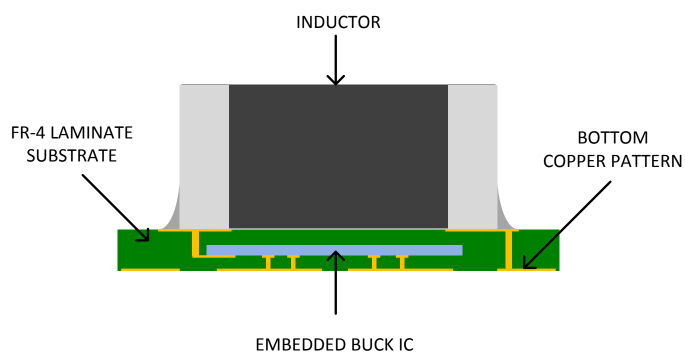


Figure 13. LMZ21700 Package Construction Cross Section (Illustration Only, Not to Scale)

7.4 Feature Description

7.4.1 Input Under Voltage Lockout

The LMZ21700 features input under voltage lockout (UVLO) circuit. It monitors the input voltage level and prevents the device from switching the power MOSFETs if V_{IN} is not high enough. The typical V_{IN} UVLO rising threshold is 2.9 V with 180 mV of hysteresis.

Feature Description (continued)

7.4.2 Enable Input (EN)

The enable pin (EN) is weakly pulled down internally through a 400 kΩ resistor to keep EN logic low when the pin is floating. The pull-down resistor is not connected when EN is set high. Once the voltage on the enable pin (EN) is set high the Nano Module will start operation. If EN is set low (< 0.3 V) the LMZ21700 will enter shutdown mode. The typical shutdown quiescent current is 1.5 μA.

7.4.3 Softstart and Tracking Function (SS)

When EN is set high for device operation the LMZ21700 will start switching after 50 μs delay and the output voltage will start rising. The V_{OUT} rising slope is controlled by the external capacitor C_{SS} connected to the softstart (SS) pin. The nano module has a 2.5 μA constant current source internally connected to the SS pin to program the softstart time T_{SS}:

$$T_{SS} = C_{SS} \times 1.25\ V / 2.5\ \mu A \quad (1)$$

The softstart capacitor voltage is reset to zero volts when EN is pulled low and when the thermal protection is active.

If tracking function is desired, the SS pin can be used to track external voltage. If the applied external tracking voltage is between 100 mV and 1.2 V, the FB voltage will follow SS according to the following relationship:

$$V_{FB} = 0.64 \times V_{SS} \quad (2)$$

7.4.4 Power Good Function (PG)

The LMZ21700 features a Power Good (PG) function which can be used for sequencing of multiple rails. The PG pin is an open-drain output and requires a pull-up resistor R_{PG} to V_{OUT} (or any other external voltage less than 7 V). When the Nano Module is enabled and UVLO is satisfied, the power good function starts monitoring the output voltage. The PG pin is kept at logic low if the output has not reached the proper regulation voltage. Refer to the Electrical Characteristics table for the PG voltage thresholds. The PG pin can sink 2 mA of current which sets the minimum limit of the R_{PG} resistance value:

$$R_{PG\text{-}MIN} = V_{PULL\text{-}UP} / 2\ mA \quad (3)$$

The PG pin goes low impedance if the device is disabled or the thermal protection is active.

7.4.5 Output Voltage Setting

The output voltage of the LMZ21700 is set by a resistive divider from V_{OUT} to GND, connected to the feedback (FB) pin. The output voltage can be set between 0.9 V and 6 V. The voltage at the FB pin is regulated to 0.8 V. The recommended minimum divider current is 2 μA. This sets a maximum limit on the bottom feedback resistor R_{FBB}. Its value should not exceed 400 kΩ. The top feedback resistor R_{FBT} can be calculated using the following formula:

$$R_{FBT} = R_{FBB} \times (V_{OUT} / 0.8 - 1) \quad (4)$$

7.4.6 Output Current Limit and Output Short Circuit Protection

The LMZ21700 has integrated protection against heavy loads and output short circuit events. Both, the high-side FET and low-side FET have current monitoring circuitry. If the current limit threshold of the high-side FET is reached , the high-side FET will be turned off and the low-side FET will be turned on to ramp down the inductor current. Once the current through the low-side FET has decreased below a safe level, the high-side device will be allowed to turn on again. The actual DC output current depends on the input voltage, output voltage, and switching frequency. Refer to the *Application Curves section f*or more information.

7.4.7 Thermal Protection

The nano module monitors its junction temperature (Tj) and shuts itself off if the it gets too hot. The thermal shutdown threshold for the junction is typically 160 °C. Both, high-side and low-side FETs are turned off until the junction temperature has decreased under the hysteresis level, typically 30 °C below the shutdown temperature.

7.5 Device Functional Modes

7.5.1 PWM Mode Operation

The LMZ21700 operates in PWM mode when the output current is greater than half the inductor ripple current. The frequency variation in PWM mode is controlled and depends on the V_{IN} and V_{OUT} settings. Refer to the *Application Curves* section for switching frequency graphs for several typical output voltage settings. As the load current is decreased and the valley of the inductor current ripple reaches 0 A the device enters PSM operation to maintain high efficiency.

7.5.2 PSM Operation

Once the load current decreases and the valley of the inductor current reaches 0 A, the LMZ21700 will transition to Power Save Mode of operation. The device will remain in PSM as long as the inductor current is discontinuous. The switching frequency will decrease linearly with the load current. If V_{IN} decreases to about 15 % above V_{OUT} the device will not enter PSM and will maintain output regulation in PWM mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ21700 is a step down DC-to-DC converter. It is used to convert higher DC voltage to a regulated lower DC voltage with maximum load current of 650 mA. The following design procedure can be used to select components for the LMZ21700. Alternatively, the WEBENCH® software can be used to select from a large database of components, run electrical simulations, and optimize the design for specific performance. Please go to webench.ti.com to access the WEBENCH® tool.

8.2 Typical Application

For a quick start, the following component values can be used as a design starting point for several typical output voltage rails and 650 mA of output load current.

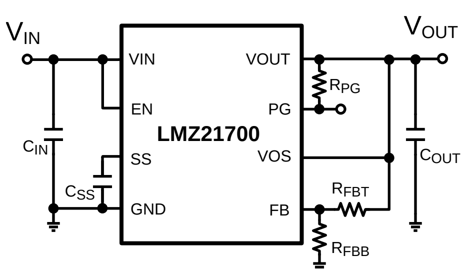


Figure 14. Typical Applications Circuit

COMPONENT VALUES FOR VOUT=1.2V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	41.2kΩ	1%	
R_{FBB}	82.5kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 15. External Component Values (V_{OUT} = 1.2 V)

Typical Application (continued)

COMPONENT VALUES FOR VOUT=1.8V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	147kΩ	1%	
R_{FBB}	118kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 16. External Component Values (V_{OUT} = 1.8 V)

COMPONENT VALUES FOR VOUT=2.5V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	357kΩ	1%	
R_{FBB}	169kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 17. External Component Values (V_{OUT} = 2.5 V)

COMPONENT VALUES FOR VOUT=3.3V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	1.21MΩ	1%	
R_{FBB}	383kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 18. External Component Values (V_{OUT} = 3.3 V)

COMPONENT VALUES FOR VOUT=5.0V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	232kΩ	1%	
R_{FBB}	44.2kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 19. External Component Values (V_{OUT} = 5.0 V)

8.2.1 Design Requirements

The design procedure requires a few typical design parameters. See Table 2 below.

Table 2. Design Parameters

Design Parameter	Value
Input Voltage (V_{IN})	Range from 3.0 V to 17 V
Output Voltage (V_{OUT})	Range from 0.9 V to 6 V
Output Current (I_{OUT})	Up to 650 mA
Softstart time (T_{SS})	Minimum of 0.5 ms recommended

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor (C_{IN})

Low ESR multi-layer ceramic capacitors (MLCC) are recommended for the input capacitor of the LMZ21700. Using a ≥ 10 µF ceramic input capacitor in ≥ 0805 (2012 metric) case size with 25 V rating typically provides sufficient VIN bypass. Use of multiple capacitors can also be considered. Ceramic capacitors with X5R and X7R temperature characteristics are recommended. These provide an optimal balance between small size, cost, reliability, and performance for applications with limited space. The DC voltage bias characteristics of the capacitors must be considered when selecting the DC voltage rating and case size of these components. The effective capacitance of an MLCC is typically reduced by the DC voltage bias applied across its terminals. Selecting a part with larger capacitance, larger case size, or higher voltage rating can compensate for the capacitance loss due to the DC voltage bias effect. For example, a 10 µF, X7R, 25 V rated capacitor used under 12 V DC bias may have approximately 8 µF effective capacitance in a 1210 (3225 metric) case size and about 6 µF in a 1206 (3216 metric) case size. As another example, a 10 µF, X7R, 16 V rated capacitor in a 1210 (3225 metric) case size used at 12 V DC bias may have approximately 5.5 µF effective capacitance. Check the capacitor specifications published by the manufacturer.

8.2.2.2 Output Capacitor (C_{OUT})

Similarly to the input capacitor, it is recommended to use low ESR multi-layer ceramic capacitors for C_{OUT}. Ceramic capacitors with X5R and X7R temperature characteristics are recommended. Use 10 µF or larger value and consider the DC voltage bias characteristics of the capacitor when choosing the case size and voltage rating. For stability, the output capacitor should be in the 10 µF – 200 µF effective capacitance range.

8.2.2.3 Softstart Capacitor (C_{SS})

The softstart capacitor is chosen according to the desired softstart time. As described in the Softstart and Tracking Function section the softstart time $T_{SS} = C_{SS}$ x 1.25 V / 2.5 µA.

A minimum C_{SS} value of 1000 pF is required for monotonic V_{OUT} ramp up.

8.2.2.4 Power Good Resistor (R_{PG})

If the Power Good function is used, a pull up resistor R_{PG} is necessary from the PG pin to an external pull-up voltage.

The minimum R_{PG} value is restricted by the pull down current capability of the internal pull down device.

$$R_{PG\text{-}MIN} = V_{PULL\text{-}UP} / 2\ mA \quad (5)$$

The maximum R_{PG} value is based on the maximum PG leakage current and the minimum “logic high” level system requirements:

$$R_{PG\text{-}MAX} = (V_{PULL\text{-}UP} – V_{LOGIC\text{-}HIGH}) / I_{LKG\_PG} \quad (6)$$

8.2.2.5 Feedback Resistors (R_{FBB} and R_{FBT})

The feedback resistors R_{FBB} and R_{FBT} set the desired output voltage. Choose R_{FBB} less than 400 kΩ and calculate the value for R_{FBT} using the following formula:

$$R_{FBT} = R_{FBB} \times (V_{OUT} / 0.8 – 1) \quad (7)$$

8.2.3 Application Curves

8.2.3.1 V_{OUT} = 1.2 V

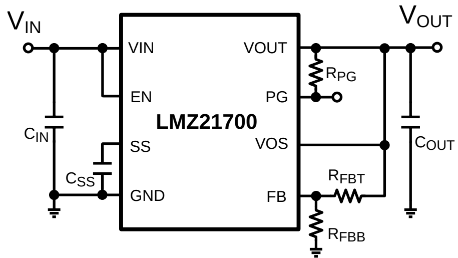


Figure 20. Typical Applications Circuit

COMPONENT VALUES FOR VOUT=1.2V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	41.2kΩ	1%	
R_{FBB}	82.5kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 21. External Component Values (V_{OUT} = 1.2V)

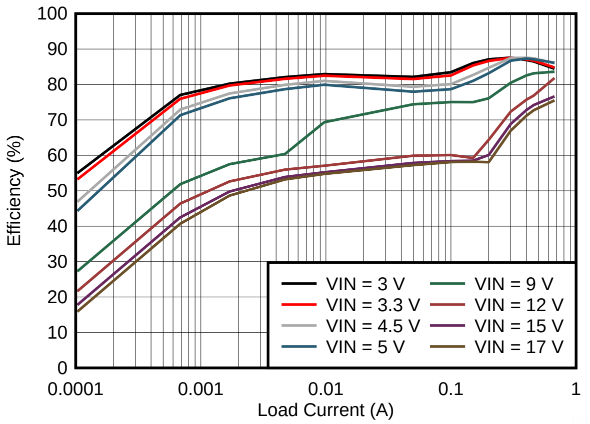


Figure 22. Efficiency V_{OUT} = 1.2V

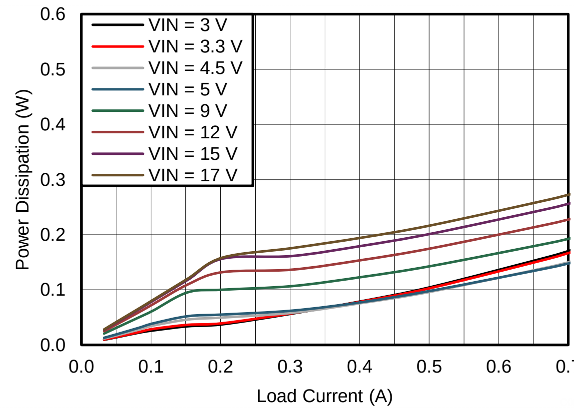


Figure 23. Power Dissipation V_{OUT} = 1.2V

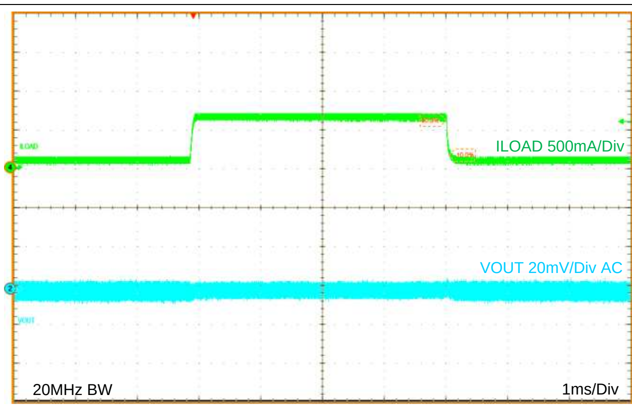


Figure 24. Load Transient V_{OUT} = 1.2V

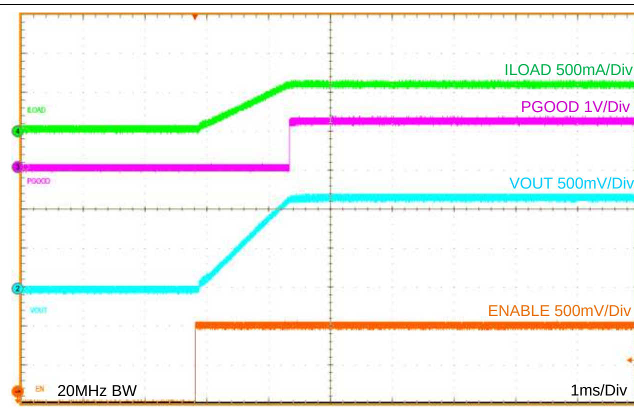


Figure 25. Startup V_{OUT} = 1.2V

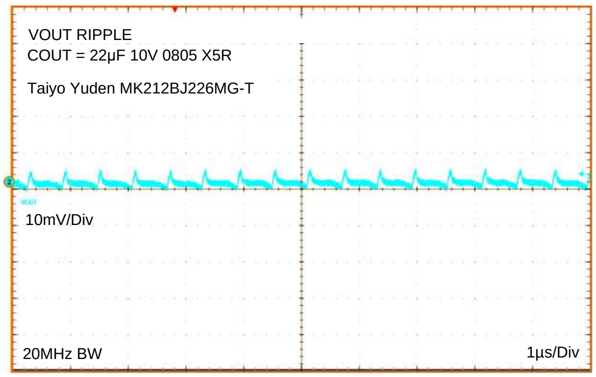


Figure 26. 20MHz Oscilloscope Bandwidth Output Voltage Ripple V_{OUT} = 1.2V

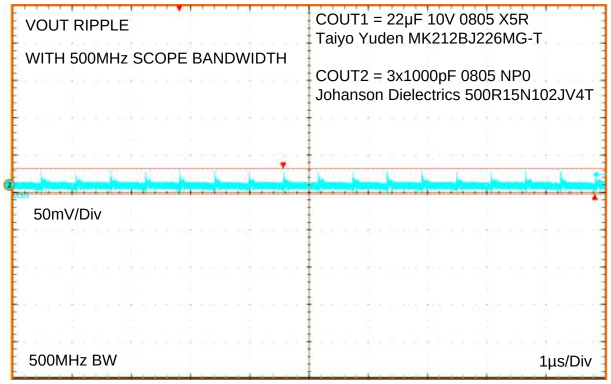


Figure 27. 500MHz Oscilloscope Bandwidth, 3x1000pF additional output capacitance Output Voltage Ripple and HF Noise V_{OUT} = 1.2V

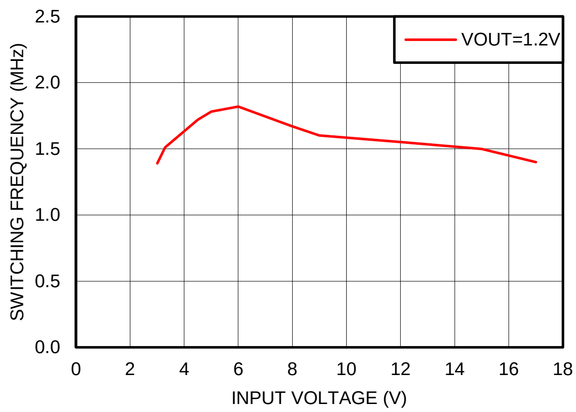


Figure 28. Typical Switching Frequency at 650mA Load V_{OUT} = 1.2V

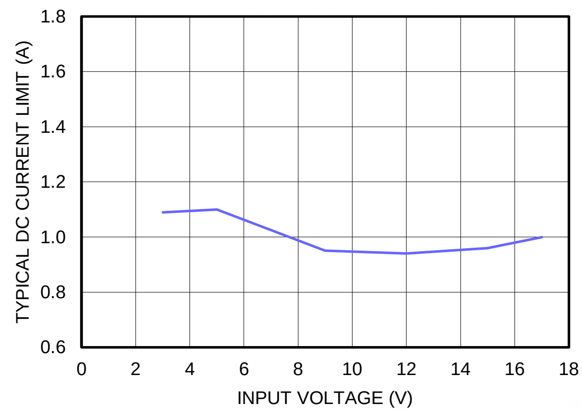


Figure 29. Typical Current Limit V_{OUT} = 1.2V, T_A = 85 °C

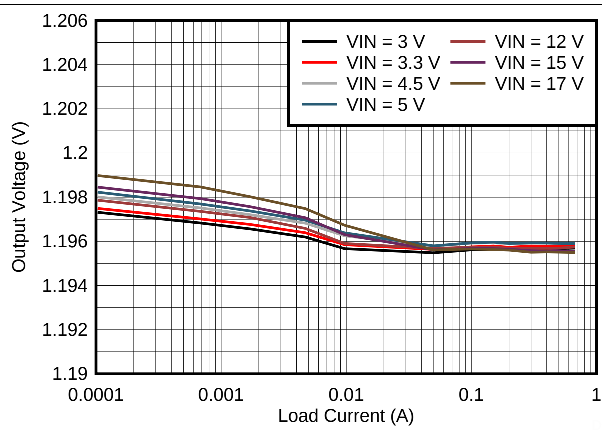


Figure 30. Line and Load Regulation V_{OUT} = 1.2V

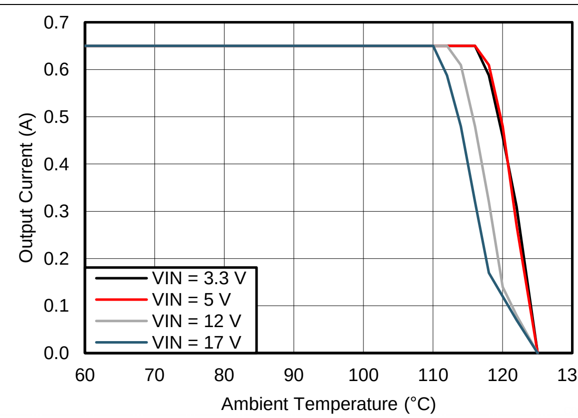


Figure 31. Thermal Derating for θ_{JA}= 47 °C/W, V_{OUT} = 1.2V

8.2.3.2 V_{OUT} = 1.8 V

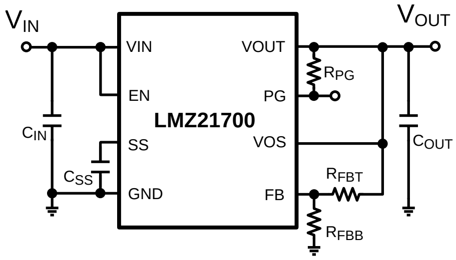


Figure 32. Typical Applications Circuit

COMPONENT VALUES FOR VOUT=1.8V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	147kΩ	1%	
R_{FBB}	118kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 33. External Component Values (V_{OUT} =1.8V)

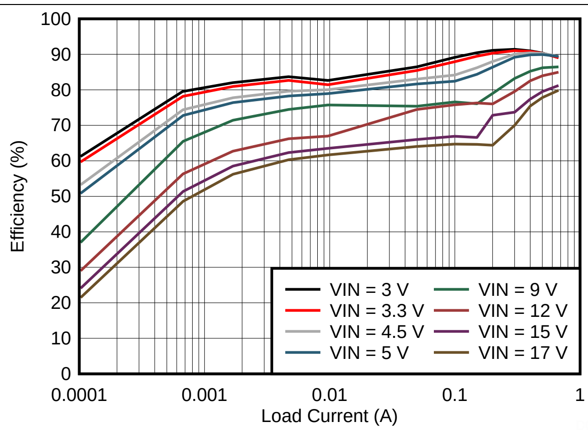


Figure 34. Efficiency V_{OUT} = 1.8 V

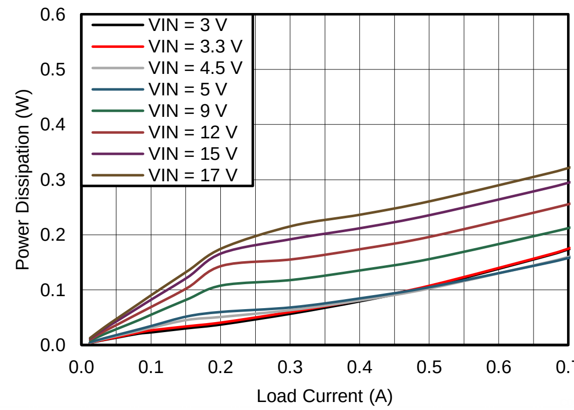


Figure 35. Power Dissipation V_{OUT} = 1.8 V

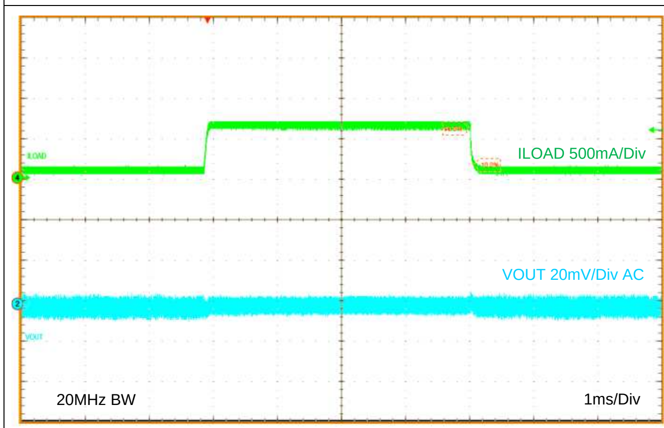


Figure 36. Load Transient V_{OUT} = 1.8 V

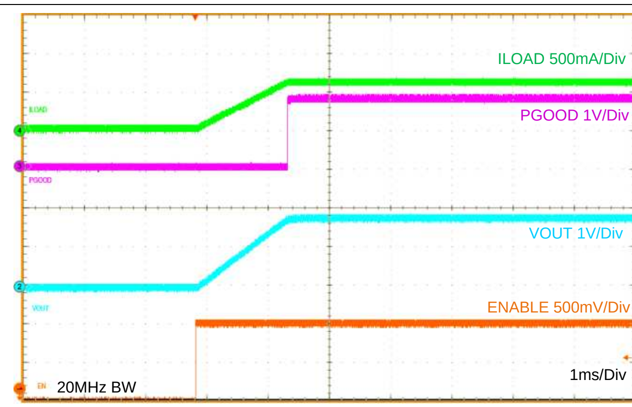


Figure 37. Startup V_{OUT} = 1.8 V

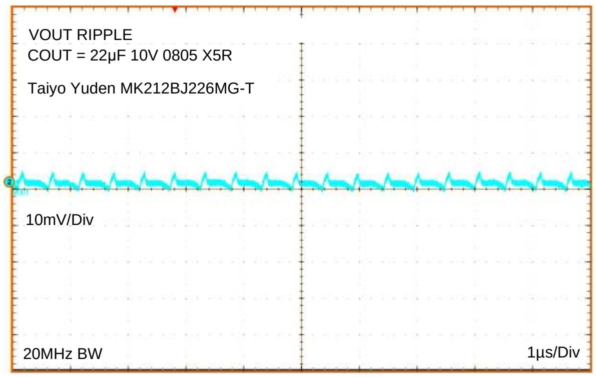


Figure 38. 20MHz Oscilloscope Bandwidth Output Voltage Ripple V_{OUT} = 1.8 V

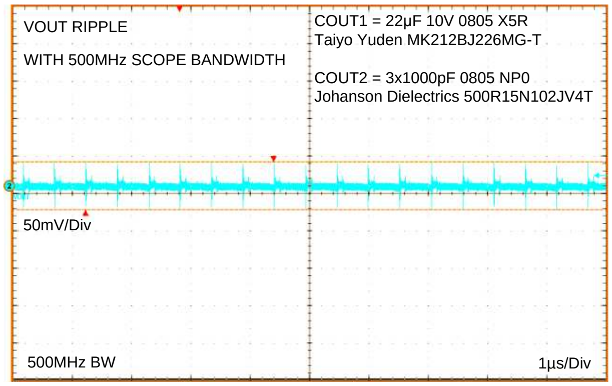


Figure 39. 500MHz Oscilloscope Bandwidth, 3x1000pF additional output capacitance Output Voltage Ripple and HF Noise V_{OUT} = 1.8 V

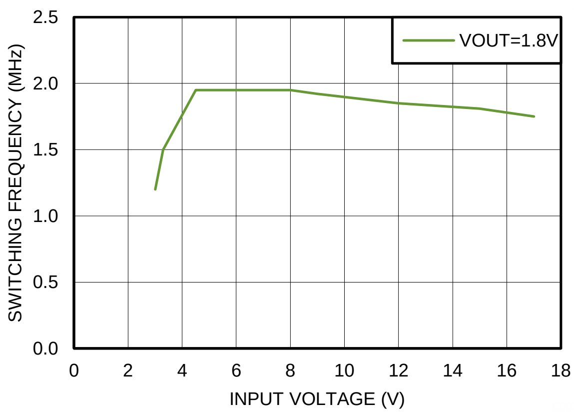


Figure 40. Typical Switching Frequency at 650mA Load V_{OUT} = 1.8 V

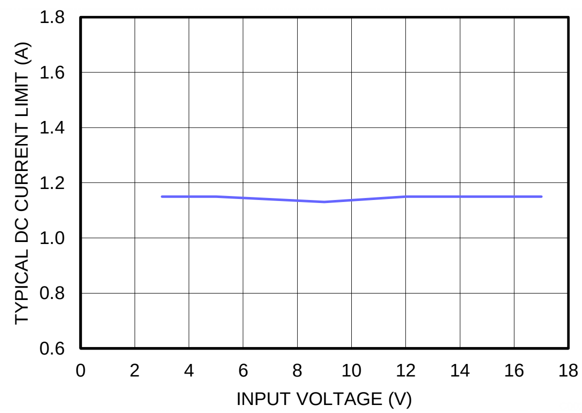


Figure 41. Typical Current Limit V_{OUT} = 1.8 V, T_A = 85 °C

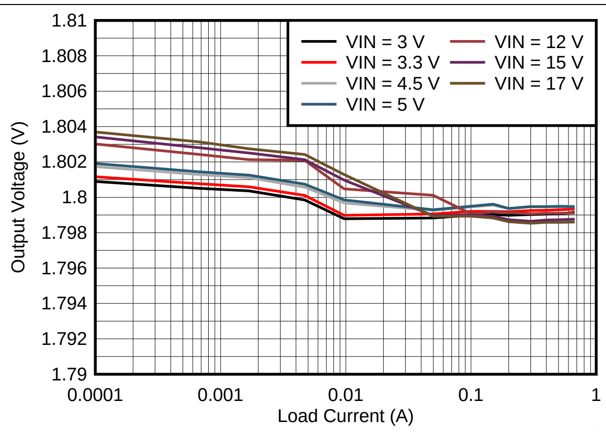


Figure 42. Line and Load Regulation V_{OUT} = 1.8 V

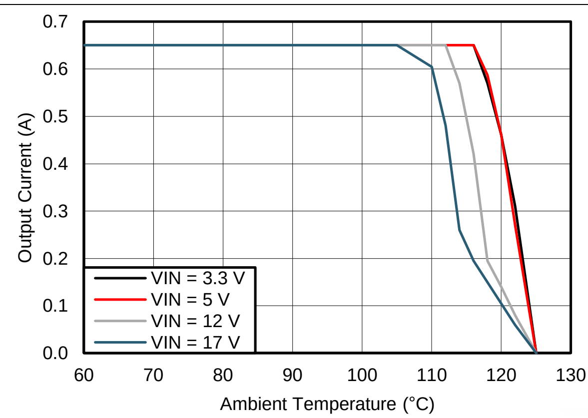


Figure 43. Thermal Derating for θ_{JA}=47ºC/W, V_{OUT} = 1.8 V

8.2.3.3 V_{OUT} = 2.5 V

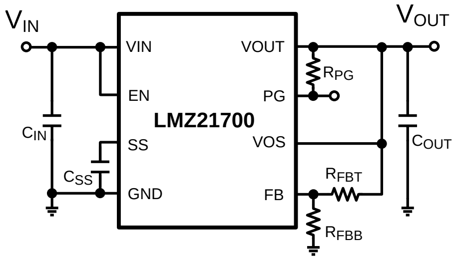


Figure 44. Typical Applications Circuit

COMPONENT VALUES FOR VOUT=2.5V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	357kΩ	1%	
R_{FBB}	169kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 45. External Component Values (V_{OUT} = 2.5 V)

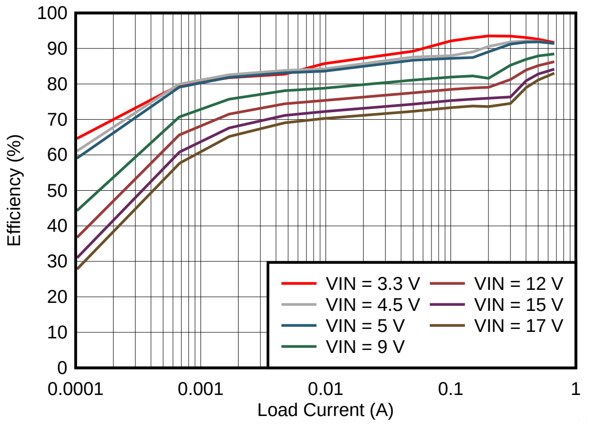


Figure 46. Efficiency V_{OUT} = 2.5 V

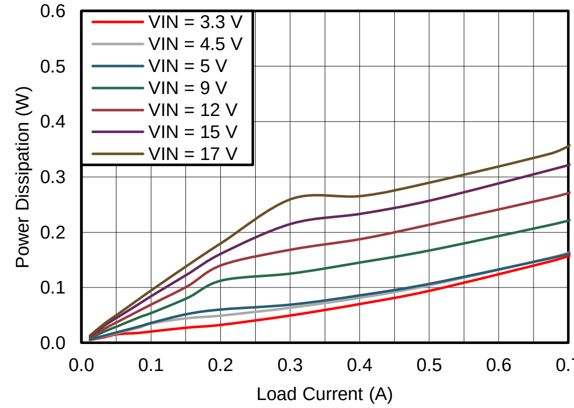


Figure 47. Power Dissipation V_{OUT} = 2.5 V

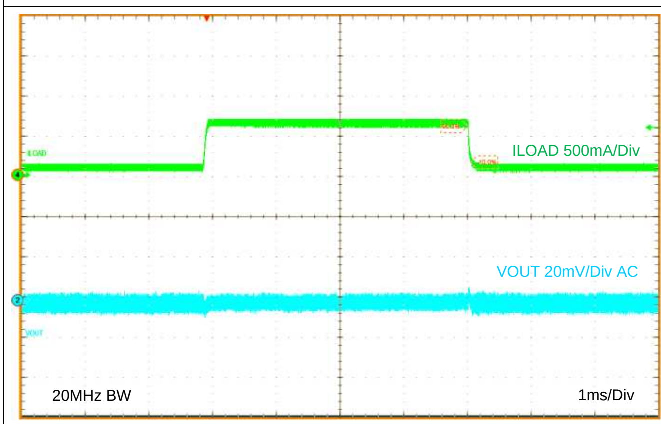


Figure 48. Load Transient V_{OUT} = 2.5 V

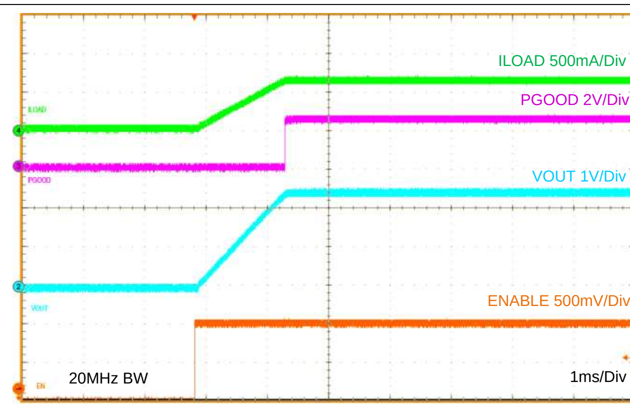


Figure 49. Startup V_{OUT} = 2.5 V

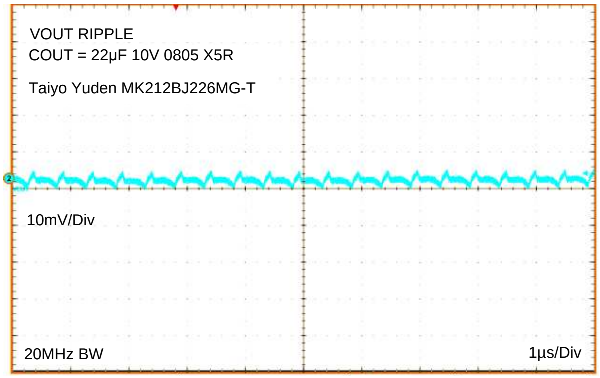


Figure 50. 20MHz Oscilloscope Bandwidth Output Voltage Ripple V_{OUT} = 2.5 V

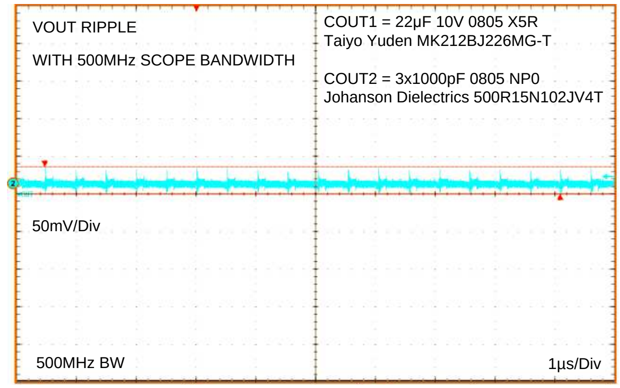


Figure 51. 500MHz Oscilloscope Bandwidth, 3x1000pF additional output capacitance Output Voltage Ripple and HF Noise V_{OUT} = 2.5 V

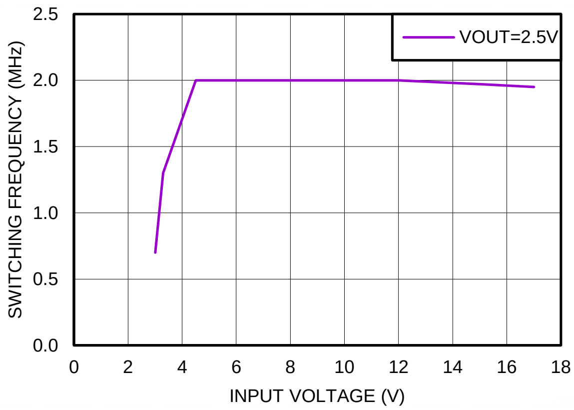


Figure 52. Typical Switching Frequency at 650mA Load V_{OUT} = 2.5 V

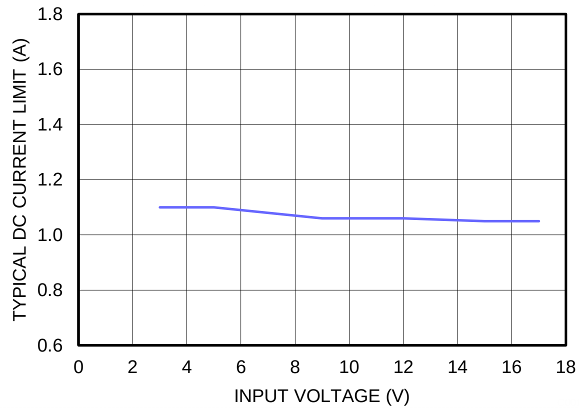


Figure 53. Typical Current Limit V_{OUT} = 2.5 V, T_A = 85 °C

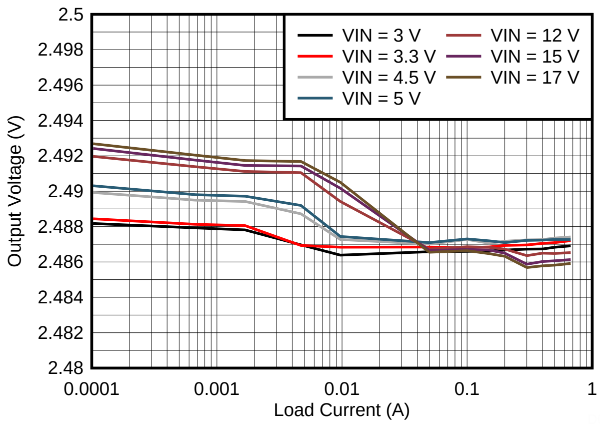


Figure 54. Line and Load Regulation V_{OUT} = 2.5 V

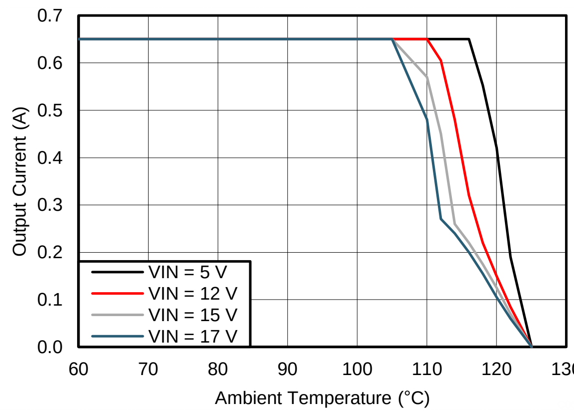


Figure 55. Thermal Derating for θ_{JA}=47ºC/W, V_{OUT} = 2.5 V

8.2.3.4 V_{OUT} = 3.3 V

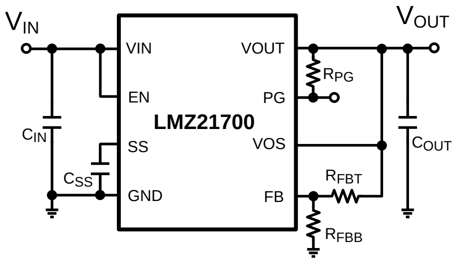


Figure 56. Typical Applications Circuit

COMPONENT VALUES FOR VOUT=3.3V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	1.21MΩ	1%	
R_{FBB}	383kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 57. External Component Values (V_{OUT} = 3.3V)

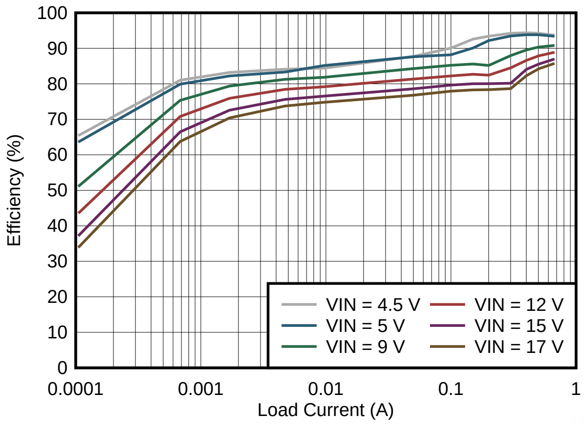


Figure 58. Efficiency V_{OUT} = 3.3 V

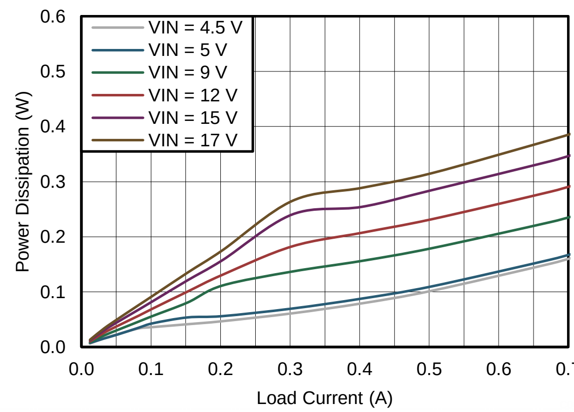


Figure 59. Power Dissipation V_{OUT} = 3.3 V

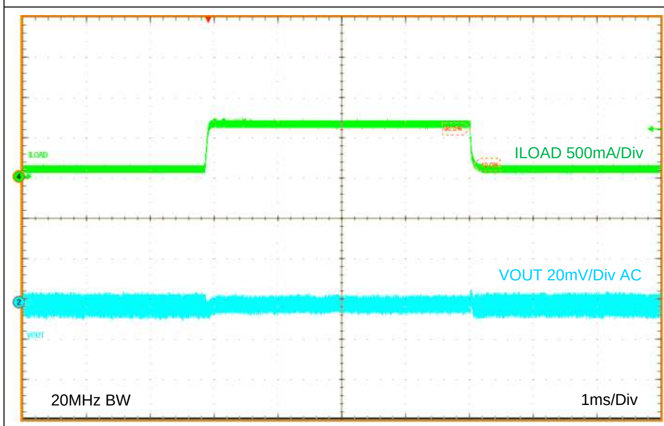


Figure 60. Load Transient V_{OUT} = 3.3 V

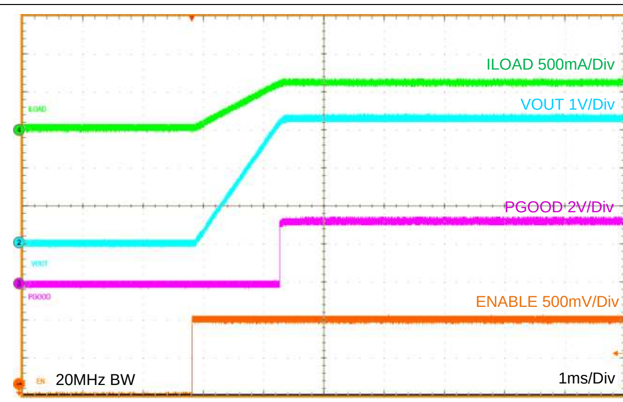


Figure 61. Startup V_{OUT} = 3.3 V

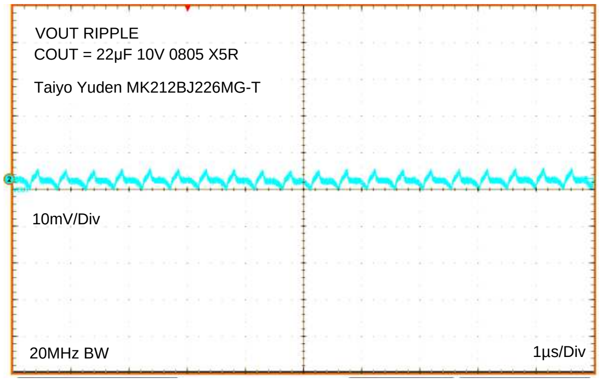


Figure 62. 20 MHz Oscilloscope Bandwidth Output Voltage Ripple V_{OUT} = 3.3 V

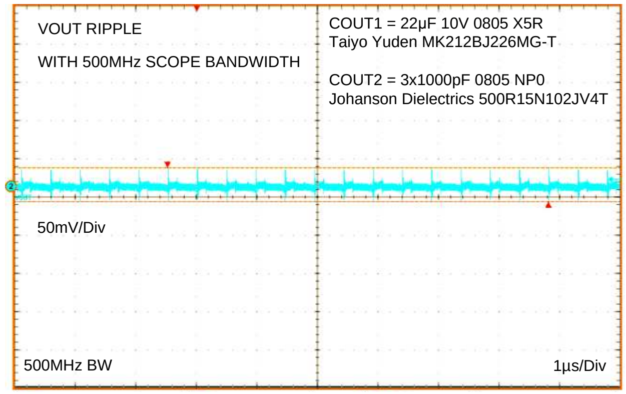


Figure 63. 500MHz Oscilloscope Bandwidth, 3x1000 pF additional output capacitance Output Voltage Ripple and HF Noise V_{OUT} = 3.3 V

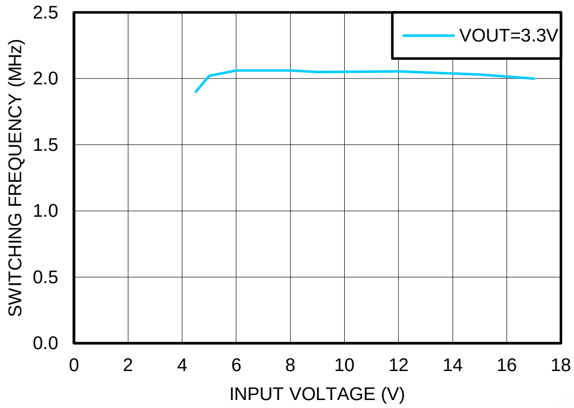


Figure 64. Typical Switching Frequency at 650mA Load V_{OUT} = 3.3 V

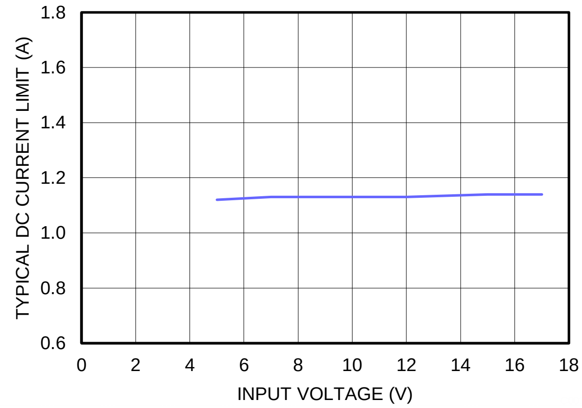


Figure 65. Typical Current Limit V_{OUT} = 3.3 V, T_A = 85 °C

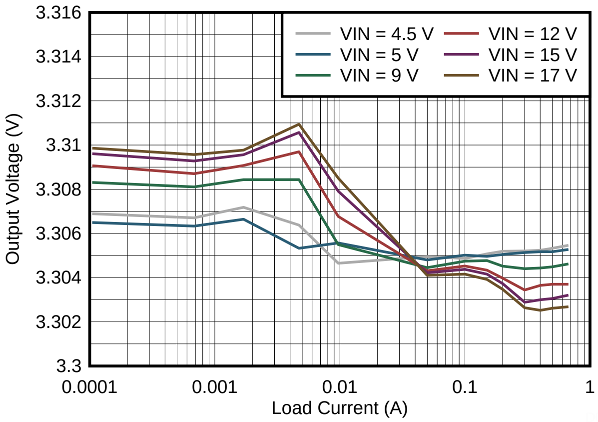


Figure 66. Line and Load Regulation V_{OUT} = 3.3 V

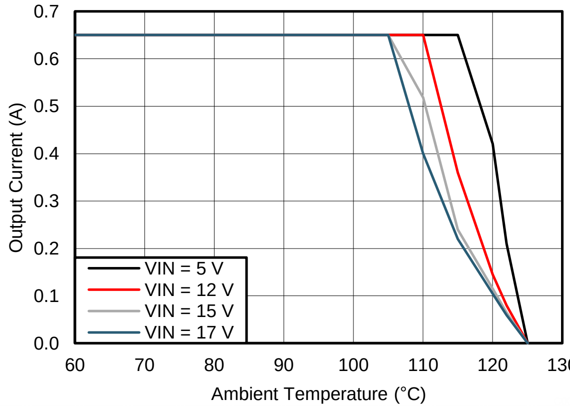


Figure 67. Thermal Derating for θ_{JA} = 47°C/W, V_{OUT} = 3.3 V

8.2.3.5 V_{OUT} = 5.0 V

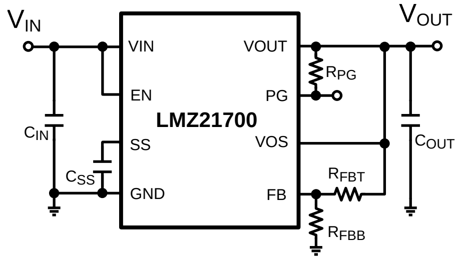


Figure 68. Typical Applications Circuit

COMPONENT VALUES FOR VOUT=5.0V			
C_{IN}	22µF	≥ 25V	X7R or X5R
C_{OUT}	22µF	≥ 10V	X7R or X5R
C_{SS}	3300pF	≥ 10V	X7R or X5R
R_{FBT}	232kΩ	1%	
R_{FBB}	44.2kΩ	1%	
R_{PG}	10kΩ	1%	

Figure 69. External Component Values (V_{OUT} = 5.0V)

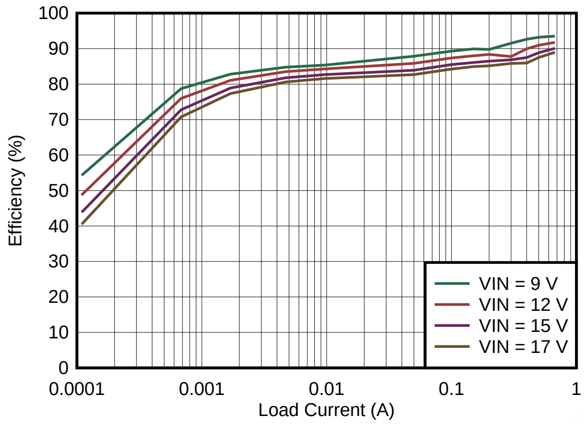


Figure 70. Efficiency V_{OUT} = 5.0 V

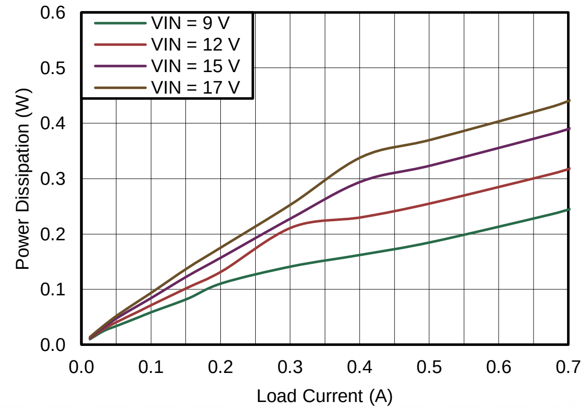


Figure 71. Power Dissipation V_{OUT} = 5.0 V

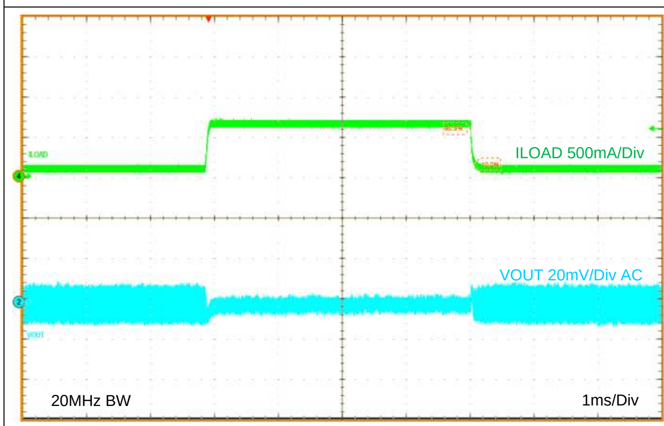


Figure 72. Load Transient V_{OUT} = 5.0 V

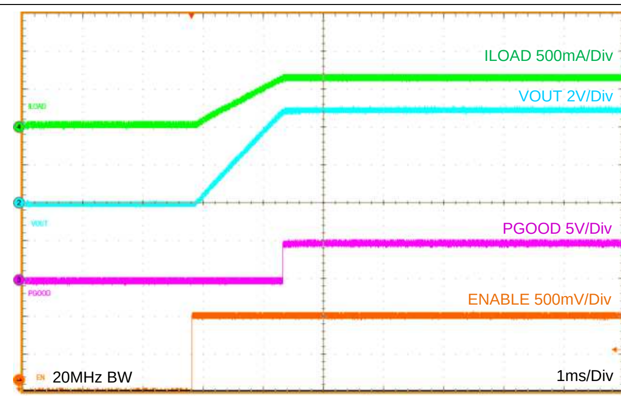


Figure 73. Startup V_{OUT} = 5.0 V

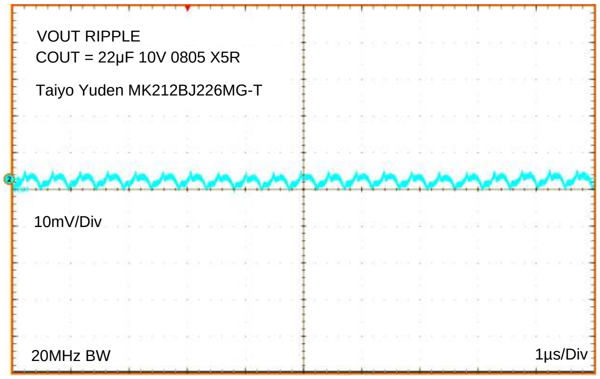


Figure 74. 20 MHz Oscilloscope Bandwidth Output Voltage Ripple V_{OUT} = 5.0 V

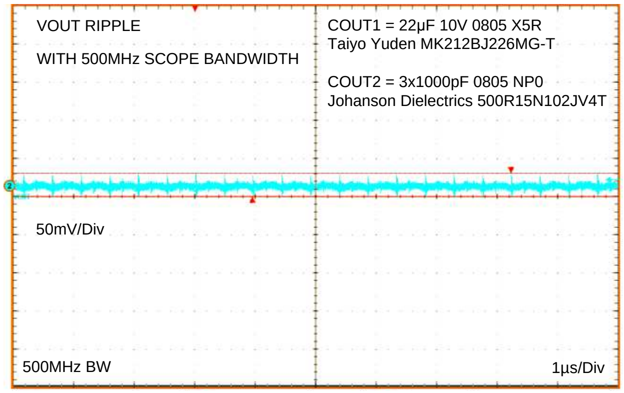


Figure 75. 500 MHz Oscilloscope Bandwidth, 3x1000 pF additional output capacitance Output Voltage Ripple and HF Noise V_{OUT} = 5.0 V

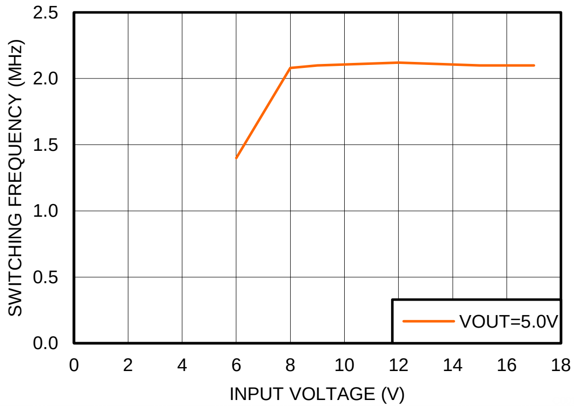


Figure 76. Typical Switching Frequency at 650 mA Load V_{OUT} = 5.0 V

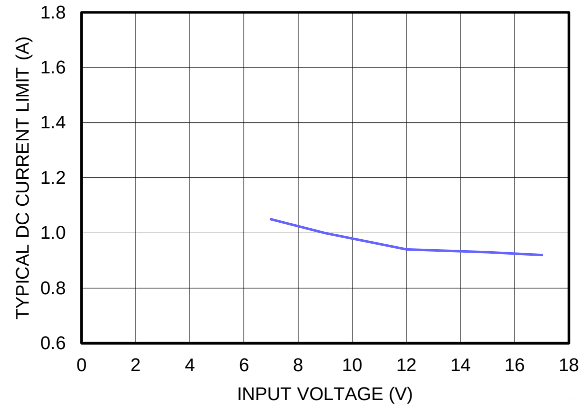


Figure 77. Typical Current Limit V_{OUT} = 5.0 V, T_A = 85 °C

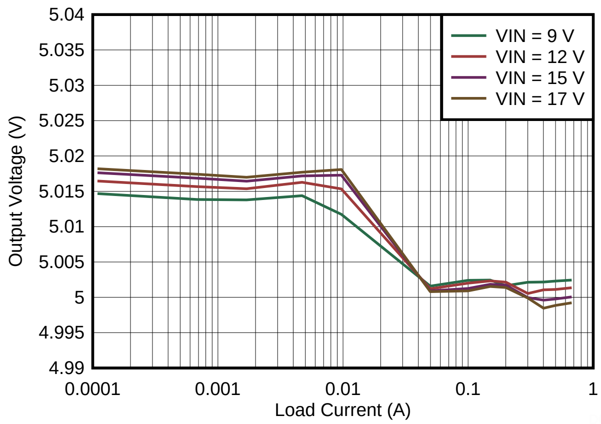


Figure 78. Line and Load Regulation V_{OUT} = 5.0 V

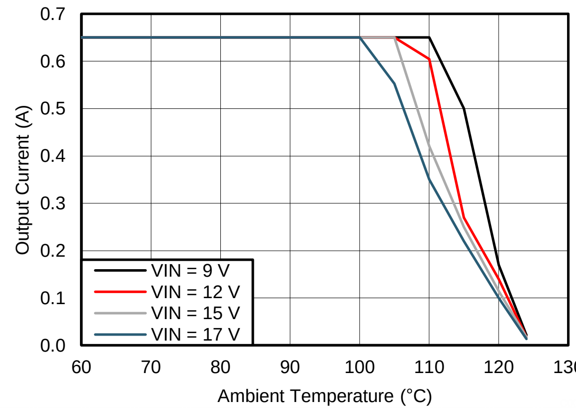


Figure 79. Thermal Derating for θ_{JA} = 47ºC/W, V_{OUT} = 5.0 V

8.3 Do's and Don'ts

- DO NOT exceed the Absolute Maximum Ratings.
- DO NOT exceed the Recommended Operating Conditions.
- DO NOT exceed the Handling Ratings.

- DO follow the Detailed Design Procedure.
- DO follow the PCB Layout Guidelines and Layout Example.
- DO follow the Power Supply Recommendations.
- DO visit the TI E2E Community Support Forum to have your questions answered and designs reviewed.

9 Power Supply Recommendations

9.1 Voltage Range

The voltage of the input supply must not exceed the Absolute Maximum Ratings and the Recommended Operating Conditions of the LMZ21700.

9.2 Current Capability

The input supply must be able to supply the required input current to the LMZ21700 converter. The required input current depends on the application's minimum required input voltage (V_{IN-MIN}), the required output power (V_{OUT} x $I_{OUT-MAX}$), and the converter efficiency (η).

$I_{IN} = V_{OUT} \times I_{OUT-MAX} / (V_{IN-MIN} \times \eta)$

For example, for a design with 10 V minimum input voltage, 5 V output, and 0.5 A maximum load, considering 90 % conversion efficiency, the required input current is 0.278 A.

9.3 Input Connection

Long input connection cables can cause issues with the normal operation of any buck converter.

9.3.1 Voltage Drops

Using long input wires to connect the supply to the input of any converter adds impedance in series with the input supply. This impedance can cause a voltage drop at the VIN pin of the converter when the output of the converter is loaded. If the input voltage is near the minimum operating voltage, this added voltage drop can cause the converter to drop out or reset. If long wires are used during testing, it is recommended to add some bulk (i.e. electrolytic) capacitance at the input of the converter.

9.3.2 Stability

The added inductance of long input cables together with the ceramic (and low ESR) input capacitor can result in an under damped RLC network at the input of the Buck converter. This can cause oscillations on the input and instability. If long wires are used, it is recommended to add some electrolytic capacitance in parallel with the ceramic input capacitor. The electrolytic capacitor's ESR will improve the damping.

Use an electrolytic capacitor with $C_{ELECTROLYTIC} \geq 4 \times C_{CERAMIC}$ and $ESR_{ELECTROLYTIC} \approx \sqrt{} (L_{CABLE} / C_{CERAMIC})$

For example, two cables (one for V_{IN} and one for GND), each 1 meter (~ 3 ft) long with ~1.0 mm diameter (18 AWG), placed 1 cm (~0.4 in) apart will form a rectangular loop resulting in about 1.2 µH of inductance. The inductance in this example can be decreased to almost half if the input wires are twisted. Based on a 22 µF ceramic input capacitor, the recommended parallel $C_{ELECTROLYTIC}$ is ≥ 88 µF. Using a 100 µF capacitor will be sufficient. The recommended $ESR_{ELECTROLYTIC} \approx$ 0.23 Ω or larger, based on about 1.2 µH of inductance and 22 µF of ceramic input capacitance.

See application note SNVA489C for more details on input filter design.

10 Layout

10.1 Layout Guidelines

The PCB layout is critical for the proper operation of any DC-DC switching converter. Although using modules can simplify the PCB layout process, care should still be taken to minimize the inductance in the high di/dt loops and to protect sensitive nodes. The following guidelines should be followed when designing a board layout with the LMZ21700:

10.1.1 Minimize the High di/dt Loop Area

The input capacitor, the V_{IN} terminal, and the GND terminal of the LMZ21700 form a high di/dt loop. Place the input capacitor as close as possible to the V_{IN} and GND terminals of the module IC. This minimizes the area of the high di/dt loop and results in lower inductance in the switching current path. Lower inductance in the switching current path translates to lower voltage spikes on the internal switch node and lower noise on the output voltage. Make the copper traces between the input capacitor and the V_{IN} and GND terminals wide and short for better current handling and minimized parasitic inductance.

10.1.2 Protect the Sensitive Nodes in the Circuit

The feedback node is a sensitive circuit which can pick up noise. Make the feedback node as small as possible. This can be achieved by placing the feedback divider as close as possible to the IC. Use thin traces to the feedback pin in order to minimize the parasitic capacitance to other nodes. The feedback network carries very small current and thick traces are not necessary. Another sensitive node to protect is the VOS pin. Use a thin and short trace from the V_{OUT} terminal of the output capacitor to the VOS pin. The VOS pin is right next to the GND terminal. For very noisy systems, a small (0402 or 0201) 0.1 µF capacitor can be placed from VOS to GND to filter high frequency noise on the VOS line.

10.1.3 Provide Thermal Path and Shielding

Using the available layers in the PCB can help provide additional shielding and improved thermal performance. Large unbroken GND copper areas provide good thermal and return current paths. Flood unused PCB area with GND copper. Use thermal vias to connect the GND copper between layers.

The required board area for proper thermal dissipation can be estimated using the power dissipation curves for the desired output voltage and the package thermal resistance vs. board area curve. Refer to the power dissipation graphs in the *Typical Characteristics* section. Using the power dissipation (P_{DISS}) for the designed input and output voltage and the max operating ambient temperature T_A for the application, estimate the required thermal resistance $R_{\theta JA}$ with the following expression.

$$R_{\theta JA\ -\ REQUIRED} \leq (125\ ^{o}C - T_A) / P_{DISS} \quad (8)$$

Then use Figure 80 to estimate the board copper area required to achieve the calculated thermal resistance.

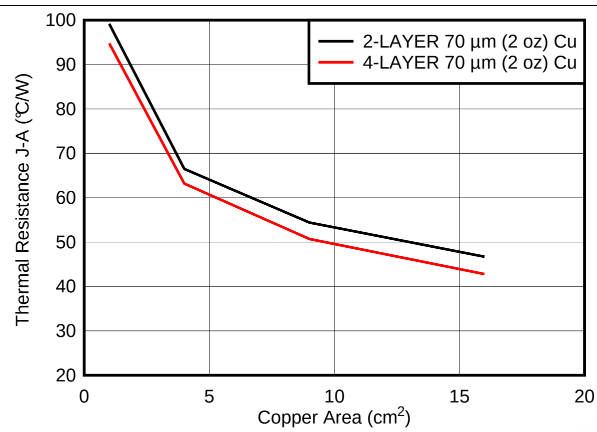


Figure 80. Package Thermal Resistance vs. Board Copper Area, No Air Flow

Layout Guidelines (continued)

For example, for a design with 17 V input and 5 V output and 0.65 A load the power dissipation according to Figure 7 is 0.43 W.

For 85 °C ambient temperature, the $R_{\theta JA\text{-}REQUIRED}$ is ≤ (125 °C - 85 °C) / 0.43 W, or ≤ 93 °C/W. Looking at Figure 80 the minimum copper area required to achieve this thermal resistance with a 4-layer board and 70 µm (2 oz) copper is approximately 1 cm^2.

10.2 Layout Example

The following example is for a 4-layer board. Layers 2 and 4 provide additional shielding and thermal path. If a 2-layer board is used, apply the Layer 1 and Layer 3 copper patterns for the top and bottom layers, respectively.

Layout Example (continued)

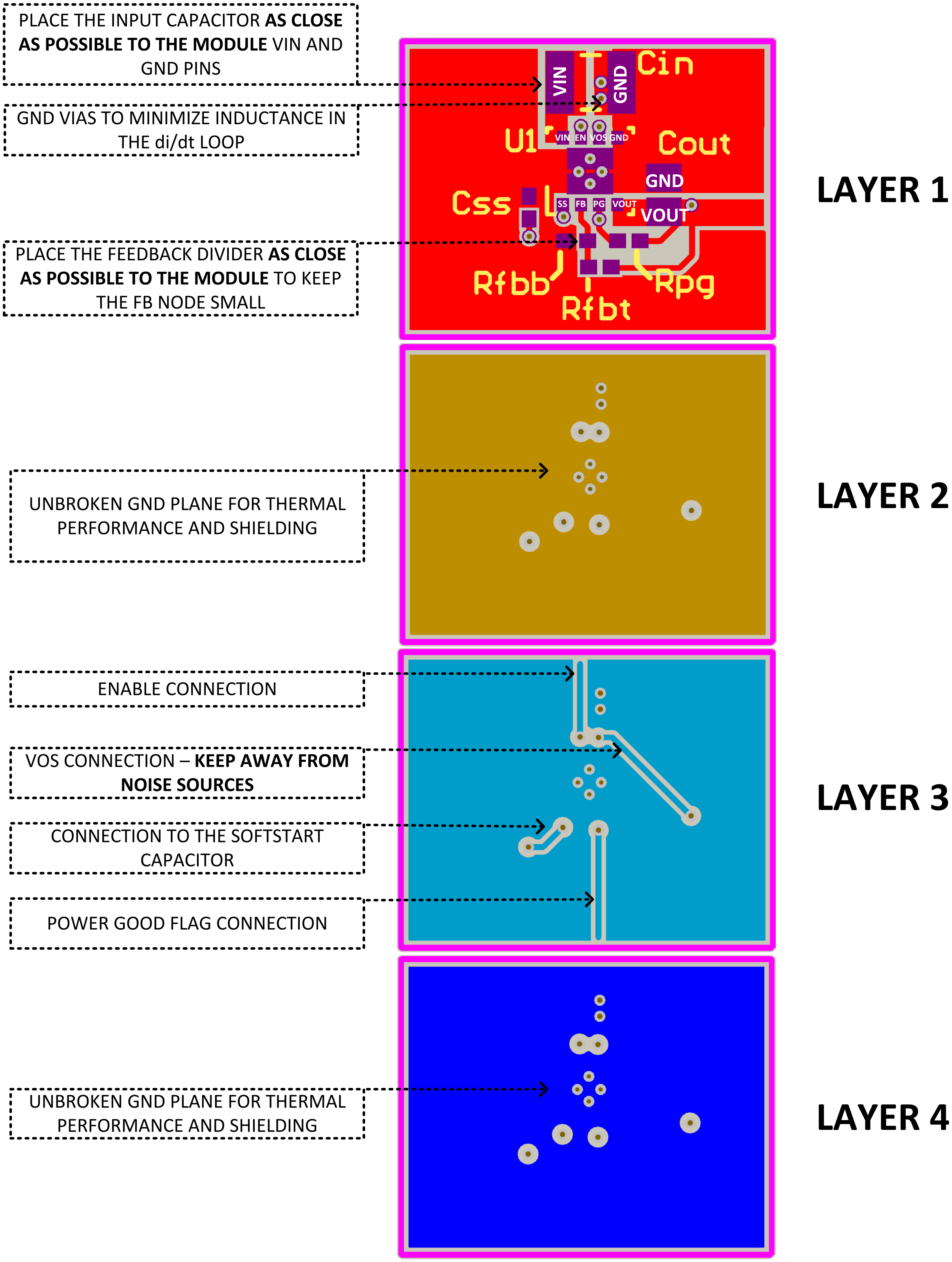


Figure 81. Layout example

Layout Example (continued)

10.2.1 High Density Layout Example for Space Constrained Applications

10.2.1.1 35 mm² Solution Size (Single Sided)

The following layout example uses 0805 case size components for the input and output capacitors and 0402 case size components for the rest of the passives.

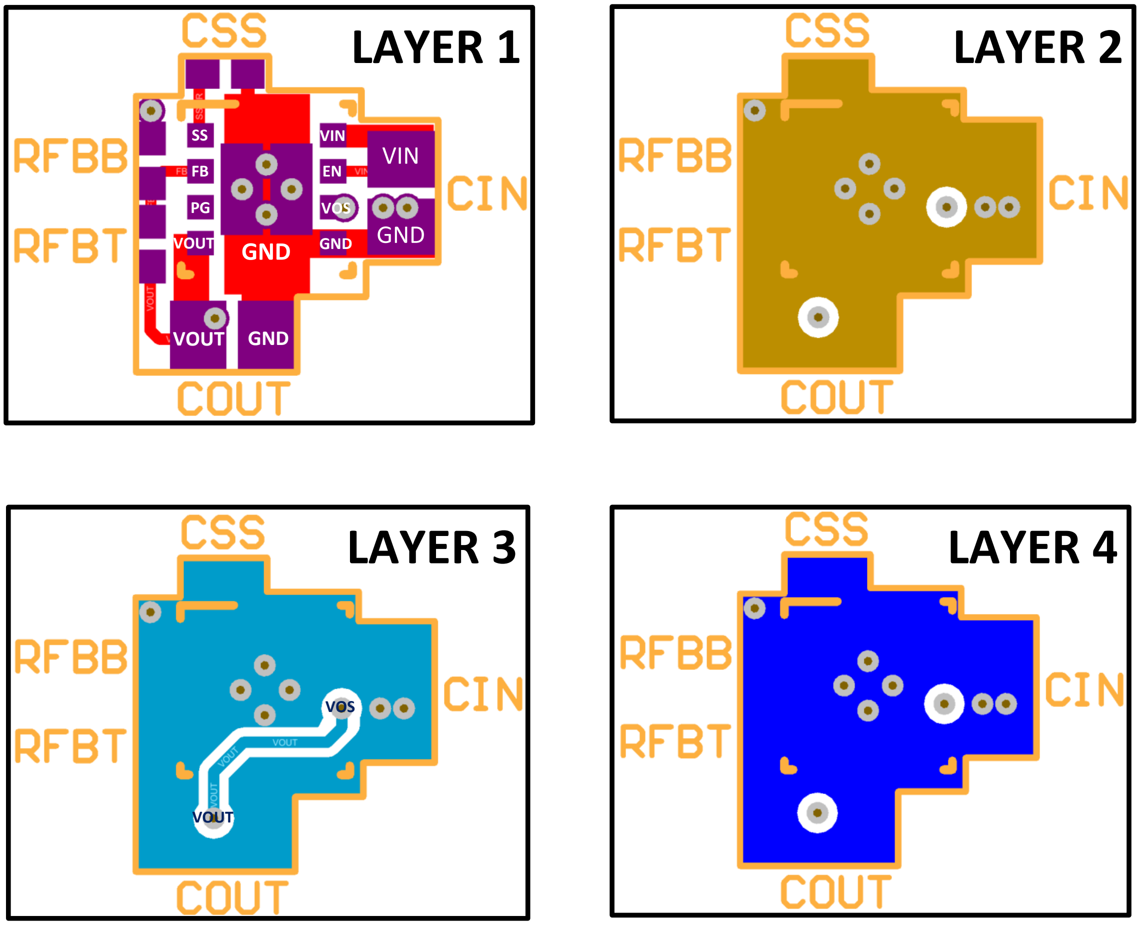


Figure 82. 35mm² Solution Size (Single Sided)

11 器件和文档支持

11.1 器件支持

如需问题解答和设计检查，请访问德州仪器 (TI) E2E 社区支持论坛。

11.2 开发支持

11.2.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 LMZ21700 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

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WEBENCH, SIMPLE SWITCHER are registered trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 术语表

SLYZ022 — *TI 术语表*。

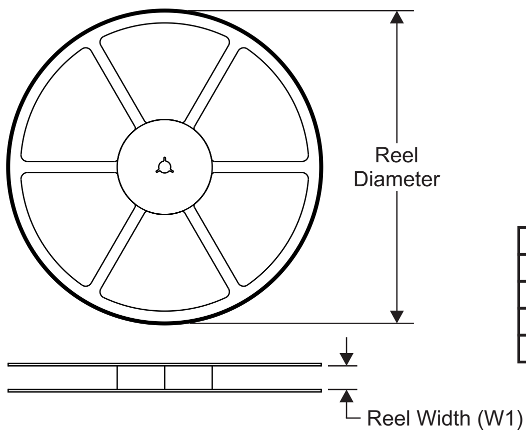
这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

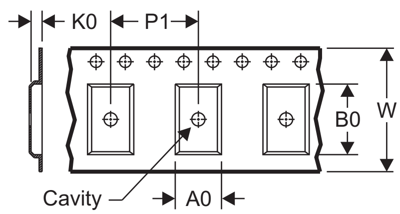
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

12.1 Tape and Reel Information

REEL DIMENSIONS

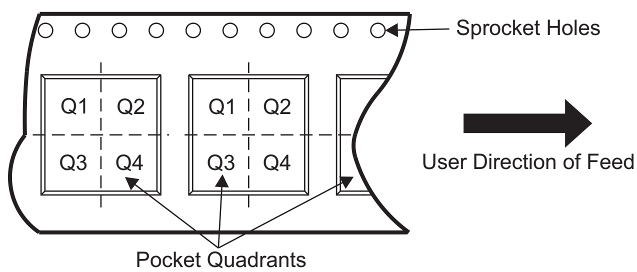


TAPE DIMENSIONS



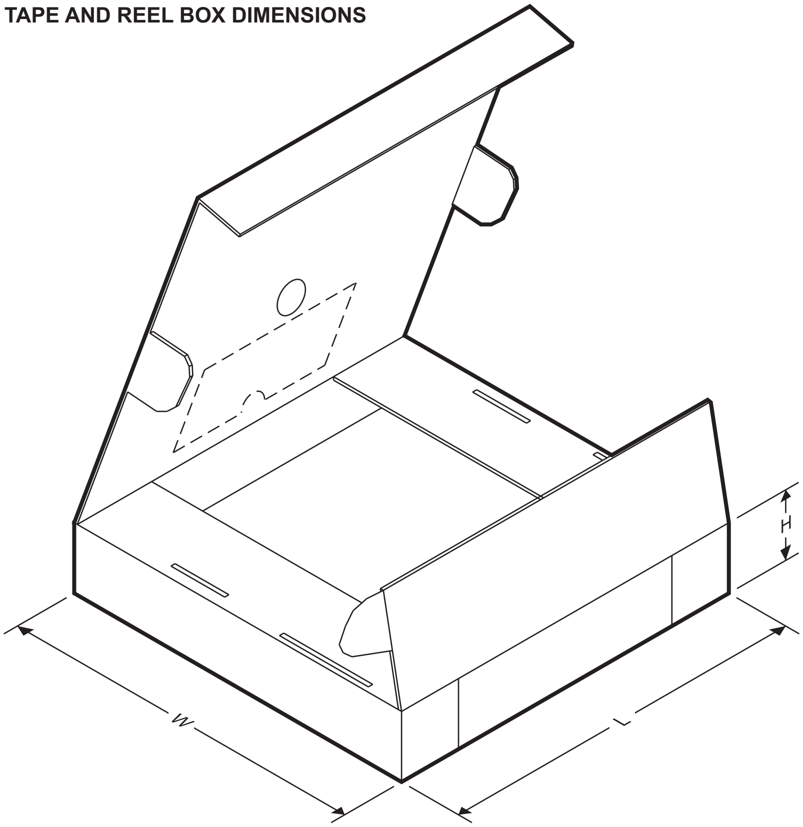
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ21700SILR	uSiP	SIL	8	3000	330.0	12.4	3.75	3.75	2.2	8.0	12.0	Q2
LMZ21700SILT	uSiP	SIL	8	250	178.0	13.2	3.75	3.75	2.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ21700SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
LMZ21700SILT	uSiP	SIL	8	250	223.0	194.0	35.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ21700SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	7485 1700 7485 D9
LMZ21700SILR.B	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	7485 1700 7485 D9
LMZ21700SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	7485 1700 7485 D9
LMZ21700SILT.B	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	7485 1700 7485 D9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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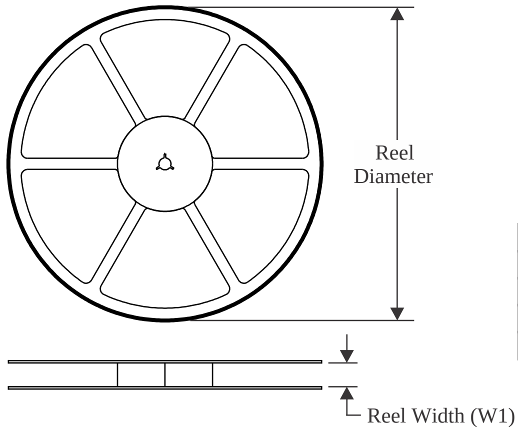
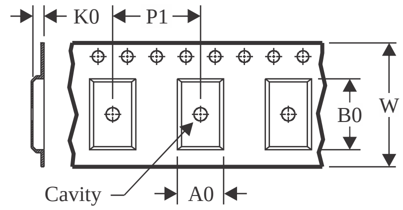
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



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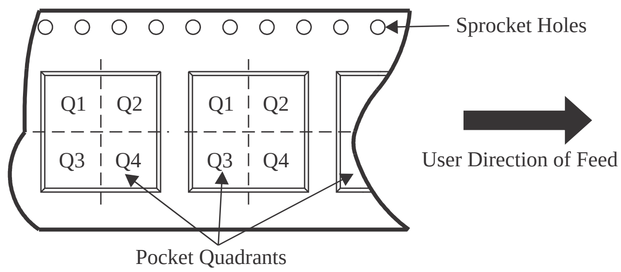
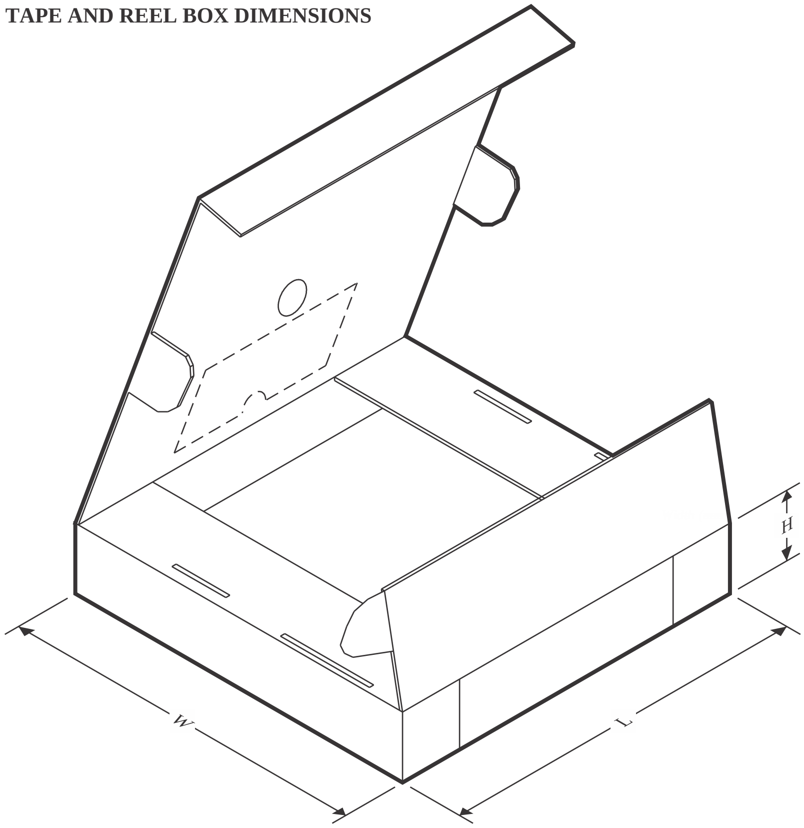


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ21700SILR	uSiP	SIL	8	3000	330.0	12.4	3.75	3.75	2.2	8.0	12.0	Q2
LMZ21700SILT	uSiP	SIL	8	250	178.0	13.2	3.75	3.75	2.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ21700SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
LMZ21700SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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