LMV7219 7-ns 2.7-V to 5-V Comparator with Rail-to-Rail Output

1 Features

- (V_S = 5 V, T_A = 25°C, Typical Values Unless Specified)
- Propagation Delay 7 ns
- Low Supply Current 1.1 mA
- Input Common Mode Voltage Range Extends 200 mv Below Ground
- Ideal for 2.7-V and 5-V Single Supply Applications
- Internal Hysteresis Ensures Clean Switching
- Fast Rise and Fall Time 1.3 ns
- Available in Space-saving Packages: SC-70 and SOT-23
- Supports 105°C PCB Temperature

2 Applications

- Portable and Battery-powered Systems
- Scanners
- Set Top Boxes
- High Speed Differential Line Receiver
- Window Comparators
- Zero-crossing Detectors
- High-speed Sampling Circuits

3 Description

The LMV7219 is a low-power, high-speed comparator with internal hysteresis. The LMV7219 operating voltage ranges from 2.7 V to 5 V with push-pull rail-to-rail output. This device achieves a 7-ns propagation delay while consuming only 1.1 mA of supply current at 5 V.

The LMV7219 inputs have a common mode voltage range that extends 200 mV below ground, allowing ground sensing. The internal hysteresis ensures clean output transitions even with slow-moving inputs signals.

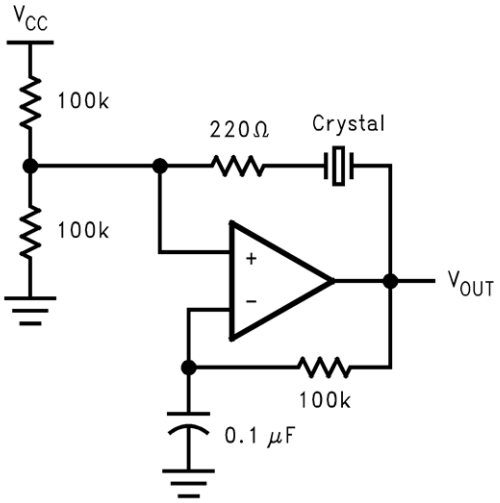
The LMV7219 is available in the SC-70 and SOT-23 packages, which are ideal for systems where small size and low power are critical.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV7219	SC-70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.88 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Copyright © 2016, Texas Instruments Incorporated

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 **Features** ... 1
2 **Applications** ... 1
3 **Description** ... 1
4 **Revision History** ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics 2.7 V ... 5
6.6 Electrical Characteristics 5 V ... 6
6.7 Typical Performance Characteristics ... 8
7 **Detailed Description** ... 11
7.1 Overview ... 11
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 11
8 **Application and Implementation** ... 12
8.1 Application Information ... 12
8.2 Typical Application ... 12
9 **Power Supply Recommendations** ... 16
10 **Layout** ... 16
10.1 Layout Guidelines ... 16
10.2 Layout Example ... 17
11 **Device and Documentation Support** ... 18
11.1 Documentation Support ... 18
11.2 Receiving Notification of Documentation Updates 18
11.3 Community Resources ... 18
11.4 Trademarks ... 18
11.5 Electrostatic Discharge Caution ... 18
12 **Mechanical, Packaging, and Orderable Information** ... 18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2016) to Revision I	Page
• Added Supports 105°C PCB Temperature to Features List	1
• Changed Operating Temperature to Ambient Temperature	4
• Added Junction Temperature of 125 °C	4
• Added PCB Temperature of 105 °C	4
• Added T_{PCB} ≤ 105°C throughout Electrical Tables	5

Changes from Revision G (January 2015) to Revision H	Page
• Changed "Infrared or Convection (20 sec)" from 235 °C	4
• Added thermal data for SOT23 and SC70 packages	4

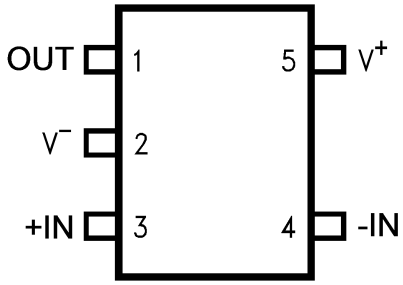
Changes from Revision F (April 2013) to Revision G	Page
• Added, updated, or renamed the following sections: Device Information Table, *Pin Configurations and Functions; Specifications; Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information*	1
• Changed from "transient response" to "eliminate possible output chatter" in *Circuit Layout and Bypassing*	16

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	1

Copyright © 2000–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

5-Pin SC-70 and SOT-23 Packages DCK and DBV (Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Output
2	V^-	I	Negative Supply
3	+IN	I	Non-inverting input
4	-IN	I	Inverting input
5	V^+	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1][2]

		MIN	MAX	UNIT
Differential input voltage			± Supply Voltage	
Output short circuit duration			See[3]	
Supply voltage (V^+ - V^-)			5.5	V
Soldering information	Infrared or Convection (20 sec)		260	°C
	Wave Soldering (10 sec)		260 (lead temp)	°C
Voltage at input/output pins			(V^+) + 0.4 (V^-) − 0.4	V
Current at input pin[4]			±10	mA
Maximum junction temperature			150	°C
Storage temperature		−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±150 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltages (V^+ - V^-)	2.7	5	V
Ambient Temperature[1]	−40	+85	°C
Junction Temperature		125	°C
PCB Temperature		105	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.4 Thermal Information

THERMAL METRIC[1]		LMV7219 DBV (SOT23) 5 PINS	LMV7219 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	209	296	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	170	132	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68	76	°C/W
ψ_{JT}	Junction-to-top characterization parameter	52	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2000–2016, Texas Instruments Incorporated

Thermal Information (continued)

THERMAL METRIC[1]		LMV7219 DBV (SOT23) 5 PINS	LMV7219 DCK (SC70) 5 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	68	75	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics 2.7 V

Unless otherwise specified, all limits ensured for T_J = 25°C, V_{CM} = V^+/2, V^+ = 2.7 V, V^- = 0 V, C_L = 10 pF and R_L > 1MΩ to V^-.

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX[2]	UNIT
V_{OS}	Input offset voltage				1	6	mV
		−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C				8	
I_B	Input bias current				450	950	nA
		−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C				2000	
I_{OS}	Input offset current				50	200	nA
		−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C				400	
CMRR	Common mode rejection ratio	0 V < V_{CM} < 1.50 V		62	85		dB
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	55			
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V		65	85		dB
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	55			
V_{CM}	Input common-voltage range	CMRR > 50 dB		V_{CC} −1.2	V_{CC} −1		V
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	V_{CC} −1.3			
					−0.2	−0.1	
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			0	
V_O	Output swing high	I_L = 4 mA, V_{ID} = 500 mV		V_{CC} −0.3	V_{CC} −0.22		V
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	V_{CC} −0.4			
		I_L = 0.4 mA, V_{ID} = 500 mV		V_{CC} −0.05	V_{CC} −0.02		
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	V_{CC} −0.15			
	Output swing low	I_L = −4 mA, V_{ID} = −500 mV			130	200	mV
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			300	
		I_L = −0.4 mA, V_{ID} = −500 mV			15	50	
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			150	
I_{SC}	Output short circuit current	Sourcing, V_O = 0 V[3]			20		mA
		Sinking, V_O = 2.7 V[3]			20		
I_S	Supply current	No Load			0.9	1.6	mA
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			2.2	
V_{HYST}	Input hysteresis voltage	See[4]			7		mV
V_{TRIP^+}	Input referred positive trip point	(see Figure 19)			3	8	mV

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{trip^+} and V_{trip^-}, while the hysteresis voltage is the difference of these two.

Copyright © 2000–2016, Texas Instruments Incorporated

Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V_{CM} = V^+/2, V^+ = 2.7 V, V^- = 0 V, C_L = 10 pF and R_L > 1MΩ to V^-.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX (2)	UNIT
V_{TRIP^-}	Input referred negative trip point	(see Figure 19)	−8	−4		mV
t_{PD}	Propagation delay	Overdrive = 5 mV, V_{CM} = 0V (5)		12		ns
		Overdrive = 15 mV, V_{CM} = 0 V (5)		11		
		Overdrive = 50 mV, V_{CM} = 0 V (5)		10	20	
t_{SKEW}	Propagation delay skew	See (6)		1		ns
t_r	Output rise time	10% to 90%		2.5		ns
t_f	Output fall time	90% to 10%		2		ns

(5) Propagation delay measurements made with 100 mV steps. Overdrive is measured relative to V_{Trip}.
(6) Propagation Delay Skew is defined as absolute value of the difference between t_{PDLH} and t_{PDHL}.

6.6 Electrical Characteristics 5 V

Unless otherwise specified, all limits ensured for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5 V, V^- = 0 V, C_L = 10 pF and R_L > 1 MΩ to V^-.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX (2)	UNIT
V_{OS}	Input offset voltage				1	6	mV
		−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C				8	
I_B	Input bias current				500	950	nA
		−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C				2000	
I_{OS}	Input offset current				50	200	nA
		−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C				400	
CMRR	Common mode rejection ratio	0 V < V_{CM} < 3.8 V		65	85		dB
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	55			
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V		65	85		dB
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	55			
V_{CM}	Input common-mode voltage range	CMRR > 50 dB		V_{CC} −1.2	V_{CC} −1		V
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	V_{CC} −1.3			
					−0.2	−0.1	V
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			0	
V_O	Output swing high	I_L = 4 mA, V_{ID} = 500 mV		V_{CC} −0.2	V_{CC} −0.13		V
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	V_{CC} −0.3			
		I_L = 0.4 mA, V_{ID} = 500 mV		V_{CC} −0.05	V_{CC} −0.02		
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	V_{CC} −0.15			
	Output swing low	I_L = −4 mA, V_{ID} = −500 mV			80	180	mV
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			280	
		I_L = −0.4 mA, V_{ID} = −500 mV			10	50	
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			150	

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

Copyright © 2000–2016, Texas Instruments Incorporated

Electrical Characteristics 5 V (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5 V, V^- = 0 V, C_L = 10 pF and R_L > 1 MΩ to V^-.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX (2)	UNIT
I_{SC}	Output short circuit current	Sourcing, V_O = 0 V (3)		30	68		mA
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	20			
		Sinking, V_O = 5 V (3)		30	65		
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C	20			
I_S	Supply current	No Load			1.1	1.8	mA
			−40°C ≤ T_J ≤ +85°C and T_{PCB} ≤ 105°C			2.4	
V_{HYST}	Input hysteresis voltage	See (4)			7.5		mV
V_{Trip^+}	Input referred positive trip point	(See Figure 19)			3.5	8	mV
V_{Trip^-}	Input referred negative trip point	(See Figure 19)		−8	−4		mV
t_{PD}	Propagation delay	Overdrive = 5 mV, V_{CM} = 0 V (5)			9		ns
		Overdrive = 15 mV, V_{CM} = 0 V (5)			8	20	
		Overdrive = 50 mV, V_{CM} = 0 V (5)			7	19	
t_{SKEW}	Propagation delay skew	See (6)			0.4		ns
t_r	Output rise time	10% to 90%			1.3		ns
t_f	Output fall time	90% to 10%			1.25		ns

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{trip^+} and V_{trip^-}, while the hysteresis voltage is the difference of these two.
(5) Propagation delay measurements made with 100 mV steps. Overdrive is measured relative to V_{Trip}.
(6) Propagation Delay Skew is defined as absolute value of the difference between t_{PDLH} and t_{PDHL}.

Copyright © 2000–2016, Texas Instruments Incorporated

6.7 Typical Performance Characteristics

Unless otherwise specified, V_S = 5 V, C_L = 10 pF, T_A = 25°C

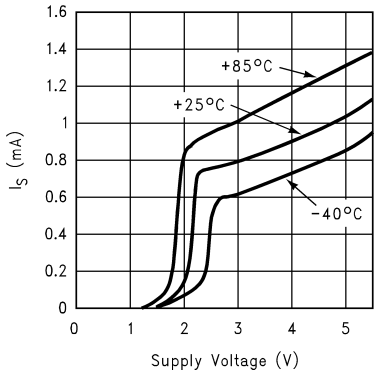


Figure 1. Supply Current vs. Supply Voltage

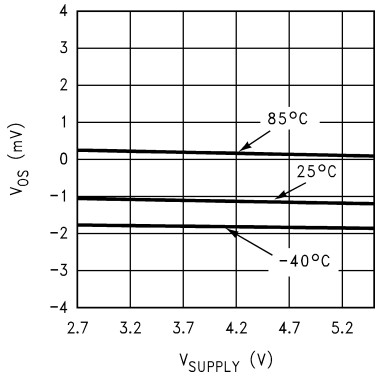


Figure 2. V_{OS} vs. Supply Voltage

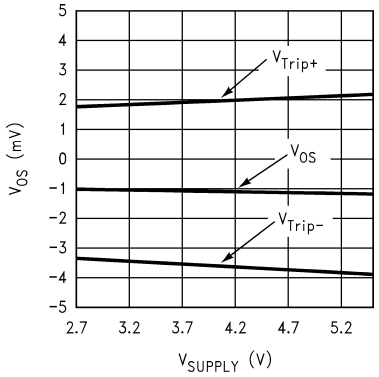
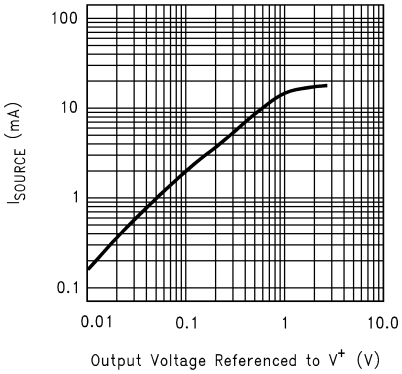
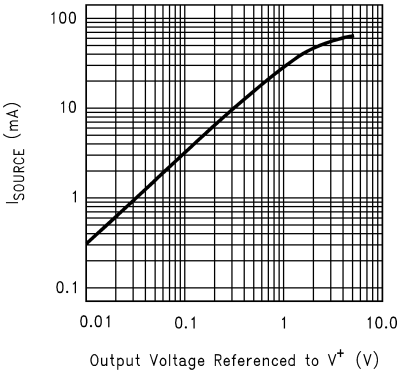


Figure 3. Input Offset and Trip Voltage vs. Supply Voltage



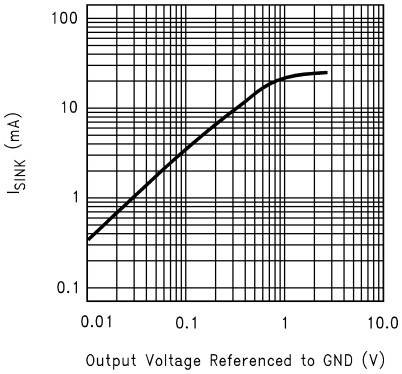
V_S = 2.7 V

Figure 4. Sourcing Current vs. Output Voltage



V_S = 5 V

Figure 5. Sourcing Current vs. Output Voltage



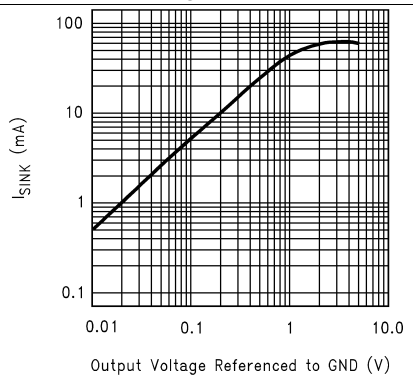
V_S = 2.7 V

Figure 6. Sinking Current vs. Output Voltage

Copyright © 2000–2016, Texas Instruments Incorporated

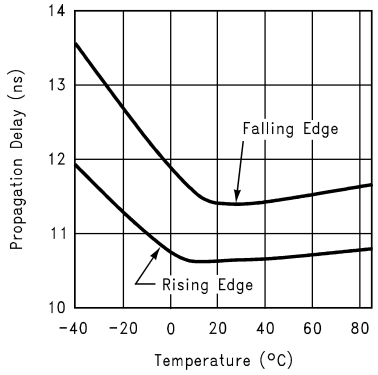
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 5 V, C_L = 10 pF, T_A = 25°C



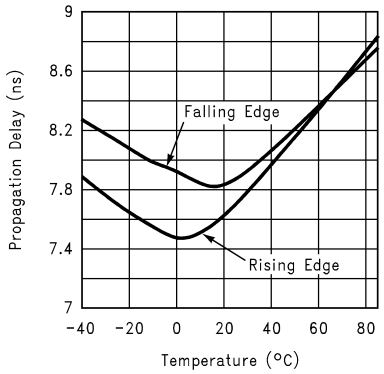
V_S = 5 V

Figure 7. Sinking Current vs. Output Voltage



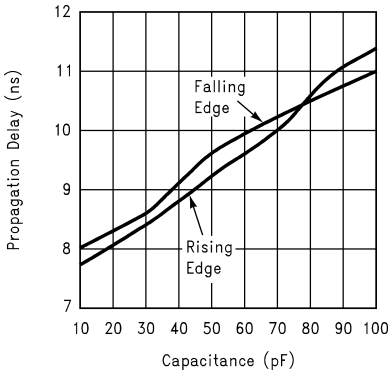
V_S = 2.7 V
V_{OD} = 15 mV

Figure 8. Propagation Delay vs. Temperature



V_S = 5V
V_{OD} = 15 mV

Figure 9. Propagation Delay vs. Temperature



V_S = 5 V
V_{OD} = 15 mV

Figure 10. Propagation Delay vs. Capacitive Load

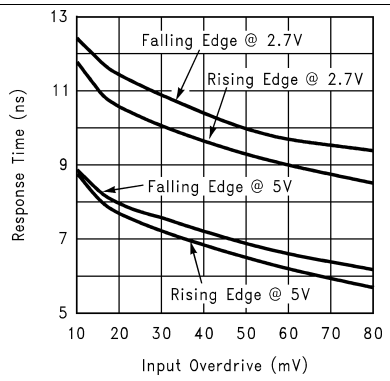
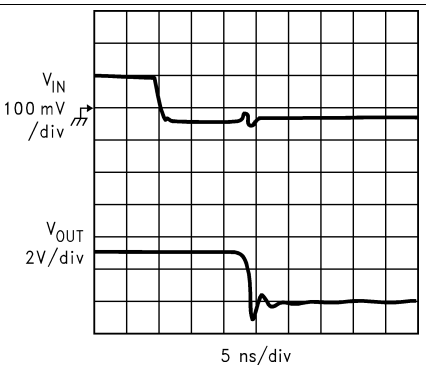


Figure 11. Propagation Delay vs. Input Overdrive

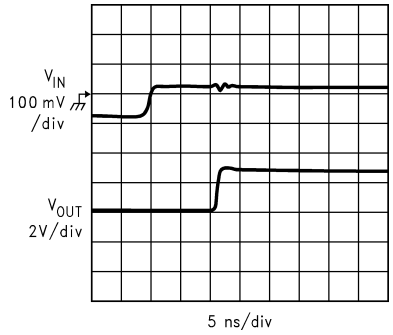


V_S = 2.7 V
C_L = 10 pF
V_{OD} = 15 mV

Figure 12. Propagation Delay (t_{PD^-})

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 5 V, C_L = 10 pF, T_A = 25°C



V_S = 2.7 V
C_L = 10 pF
V_{OD} = 15 mV

Figure 13. Propagation Delay (t_{PD}^+)

Copyright © 2000–2016, Texas Instruments Incorporated

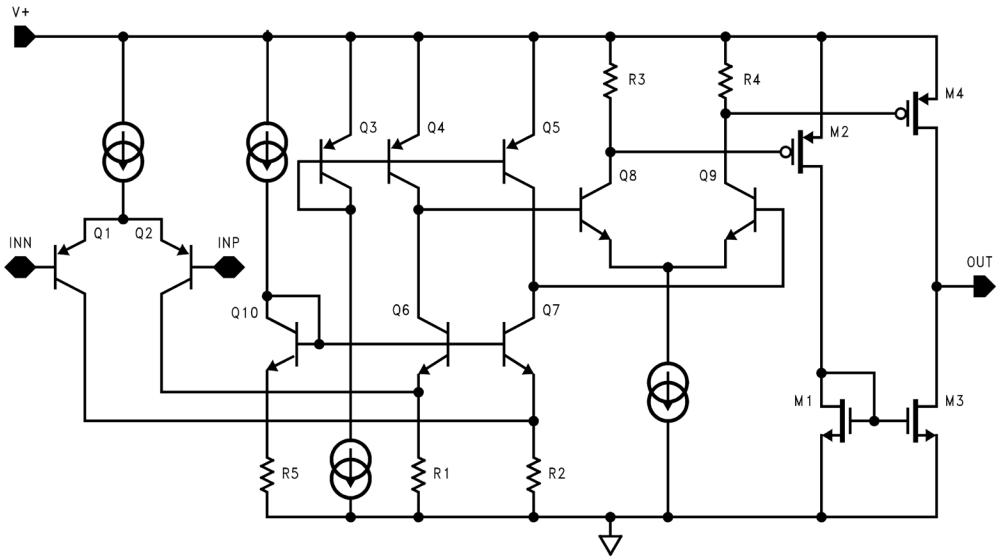
7 Detailed Description

7.1 Overview

LMV7219 is a single supply comparator with internal hysteresis, 7 ns of propagation delay and only 1.1 mA of supply current.

The LMV7219 has a typical input common mode voltage range of −0.2 V below the ground to 1 V below V_{CC}. The differential input stage is a pair of PNP transistors, therefore, the input bias current flows out of the device. If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on, resulting in an increase of input bias current.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

7.4 Device Functional Modes

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damages to the input stage.

The LMV7219 has a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing high output sinking or sourcing current during the transition. After the transition, the output current decreases and the supply current settles back to about 1.1 mA at 5 V, thus conserving power consumption.

Most high-speed comparators oscillate when the voltage of one of the inputs is close to or equal to the voltage on the other input due to noise or undesirable feedback. The LMV7219 has 7 mV of internal hysteresis to counter parasitic effects and noise. The hysteresis does not change significantly with the supply voltages and the common mode input voltages as reflected in the specification table.

8 Application and Implementation

NOTE

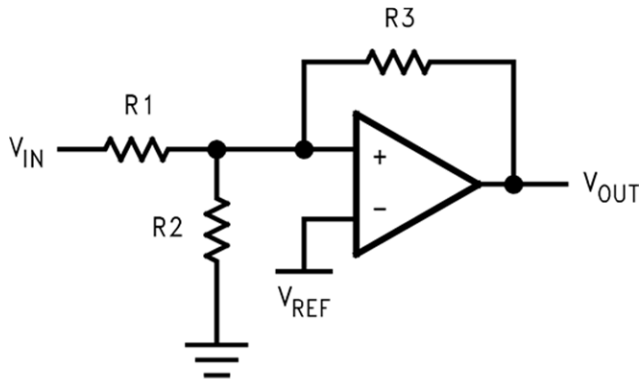
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section explains in detail how to manipulate the hysteresis voltage of the LMV7219. Detailed expressions are provided along with practical considerations for designing hysteresis.

8.2 Typical Application

Figure 14 shows the typical method of adding external hysteresis to a comparator. The positive feedback is responsible for shifting the comparator trip point depending on the state of the output.



Copyright © 2016, Texas Instruments Incorporated

Figure 14. Additional Hysteresis

8.2.1 Design Requirements

The internal hysteresis creates two trip points, one for the rising input voltage and one for the falling input voltage, as shown in Figure 19. The difference between the trip points is the hysteresis. With internal hysteresis, when the comparator's input voltages are equal, the hysteresis effectively causes one comparator-input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The fixed internal hysteresis eliminates these resistors.

8.2.2 Detailed Design Procedure

8.2.2.1 Additional Hysteresis

If additional hysteresis is desired, this can be done with the addition of three resistors using positive feedback, as shown in Figure 14. The positive feedback method slows the comparator response time. Calculate the resistor values as follows:

1. Select R3. The current through R3 should be greater than the input bias current to minimize errors. The current through R3 (I_F) at the trip point is (V_{REF} - V_{OUT}) /R3. Consider the two possible output states when solving for R3, and use the smaller of the two resulting resistor values. The two formulas are:

$$R3 = V_{REF}/I_F \quad (1)$$

When V_{OUT} = 0:

Copyright © 2000–2016, Texas Instruments Incorporated

Typical Application (continued)

$$R3 = V_{CC} - V_{REF} / I_F \quad (2)$$

When $V_{OUT} = V_{CC}$:

2. Choose a hysteresis band required (V_{HB}).

3. Calculate R1, where R1 = R3 X(V_{HB}/V_{CC})

4. Choose the trip point for V_{IN} rising. This is the threshold voltage (V_{THR}) at which the comparator switches from low to high as V_{IN} rises about the trip point.

5. Calculate R2 as follows:

$$R_2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R_1}\right) - \frac{1}{R_1} - \frac{1}{R_3}} \quad (3)$$

6. Verify the trip voltage and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R_1 \times \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)$$

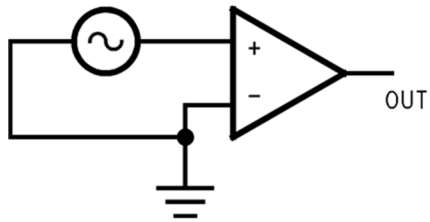
$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R_1 \times V_{CC}}{R_3}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF} \quad (4)$$

This method is recommended for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to affect the bias string and adjustment of R1 may be also required.

8.2.2.2 Zero-Crossing Detector

The inverting input is connected to ground and the non-inverting input is connected to 100mVp-p signal. As the signal at the non-inverting input crosses 0 V, the comparator's output Changes State.



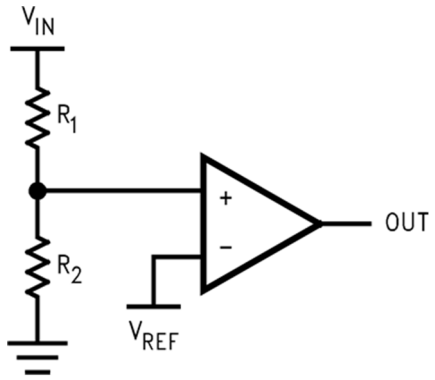
Copyright © 2016, Texas Instruments Incorporated

Figure 15. Zero-Crossing Detector

8.2.2.3 Threshold Detector

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. The non-inverting input is connected to the input. As the input passes the V_{REF} threshold, the comparator's output changes state.

Typical Application (continued)

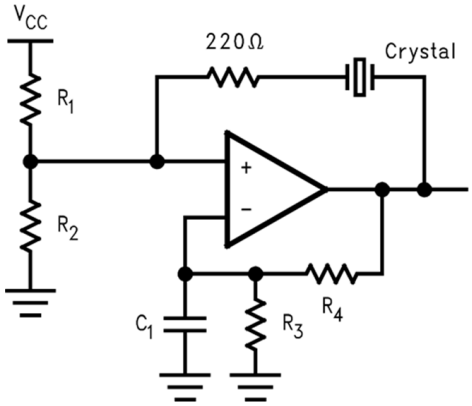


Copyright © 2016, Texas Instruments Incorporated

Figure 16. Threshold Detector

8.2.2.4 Crystal Oscillator

A simple crystal oscillator using the LMV7219 is shown in Figure 17. Resistors R1 and R2 set the bias point at the comparator's non-inverting input. Resistors R3, R4 and C1 sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.



Copyright © 2016, Texas Instruments Incorporated

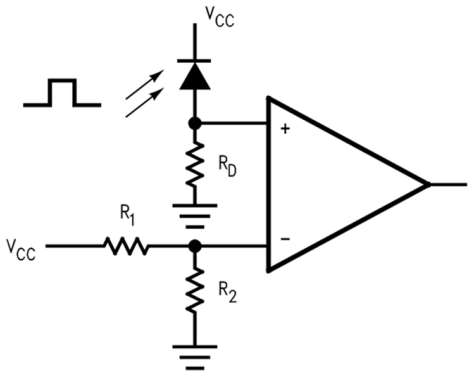
Figure 17. Crystal Oscillator

8.2.2.5 IR Receiver

The LMV7219 is an ideal candidate to be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across RD. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions.

Copyright © 2000–2016, Texas Instruments Incorporated

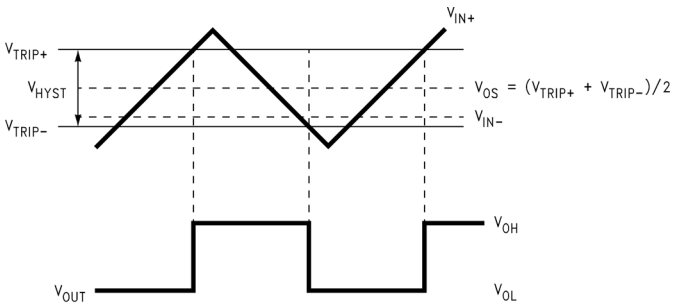
Typical Application (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 18. IR Receiver

8.2.3 Application Curve



Copyright © 2016, Texas Instruments Incorporated

Figure 19. Input and Output Waveforms, Non-Inverting Input Varied

9 Power Supply Recommendations

The LMV7219 can operate off a single supply or with dual supplies as long as the input CM voltage range (V_{CM}) has the required headroom to the positive rail V+. The input range extends to slightly below V- voltage. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

10 Layout

10.1 Layout Guidelines

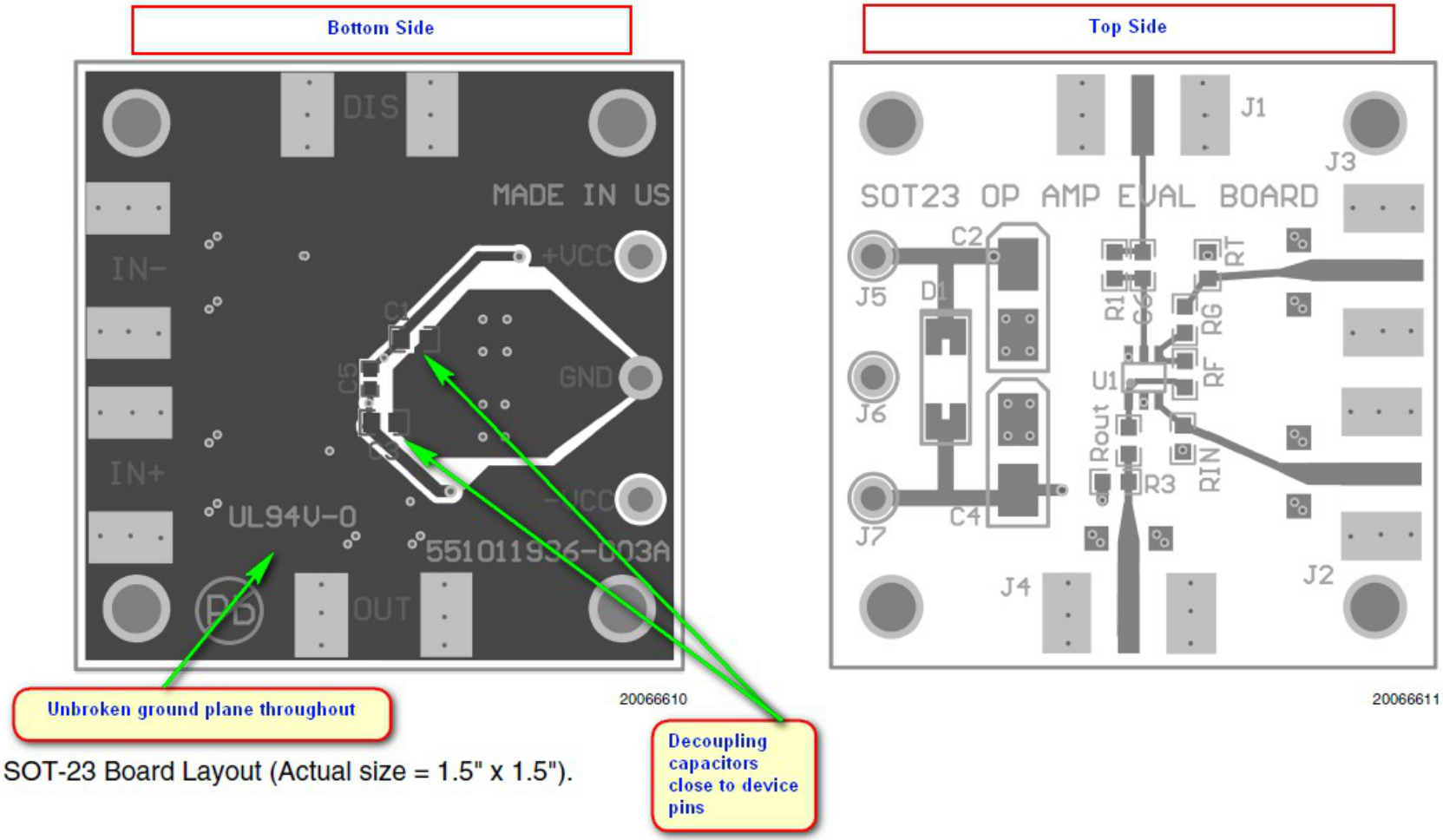
10.1.1 Circuit Layout and Bypassing

The LMV7219 requires high-speed layout. Follow these layout guidelines:

1. Power supply bypassing is critical, and will improve stability and eliminate possible output chatter. A decoupling capacitor such as 0.1-µF ceramic should be placed as close as possible to V^+ pin (and to V- pin if used with dual supplies) as shown in Figure 20. An additional 2.2-µF tantalum capacitor may be required for extra noise reduction.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize unwanted parasitic feedback around the comparator.
3. The device should be soldered directly to the PC board instead of using a socket.
4. Use a PC board with a good, unbroken low inductance ground plane as shown in Figure 20. Make sure ground paths are low-impedance, especially were heavier currents are flowing.
5. Input traces should be kept away from output traces. This can be achieved by running a topside ground plane between the output and inputs.
6. Run the ground trace under the device up to the bypass capacitor to shield the inputs from the outputs.
7. To prevent parasitic feedback when input signals are slow-moving, a small capacitor of 1000 pF or less can be placed between the inputs. It can also help eliminate oscillations in the transition region. However, this capacitor can cause some degradation to t_{pd} when the source impedance is low.

Copyright © 2000–2016, Texas Instruments Incorporated

10.2 Layout Example



SOT-23 Board Layout (Actual size = 1.5" x 1.5").

Figure 20. SOT-23 Board Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2000–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV7219M5	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	C14A
LMV7219M5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 85	C14A
LMV7219M5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C14A
LMV7219M5X	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	C14A
LMV7219M5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	C14A
LMV7219M5X/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C14A
LMV7219M7	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 85	C15
LMV7219M7/NOPB	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C15
LMV7219M7/NOPB.A	Active	Production	SC70 (DCK) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C15
LMV7219M7X/NOPB	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C15
LMV7219M7X/NOPB.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C15

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

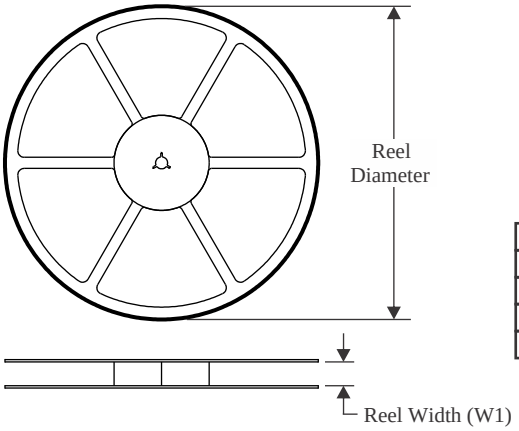
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

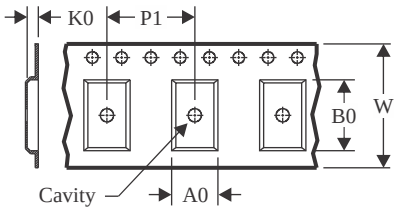
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

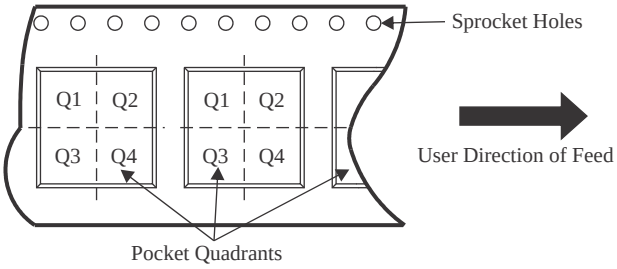


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

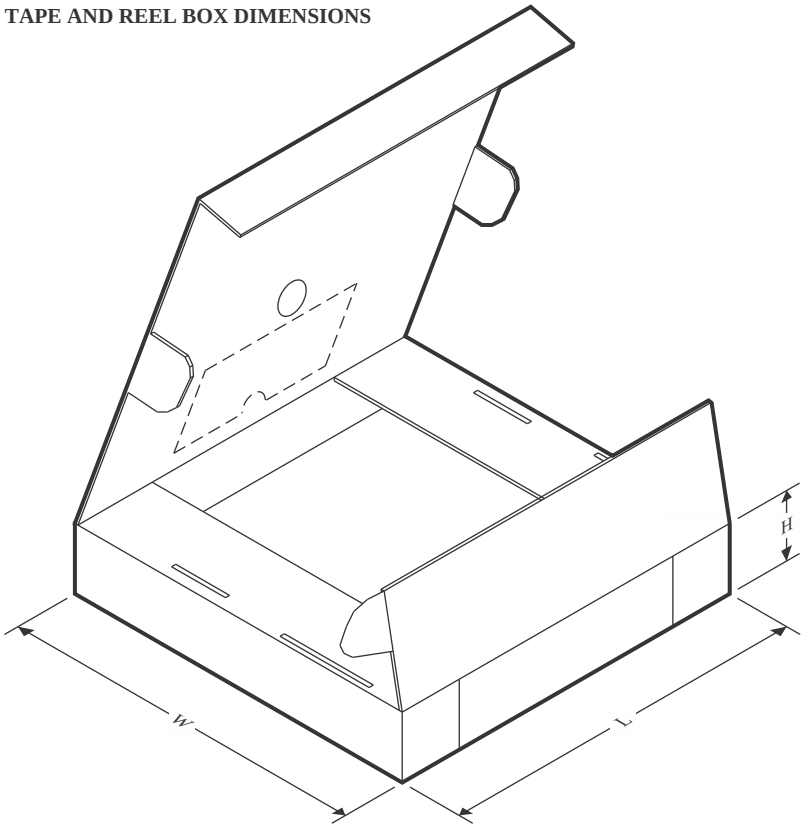
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

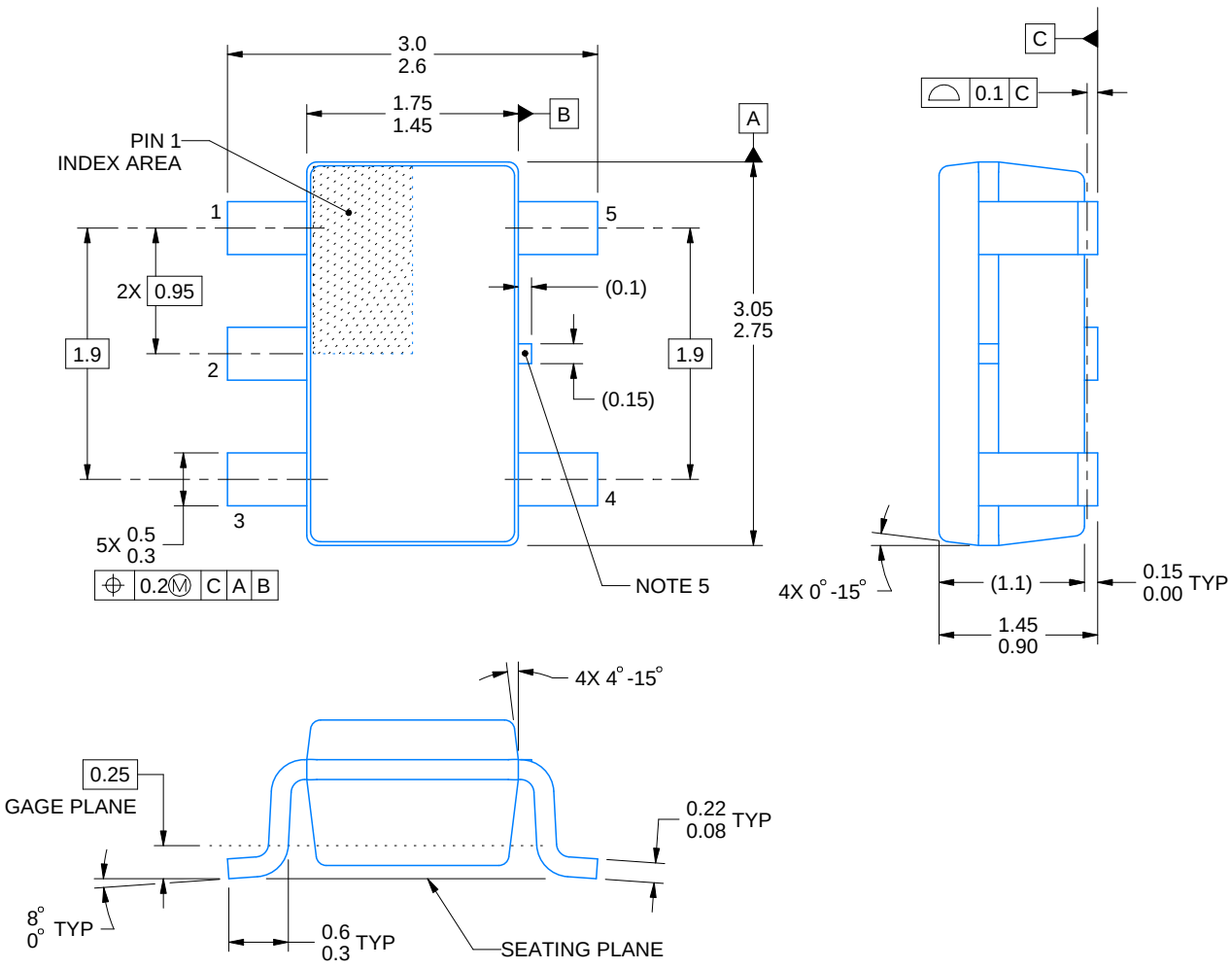
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7219M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7219M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

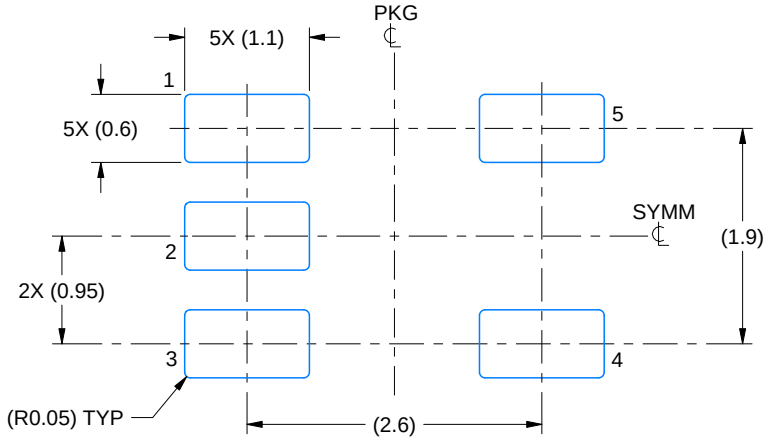
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7219M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV7219M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV7219M7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV7219M7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0



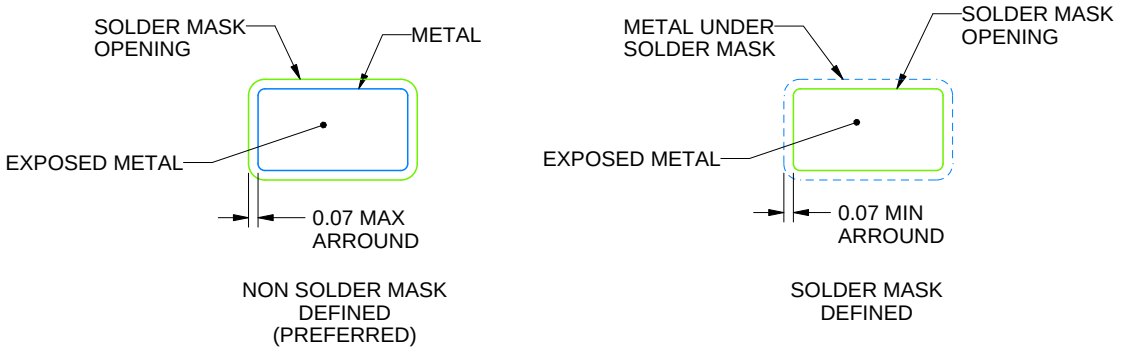
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

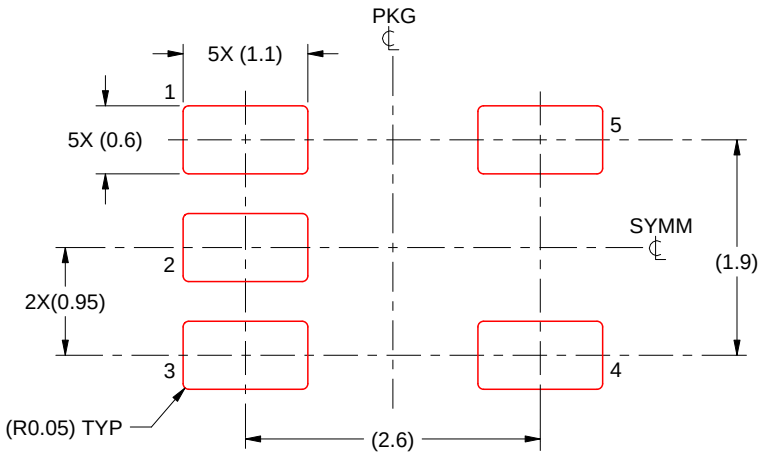


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

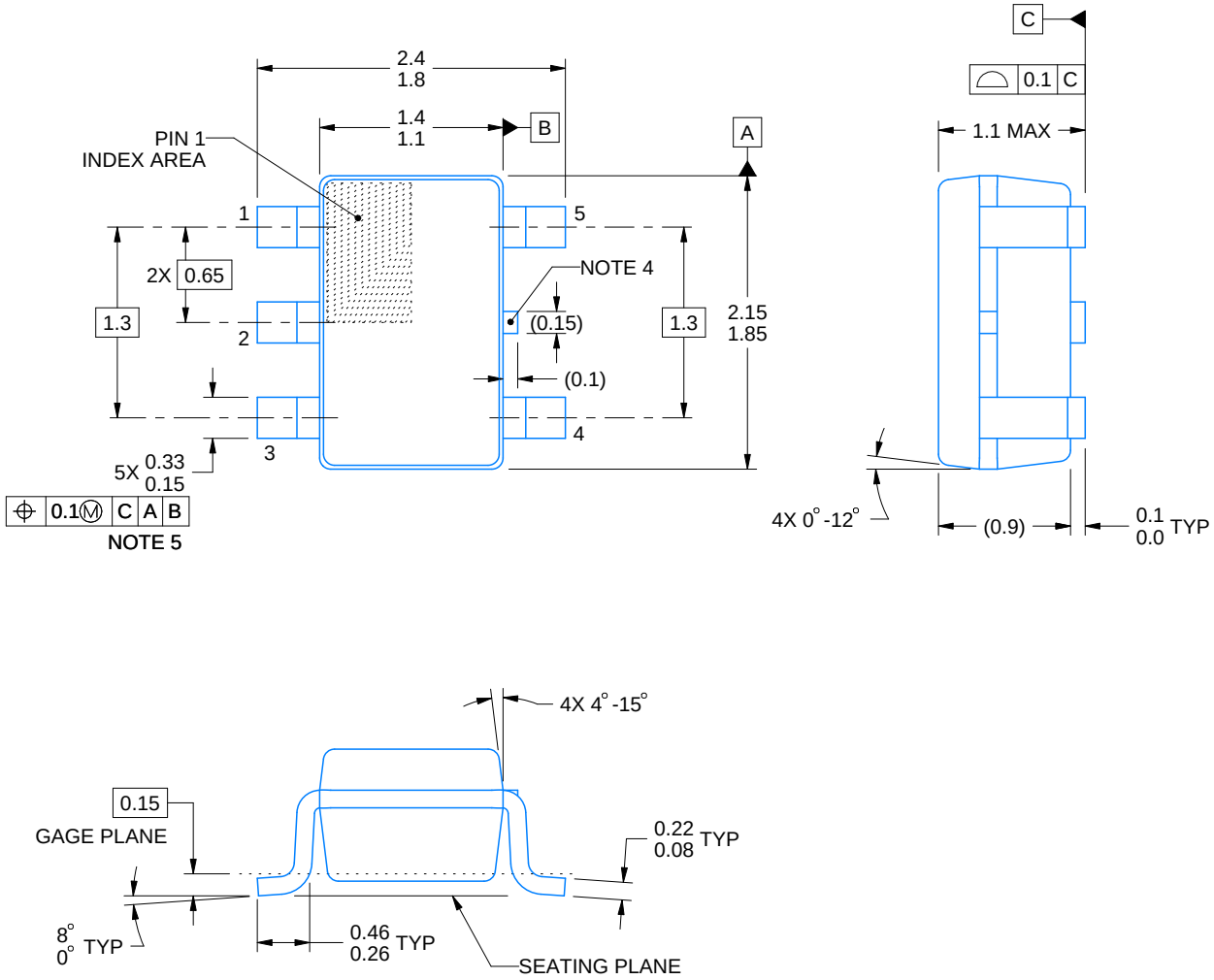


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

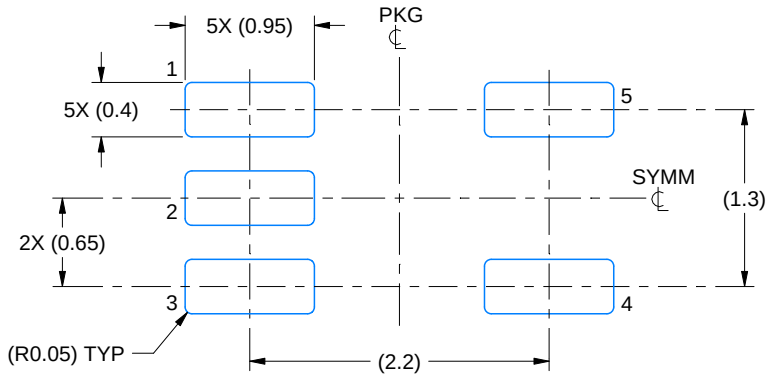
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

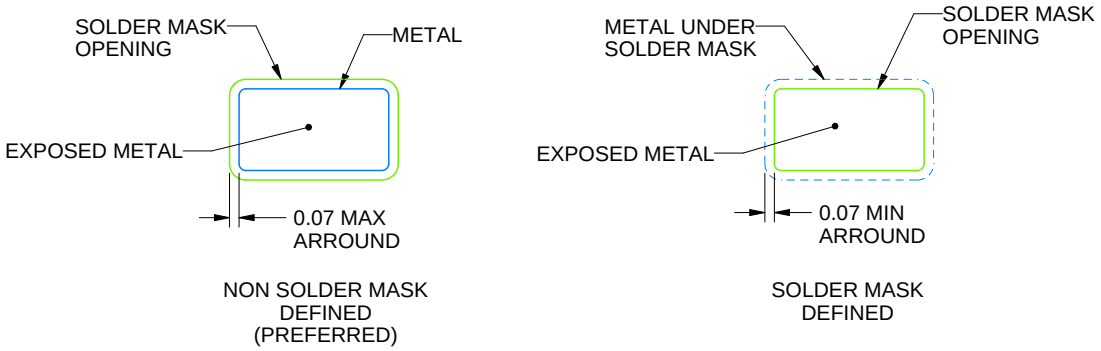


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

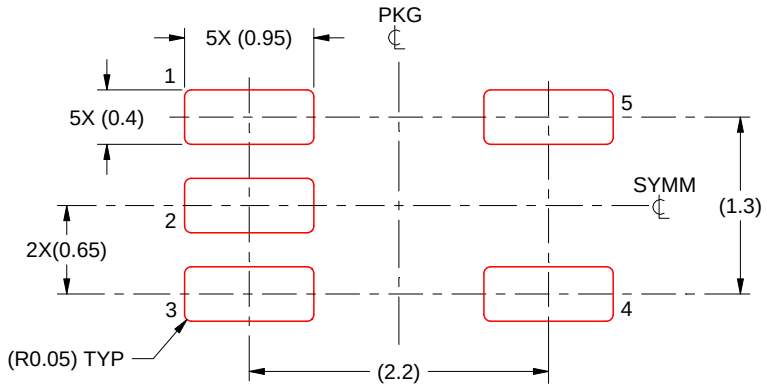


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025