LMV601/LMV602/LMV604 1MHz，低功耗通用，2.7V 运算放大器

查询样品: LMV601, LMV602, LMV604

特性

- （典型 **2.7V** 电源值；除非另外注明）
- **2.7V** 和 **5V** 技术规格
- 电源电流（每个放大器）**100μA**
- 增益带宽产品 **1.0MHz**
- 关断电流 **(LMV601) 45pA**
- 从关断中的接通时间 **(LMV601) 5μs**
- 内部偏置电流 **20fA**

应用范围

- 无绳/蜂窝电话
- 笔记本电脑
- 掌上电脑 **(PDA)**
- **PCMCIA** 卡/音频
- 便携式/电池供电类设备
- 电源电流监控
- 电池监控
- 缓冲器
- 滤波器
- 驱动器

说明

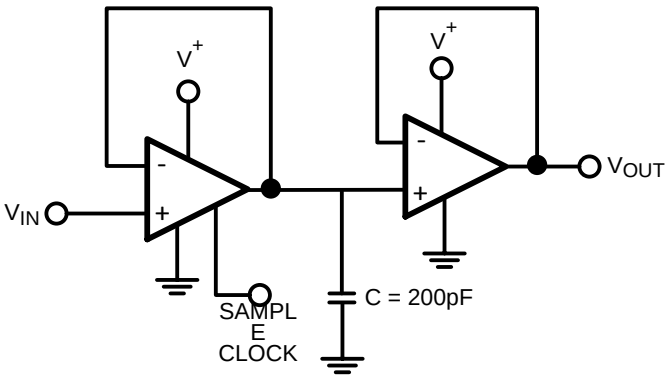
LMV601/LMV602/LMV604 是单路、双路和四路低压、低功率运算放大器。 它们专门针对低压通用应用而设计。 其它重要产品特性是低输入偏置电流、轨到轨输出和宽温度范围。 LMV601/LMV602/LMV604 在 10KHz，1MHz GBW，1.0V/μs 转换率和 0.25mV Vos 时的电压噪声为 29nV。 LMV601/2/4 可由一个低至 2.7V 的单个电源电压供电运行，同时汲取的静态电流为 100uA（典型值）。 在关断模式中，此电流可被减至 45pA。

−40°C 至 125°C 的工业增强型温度范围使得 LMV601/LMV602/LMV604 能够适应广泛的广泛环境应用。

LMV601 提供一个可用来禁用器件的关断引脚。 一旦处于关断模式，电源电流被减少至 45pA（典型值）。

LMV601 采用微型 6 引脚 SC70 封装，LMV602 采用节省空间的 8 引脚超薄型小外形尺寸封装 (VSSOP) 和小外形尺寸集成电路封装 (SOIC)，而 LMV604 采用 14 引脚薄型小外形尺寸封装 (TSSOP) 和 SOIC 封装。 这些小型封装放大器为需要最小印刷电路板 (PCB) 封装尺寸的应用提供了理想的解决方案。 有空间受限 PC 电路板要求的应用包含便携式和电池供电类电子元器件。

采样和保持电路



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Machine Model	200V
	Human Body Model	2000V
Differential Input Voltage		± Supply Voltage
Supply Voltage (V^+ -V^-)		6.0V
Output Short Circuit to V^+		See(4)
Output Short Circuit to V^-		See(5)
Storage Temperature Range		−65°C to 150°C
Junction Temperature(6)		150°C
Mounting Temperature	Infrared or Convection Reflow (20 sec.)	235°C
	Wave Soldering Lead Temp. (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Shorting output to V^+ will adversely affect reliability.
(5) Shorting output to V^- will adversely affect reliability.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Supply Voltage		2.7V to 5.5V
Temperature Range		−40°C to 125°C
Thermal Resistance (θ_{JA})	6-Pin SC70	414°C/W
	8-Pin SOIC	190°C/W
	8-Pin VSSOP	235°C/W
	14-Pin TSSOP	155°C/W
	14-Pin SOIC	145°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics(1)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage	LMV601		0.25	4	mV
		LMV602/LMV604		0.55	5	
TCV_{OS}	Input Offset Voltage Average Drift			1.7		µV/°C
I_B	Input Bias Current			0.02		pA
I_{OS}	Input Offset Current			6.6		fA
I_S	Supply Current	Per Amplifier		100	170	µA
		Shutdown Mode, V_{SD} = 0V (LMV601)		45pA	1µA	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V 0V ≤ V_{CM} ≤ 1.6V		80		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V		82		dB
V_{CM}	Input Common Mode Voltage	For CMRR ≥ 50dB	0	−0.2 to 1.9 (Range)	1.7	V
A_V	Large Signal Voltage Gain	R_L = 10kΩ to 1.35V		113		dB
V_O	Output Swing	R_L = 10kΩ to 1.35V		5.0	30	mV
			30	5.3		
I_O	Output Short Circuit Current	Sourcing LMV601/LMV602		32		mA
		Sourcing LMV604		24		
		Sinking		24		
t_{on}	Turn-on Time from Shutdown	(LMV601)		5		µs
V_{SD}	Shutdown Pin Voltage Range	ON Mode (LMV601)		1.7 to 2.7	2.4 to 2.7	V
		Shutdown Mode (LMV601)		0 to 1	0 to 0.8	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

2.7V AC Electrical Characteristics(1)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
SR	Slew Rate	R_L = 10kΩ,(4)		1.0		V/µs
GBW	Gain Bandwidth Product	R_L = 100kΩ, C_L = 200pF		1.0		MHz
Φ_m	Phase Margin	R_L = 100kΩ		72		deg
G_m	Gain Margin	R_L = 100kΩ		20		dB
e_n	Input-Referred Voltage Noise	f = 1kHz		40		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = $1V_{PP}$		0.017		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Connected as voltage follower with $2V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

5V DC Electrical Characteristics(1)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage	LMV601		0.25	4	mV
		LMV602/LMV604		0.70	5	
TCV_{OS}	Input Offset Voltage Average Drift			1.9		µV/°C
I_B	Input Bias Current			0.02		pA
I_{OS}	Input Offset Current			6.6		fA
I_S	Supply Current	Per Amplifier		107	200	µA
		Shutdown Mode, V_{SD} = 0V (LMV601)		0.033	1	µA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V 0V ≤ V_{CM} ≤ 3.9V		86		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V		82		dB
V_{CM}	Input Common Mode Voltage	For CMRR ≥ 50dB	0	−0.2 to 4.2 (Range)	4	V
A_V	Large Signal Voltage Gain(4)	R_L = 10kΩ to 2.5V		116		dB
V_O	Output Swing	R_L = 10kΩ to 2.5V		7	30	mV
			30	7		
I_O	Output Short Circuit Current	Sourcing		113		mA
		Sinking		75		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) R_L is connected to mid-supply. The output voltage is GND + 0.2V ≤ V_O ≤ V^+ −0.2V

5V DC Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
t_{on}	Turn-on Time from Shutdown	(LMV601)		5		µs
V_{SD}	Shutdown Pin Voltage Range	ON Mode (LMV601)		3.1 to 5	4.5 to 5.0	V
		Shutdown Mode (LMV601)		0 to 1	0 to 0.8	

5V AC Electrical Characteristics(1)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
SR	Slew Rate	R_L = 10kΩ,(4)		1.0		V/µs
GBW	Gain-Bandwidth Product	R_L = 10kΩ, C_L = 200pF		1.0		MHz
Φ_m	Phase Margin	R_L = 100kΩ		70		deg
G_m	Gain Margin	R_L = 100kΩ		20		dB
e_n	Input-Referred Voltage Noise	f = 1kHz		39		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1V_{PP}		0.012		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

Connection Diagrams

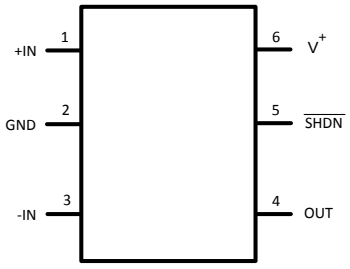


Figure 1. 6-Pin SC70 – Top View
See Package Number DCK

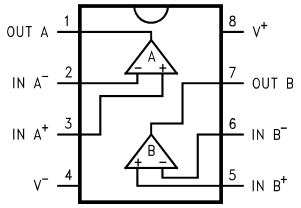


Figure 2. 8-Pin VSSOP/SOIC – Top View
See Package Number DGK or D

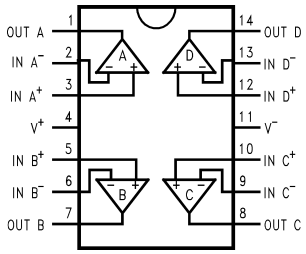


Figure 3. 14-Pin TSSOP/SOIC Top View
See Package Number PW or D

Typical Performance Characteristics

Supply Current vs. Supply Voltage (LMV601)

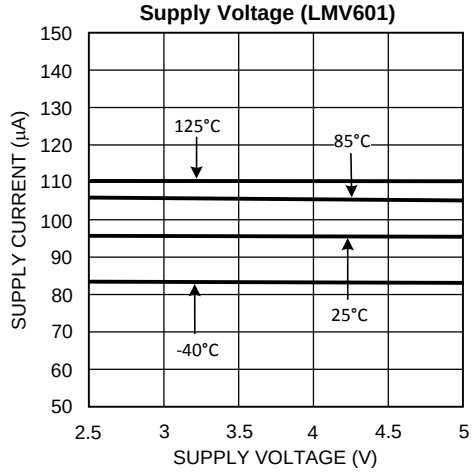


Figure 4.

Input Current vs. Temperature

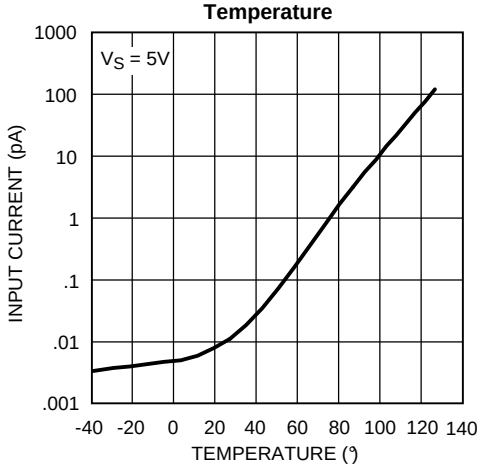


Figure 5.

Output Voltage Swing vs. Supply Voltage

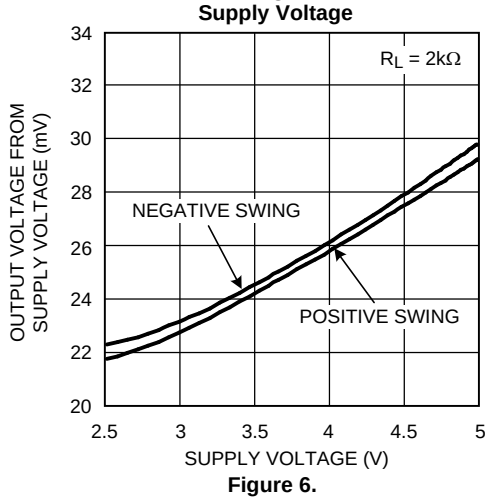


Figure 6.

Output Voltage Swing vs. Supply Voltage

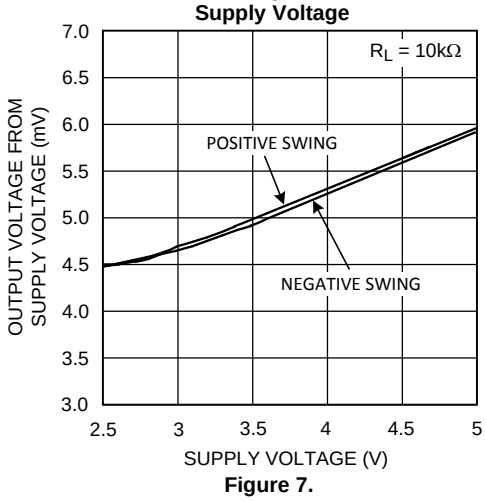


Figure 7.

I_{SOURCE} vs. V_{OUT}

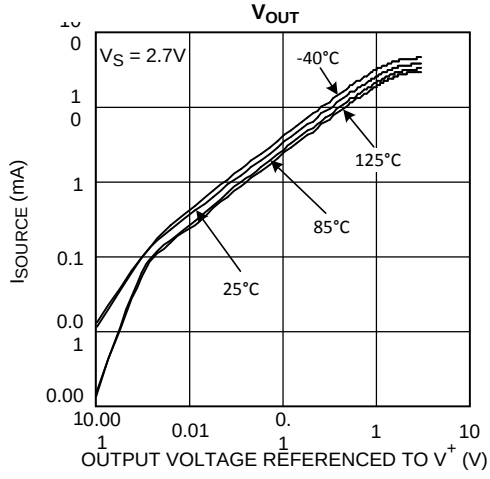


Figure 8.

I_{SOURCE} vs. V_{OUT}

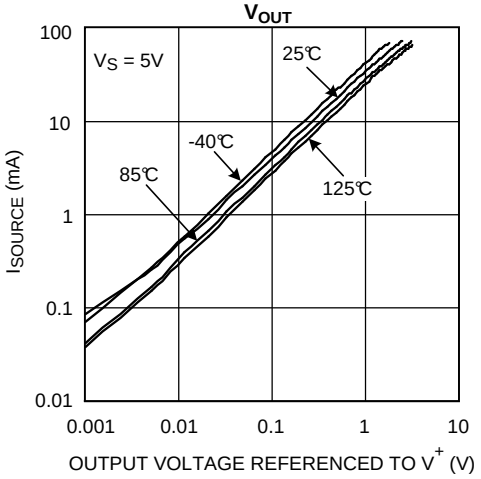


Figure 9.

Typical Performance Characteristics (continued)

I_{SINK} vs. V_{OUT}

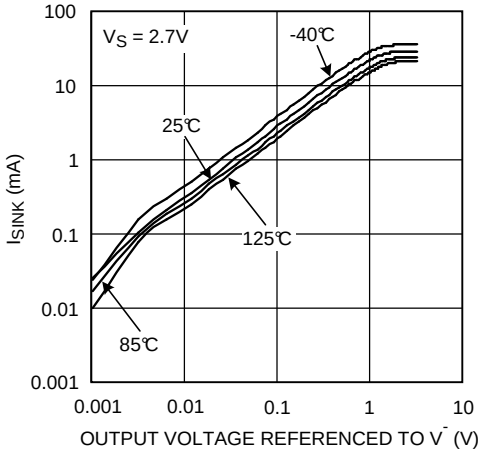


Figure 10.

I_{SINK} vs. V_{OUT}

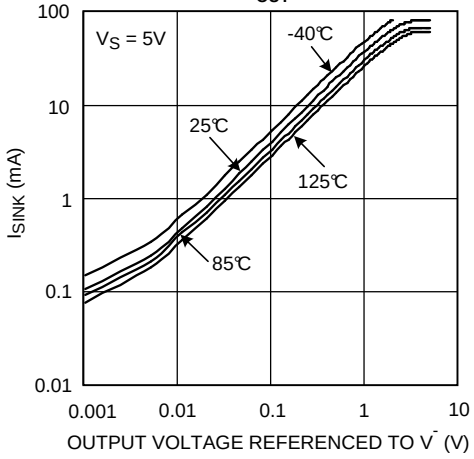


Figure 11.

V_{OS} vs. V_{CM}

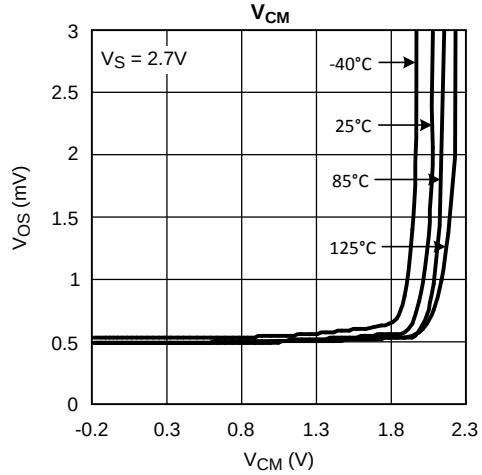


Figure 12.

V_{OS} vs. V_{CM}

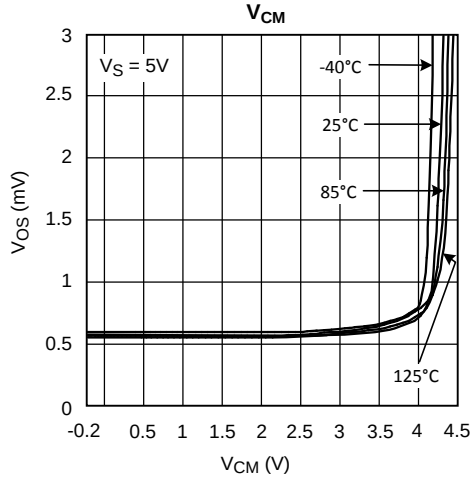


Figure 13.

V_{IN} vs. V_{OUT}

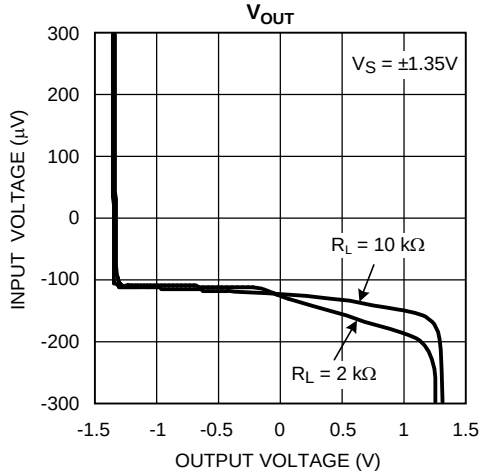


Figure 14.

V_{IN} vs. V_{OUT}

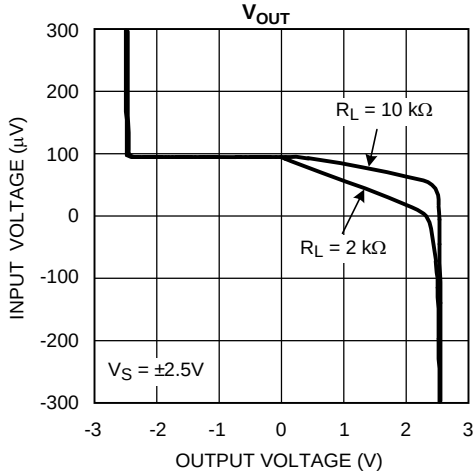


Figure 15.

Typical Performance Characteristics (continued)

CMRR vs. Frequency

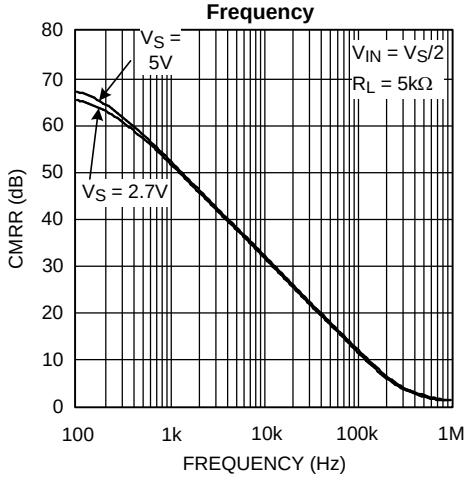


Figure 16.

PSRR vs. Frequency

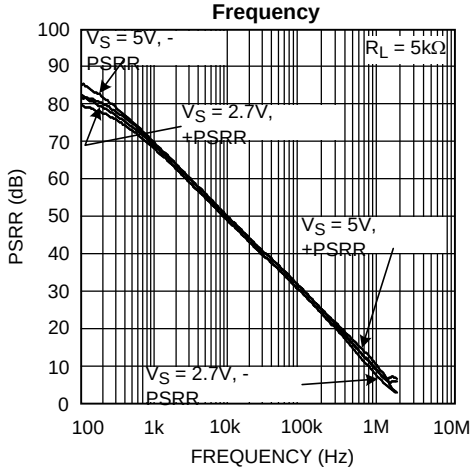


Figure 17.

Input Voltage Noise vs. frequency

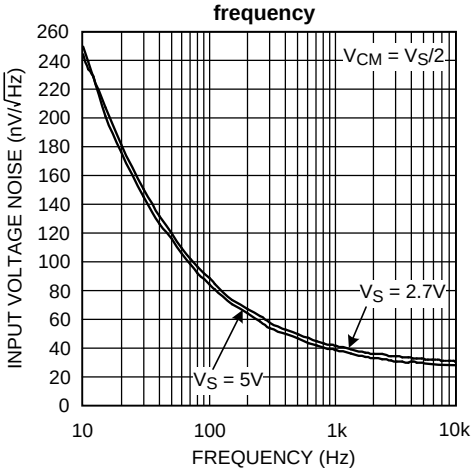


Figure 18.

Slew Rate vs. V_{SUPPLY}

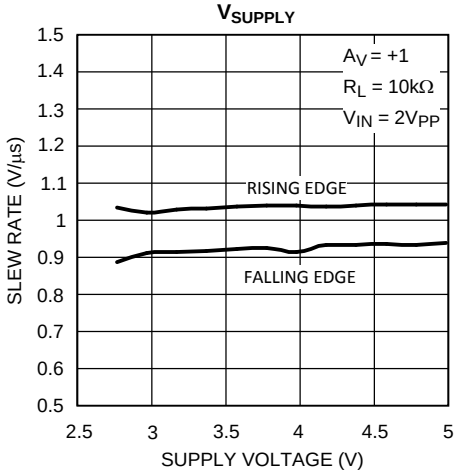


Figure 19.

Slew Rate vs. Temperature

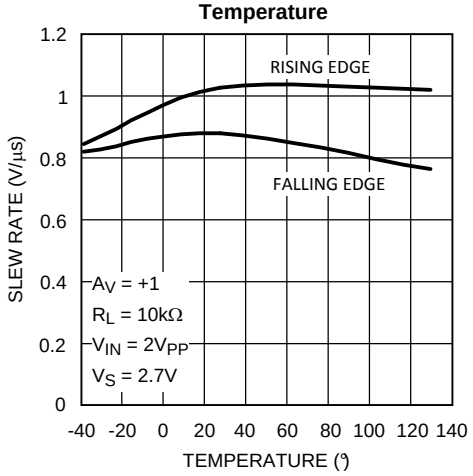


Figure 20.

Slew Rate vs. Temperature

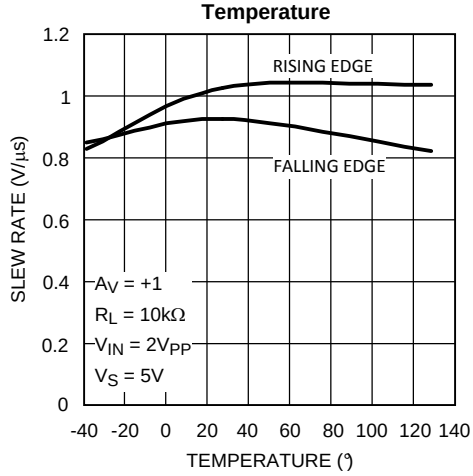


Figure 21.

Typical Performance Characteristics (continued)

THD+N vs. Frequency

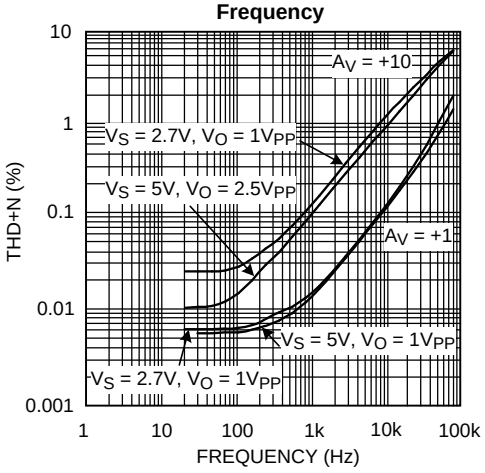


Figure 22.

THD+N vs. V_{OUT}

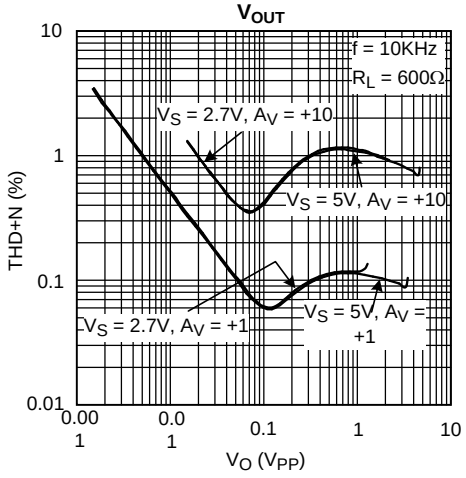


Figure 23.

Open Loop Frequency Over Temperature

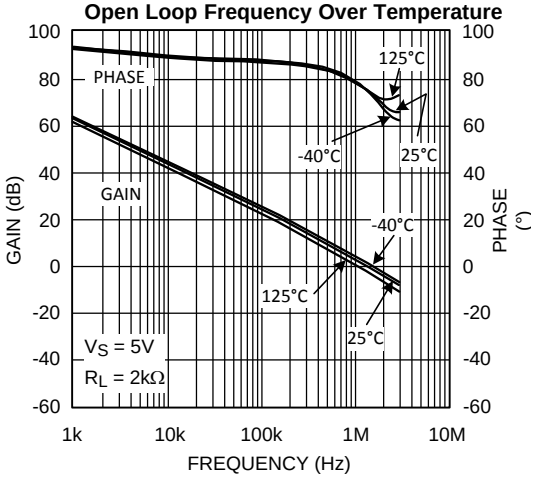


Figure 24.

Open Loop Frequency Response

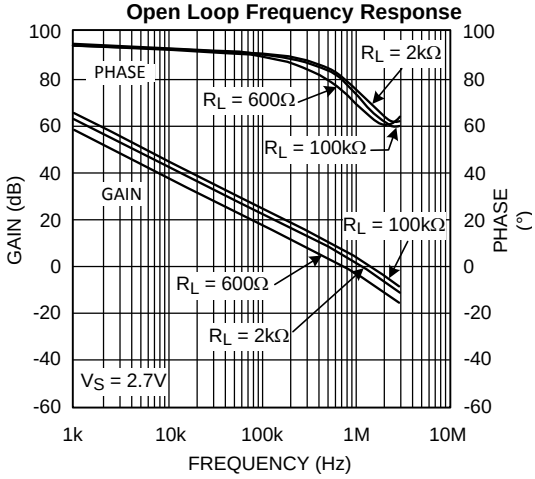


Figure 25.

Open Loop Frequency Response

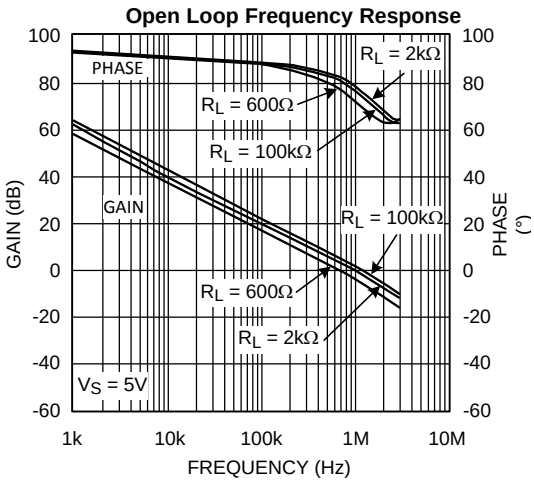


Figure 26.

Gain and Phase vs. C_L

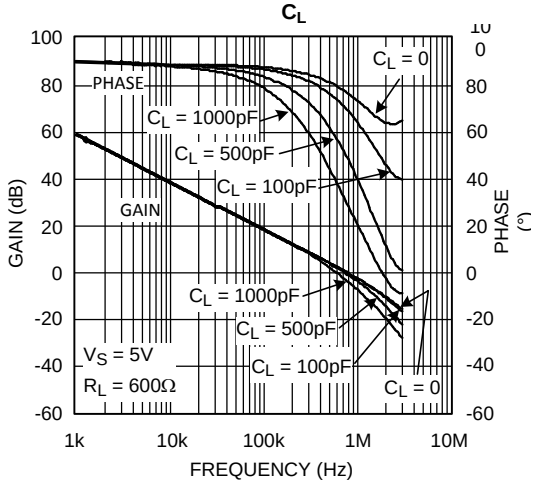


Figure 27.

Typical Performance Characteristics (continued)

Gain and Phase vs. C_L

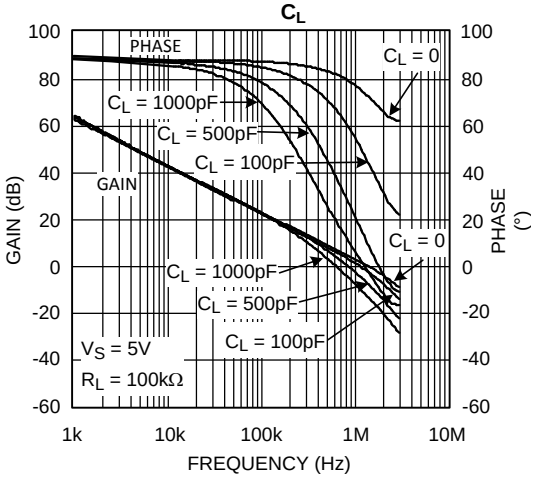


Figure 28.

Stability vs. Capacitive Load

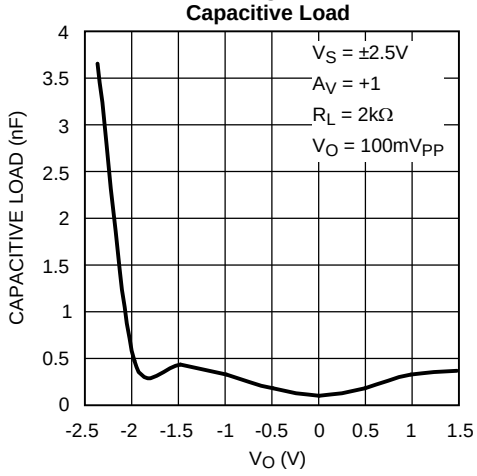


Figure 29.

Stability vs. Capacitive Load

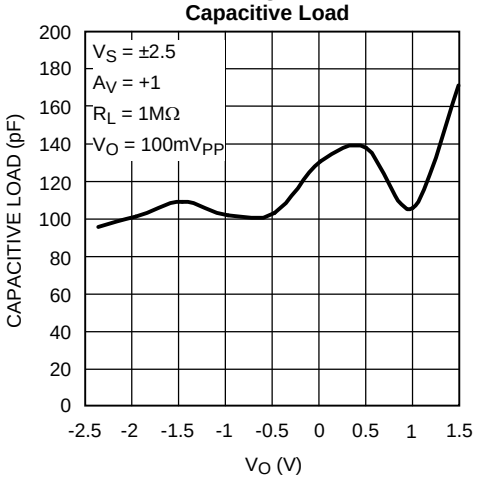


Figure 30.

Non-Inverting Small Signal Pulse Response

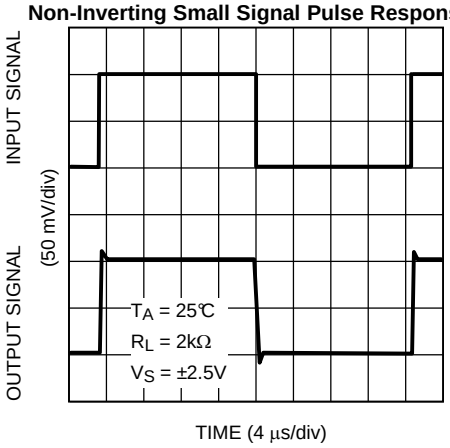


Figure 31.

Non-Inverting Large Signal Pulse Response

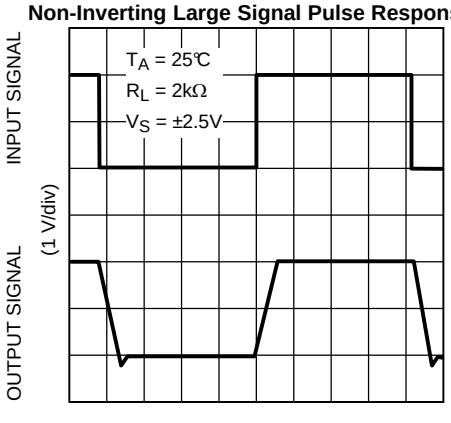


Figure 32.

Non-Inverting Small Signal Pulse Response

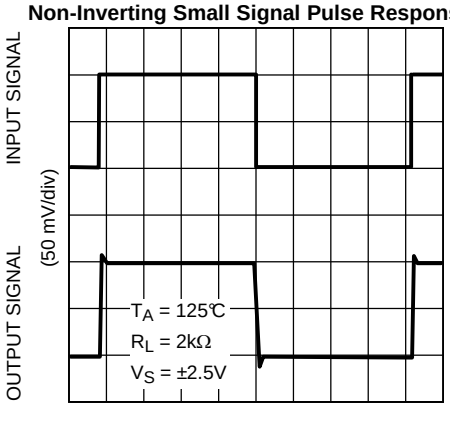


Figure 33.

Typical Performance Characteristics (continued)

Non-Inverting Large Signal Pulse Response

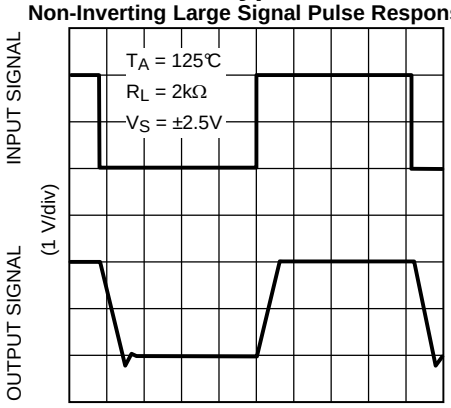


Figure 34.

Non-Inverting Small Signal Pulse Response

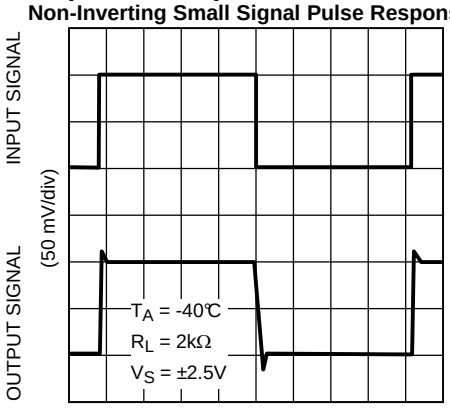


Figure 35.

Non-Inverting Large Signal Pulse Response

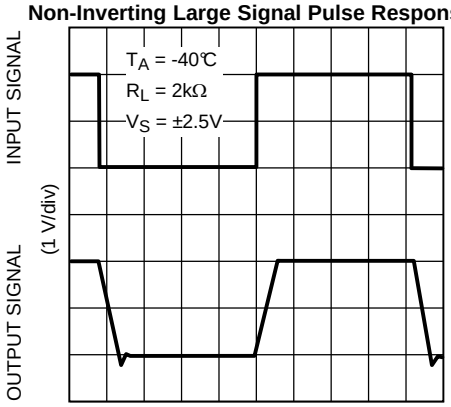


Figure 36.

Inverting Small Signal Pulse Response

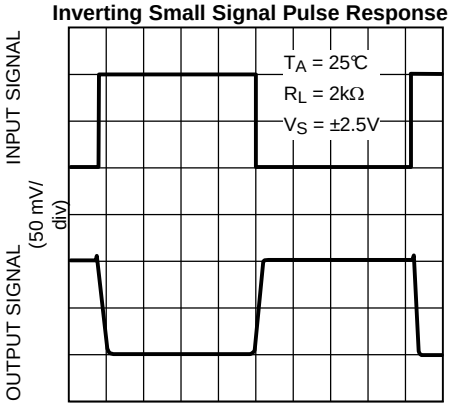


Figure 37.

Inverting Large Signal Pulse Response

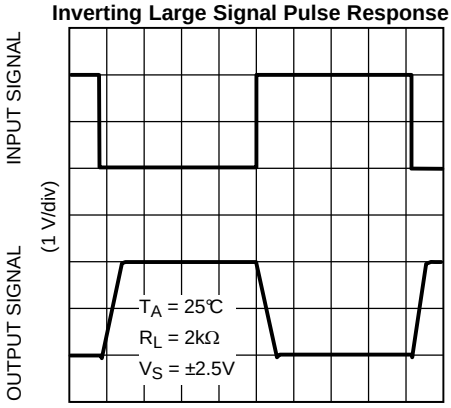


Figure 38.

Inverting Small Signal Pulse Response

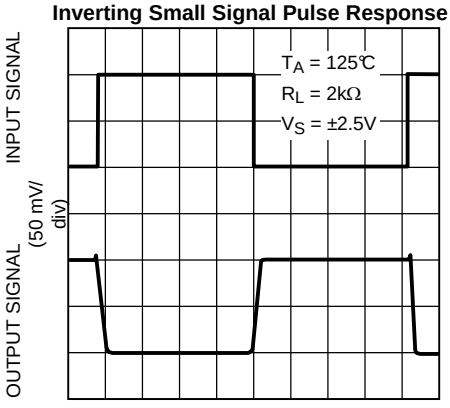


Figure 39.

Typical Performance Characteristics (continued)

Inverting Large Signal Pulse Response

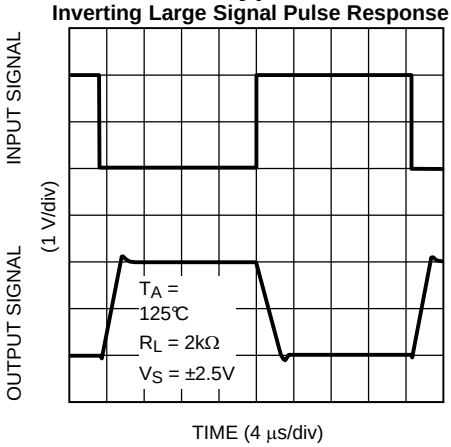


Figure 40.

Inverting Small Signal Pulse Response

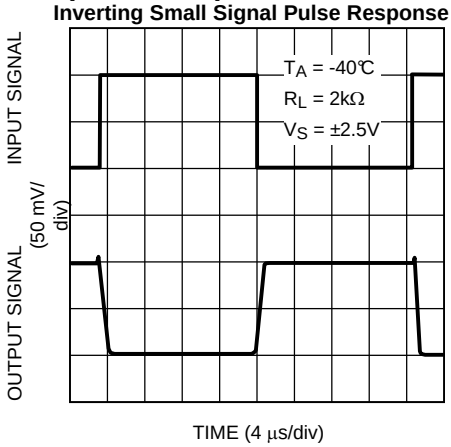


Figure 41.

Inverting Large Signal Pulse Response

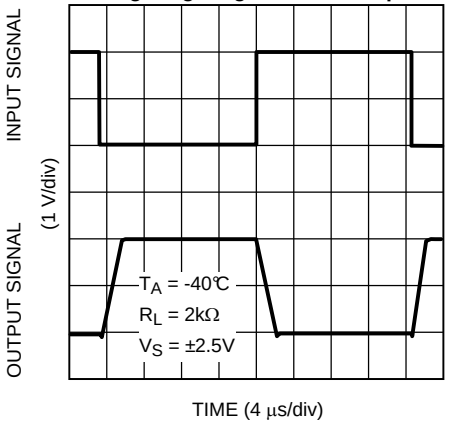


Figure 42.

Crosstalk Rejection vs. Frequency

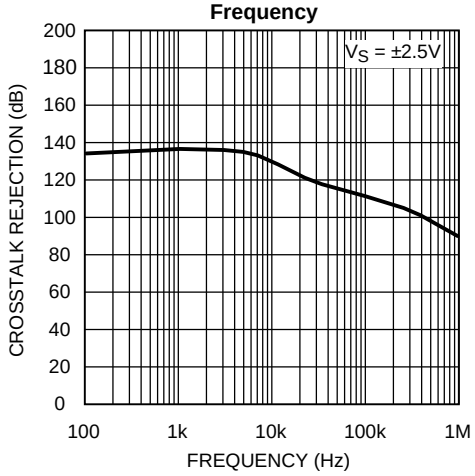


Figure 43.

APPLICATION SECTION

LMV601/LMV602/LMV604

The LMV601/LMV602/LMV604 family of amplifiers features low voltage, low power, and rail-to-rail output operational amplifiers designed for low voltage portable applications. The family is designed using all CMOS technology. This results in an ultra low input bias current. The LMV601 has a shutdown option, which can be used in portable devices to increase battery life.

A simplified schematic of the LMV601/LMV602/LMV604 family of amplifiers is shown in Figure 44. The PMOS input differential pair allows the input to include ground. The output of this differential pair is connected to the Class AB turnaround stage. This Class AB turnaround has a lower quiescent current, compared to regular turnaround stages. This results in lower offset, noise, and power dissipation, while slew rate equals that of a conventional turnaround stage. The output of the Class AB turnaround stage provides gate voltage to the complementary common-source transistors at the output stage. These transistors enable the device to have rail-to-rail output.

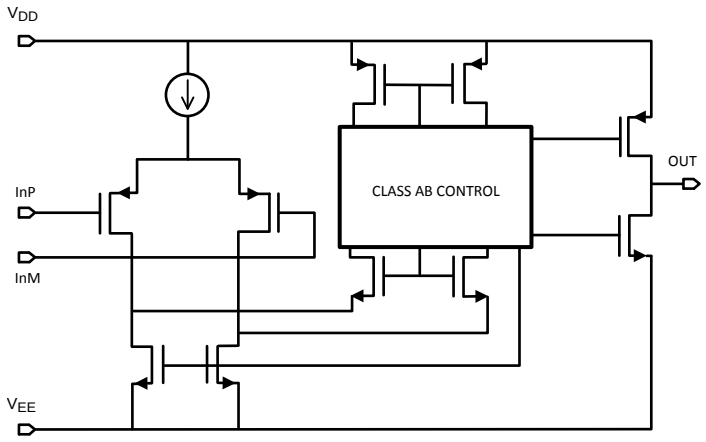


Figure 44. Simplified Schematic

CLASS AB TURNAROUND STAGE AMPLIFIER

This patented folded cascode stage has a combined class AB amplifier stage, which replaces the conventional folded cascode stage. Therefore, the class AB folded cascode stage runs at a much lower quiescent current compared to conventional folded cascode stages. This results in significantly smaller offset and noise contributions. The reduced offset and noise contributions in turn reduce the offset voltage level and the voltage noise level at the input of the LMV601/LMV602/LMV604. Also the lower quiescent current results in a high open-loop gain for the amplifier. The lower quiescent current does not affect the slew rate of the amplifier nor its ability to handle the total current swing coming from the input stage.

The input voltage noise of the device at low frequencies, below 1kHz, is slightly higher than devices with a BJT input stage; However the PMOS input stage results in a much lower input bias current and the input voltage noise drops at frequencies above 1kHz.

SAMPLE AND HOLD CIRCUIT

The lower input bias current of the LMV601 results in a very high input impedance. The output impedance when the device is in shutdown mode is quite high. These high impedances, along with the ability of the shutdown pin to be derived from a separate power source, make LMV601 a good choice for sample and hold circuits. The sample clock should be connected to the shutdown pin of the amplifier to rapidly turn the device on or off.

Figure 45 shows the schematic of a simple sample and hold circuit. When the sample clock is high the first amplifier is in normal operation mode and the second amplifier acts as a buffer. The capacitor, which appears as a load on the first amplifier, will be charging at this time. The voltage across the capacitor is that of the non-inverting input of the first amplifier since it is connected as a voltage-follower. When the sample clock is low the first amplifier is shut off, bringing the output impedance to a high value. The high impedance of this output, along with the very high impedance on the input of the second amplifier, prevents the capacitor from discharging. There is very little voltage droop while the first amplifier is in shutdown mode. The second amplifier, which is still in normal operation mode and is connected as a voltage follower, also provides the voltage sampled on the capacitor at its output.

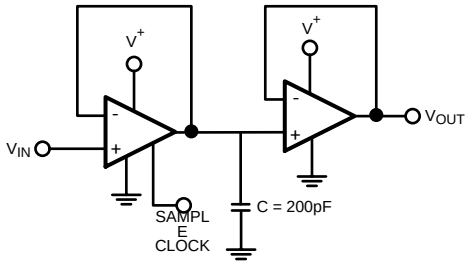


Figure 45. Sample and Hold Circuit

SHUTDOWN FEATURE

The LMV601 is capable of being turned off in order to conserve power and increase battery life in portable devices. Once in shutdown mode the supply current is drastically reduced, 1µA maximum, and the output will be "tri-stated."

The device will be disabled when the shutdown pin voltage is pulled low. The shutdown pin should never be left unconnected. Leaving the pin floating will result in an undefined operation mode and the device may oscillate between shutdown and active modes.

The LMV601 typically turns on 2.8µs after the shutdown voltage is pulled high. The device turns off in less than 400ns after shutdown voltage is pulled low. Figure 46 and Figure 47 show the turn-on and turn-off time of the LMV601, respectively. In order to reduce the effect of the capacitance added to the circuit by the scope probe, in the turn-off time circuit a resistive load of 600Ω is added. Figure 48 and Figure 49 show the test circuits used to obtain the two plots.

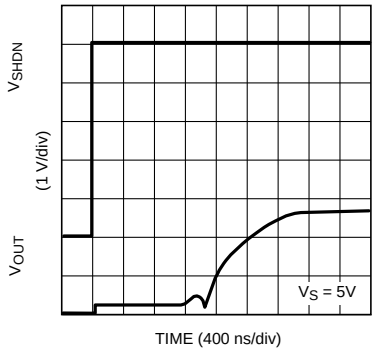


Figure 46. Turn-on Time

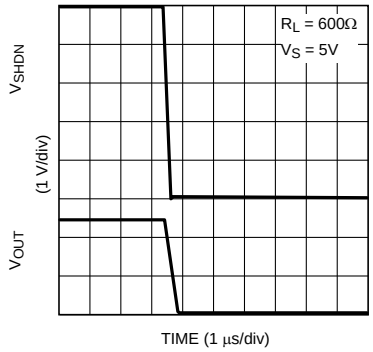


Figure 47. Turn-off Time

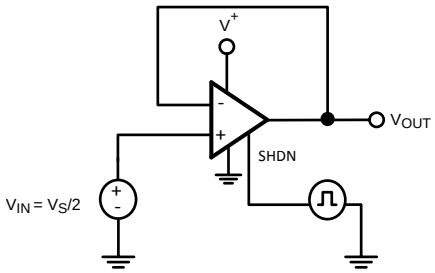


Figure 48. Turn-on Time

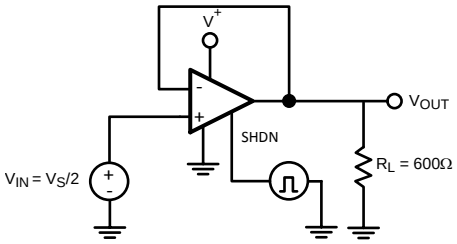


Figure 49. Turn-off Time

LOW INPUT BIAS CURRENT

The LMV601/LMV602/LMV604 Amplifiers have a PMOS input stage. As a result, they will have a much lower input bias current than devices with BJT input stages. This feature makes these devices ideal for sensor circuits. A typical curve of the input bias current of the LMV601 is shown in Figure 50.

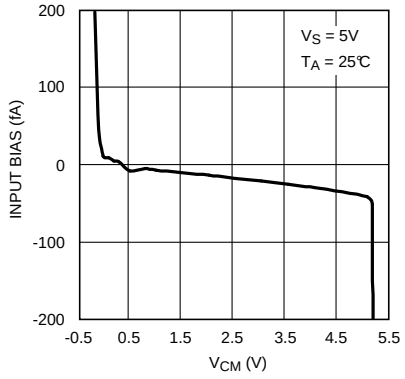


Figure 50. Input Bias Current vs. V_{CM}

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV601MG/NOPB	Active	Production	SC70 (DCK) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV601MG/NOPB.A	Active	Production	SC70 (DCK) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV601MGX/NOPB	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV601MGX/NOPB.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AUA
LMV602MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	LMV60 2MA
LMV602MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV602MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV602MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV602MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC9A
LMV604MA/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MA/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MA/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	-	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MAX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MAX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MAX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	LMV604MA
LMV604MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV604 MT
LMV604MT/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV604 MT
LMV604MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV604 MT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV604MTX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV604 MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

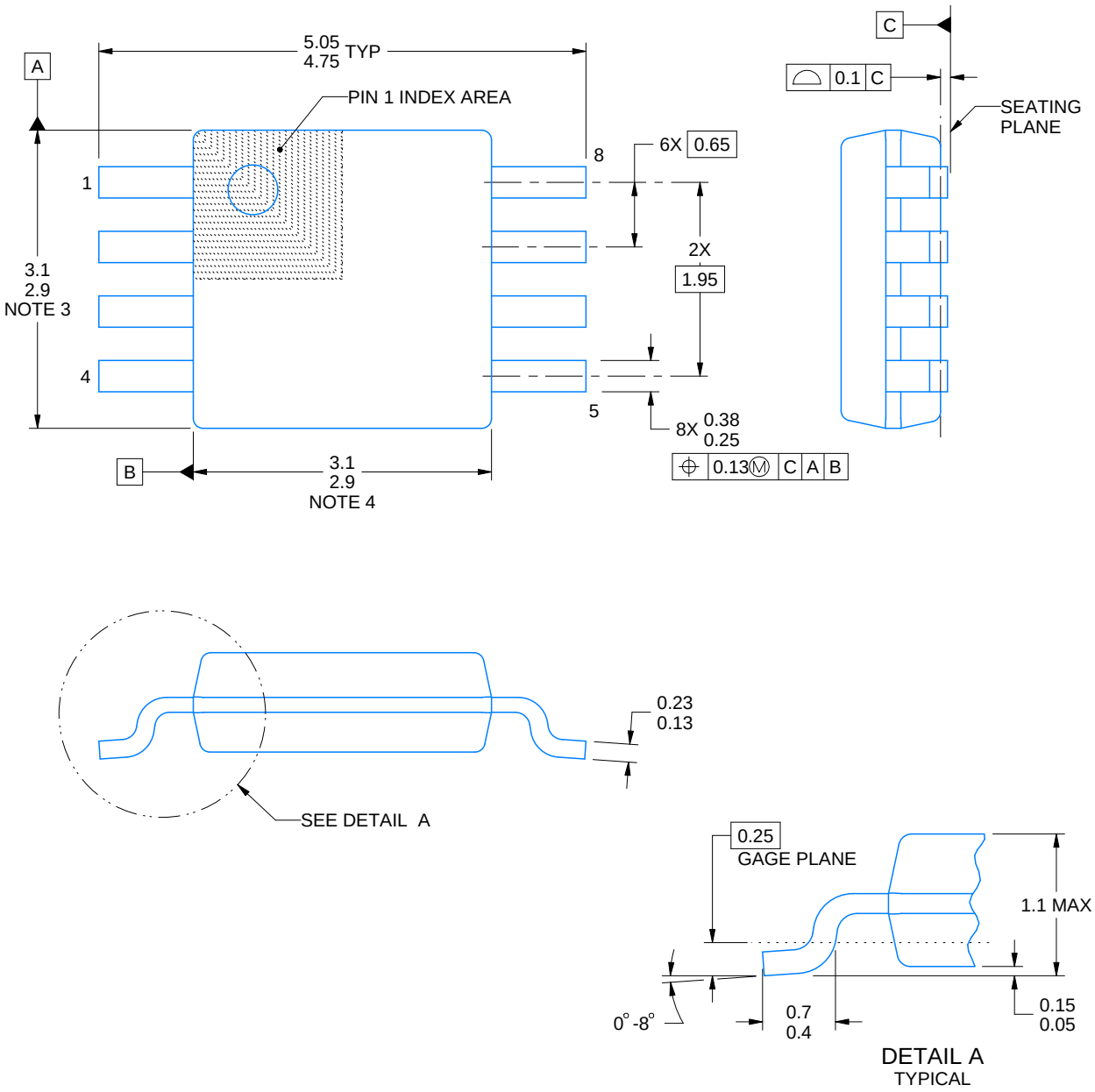
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

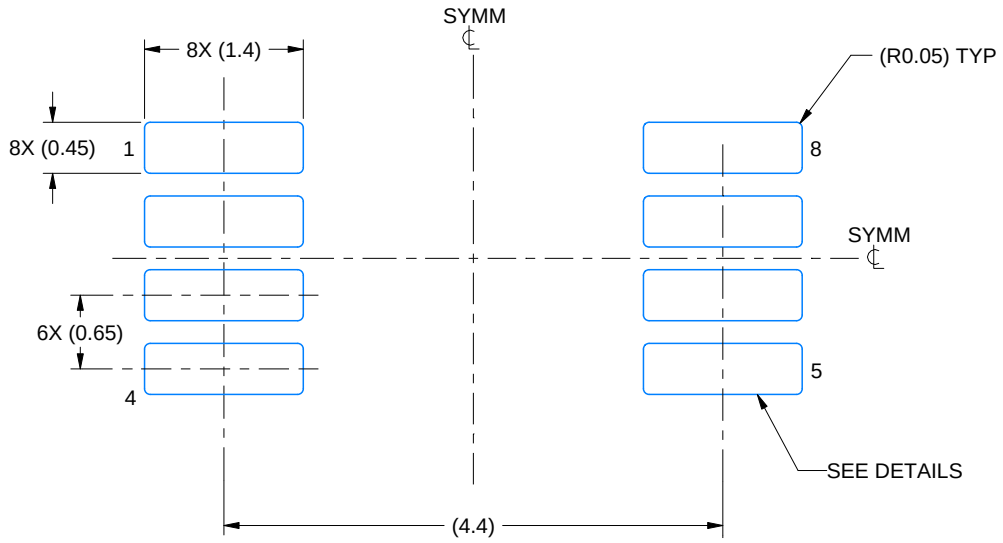
SMALL OUTLINE PACKAGE



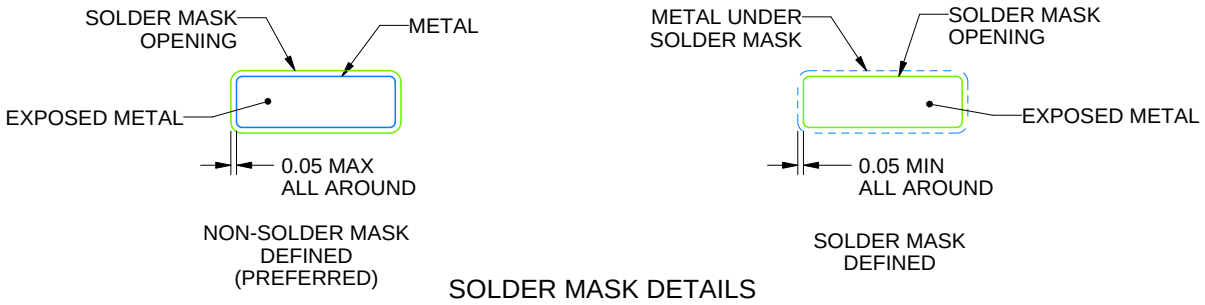
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

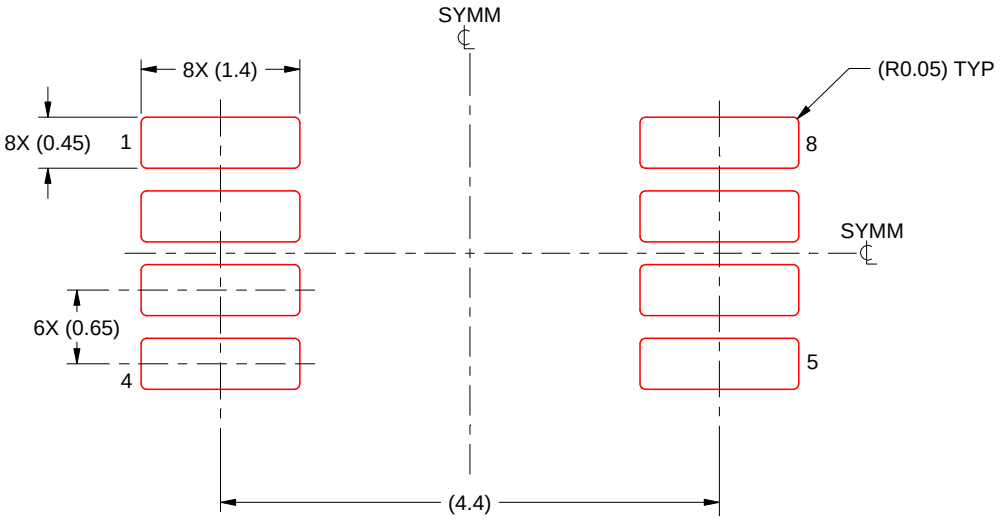


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

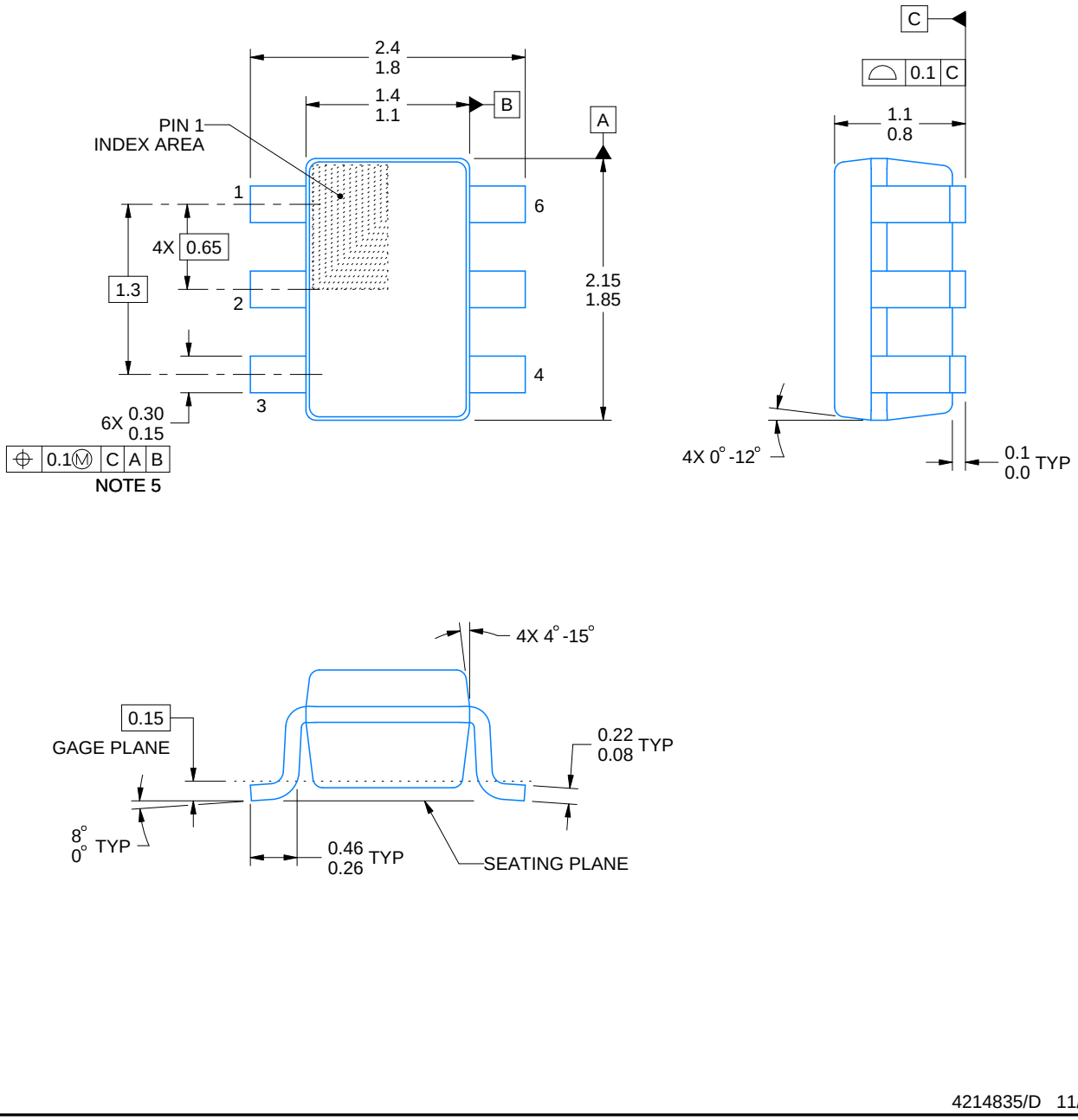
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

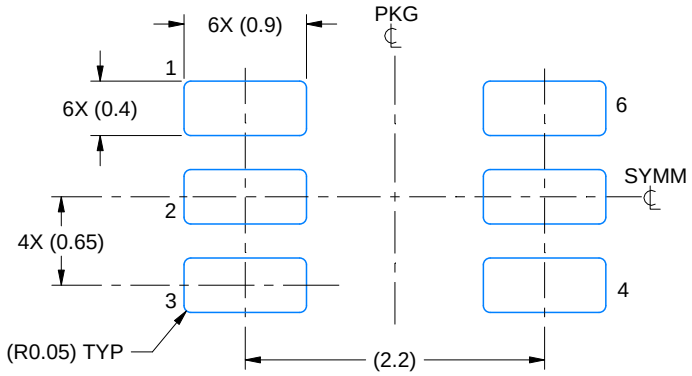
SMALL OUTLINE TRANSISTOR



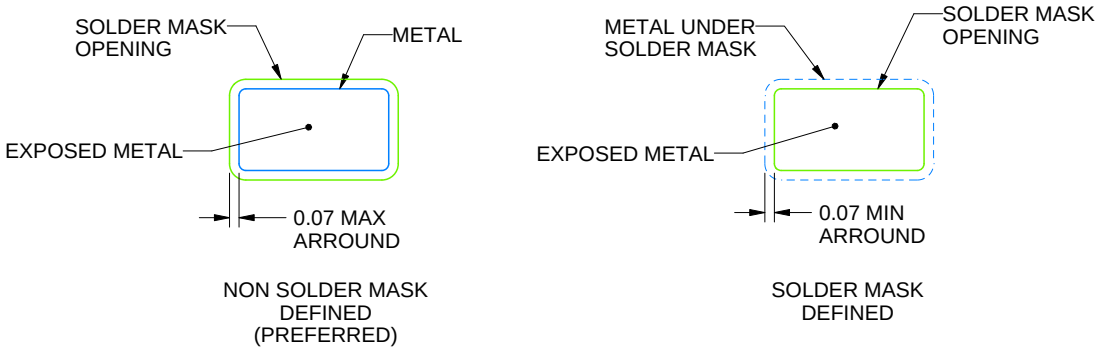
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

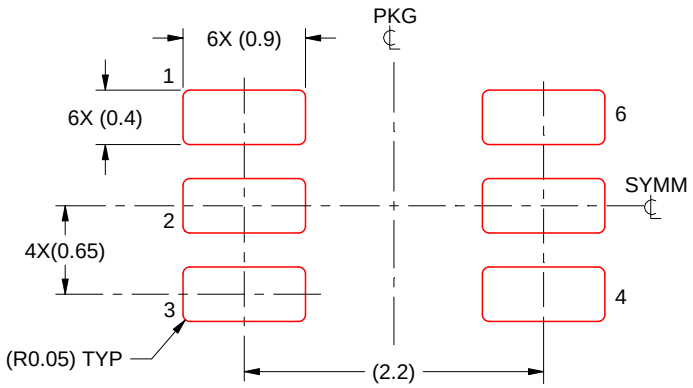


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

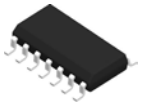


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

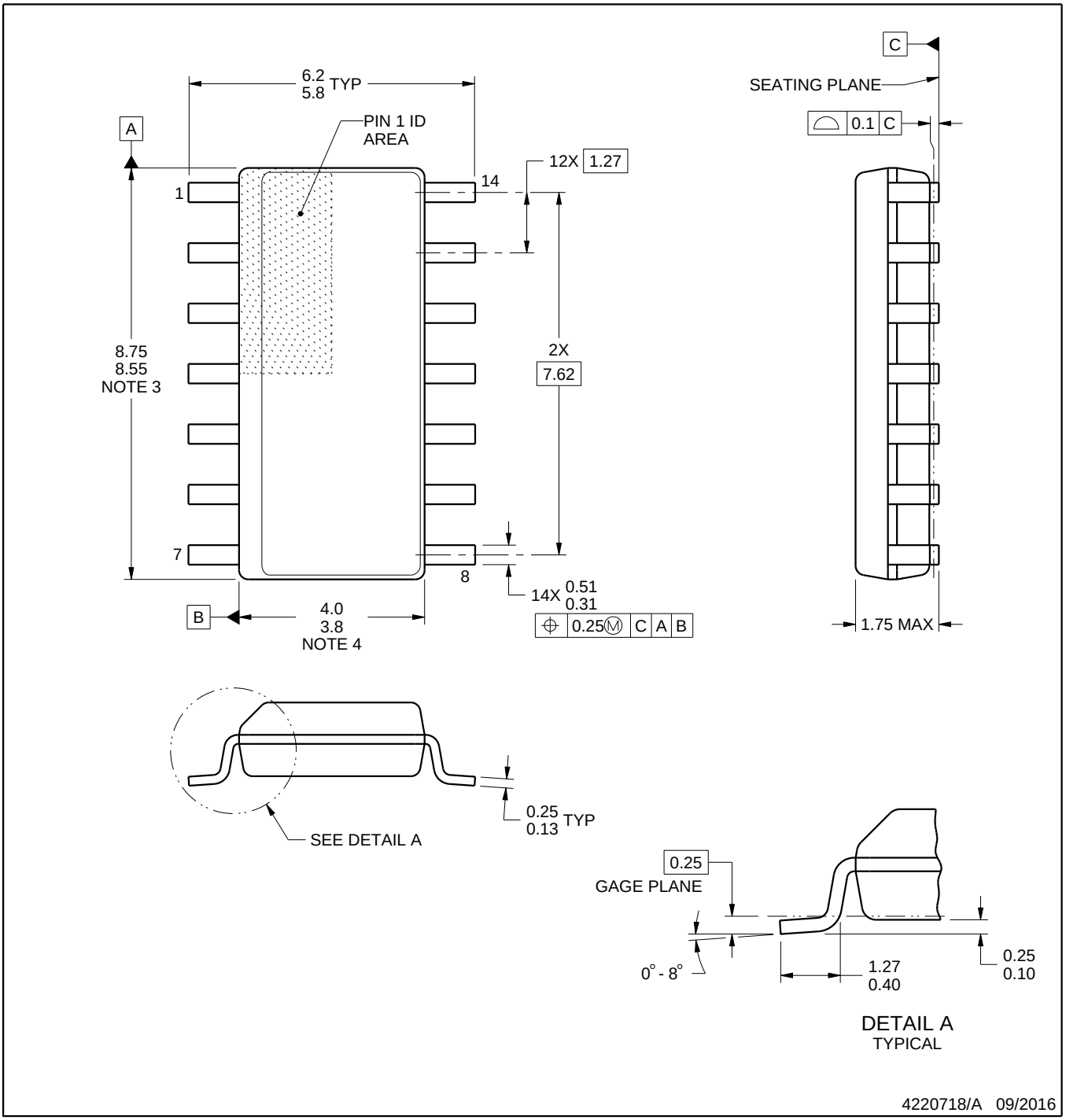


PACKAGE OUTLINE

D0014A

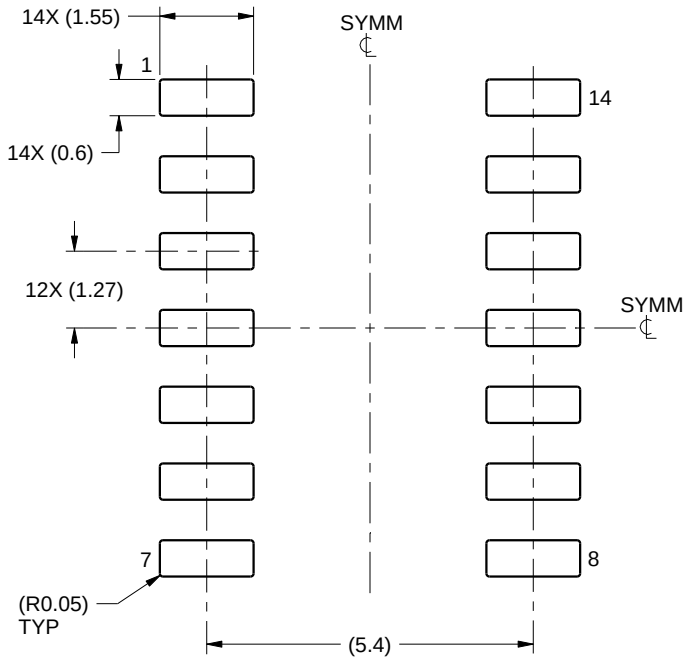
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

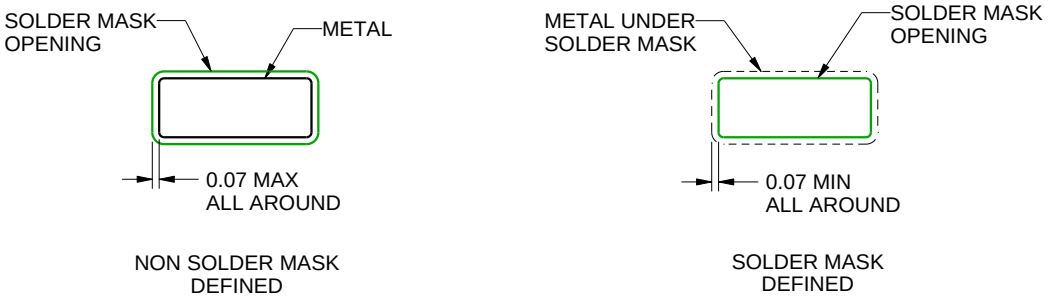


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

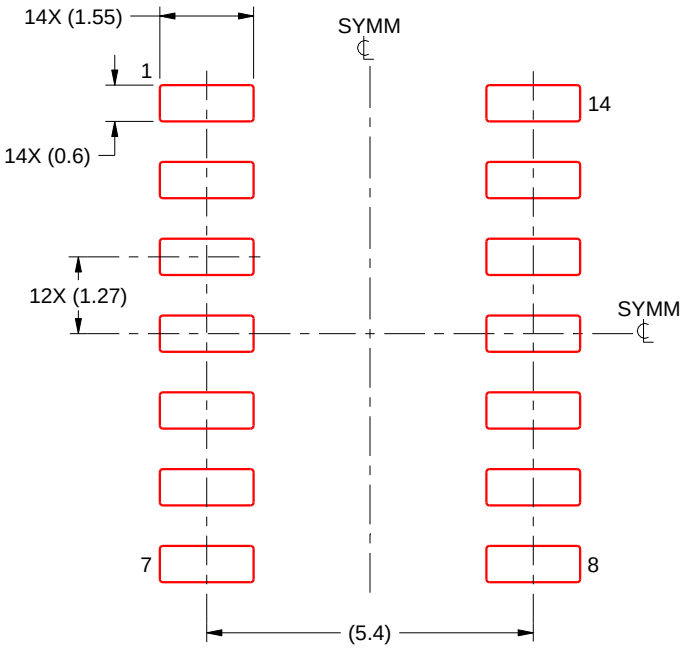
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

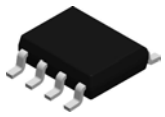


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

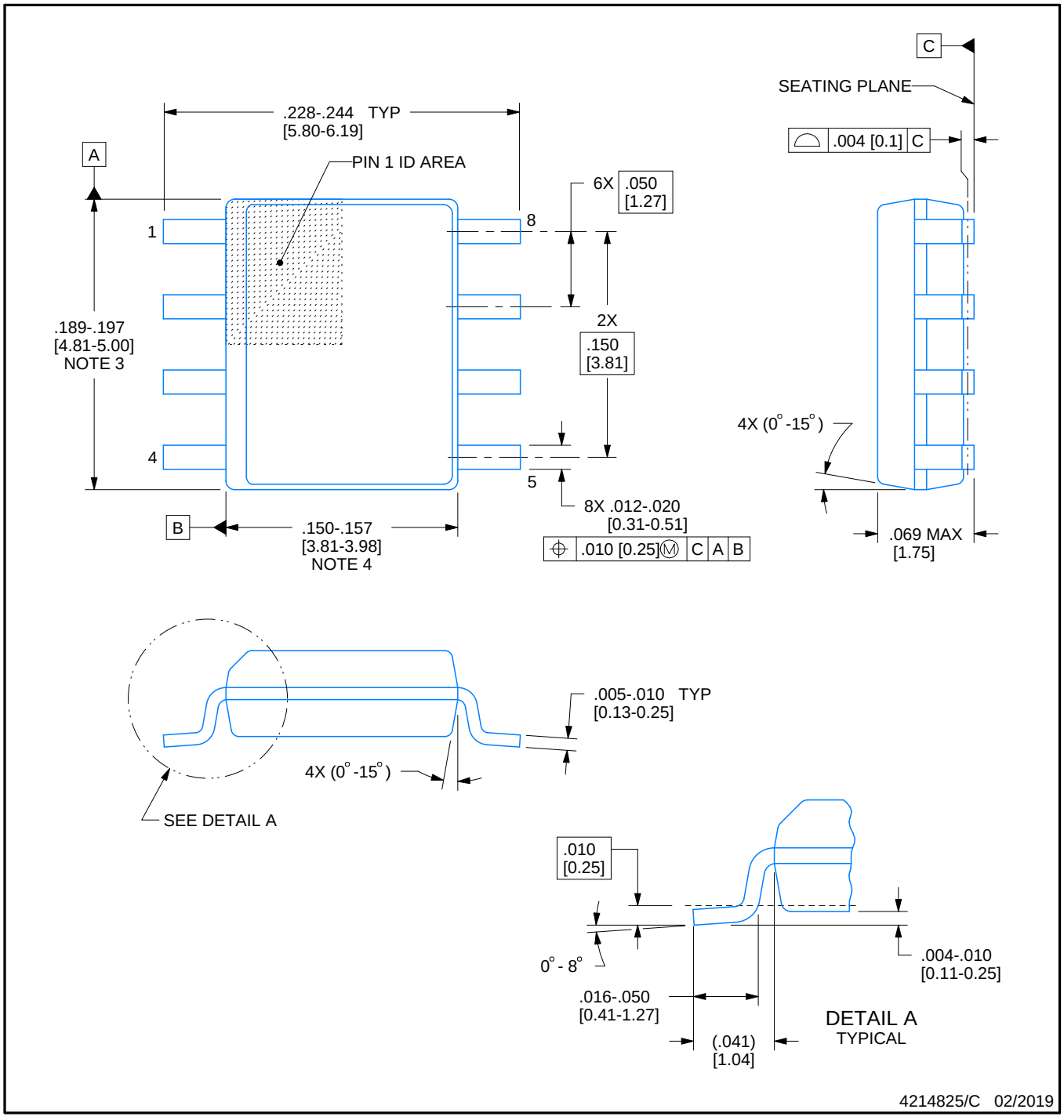


PACKAGE OUTLINE

D0008A

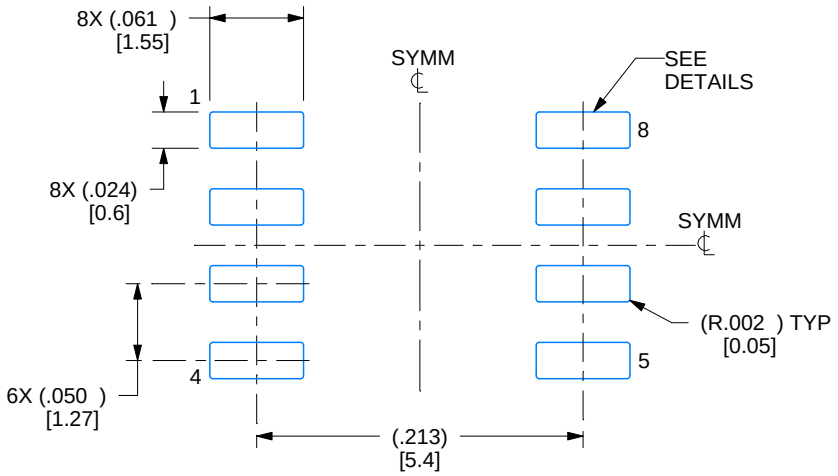
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

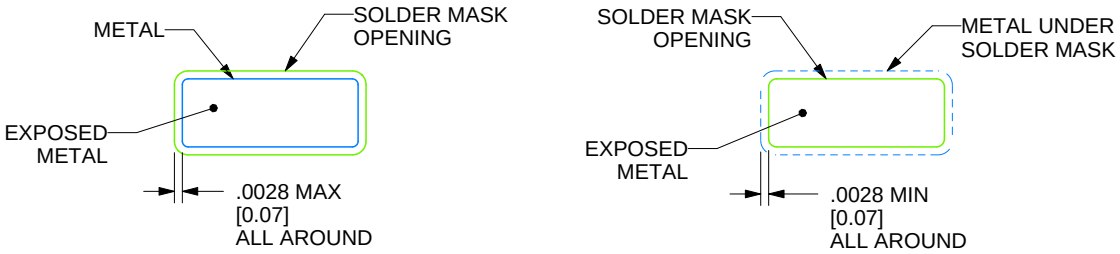


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

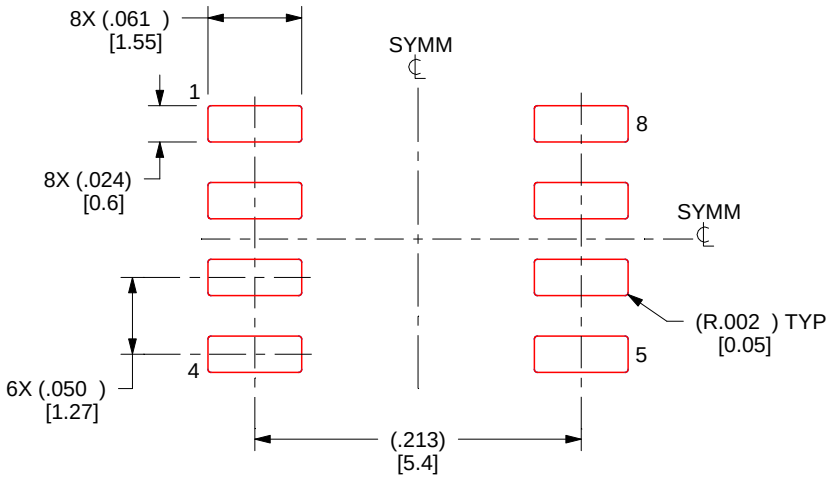
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

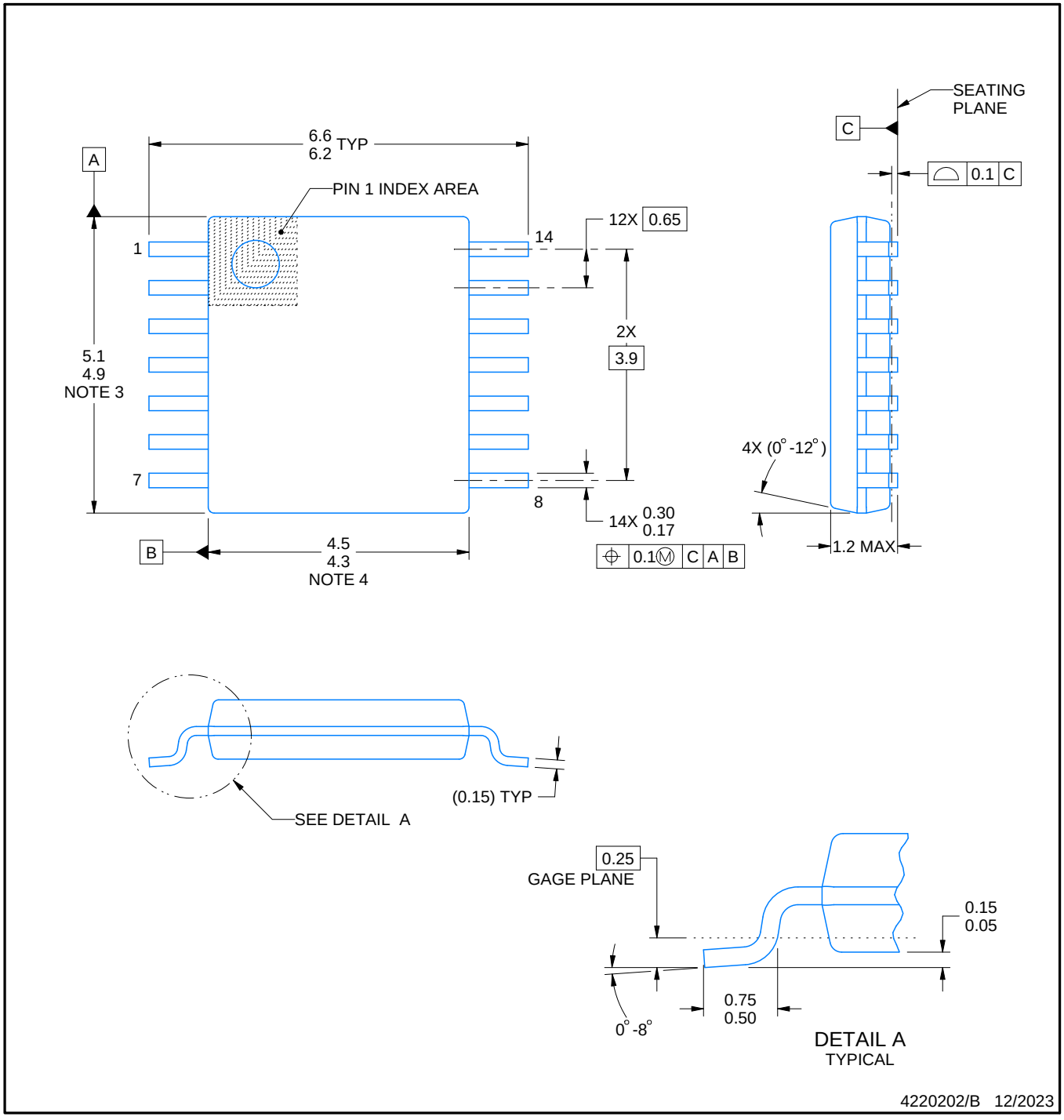
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

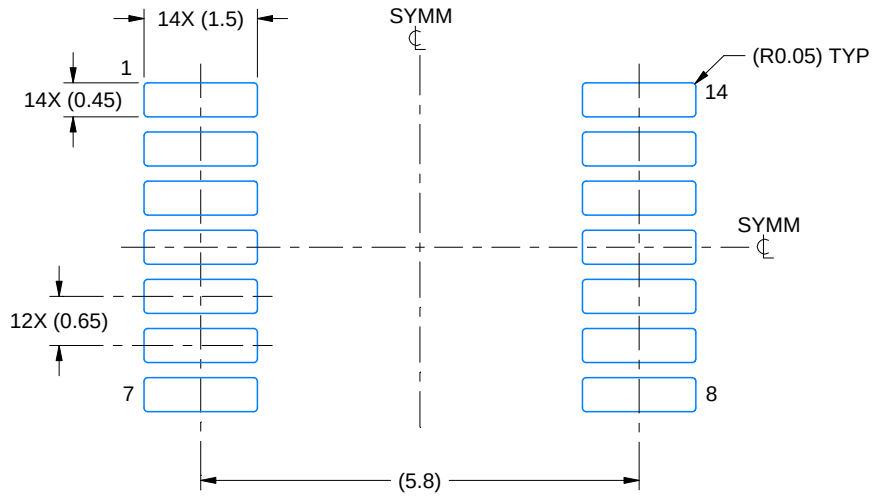
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

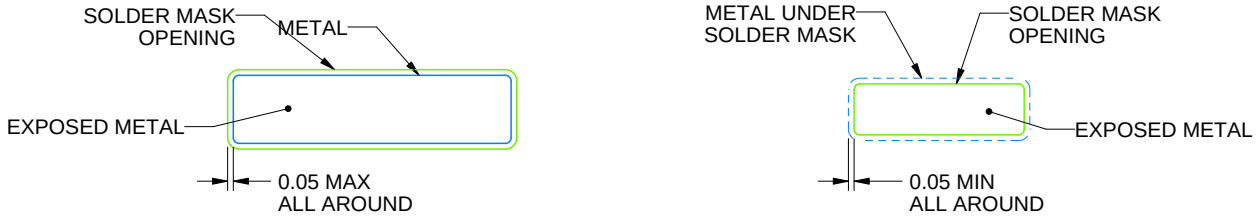


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

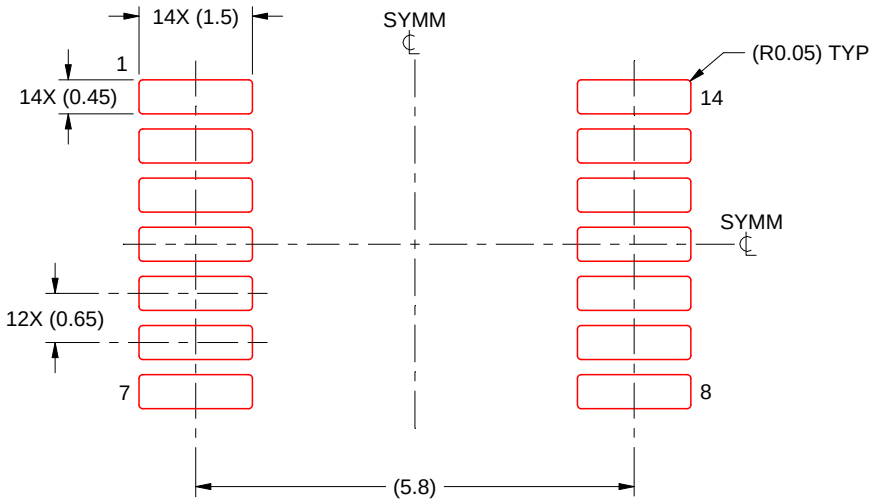


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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