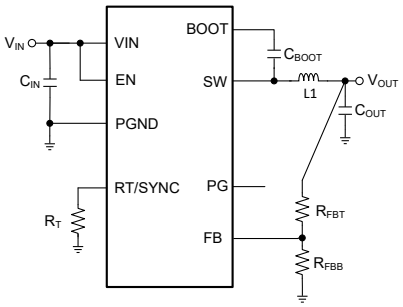
# LMR38020-Q1 具有 40µA $I_Q$ 的 4.2V 至 80V、2A、汽车类同步 SIMPLE SWITCHER® 电源转换器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C，$T_A$
- 功能安全型
  - 可提供用于功能安全系统设计的文档
- 专用于条件严苛的汽车应用
  - 输入电压范围为 4.2V 至 80V
  - 2A 持续输出电流
  - 40µA 超低工作静态电流
  - VIN 和 GND 引脚之间的距离大于 1.5mm
  - 200kHz 至 2.2MHz 可调节开关频率
  - 与外部时钟频率同步
  - 展频可降低 EMI
  - 97% 最大占空比
  - 支持带预偏置输出的启动
  - 室温下 ±1.0% 容差电压基准
  - 精密使能端
  - 器件易于使用，具有集成补偿网络，可实现较少的 BOM 数量
  - 集成同步整流
  - 采用 PowerPAD™ 集成电路封装的 8 引脚 HSOIC
  - PFM 和强制 PWM (FPWM) 选项
  - 提供 1A LMR38010-Q1
- 使用 LMR38020-Q1 并借助 WEBENCH® Power Designer 创建定制设计

## 2 应用

- 汽车逆变器和电机控制
- 汽车直流/直流转换器
- 汽车电池管理系统
- 汽车类 48V 轻混合动力 ECU 辅助电源




简化版原理图

## 3 说明

LMR38020-Q1 同步降压转换器用于在宽输入电压范围内进行调节，从而尽可能减少对外部浪涌抑制元件的需求。LMR38020-Q1 能够在输入电压突降至 4.2V 时根据需要以接近 100% 的占空比继续工作，因而是 48V 电池汽车应用和 MHEV/EV 系统的理想选择。

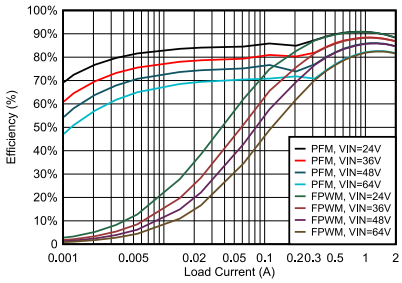
LMR38020-Q1 使用精密使能端，通过支持直接连接到宽输入电压或对器件启动和关断进行精确控制来提供灵活性。附带内置滤波和延迟功能的电源正常状态标志可提供系统状态的真实指示，免去了使用外部监控器的麻烦。该器件采用假随机展频，具有超低 EMI，并且开关频率可以在 200kHz 和 2.2MHz 之间配置，从而避开噪声敏感频带。另外，可以选择频率，从而在低工作频率下提高效率，或在高工作频率下缩小设计尺寸。

该器件具有内置的保护功能，例如逐周期电流限制、断续模式短路保护以及功耗过大情况下的热关断功能。LMR38020-Q1 符合汽车 AEC-Q100 1 级标准并采用 8 引脚 HSOIC PowerPAD 集成电路封装。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) |
|---|---|---|
| LMR38020-Q1 | DDA（HSOIC，8） | 4.89mm × 3.90mm |

(1) 有关更多信息，请参阅 节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。




效率与输出电流间的关系 $V_{OUT}$ = 5V，400kHz

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## 4 Device Comparison Table

| ORDERABLE PART NUMBER | CURRENT | FPWM | SPREAD SPECTRUM |
|---|---|---|---|
| LMR38020SQDDARQ1 | 2 A | No | Yes |
| LMR38020FSQDDARQ1 | 2 A | Yes | Yes |

## 5 Pin Configuration and Functions

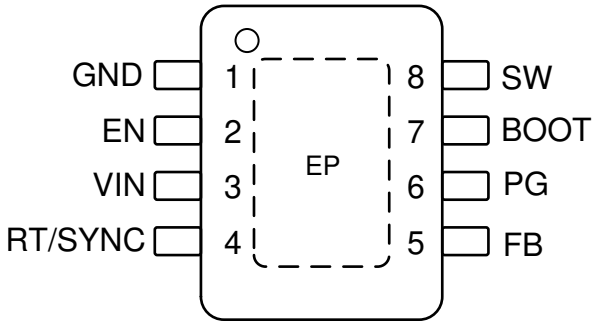



**图 5-1. DDA Package, 8-Pin HSOIC (Top View)**

**表 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 1 | G | Power and analog ground terminal. All electrical parameters are measured with respect to this pin. Connect a high-quality bypass capacitor directly to this pin and VIN with short and wide traces. |
| EN | 2 | A | Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float*. |
| VIN | 3 | P | Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND with short and wide traces. |
| RT/SYNC | 4 | A | Resistor timing or external clock input. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to frequency programming by resistor. |
| FB | 5 | A | Feedback input to the regulator. Connect to tap point of the feedback voltage divider. *Do not float*. *Do not ground*. |
| PG | 6 | A | Open-drain power-good flag output. Connect to a suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. The flag pulls low when EN = low. Can be left open when not used. |
| BOOT | 7 | P | Bootstrap supply voltage for the internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. |
| SW | 8 | P | Regulator switch node. Connect to a power inductor. |
| EP | THERMAL PAD | Thermal | Connect to system ground. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over junction temperature range of -40°C to 150°C (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN to PGND | –0.3 | 85 | V |
| | EN to PGND | –0.3 | VIN+0.3 | V |
| | FB to PGND | –0.3 | 5.5 | V |
| | RT/SYNC to PGND | –0.3 | 5.5 | V |
| Output voltage | BOOT to SW | –0.3 | 5.5 | V |
| | SW to PGND | –0.3 | 85 | V |
| | SW to PGND less than 10-ns transients | –5.0 | 85.3 | V |
| | PGOOD to PGND | –0.3 | 20 | V |
| Junction Temperature $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1)<br>Device HBM Classification Level 2 | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011<br>Device CDM Classification Level C5 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted) (1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | Input voltage range after start-up | 4.2 | | 80 | V |
| Input voltage | EN to PGND | | | VIN | V |
| Input voltage | RT to PGND | | | 5 | V |
| Input voltage | PGOOD to PGND | | | 20 | V |
| Output voltage | SW to PGND | | | 80 | V |
| Output voltage | Output voltage range for adjustable version (2) | 1 | | 75 | V |
| Frequency | Frequency adjustment range | 200 | | 2200 | kHz |
| Sync frequency | Synchronization frequency range | 300 | | 2100 | kHz |
| Load current | Output DC current range LMR38020-Q1 (3) | 0 | | 2 | A |
| Temperature | Operating junction temperature $T_J$ range (4) | –40 | | 150 | °C |

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For compliant specifications, see Electrical Characteristics table.
(2) Under no conditions should the output voltage be allowed to fall below zero volts.
(3) Maximum continuous DC current may be derated when operating with high switching frequency and/or high ambient temperature. See Application section for details.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 150℃.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LMR38020-Q1 DDA (HSOIC) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 42.9 | °C/W |
| $R_{\theta JA(Effecitve)}$ | Junction-to-ambient thermal resistance with TI EVM board | 29 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Limits apply over operating junction temperature ($T_J$ ) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN}$ = 24 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | |
| $V_{IN\_OPERATE}$ | Input operating voltage | Needed to start up | | | 4.2 | V |
| | | Once operating | | | 3.8 | V |
| $I_{Q(Non-SW)}$ | Non-switching quiescent current | $V_{EN}$ = 3.3 V (PFM variant only) | | 40 | | µA |
| $I_{SD}$ | Shutdown quiescent current; measured at VIN pin | $V_{EN}$ = 0 V | | 3 | 10 | µA |
| **ENABLE** | | | | | | |
| $V_{EN-H}$ | Enable input high level | $V_{EN}$ rising | 1.1 | 1.25 | 1.4 | V |
| $V_{EN-L}$ | Enable input low level | $V_{EN}$ falling | 0.95 | 1.10 | 1.22 | V |
| $I_{LKG-EN}$ | Enable input leakage current | $V_{EN}$ = 3.3V | | 5.0 | | nA |
| **VOLTAGE REFERENCE (FB PIN)** | | | | | | |
| $V_{REF}$ | Feedback reference voltage | Vin=4.2V to 80V, $T_J$=25°C, FPWM | 0.99 | 1 | 1.01 | V |
| $V_{REF}$ | Feedback reference voltage | FPWM | 0.985 | 1 | 1.015 | V |
| $I_{LKG-FB}$ | Feedback leakage current | FB = 1.2 V | | 2.1 | | nA |
| **CURRENT LIMITS AND HICCUP** | | | | | | |
| $I_{HS-LIMIT}$ | High-side current limit(2) | 2A Version | 2.6 | 3.2 | 3.8 | A |
| $I_{LS-LIMIT}$ | Low-side current limit(2) | 2A Version | 1.8 | 2.3 | 2.8 | A |
| $I_{L-ZC}$ | Zero cross detector threshold | PFM variants only | | 0.01 | | A |
| $I_{PEAK-MIN}$ | Minimum inductor peak current(2) | 2A Version, PFM variants only | | 0.5 | | A |
| $I_{L-NEG}$ | Negative current limit(2) | 2A Version, FPWM variant only | | –0.9 | | A |
| **POWER STAGE** | | | | | | |
| $R_{DS-ON-HS}$ | High-side MOSFET ON-resistance | | | 303 | | mΩ |
| $R_{DS-ON-LS}$ | Low-side MOSFET ON-resistance | | | 133 | | mΩ |
| $t_{ON-MIN}$ | Minimum switch on-time(3) | VIN =24 V, Iout = 1 A | | 80 | 131 | ns |
| $t_{OFF-MIN}$ | Minimum switch off-time | | | 190 | 300 | ns |
| $t_{ON-MAX}$ | Maximum switch on-time | | | 5 | | us |
| **SWITCHING FREQUENCY AND SYNCHRONIZATION** | | | | | | |
| $F_{OSC}$ | Switching frequency | $R_T$ = 64.9 kΩ | 320 | 400 | 480 | kHz |

## 6.5 Electrical Characteristics（续）

Limits apply over operating junction temperature ($T_J$) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN}$ = 24 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $F_{SPREAD}$ | Spread of internal oscillator with Spread Spectrum Enabled | | -8 | | 8 | % |
| VSYNC_HI | SYNC clock high level threshold | | | | 2 | V |
| VSYNC_LO | SYNC clock low level threshold | | 0.6 | | | V |
| $t_{PULSE\_H}$ | High duration needed to be recognized as a pulse | | | | 50 | ns |
| $C_{LOCK}$ | Time needed for clock to lock to a valid synchronization signal in sync cycles | | | | 230 | us |
| **STARTUP AND TRACKING** | | | | | | |
| $t_{SS}$ | Internal soft-start time | | | 4 | | ms |
| **POWER GOOD** | | | | | | |
| $V_{PG-HIGH-UP}$ | Power-Good upper threshold - rising | % of FB voltage | 110% | 112% | 114% | |
| $V_{PG-LOW-DN}$ | Power-Good lower threshold - falling | % of FB voltage | 90% | 92% | 94% | |
| $V_{PG-HYS}$ | Power-Good hysteresis (rising & falling) | % of FB voltage | | 2.2% | | |
| $V_{PG-VALID}$ | Minimum input voltage for proper Power-Good function | | | | 2 | V |
| $R_{PG}$ | Power-Good on-resistance | $V_{EN}$ = 0 V | | 140 | | Ω |
| $R_{PG}$ | Power-Good on-resistance | $V_{EN}$ = 3.3V | | 92 | | Ω |
| $t_{PGDFLT(fall)}$ | Glitch filter time constant for PGOOD function | | | 40 | | us |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD-Rising}$ (4) | Thermal shutdown | Shutdown threshold | | 163 | | ℃ |
| $T_{SD-Falling}$ (4) | Thermal shutdown | Recovery threshold | | 150 | | ℃ |

(1) MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.
(3) Not production tested. Specified by correlation by design at 1A load
(4) Not production tested. Specified by design

## 6.6 System Characteristics

The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to $T_J$ = 25℃ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J$ = –40℃ to 150℃. *These specifications are not ensured by production testing.*

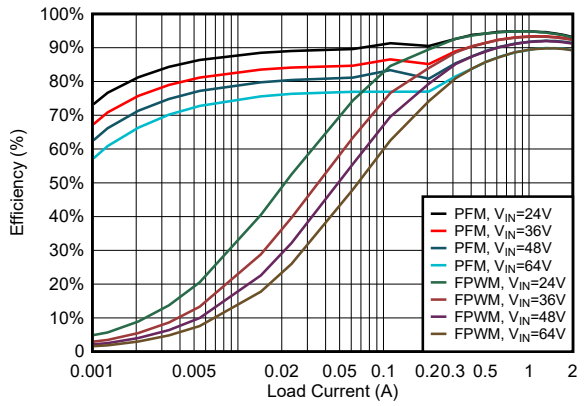
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating input voltage range | | 4.2 | | 80 | V |
| $V_{OUT}$ | Adjustable output voltage regulation(1) | PFM operation | –1.5% | | 2.5% | |
| $V_{OUT}$ | Adjustable output voltage regulation(1) | FPWM operation | –1.5% | | 1.5% | |
| $I_{SUPPLY}$ | Input supply current when in regulation | $V_{IN}$ = 24 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 0 A, $R_{FBT}$ = 1 MΩ, PFM variant | | 40 | | µA |
| $D_{MAX}$ | Maximum switch duty cycle(2) | | | 97% | | |
| $V_{HC}$ | FB pin voltage required to trip short-circuit hiccup mode | | | 0.4 | | V |
| $t_D$ | Switch voltage dead time | | | 5 | | ns |
| $T_{SD}$ | Thermal shutdown temperature | Shutdown temperature | | 163 | | °C |
| $T_{SD}$ | Thermal shutdown temperature | Recovery temperature | | 150 | | °C |

(1) Deviation in $V_{OUT}$ from nominal output voltage value at $V_{IN}$ = 24 V, $I_{OUT}$ = 0 A to full load

(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $F_{MIN} = 1 / (t_{ON\text{-}MAX} + t_{OFF\text{-}MIN})$. $D_{MAX} = t_{ON\text{-}MAX} / (t_{ON\text{-}MAX} + t_{OFF\text{-}MIN})$.

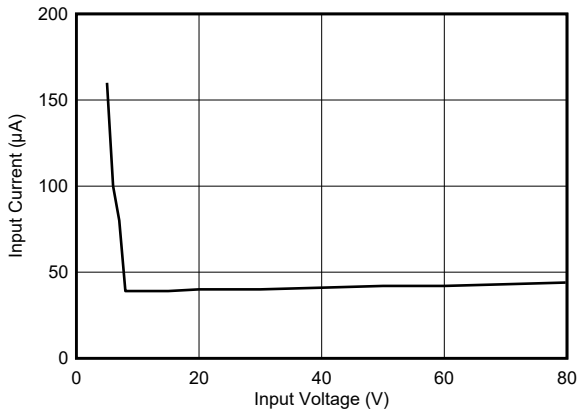
## 6.7 Typical Characteristics

Unless otherwise specified the following conditions apply: $T_A$ = 25°C, $V_{IN}$ = 24 V, $f_{SW}$ = 400 kHz



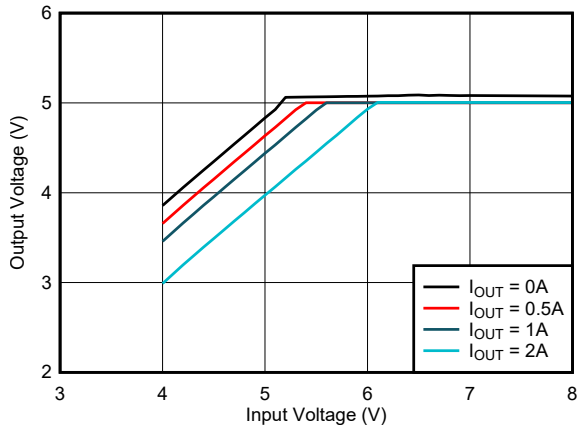

$F_{SW}$ = 400 kHz $V_{OUT}$ = 12.0 V

**图 6-1. Efficiency vs Load Current**



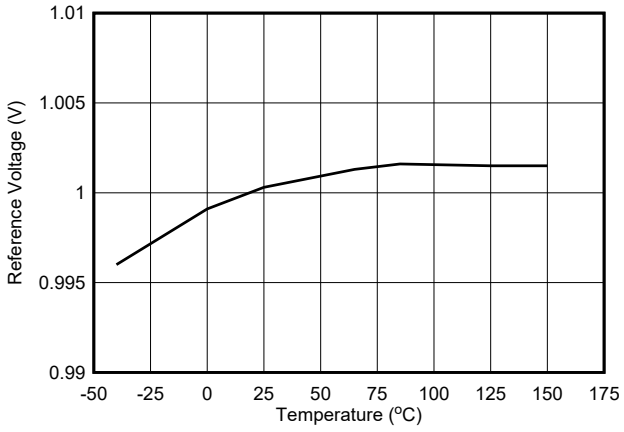

$V_{OUT}$ = 5 V $R_{FBB}$ = 100 k L = 15 µH (PFM)

**图 6-2. No Load Input Current vs Input Voltage**



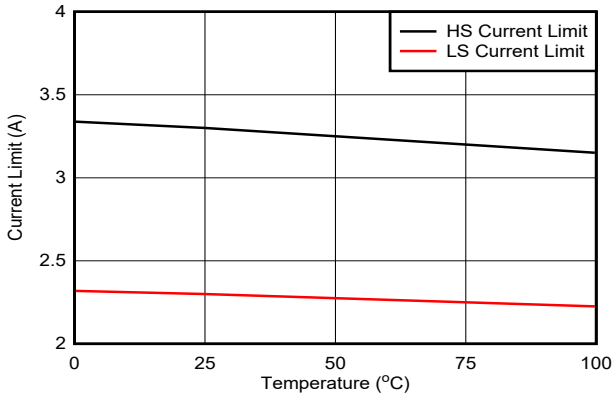

$F_{SW}$ = 400 kHz $V_{OUT}$ = 5.0 V PFM version

**图 6-3. 5-V Dropout**




Input voltage = 48 V $I_{OUT}$ = 2 A FPWM version

**图 6-4. Reference Voltage vs Temperature**




$V_{OUT}$ = 5.0 V FPWM version

**图 6-5. High-Side and Low-Side Current Limit vs Temperature**

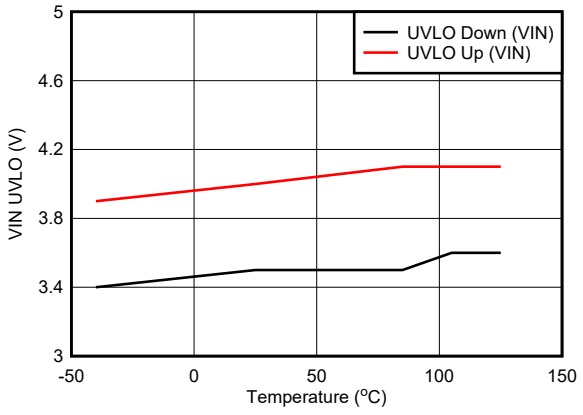



**图 6-6. $V_{IN}$ UVLO vs Temperature**

# 7 Detailed Description

## 7.1 Overview

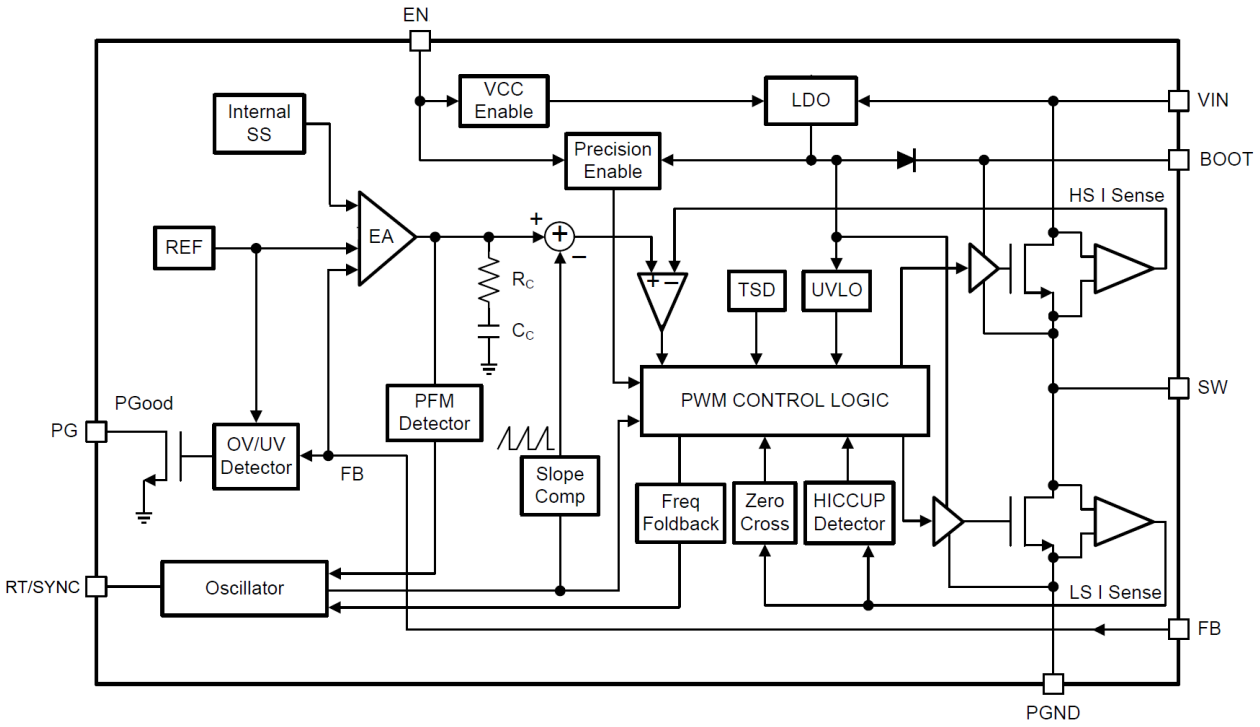
The LMR38020-Q1 converter is an easy-to-use synchronous step-down DC/DC converter that operates from a 4.2-V to 80-V supply voltage. The device is capable of delivering up to 2-A DC load current in a small solution size. The LMR38020-Q1 employs peak-current mode control. The device enters PFM mode at light load to achieve high efficiency for PFM version. A FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time, and requires few external components.

Additional features, such as precision enable and internal soft start, provide a flexible and easy-to-use solution for a wide range of applications. Protection features include the following:

- Thermal shutdown
- $V_{IN}$ undervoltage lockout
- Cycle-by-cycle current limit
- Hiccup mode short-circuit protection

The family requires very few external components and has a pinout designed for a simple, optimal PCB layout.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Fixed Frequency Peak Current Mode Control

The LMR38020-Q1 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR38020-Q1 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During high-side switch on time, the SW pin voltage swings up to approximately $V_{IN}$, and the inductor current, $i_L$, increases with a linear slope ($V_{IN}$ – $V_{OUT}$) / L. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of – $V_{OUT}$ / L. The

control parameter of a buck converter is defined as Duty Cycle D = $t_{ON}$ / $T_{SW}$, where $t_{ON}$ is the high-side switch on time and $T_{SW}$ is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = $V_{OUT}$ / $V_{IN}$.

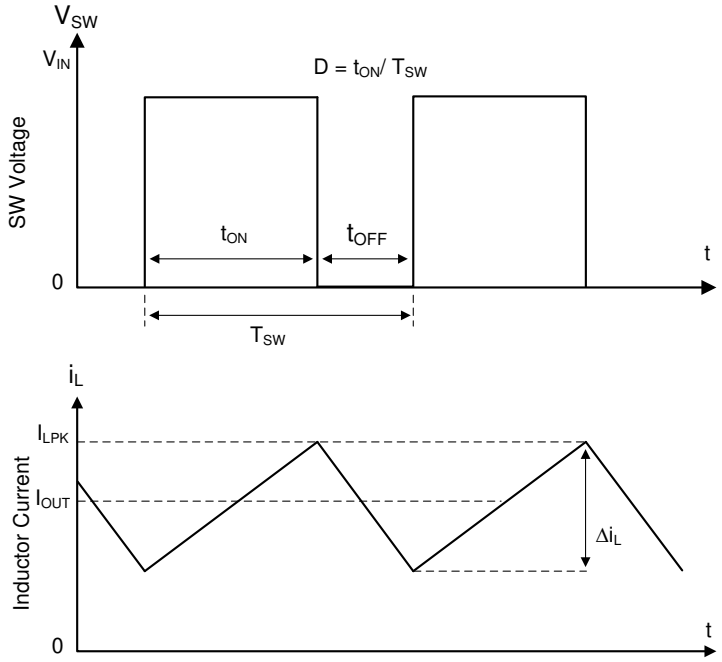



**图 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)**

The LMR38020-Q1 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the on time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making it easy to design and providing stable operation with almost any combination of output capacitors. The converter operates with fixed switching frequency at normal load condition. At light-load condition, the LMR38020-Q1 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

### 7.3.2 Adjustable Output Voltage

A precision 1.0-V reference voltage ($V_{REF}$) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from the output voltage to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor $R_{FBB}$ for the desired divider current and use 方程式 1 to calculate the top-side resistor $R_{FBT}$. TI recommends $R_{FBT}$ in the range from 10 kΩ to 100 kΩ for most applications. A lower $R_{FBT}$ value can be used if static loading is desired to reduce $V_{OUT}$ offset in PFM operation. Lower $R_{FBT}$ reduces efficiency at very light load. Less static current goes through a larger $R_{FBT}$ and can be more desirable when light-load efficiency is critical. TI does not recommend $R_{FBT}$ larger than 1 MΩ because it makes the feedback path more susceptible to noise. Larger $R_{FBT}$ values require more carefully designed feedback path on the PCB. The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

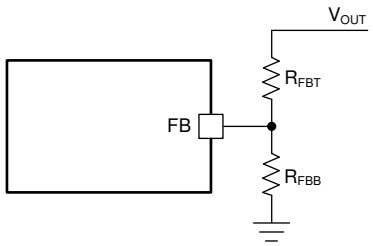



**图 7-2. Output Voltage Setting**

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

### 7.3.3 Enable

The voltage on the EN pin controls the ON or OFF operation of the LMR38020-Q1. A voltage below 0.95 V shuts the device down, while a voltage above 1.4 V is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR38020-Q1 is to connect the EN to VIN. This allows self-start-up of the LMR38020-Q1 when $V_{IN}$ is within the operating range.

Many applications benefit from the employment of an enable divider $R_{ENT}$ and $R_{ENB}$ (图 7-3) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. System UVLO can be used for sequencing, making sure the user has reliable operation or supply protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection. Note that the EN pin voltage must never be higher than $V_{IN}$ + 0.3 V.

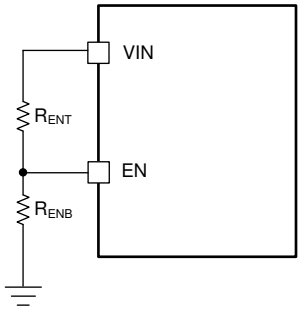



**图 7-3. System UVLO by Enable Divider**

### 7.3.4 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the LMR38020-Q1 can be programmed by the resistor RT from the RT/SYNC pin and GND pin. The RT/SYNC pin cannot be left floating or shorted to ground. To determine the timing resistance for a given switching frequency, use 方程式 2 or the curve in 图 7-4. 表 7-1 gives typical $R_T$ values for a given $f_{SW}$.

$$R_T(k\Omega) = 30970 \times f_{SW}(kHz)^{-1.027} \quad (2)$$

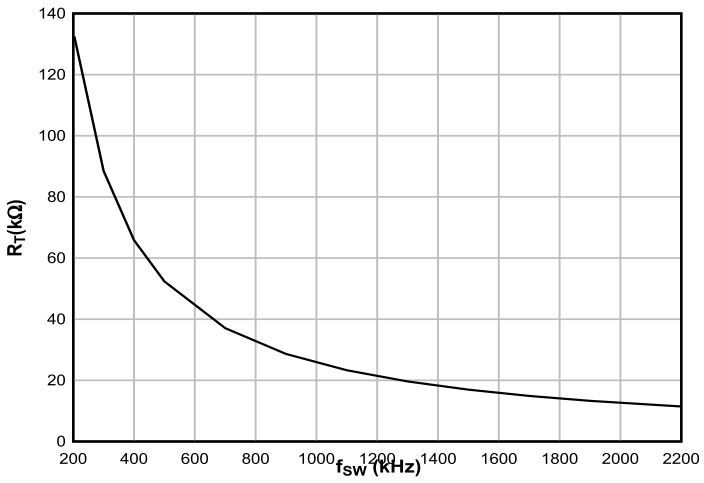



图 7-4. $R_T$ Versus Frequency Curve

表 7-1. Typical Frequency Setting $R_T$ Resistance

| $f_{SW}$ (kHz) | $R_T$ (kΩ) |
|---|---|
| 200 | 133 |
| 400 | 64.9 |
| 500 | 52.3 |
| 750 | 34.8 |
| 1000 | 25.5 |
| 1500 | 16.9 |
| 2000 | 12.7 |
| 2200 | 11.5 |

The LMR38020-Q1 switching action can also be synchronized to an external clock from 300 kHz to 2.1 MHz. Connect a square wave to the RT/SYNC pin through either circuit network shown in 图 7-5. The internal oscillator is synchronized by the falling edge of external clock. The recommendations for the external clock include: high level no lower than 2.0 V, low level no higher than 0.6 V, and have a pulse width greater than 50 ns. When using a low impedance signal source, the frequency setting resistor $R_T$ is connected in parallel with an AC coupling capacitor, $C_{COUP}$, to a termination resistor, $R_{TERM}$ (for example, 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10-pF ceramic capacitor can be used for $C_{COUP}$.

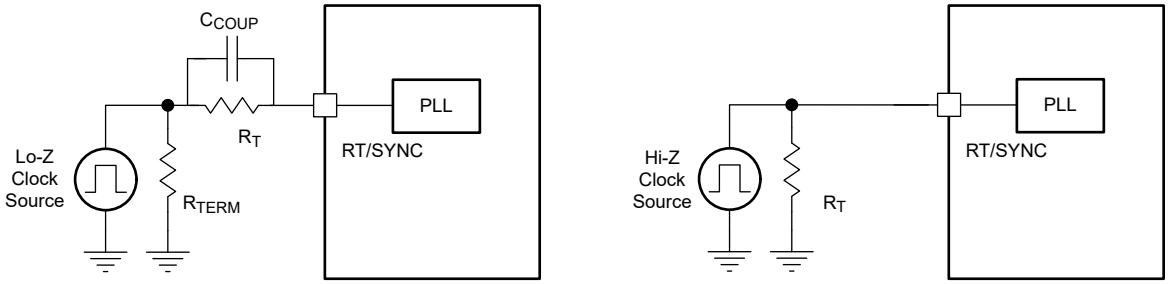



图 7-5. Synchronizing to an External Clock

### 7.3.5 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR38020-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault

conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions lasting less than $t_{PG}$ do not trip the power-good flag. Note that during initial power up, a delay of approximately 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open-drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or $V_{OUT}$, through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is greater than or equal to 2 V (typical). Limit the current into the power-good flag pin to less than 5-mA D.C. The maximum current is internally limited to approximately 35 mA when the device is enabled and approximately 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.

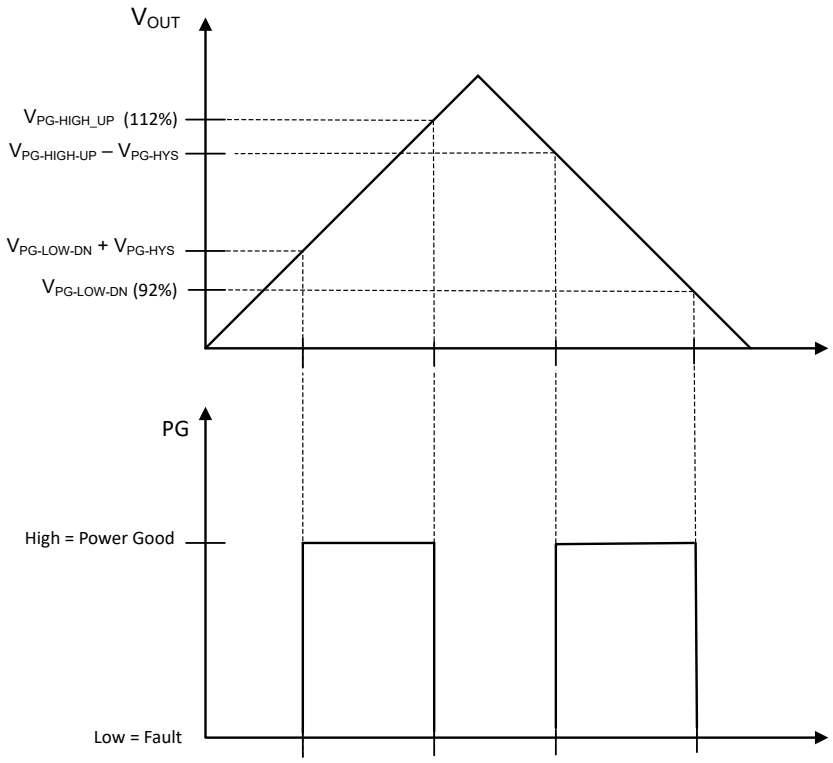



**图 7-6. Static Power-Good Operation**

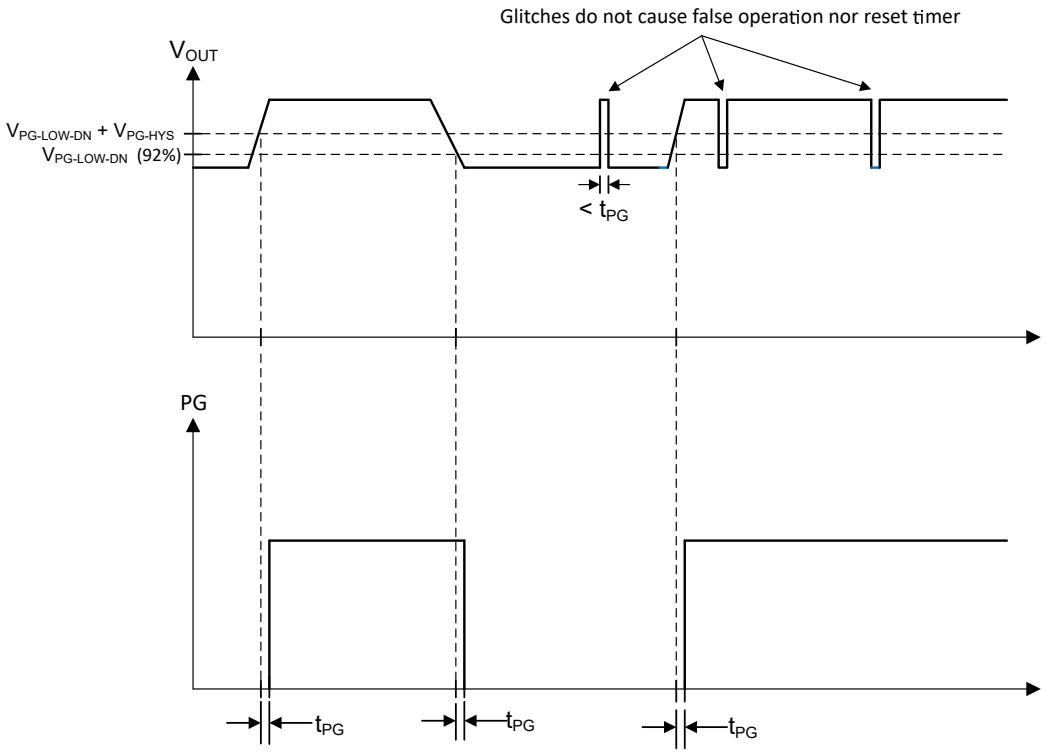



**图 7-7. Power-Good Timing Behavior**

### 7.3.6 Minimum On Time, Minimum Off Time, and Frequency Foldback

Minimum on time ($T_{ON\_MIN}$) is the smallest duration of time that the high-side switch can be on. $T_{ON\_MIN}$ is typically 75 ns in the LMR38020-Q1. Minimum off time ($T_{OFF\_MIN}$) is the smallest duration that the high-side switch can be off. $T_{OFF\_MIN}$ is typically 190 ns. In CCM operation, $T_{ON\_MIN}$ and $T_{OFF\_MIN}$ limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = T_{ON-MIN} \times f_{SW} \quad (3)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - (T_{OFF-MIN} \times f_{SW}) \quad (4)$$

Given a required output voltage, the maximum $V_{IN}$ without frequency foldback can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{T_{ON-MIN} \times f_{SW}} \quad (5)$$

The minimum $V_{IN}$ without frequency foldback can be calculated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - (T_{OFF-MIN} \times f_{SW})} \quad (6)$$

In the LMR38020-Q1, a frequency foldback scheme is employed after $T_{ON\_MIN}$ or $T_{OFF\_MIN}$ is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while $V_{IN}$ voltage increases. After the on time decreases to $T_{ON\_MIN}$, the switching frequency starts to decrease while $V_{IN}$ continues to go up, which lowers the duty cycle further to keep $V_{OUT}$ in regulation according to 方程式 3.

The frequency foldback scheme also works after larger duty cycle is needed under low $V_{IN}$ condition. The frequency decreases after the device hits its $T_{OFF\_MIN}$, which extends the maximum duty cycle according to 方程式 4. In such condition, the frequency can be as low as approximately 133 kHz minimum. Wide range of frequency foldback allows the LMR38020-Q1 output voltage stay in regulation with a much lower supply voltage $V_{IN}$, which leads to a lower effective dropout.

The fixed frequency operation at FPWM mode with switching frequency greater than 1.2 MHz, is maintained with minimum load current about 100 mA for wider input voltage range. And for very light load and switching frequency over 1.2 MHz, frequency drop can be expected during mintoff frequency foldback.

With frequency foldback, $V_{IN\_MAX}$ is raised, and $V_{IN\_MIN}$ is lowered by decreased $f_{SW}$.

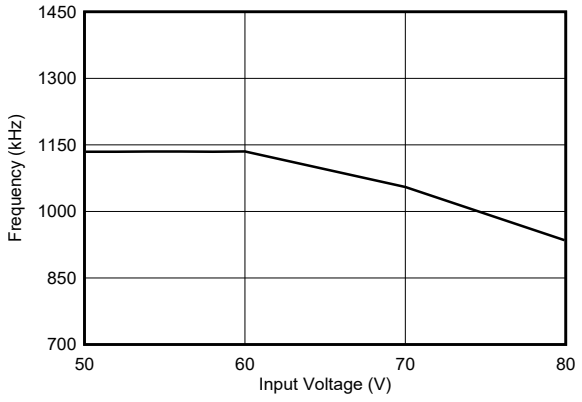



图 7-8. Typical Frequency Foldback at $T_{ON\_MIN}$

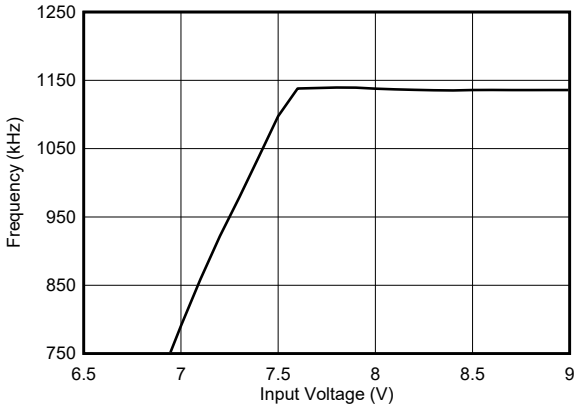



图 7-9. Typical Frequency Foldback at $T_{OFF\_MIN}$

### 7.3.7 Bootstrap Voltage

The LMR38020-Q1 provides an integrated bootstrap voltage converter. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the bootstrap capacitor is 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher for stable performance over temperature and voltage.

### 7.3.8 Overcurrent and Short Circuit Protection

The LMR38020-Q1 is protected from overcurrent conditions by cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode is activated if a fault condition persists to prevent overheating.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch current is compared to the output of the error amplifier (EA) minus slope compensation every switching cycle. The peak current of high-side switch is limited by a clamped maximum peak current threshold, $I_{HS\text{-}LIMIT}$, which is constant.

The current going through the low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is turned OFF at the end of a switching cycle if its current is above the low-side current limit, $I_{LS\_LIMIT}$. The low-side switch is kept on so that inductor current keeps ramping down until the inductor current ramps below the $I_{LS\_LIMIT}$. Then the low-side switch is turned OFF and the high-side switch is turned on after a dead time. This is somewhat different to the more typical peak current limit and results in 方程式 7 for the maximum load current.

If the feedback voltage is lower than 40% of $V_{REF}$, the current of the low-side switch triggers $I_{LS\_LIMIT}$ for 256 consecutive cycles and hiccup current protection mode is activated. In hiccup mode, the converter shuts down and stays off for a period of hiccup, $T_{HICCUP}$ (76-ms typical), before the LMR38020-Q1 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions and prevents overheating and potential damage to the device.

$$I_{OUT_{MAX}} = I_{LS} + \left(\frac{V_{IN} - V_{OUT}}{L \times 2 \times f_{SW}}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For FPWM version, the inductor current is allowed to go negative. When this current exceeds the low-side negative current limit, $I_{LS\_NEG}$, the low-side switch is turned off and high-side switch is turned on immediately. This is used to protect the low-side switch from excessive negative current.

### 7.3.9 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LMR38020-Q1 and the input power supply. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. The typical soft-start time is 4.0 ms.

The LMR38020-Q1 also employs overcurrent protection blanking time, $T_{OCP\_BLK}$ (18-ms typical), at the beginning of power up. Without this feature, in applications with a large amount of output capacitors and high $V_{OUT}$, the inrush current is large enough to trigger current-limit protection, which can make the device enter into hiccup mode. The device tries to restart after the hiccup period, then hits the current limit and enters into hiccup mode again, so $V_{OUT}$ cannot ramp up to the setting voltage ever. By introducing the OCP blanking feature, the hiccup protection function is disabled during $T_{OCP\_BLK}$, and LMR38020-Q1 charges the $V_{OUT}$ with its maximum limited current, which maximizes the output current capacity during this period. Note that the peak current limit ($I_{HS\_LIMIT}$) and valley current limit ($I_{LS\_LIMIT}$) protection functions are still available during $T_{OCP\_BLK}$, so there is no concern of inductor current running away.

### 7.3.10 Thermal Shutdown

The LMR38020-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 163°C. Both high-side and low-side FETs stop switching in thermal shutdown. After the die temperature falls below 150°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

## 7.4 Device Functional Modes

### 7.4.1 Auto Mode

In auto mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM.

In PWM, the regulator operates as a constant frequency, current mode, full-synchronous converter using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK\text{-}MIN}$. The frequency of these bursts is adjusted to regulate the output, while diode emulation is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depend on the input voltage, output voltage, and load.

### 7.4.2 Forced PWM Operation

The forced PWM option is choiced for cases when constant frequency operation is more important than light-load efficiency.

In FPWM operation, the diode emulation feature is turned off. This means that the device remains in CCM under light loads. Under conditions where the device must reduce the on time or off time below the compliant minimum to maintain regulation, the frequency reduces to maintain the effective duty cycle required for regulation. This occurs for very high and very low input and output voltage ratios. In FPWM mode, a limited reverse current is allowed through the inductor, allowing power to pass from the output of the regulator to the input of the regulator. Note that in FPWM mode, larger currents pass through the inductor, if lightly loaded, than in auto mode. After loads are heavy enough to necessitate CCM operation, FPWM mode has no measurable effect on regulator operation.

### 7.4.3 Dropout

The dropout performance of any buck regulator is affected by the $R_{DSON}$ of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage is reduced to the output voltage, the off time of the high-side MOSFET starts to approach the minimum value.

Beyond this point, the switching can become erratic and the output voltage falls out of regulation. To avoid this problem, the LMR38020-Q1 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet, the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of the nominal value. Under this condition, the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4-V short circuit detection threshold is not activated when in dropout mode.

### 7.4.4 Minimum Switch On Time

Every switching regulator has a minimum controllable on time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR38020-Q1 automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage for a given output voltage, before frequency foldback occurs, is found in 方程式 8 . As the input voltage is increased, the switch on time (duty cycle) reduces to regulate the output voltage. When the on time reaches the limit, the switching frequency drops, while the on time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \times f_{SW}} \tag{8}$$

# 8 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 8.1 Application Information

The LMR38020-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMR38020-Q1. Alternately, use the WEBENCH Design Tool to generate a complete design. This tool uses an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

**备注**

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

## 8.2 Typical Application

图 8-1 shows a typical application circuit for the LMR38020-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick-start guide, 表 8-1 provides typical component values for a range of the most common output voltages.

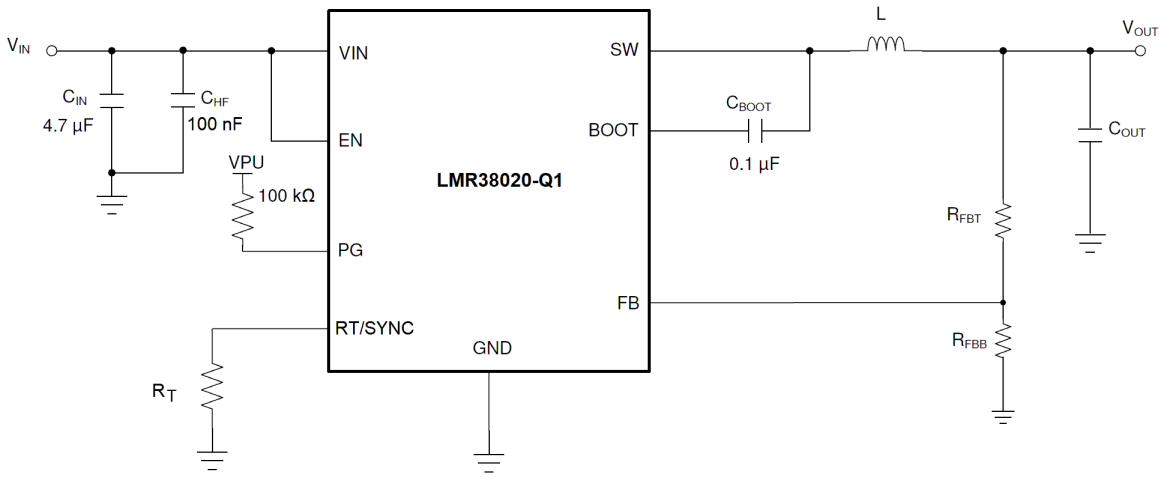



图 8-1. Example Application Circuit

表 8-1. Typical External Component Values for 2-A Output Current

| $f_{SW}$ (kHz) | $V_{IN}$ (V) Typical | $V_{OUT}$ (V) | L (µH) | NOMINAL $C_{OUT}$ (RATED CAPACITANCE) | MINIMUM $C_{OUT}$ (RATED CAPACITANCE) | $R_{FBT}$ (Ω) | $R_{FBB}$ (Ω) |
|---|---|---|---|---|---|---|---|
| 400 | 48 | 5 | 15 | 3 × 22 µF | 2 × 22 µF | 100 k | 24.9 k |
| 1000 | 24 | 5 | 6.8 | 2 × 22 µF | 2 × 15 µF | 100 k | 24.9 k |
| 400 | 48 | 12 | 33 | 1× 22 µF | 1 × 15 µF | 100 k | 9.09 k |
| 1000 | 24 | 12 | 10 | 2 × 10 µF | 1 × 10 µF | 100 k | 9.09 k |
| 500 | 48 | 24 | 47 | 1 × 22 µF | 1 × 15 µF | 100 k | 4.32 k |

### 8.2.1 Design Requirements

节 8.2.2 provides a detailed design procedure based on 表 8-2.

表 8-2. Detailed Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 6 V to 80 V |
| Output voltage | 5 V |
| Maximum output current | 0 A to 2 A |
| Switching frequency | 400 kHz |

### 8.2.2 Detailed Design Procedure

The following design procedure applies to 图 8-1 and 表 8-1.

#### *8.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the LMR38020-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### *8.2.2.2 Choosing the Switching Frequency*

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 400 kHz is used.

#### *8.2.2.3 FB for Adjustable Output*

In an adjustable output voltage version, pin 5 of the device is FB. The output voltage of the LMR38020-Q1 is externally adjustable using an external resistor divider network. The divider network is comprised of $R_{FBT}$ and $R_{FBB}$ and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, $V_{REF}$. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity, but also reduce the light-load efficiency. The recommended value for $R_{FBT}$ is 100 kΩ with a maximum value of 1 MΩ. After $R_{FBT}$ is selected, 方程式 9 is used to select $R_{FBB}$. $V_{REF}$ is nominally 1 V.

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{9}$$

For this 5-V example, $R_{FBT}$ = 100 kΩ and $R_{FBB}$ = 24.9 kΩ is chosen.

#### *8.2.2.4 Inductor Selection*

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. 方程式 10 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, choose K = 0.4 and find an inductance of L = 14 µH. Select the next standard value of L = 15 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUT_{max}}} \times \frac{V_{OUT}}{V_{IN}} \tag{10}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{SC}$. This makes sure that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{LIMIT}$, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above

approximately 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, the inductance value must not be less than that given in 方程式 11:

$$L_{MIN} \geq M \times \frac{V_{OUT}}{f_{SW}} \quad (11)$$

where

- $L_{MIN}$ = minimum inductance (H)
- M = 0.25 for a 2-A device
- $f_{SW}$ = switching frequency (Hz)

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

#### *8.2.2.5 Output Capacitor Selection*

The current mode control scheme of the LMR38020-Q1 devices allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Refer to 表 8-1 for typical output capacitor values for 5-V to 24-V output voltages. For a 5-V output design, TI recommends 3 × 22-µF ceramic output capacitors for this example. For other designs with other output voltages, WEBENCH can be used as a starting point for selecting the value of output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to approximately 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

#### *8.2.2.6 Input Capacitor Selection*

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7 µF is required on the input of the LMR38020-Q1. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF to 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example, a 4.7-µF, 100-V, X7R (or better) ceramic capacitor is chosen. The 100 nF must also be rated at 100 V with an X7R dielectric.

Using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from 方程式 12 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \quad (12)$$

#### 8.2.2.7 $C_{BOOT}$

The LMR38020-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

#### 8.2.2.8 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 8-2. The turn-on voltage is designated as $V_{ON}$ while the turn-off voltage is $V_{OFF}$. First, a value for $R_{ENB}$ is chosen in the range of 10 kΩ to 100 kΩ, then 方程式 13 and 方程式 14 are used to calculate $R_{ENT}$ and $V_{OFF}$.

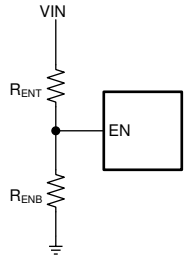



**图 8-2. Setup for External UVLO Application**

$$R_{ENT} = R_{ENB} \times \left( \frac{V_{ON}}{V_{EN-H}} - 1 \right) \quad (13)$$

$$V_{OFF} = V_{EN-L} \times \left( \frac{V_{ON}}{V_{EN-H}} \right) \quad (14)$$

where

- $V_{ON}$ = $V_{IN}$ turn-on voltage
- $V_{OFF}$ = $V_{IN}$ turn-off voltage

#### 8.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the device dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature ($T_J$) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum junction temperature for the LMR38020-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. 方程式 15 shows the relationships between the important parameters. Seeing that larger ambient temperatures ($T_A$) and larger values of $R_{\theta JA}$ reduce the maximum available output current is easy. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* , the values given in the *Thermal Information* are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT_{MAX}} = \left( \frac{T_J - T_A}{R_{\theta JA}} \right) \times \left( \frac{\eta}{1-\eta} \right) \times \left( \frac{1}{V_{OUT}} \right) \quad (15)$$

where

- $\eta$ = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

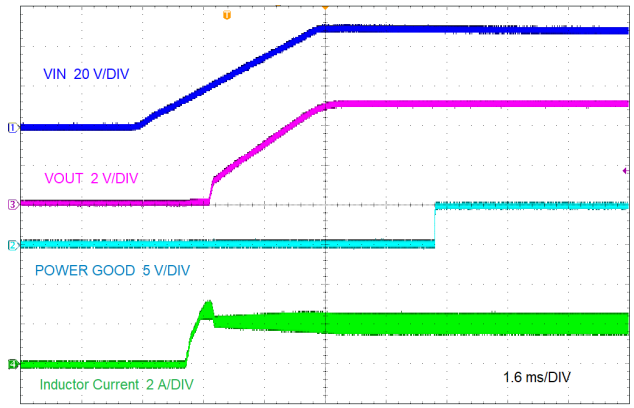
- Power dissipation
- Air temperature, flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* application report
- *Semiconductor and IC Package Thermal Metrics* application report
- *How to Properly Evaluate Junction Temperature with Thermal Metrics* application report
- *Using New Thermal Metrics* application report

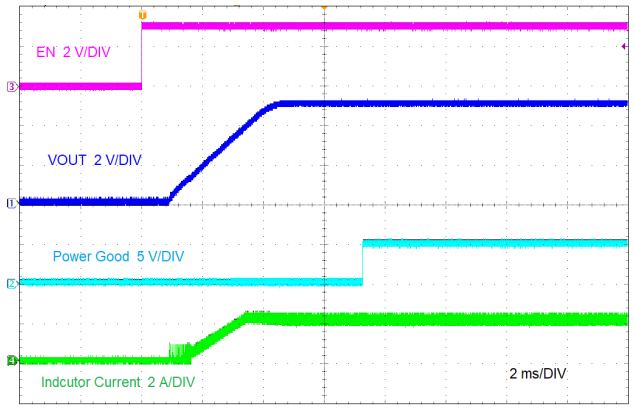
### 8.2.3 Application Curves

Unless otherwise specified the following conditions apply: $V_{IN}$ = 48 V, L = 15 µH , $T_A$ = 25°C.



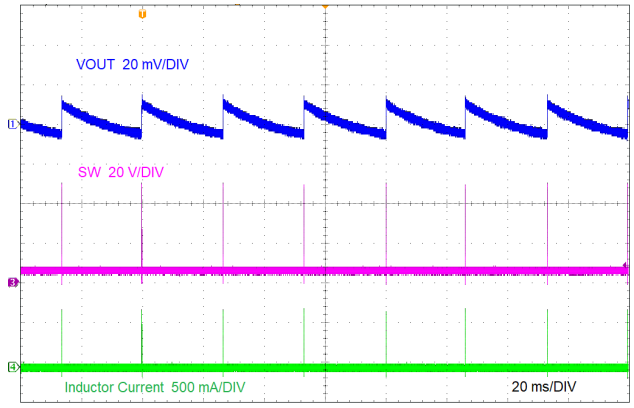

LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz

**图 8-3. Start-Up by VIN**



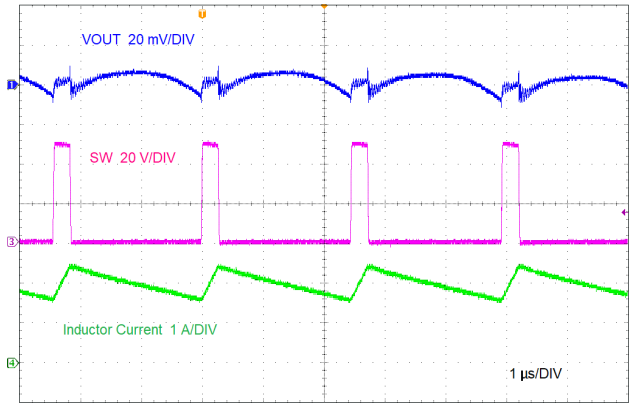

LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz

**图 8-4. Start-Up by EN**



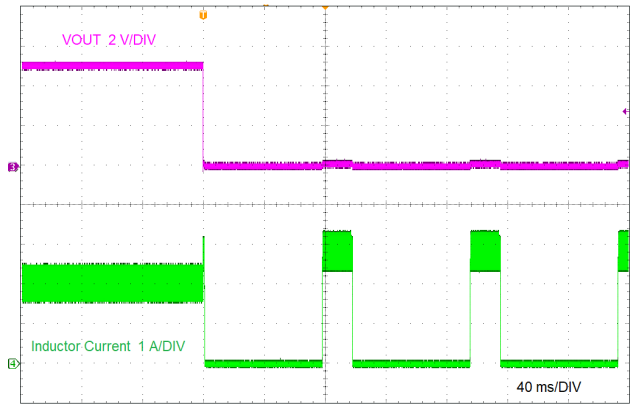

LMR38020-Q1 $V_{OUT}$ = 5 V No Load
AC Coupled

**图 8-5. PFM Switching**



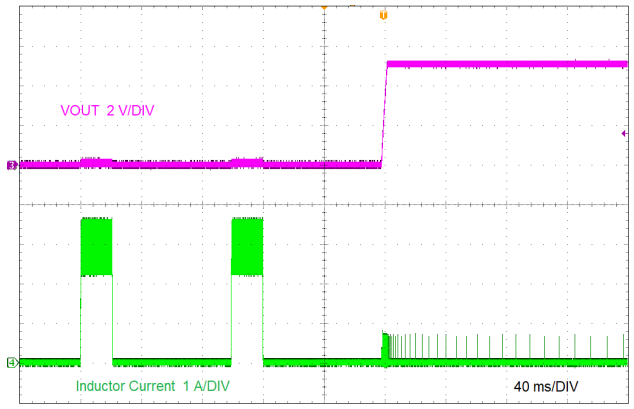

LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz
AC Coupled

**图 8-6. Full Load Switching**



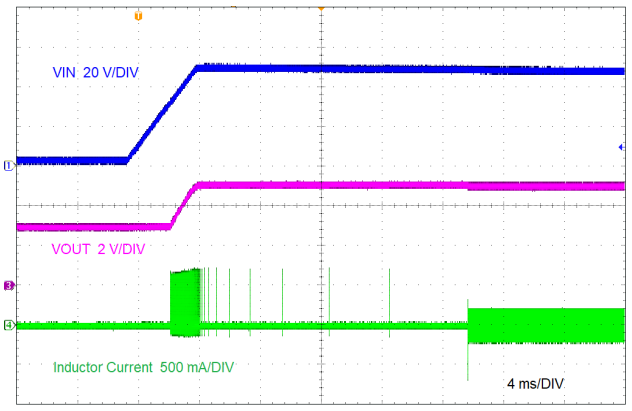

LMR38020-Q1 $V_{OUT}$ = 5 V 2 A to Short

**图 8-7. Short Circuit Applied**



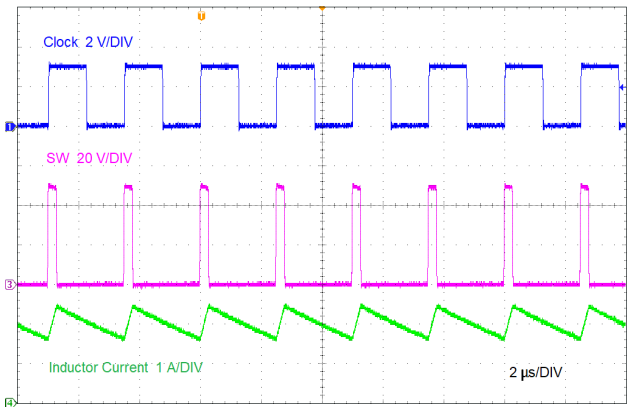

LMR38020-Q1 $V_{OUT}$ = 5 V Short Recovery

**图 8-8. Short-Circuit Recovery**



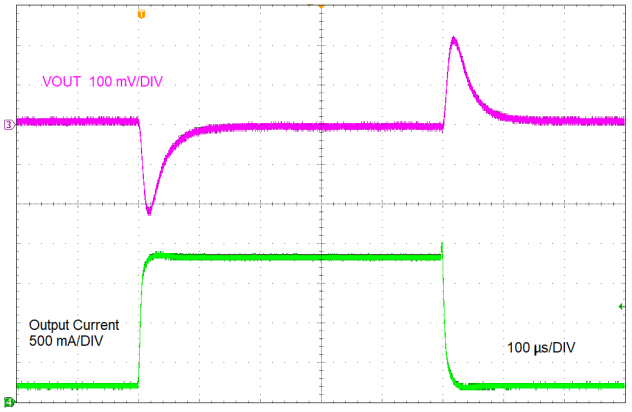

LMR38020-Q1 $V_{OUT}$ = 5 V No Load
FPWM Bias to 3 V

**图 8-9. Start-Up with Prebias**



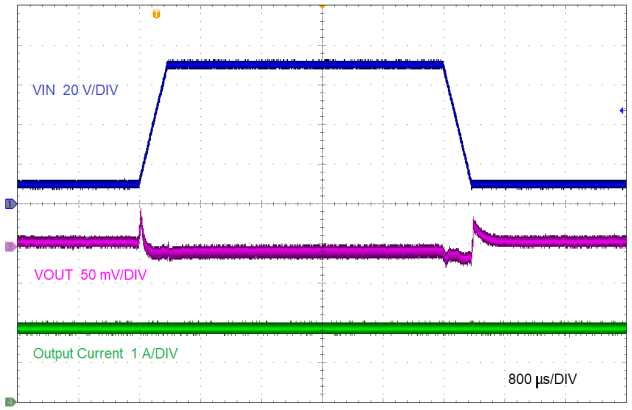

LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz

**图 8-10. Frequency Synchronization**



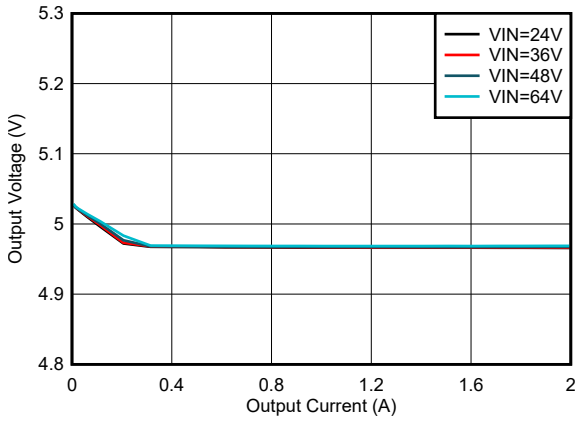

LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz
(AC Coupled)
200 mA to 1.8 A at 200 mA/µs

**图 8-11. Load Transient**



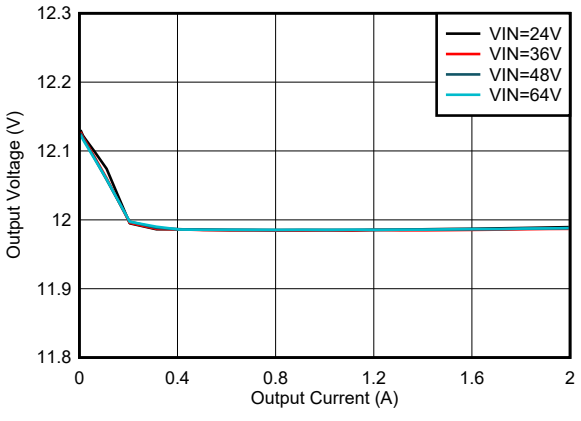

LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz
(AC Coupled)
10 V to 70 V at 200 V/ms

**图 8-12. Line Transient**




LMR38020-Q1 $V_{OUT}$ = 5 V 400 kHz
PFM Version

**图 8-13. 5-V Load Regulation**




LMR38020-Q1 $V_{OUT}$ = 12 V 400 kHz
PFM Version

**图 8-14. 12-V Load Regulation**

## 8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

## 8.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 方程式 16.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (16)$$

where

- $\eta$ = efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator, use an aluminum or tantalum input capacitor in parallel with the ceramics, or both. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 22 µF to 68 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This usage can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success With Conducted EMI From DCDC Converter* application report provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharges through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

## 8.5 Layout

### 8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB

layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or input capacitors, and power ground, as shown in 图 8-15. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 图 8-16 shows a recommended layout for the critical components of the LMR38020-Q1.

- ***Place the input capacitor or capacitors as close as possible to the VIN and GND terminals.*** VIN and GND pins are adjacent, simplifying the input capacitor placement.
- ***Place vias around the input capacitors on the VIN and GND planes.*** Placing vias reduces the effective inductance and allows for a lower impedance path. Please refer to the evaluation board for guidance.
- ***Use wide traces for the $C_{BOOT}$ capacitor***. Place $C_{BOOT}$ close to the device with short/wide traces to the BOOT and SW pins.
- ***Place the feedback divider as close as possible to the FB pin of the device***. Place $R_{FBB}$, $R_{FBT}$, and $C_{FF}$, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to $V_{OUT}$ can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- ***Use at least one ground plane in one of the middle layers***. This plane acts as a noise shield and also act as a heat dissipation path.
- ***Connect the thermal pad to the ground plane.*** The HSOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
- ***Provide wide paths for VIN, VOUT, and GND***. Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- ***Provide enough PCB area for proper heat sinking***. Enough copper area must be used to keep a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
- ***Keep switch area small***. Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *AN-1149 Layout Guidelines for Switching Power Supplies* application report
- *AN-1229 Simple Switcher® PCB Layout Guidelines* application report
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

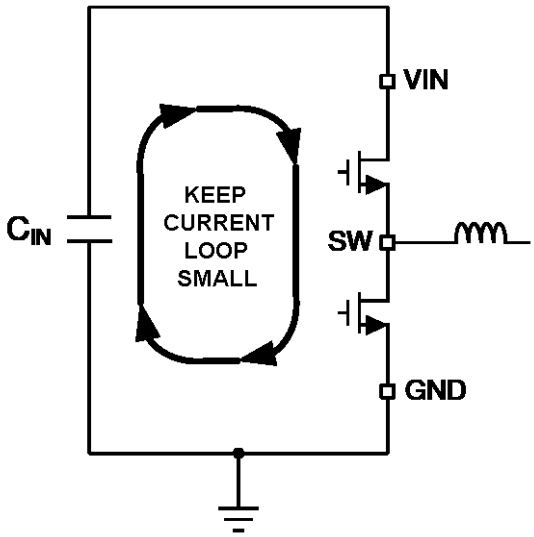



图 8-15. Current Loops with Fast Edges

#### *8.5.1.1 Ground and Thermal Considerations*

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. A ground plane also provides a quiet reference potential for the control circuitry. GND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The GND net contains noise at the switching frequency and can bounce due to load variations. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10-mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

### 8.5.2 Layout Example

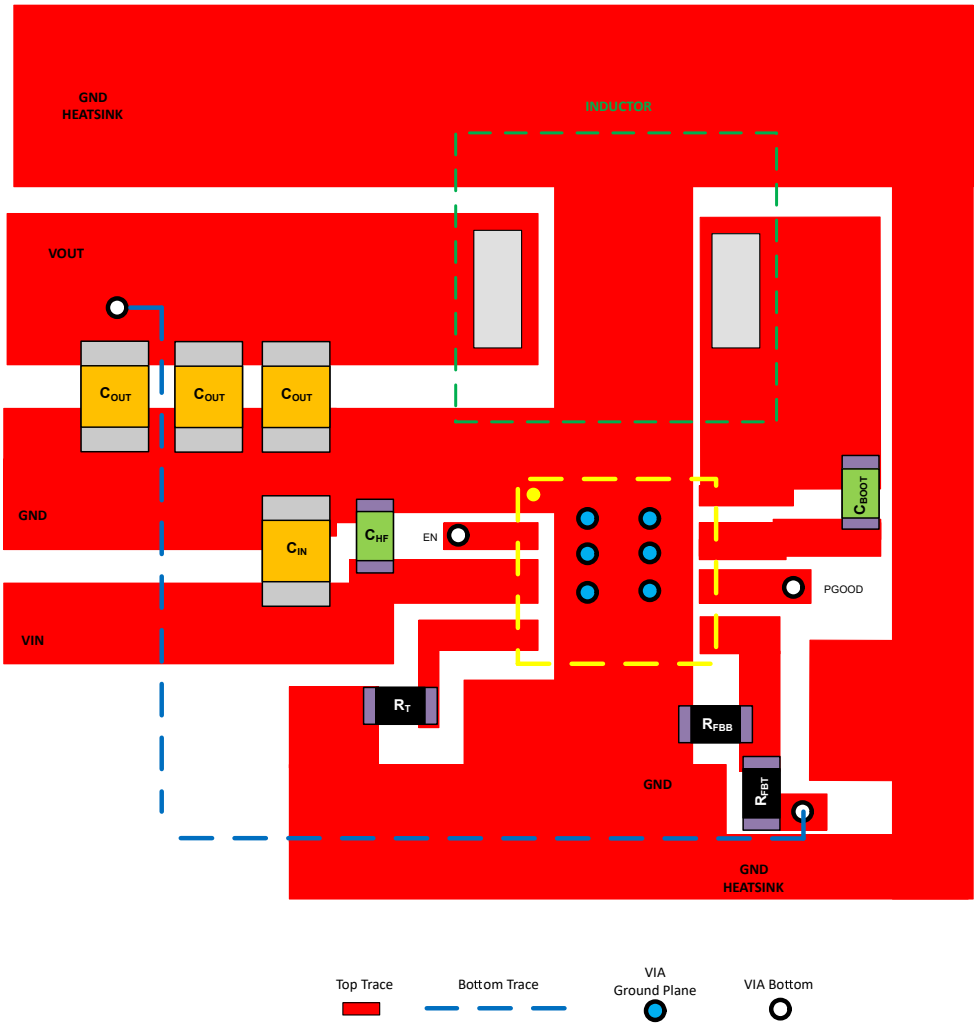



图 8-16. Example Layout for HSOIC (DDA) Package

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

### 9.1.2 Development Support

#### *9.1.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the LMR38020-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DCDC Converter* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* application report
- Texas Instruments, *How to Properly Evaluate Junction Temperature with Thermal Metrics* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *AN-1229 Simple Switcher® PCB Layout Guidelines* application report
- Texas Instruments, *Construction Your Power Supply- Layout Considerations*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

## 9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 9.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.

### 9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (May 2023) to Revision B (January 2024) | Page |
|---|---|
| • 更新了*特性* 列表中的 WEBENCH 链接 | 1 |
| • Updated SW to PGND less than 10-ns | 4 |

| Changes from Revision * (January 2023) to Revision A (May 2023) | Page |
|---|---|
| • 将文档状态从“预告信息”更改为“量产数据” | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMR38020FSQDDARQ1 | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 802FSQ |
| LMR38020FSQDDARQ1.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 802FSQ |
| LMR38020SQDDARQ1 | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 802SQ |
| LMR38020SQDDARQ1.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 802SQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

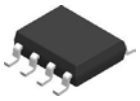
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF LMR38020-Q1 :**

- Catalog : LMR38020

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

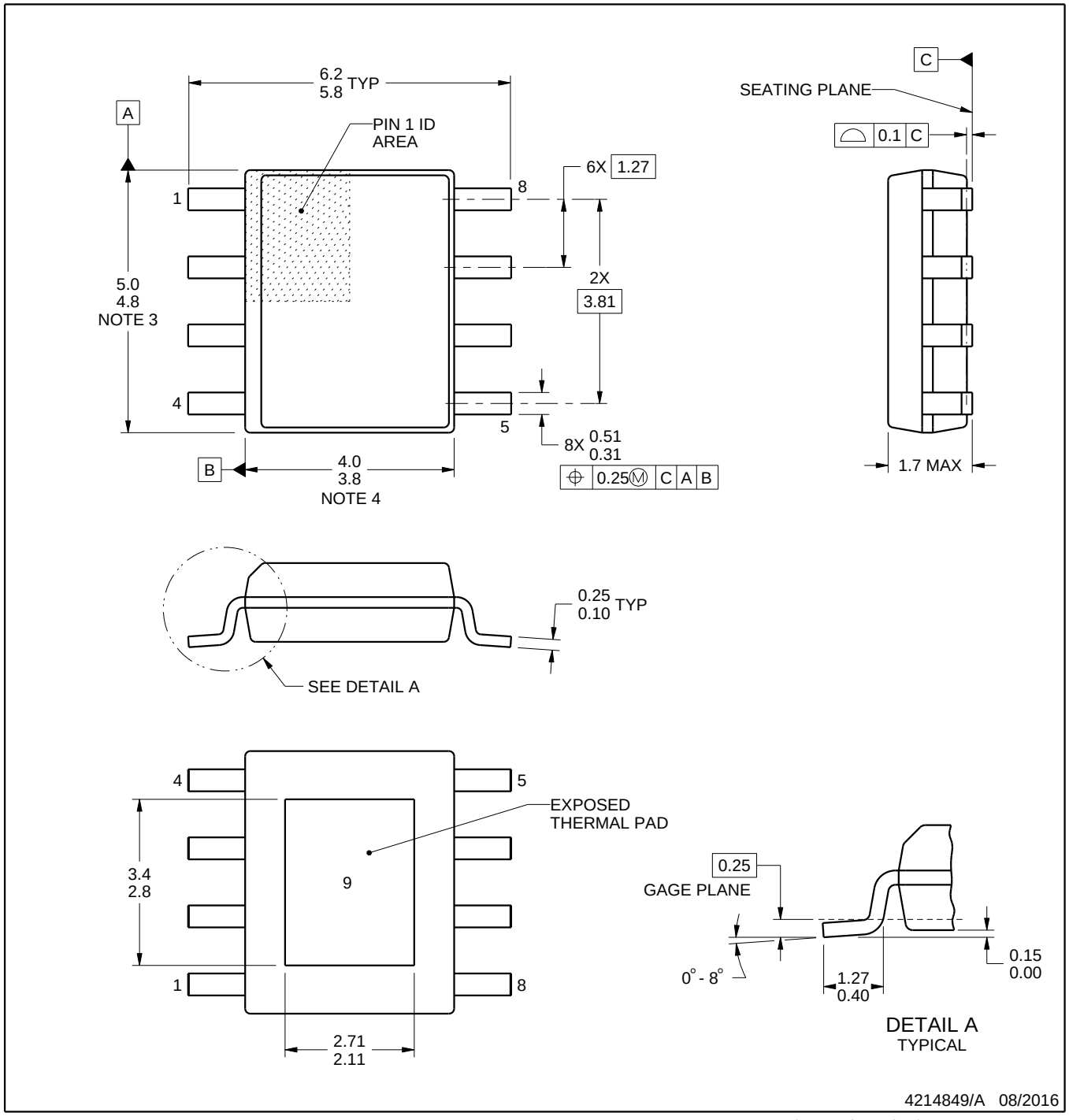


# PACKAGE OUTLINE

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

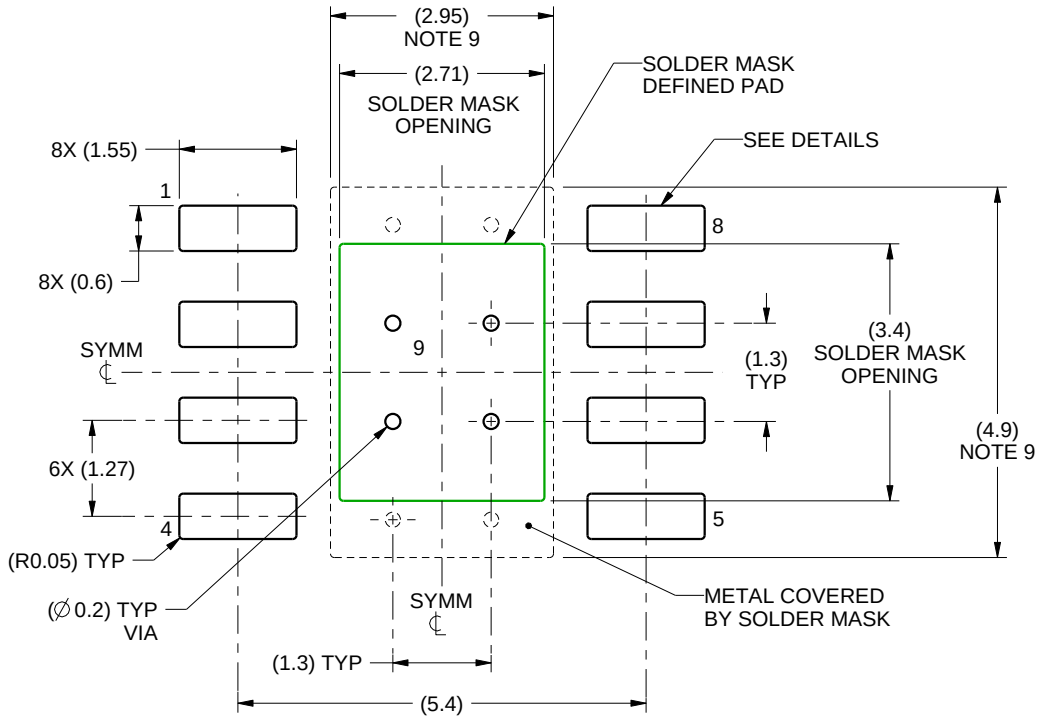
PLASTIC SMALL OUTLINE



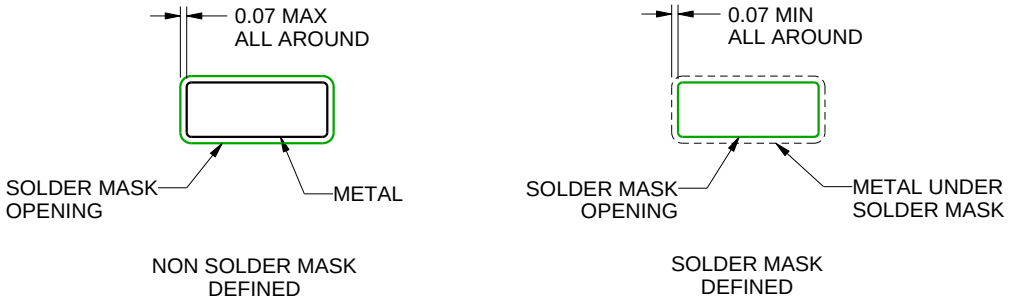

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

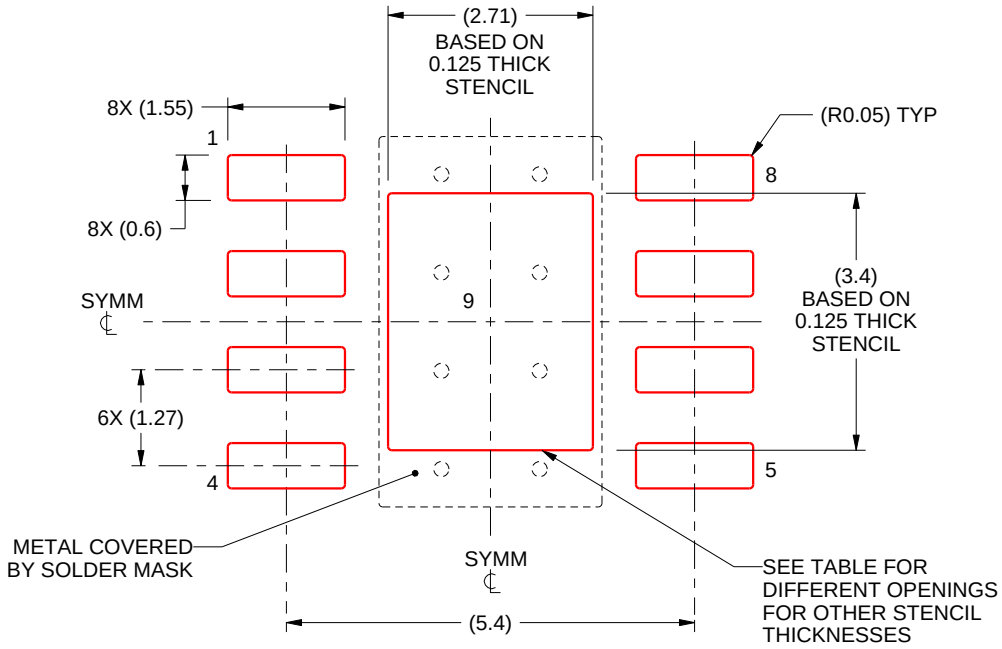
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

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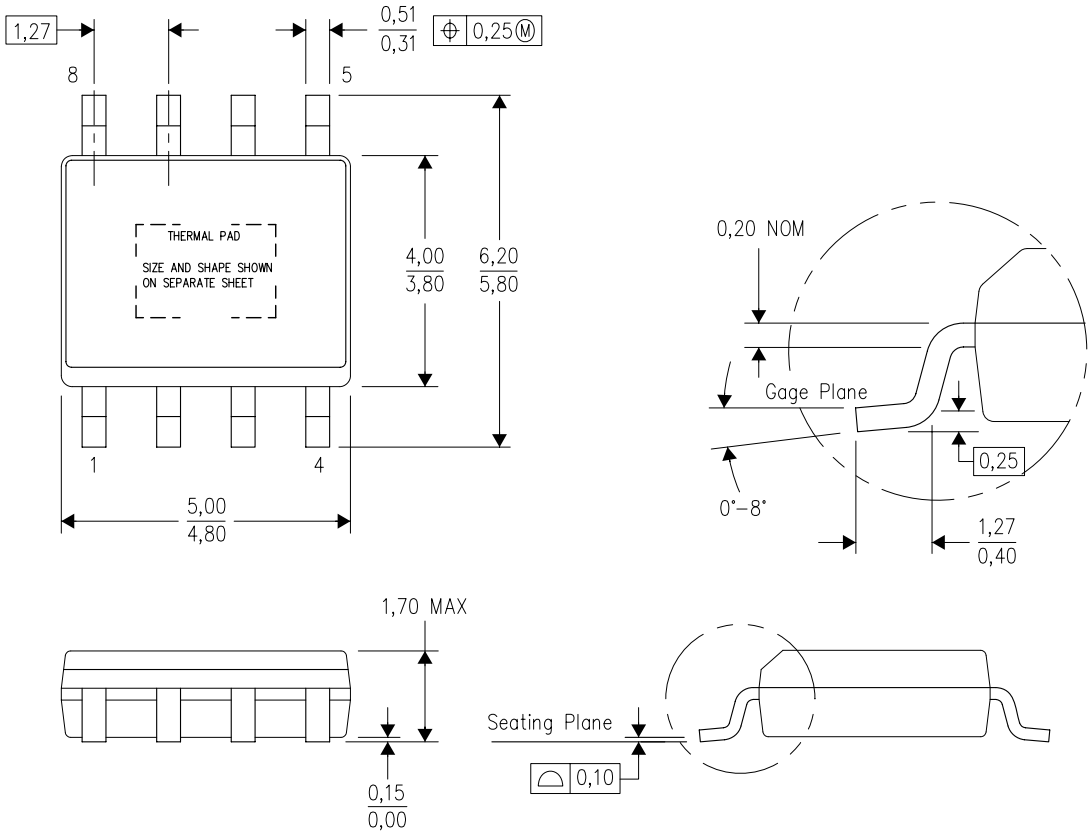
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

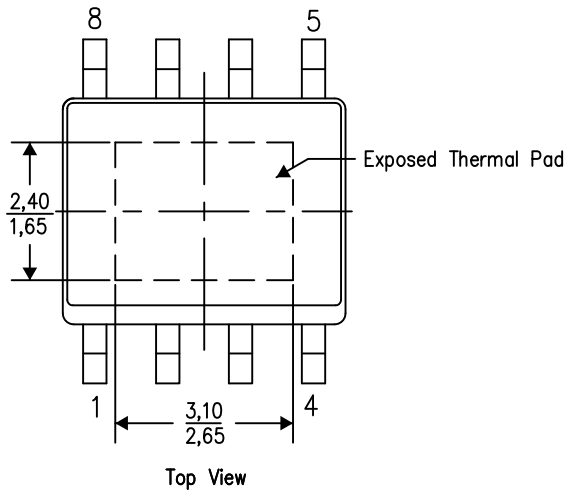
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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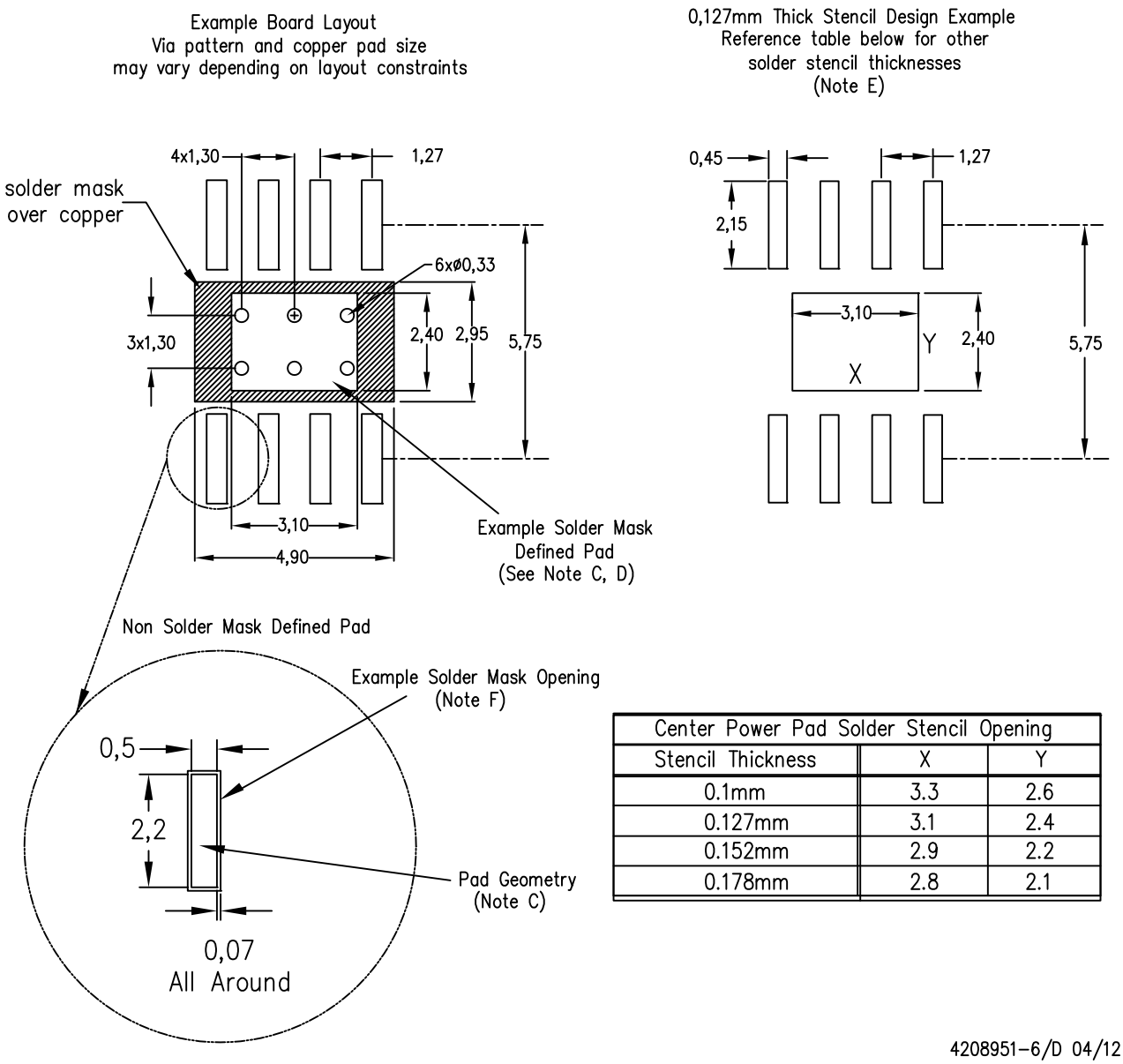
# DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.3 | 2.6 |
| 0.127mm | 3.1 | 2.4 |
| 0.152mm | 2.9 | 2.2 |
| 0.178mm | 2.8 | 2.1 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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