LMP92064 具有 SPI 接口的精密低侧 125kSps 同步采样电流传感器和电压监视器

1 特性

- 2 个 12 位同步采样模数转换器 (ADC)
  - 转换速率：125kSps（最小值）
- 12 位电流感测通道
  - 输入引入偏移电压：±15μV
  - 共模电压范围：–0.2V 至 2V
  - 最大差分输入电压：75mV
  - 固定增益：25V/V
  - 增益误差：±0.75%（最大值）
  - 带宽 (–3dB)：70kHz
  - 直流电源抑制比 (PSRR)：100dB
  - 直流共模抑制比 (CMRR)：110dB
- 12 位电压通道
  - 积分非线性 (INL)：±1 最低有效位 (LSB)
  - 偏移误差：±2mV（最大值）
  - 增益误差：±0.75%（最大值）
  - 最大输入电压：2.048V
  - 带宽：100kHz
- 内部基准电压
- 串行外设接口 (SPI) 频率：高达 20MHz
- 温度范围：–40°C 至 105°C
- 16 引脚晶圆级小外形无引线 (WSON) 封装

2 应用

- 企业级服务器
- 电信
- 电源管理

3 说明

LMP92064 是一款具有数字 SPI 接口的精密低侧数字电流传感器和电压监视器。 该模拟前端 (AFE) 包括一个精密电流感测放大器和一个缓冲电压通道，分别用于测量分流电阻的负载电流和负载的供电电压。 该器件通过独立的 125kSps、12 位 ADC 转换器对电流和电压通道进行同步采样，以在单向感测应用中实现极为精确的功率计算。

LMP92064 为 ADC 提供了 2.048V 内部基准电压，不仅消除了对外部基准电压的需求，同时还减少了元件数量并节省了电路板空间。

主机可通过四线 SPI 接口以高达 20MHz 的运行速度与 LMP92064 通信。 凭借这一快速的 SPI 接口，用户能够利用较高带宽 ADC 来捕获快速变化的信号。 此外，该四线接口还具有专用单向输入和输出线，这使得需要隔离的应用能够轻松连接数字隔离器。

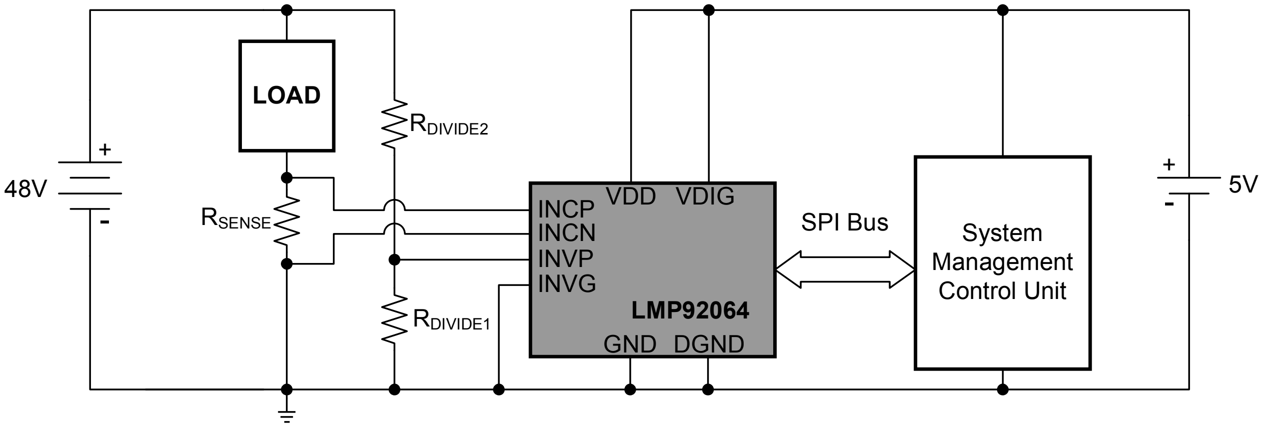
LMP92064 由 4.5V 至 5.5V 的单电源供电运行，并且具有一个独立的数字电源引脚。 LMP92064 采用 16 引脚 5mm x 4mm WSON 封装，额定温度范围为 -40°C 至 105°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMP92064	WSON (16)	5.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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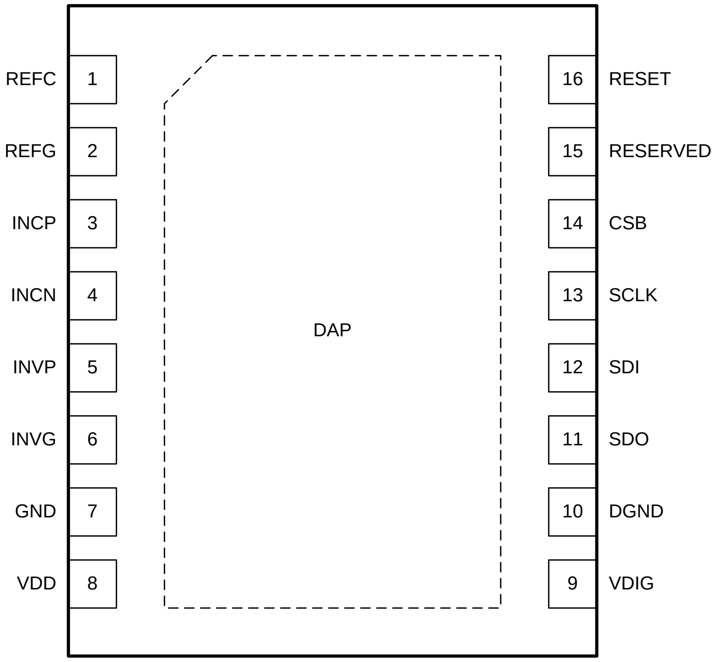
4 修订历史记录

Changes from Original (June 2013) to Revision A	**Page**
• 已添加 *引脚配置和功能部分，ESD 额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分*	1

5 Pin Configuration and Functions

WSON Package
16 Pins
Top View



Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
REFC	1	—	Internal reference bypass capacitor pin
REFG	2	G	Internal reference ground
INCP	3	I	Positive current channel input
INCN	4	I	Negative current channel input
INVP	5	I	Positive voltage channel input
INVG	6	G	Ground reference for the negative voltage channel input
GND	7	G	Analog ground
VDD	8	P	Analog power supply
VDIG	9	P	Digital power supply
DGND	10	G	Digital ground
SDO	11	O	SPI Bus push-pull serial data digital output
SDI	12	I	SPI Bus serial data digital input
SCLK	13	I	SPI Bus clock digital input
CSB	14	I	SPI Bus chip select bar digital input
RESERVED	15	—	Reserved (Do not connect)
RESET	16	I	Reset (high-active)
DAP	n/a	—	No connection (Do not connect)

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)(2)

		MIN	MAX	UNIT
Analog Supply Voltage (VDD)		–0.3	6.0	V
Digital Supply Voltage (VDIG)		VDD-0.3	VDD+0.3	
Voltage at Input Pins(3)		–0.3	VDD+0.3	V
Junction Temperature			150	°C
Mounting temperature	Infrared or convection (20 sec)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) All voltages are measured with respect to GND = DGND = 0 V, unless otherwise specified.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) When the input voltage (VIN), at any pin exceeds power supplies (VIN < GND or VIN > VDD), the current at that pin must not exceed 5 mA, and the voltage (VIN) at that pin must not exceed 6.0 V. See *Pin Description* for additional details of input circuitry.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Analog Supply Voltage (VDD)	4.5	5.5	V
Digital Supply Voltage (VDIG)	VDD	VDD	V
Temperature Range	–40	105	ºC

(1) All voltages are measured with respect to GND = DGND = 0 V, unless otherwise specified.

6.4 Thermal Information

Over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		LMP92064	UNIT
		NHR	
		16 PINS	
$R_{\theta JA}$	Package thermal resistance(2)	44	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7. The maximum power dissipation must be de-rated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/\theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

6.5 Electrical Characteristics

Typical specifications are at 25ºC. All specifications are at 4.5 V ≤ VDD ≤ 5.5 V, VDIG = VDD and –0.2 V ≤ VCM ≤ 2 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE INPUT CHANNEL						
V_{OS}	Input-referred Offset Voltage			±15		μV
		Temperature extremes	-60		60	
TCV_{OS}	Input-referred Offset Voltage Drift			±280		nV/ºC
	Long-term Stability			0.3		μV/mo
	Resolution			12 20		Bits μV
INL	Integral Non-Linearity Error			±1% ±0.025%		LSB
DNL	Differential Non-Linearity Error			±0.5		LSB
DC CMRR	Common-Mode Rejection Ratio	–0.2 V ≤ VCM ≤ 2 V		110		dB
DC PSRR	Power Supply Rejection Ratio	4.5 V ≤ VDD ≤ 5.5 V		100		dB
CMVR	Common-Mode Voltage Range	Low VCM		–0.2		V
		High VCM		2		
$V_{DIFF(MAX)}$	Maximum Differential Input Voltage Range			75		mV
A_V	Current Shunt Amplifier Gain			25		V/V
	Current Sense Channel Gain			50		kCode/V
GE	Gain Error (CSA, VREF and ADC)	Temperature extremes	-0.75%		0.75 %	
GD	Gain Drift			±25		ppm/°C
RIN	Input Impedance			100		GΩ
BW	–3dB Bandwidth			70		kHz
VOLTAGE INPUT CHANNEL						
	Offset Error (Buffer and ADC)	Temperature extremes	-2		2	mV
	Resolution			12		Bits
INL	Integral Non-Linearity Error			±1% ±0.025%		LSB
DC PSRR	Power Supply Rejection Ratio			70		dB
V_{CHVP}	Full-Scale Input Voltage			2.048		V
A_V	Buffer Amplifier Gain			1		V/V
	Voltage Sense Channel Gain			2		kCode/V
GE	Gain Error (Buffer, VREF and ADC)	Temperature extremes	-0.75%		0.75 %	
RIN	Input Impedance			100		GΩ
BW	Bandwidth(1)			100		kHz
DIGITAL INPUT/OUTPUT CHARACTERISTICS						
V_{IH}	Logical “1” Input Voltage	Temperature extreme	0.7*VDIG			V
V_{IL}	Logical “0” Input Voltage	Temperature extreme			0.3*VDIG	V
V_{OH}	Logical “1” Output Voltage	I_{SOURCE} = 300 μA				V
		Temperature extreme	VDIG –0.15			
V_{OL}	Logical “0” Output Voltage	I_{SINK} = 300 μA				V
		Temperature extreme			DGND +0.15	
SUPPLY CHARACTERISTICS						
I_{VDD}	Analog Supply Current			11		mA
I_{VDIG}	Digital Supply Current			2		mA

(1) No analog filter; limited by sampling rate.

6.6 Timing Requirements

Typical specifications are at 25ºC. All specifications are at 4.5 V ≤ VDD ≤ 5.5 V, VDIG = VDD and a 20 pF capacitive load on SDO, unless otherwise specified.

		MIN	MAX	UNIT
t_{DS}	SDI to SCLK rising edge setup time	10		ns
t_{DH}	SCLK rising edge to SDI hold time	10		ns
f_{CLK}	Frequency of SCLK	100		Hz
			20	MHz
t_{HIGH}	High width of SPI clock	25		ns
t_{LOW}	Low width of SPI clock	25		ns
t_S	CSB falling edge to SCLK rising edge setup time	10		ns
t_C	SCLK rising edge to CSB rising edge hold time	30		ns
t_{DV}	SCLK falling edge to valid SDO readback data		20	ns
t_{RST}	Reset pin pulse width	3.5		ns
t_{CONV}	Conversion rate of all channels	125		kSps

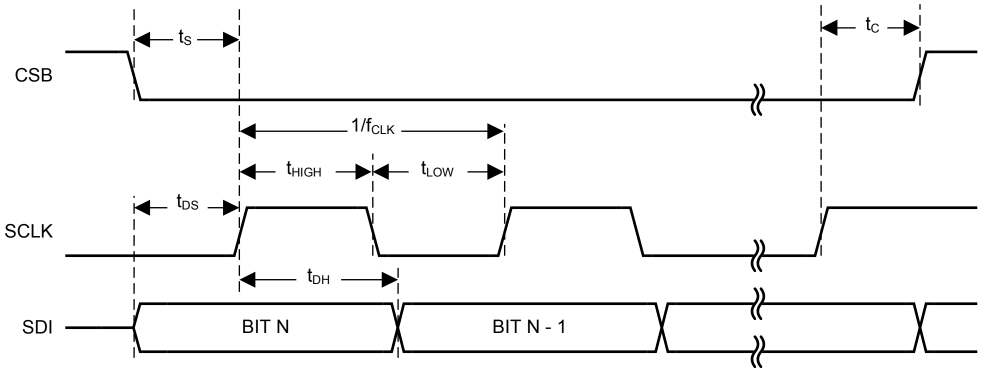


Figure 1. Serial Control Port Timing – Write

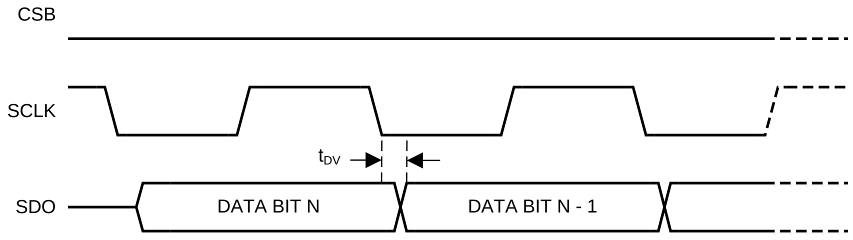


Figure 2. Serial Control Port Timing – Read

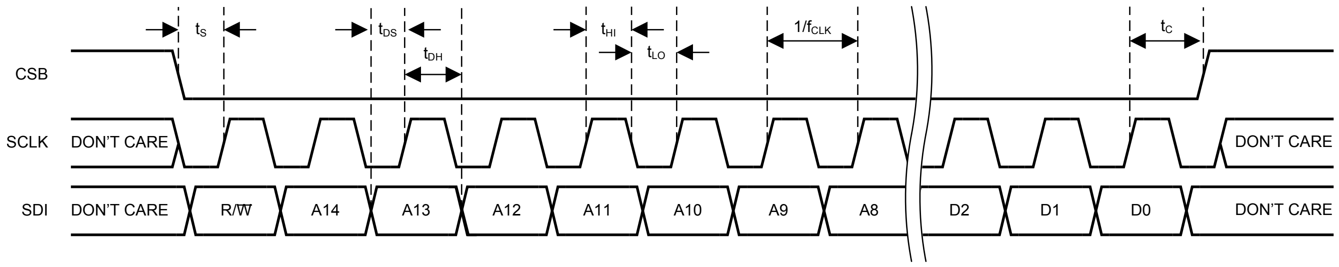


Figure 3. Serial Control Port Write – MSB First, 16-Bit Instruction, Timing Measurements

6.7 Typical Characteristics

All plots at T_A = 25ºC, VDD = 5.0 V, VDIG = 5.0 V, VCM = 0 V and GND = DGND = 0 V, unless otherwise specified.

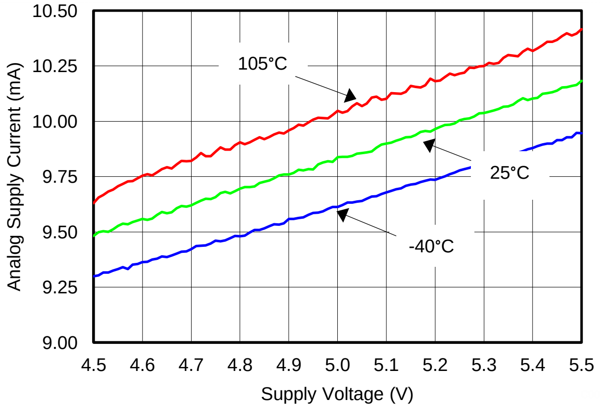


Figure 4. Analog Supply Current vs Supply Voltage

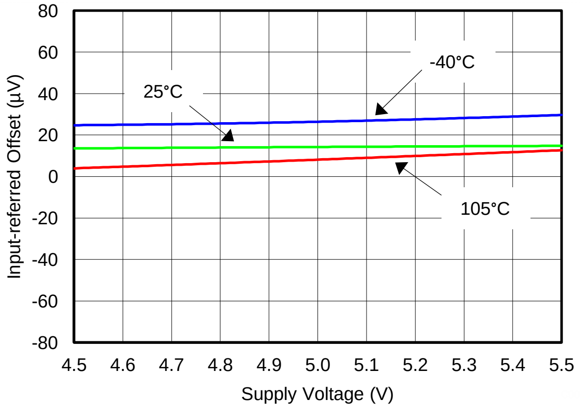


Figure 5. Input-Referred Offset vs Supply Voltage (Current Channel)

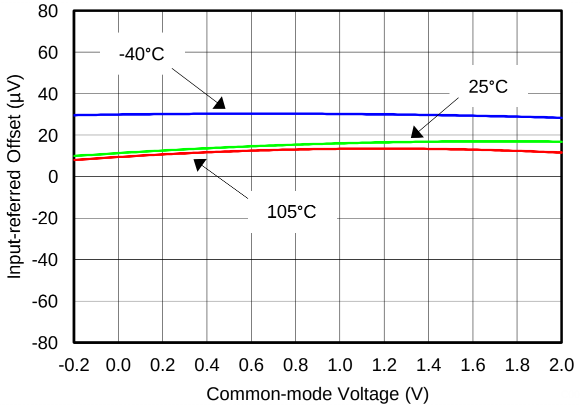


Figure 6. Input-Referred Offset Vscommon-Mode Voltage (Current Channel)

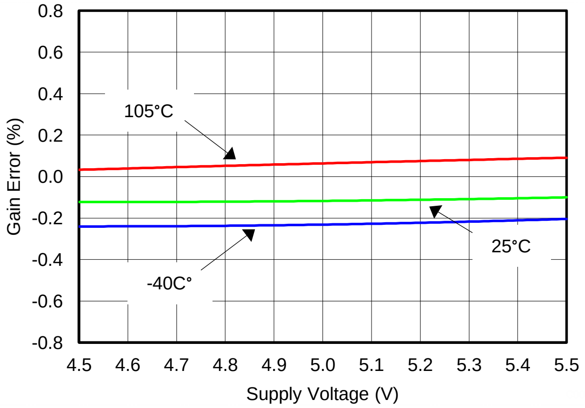


Figure 7. Gain Error vs Supply Voltage (Current Channel)

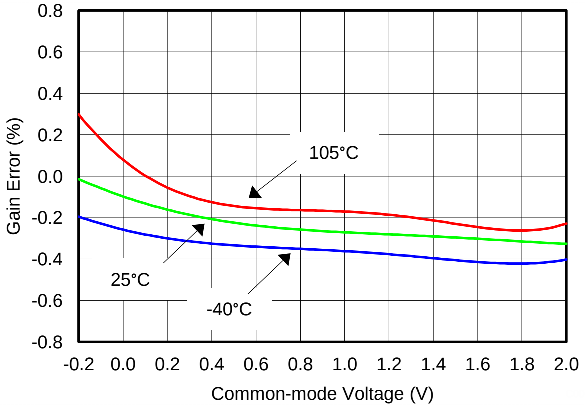


Figure 8. Gain Error vs Common-Mode Voltage (Current Channel)

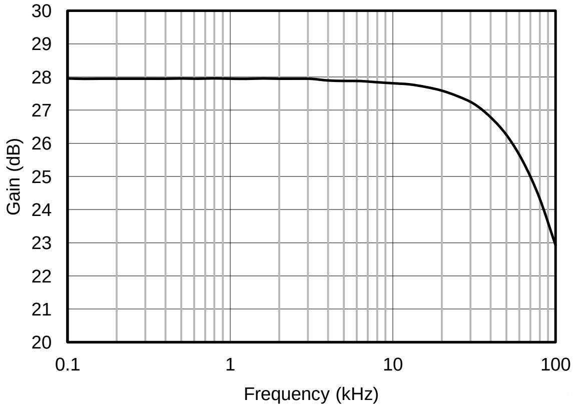


Figure 9. Gain Vsfrequency (Current Channel)

Typical Characteristics (continued)

All plots at T_A = 25ºC, VDD = 5.0 V, VDIG = 5.0 V, VCM = 0 V and GND = DGND = 0 V, unless otherwise specified.

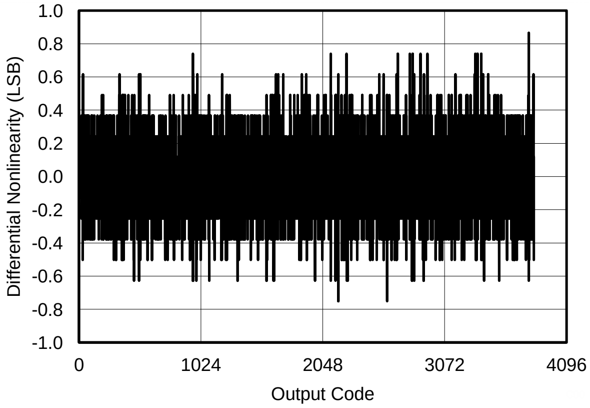


Figure 10. Differential Nonlinearity (Current Channel)

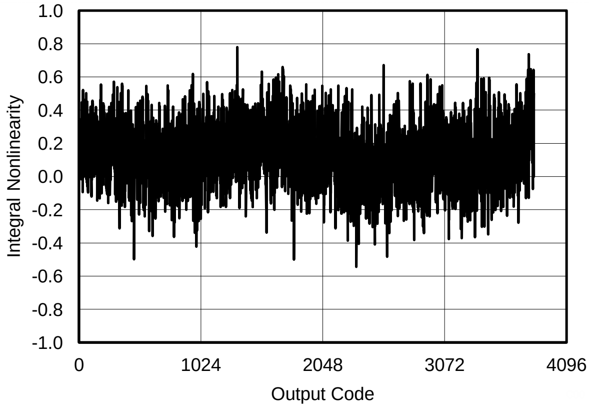


Figure 11. Integral Nonlinearity (Current Channel)

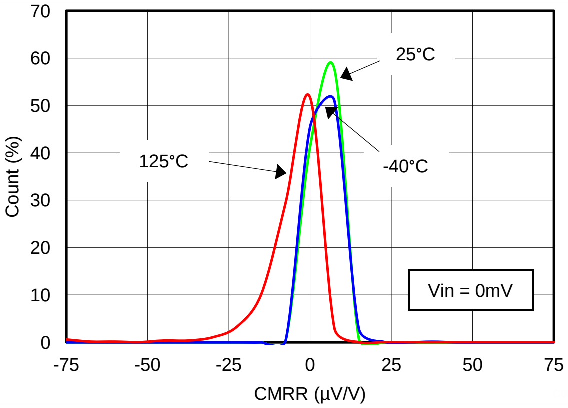


Figure 12. Common-Mode Rejection Ratio Distribution (Current Channel)

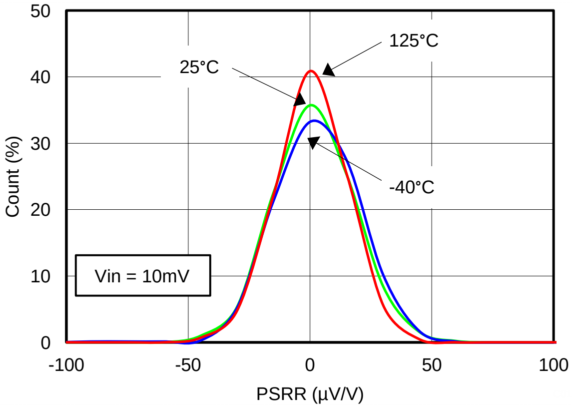


Figure 13. Power Supply Rejection Ratio Distribution Vcm = -0.2 V (Current Channel)

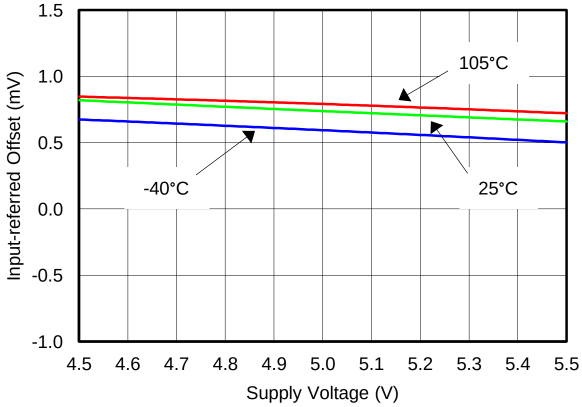


Figure 14. Input-Referred Offset Vssupply Voltage (Voltage Channel)

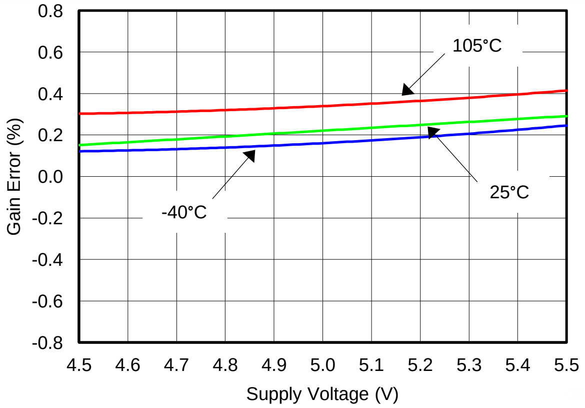


Figure 15. Gain Error vs Supply Voltage (Voltage Channel)

Typical Characteristics (continued)

All plots at T_A = 25ºC, VDD = 5.0 V, VDIG = 5.0 V, VCM = 0 V and GND = DGND = 0 V, unless otherwise specified.

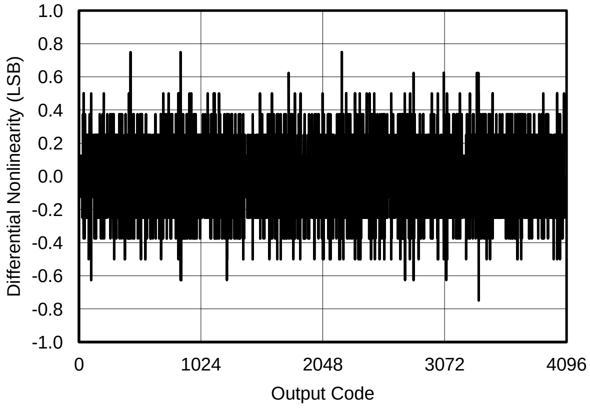


Figure 16. Differential Nonlinearity (Voltage Channel)

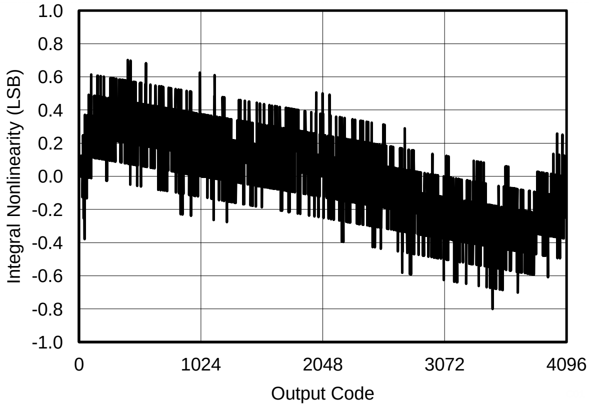


Figure 17. Integral Nonlinearity (Voltage Channel)

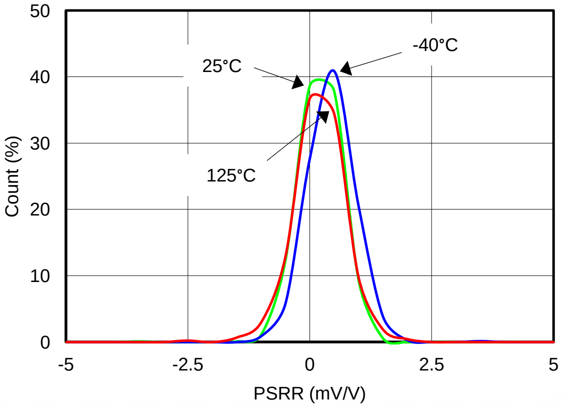


Figure 18. Power Supply Rejection Ratio Distribution (Voltage Channel)

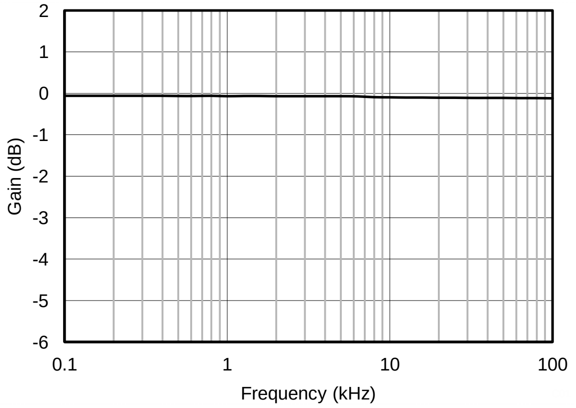


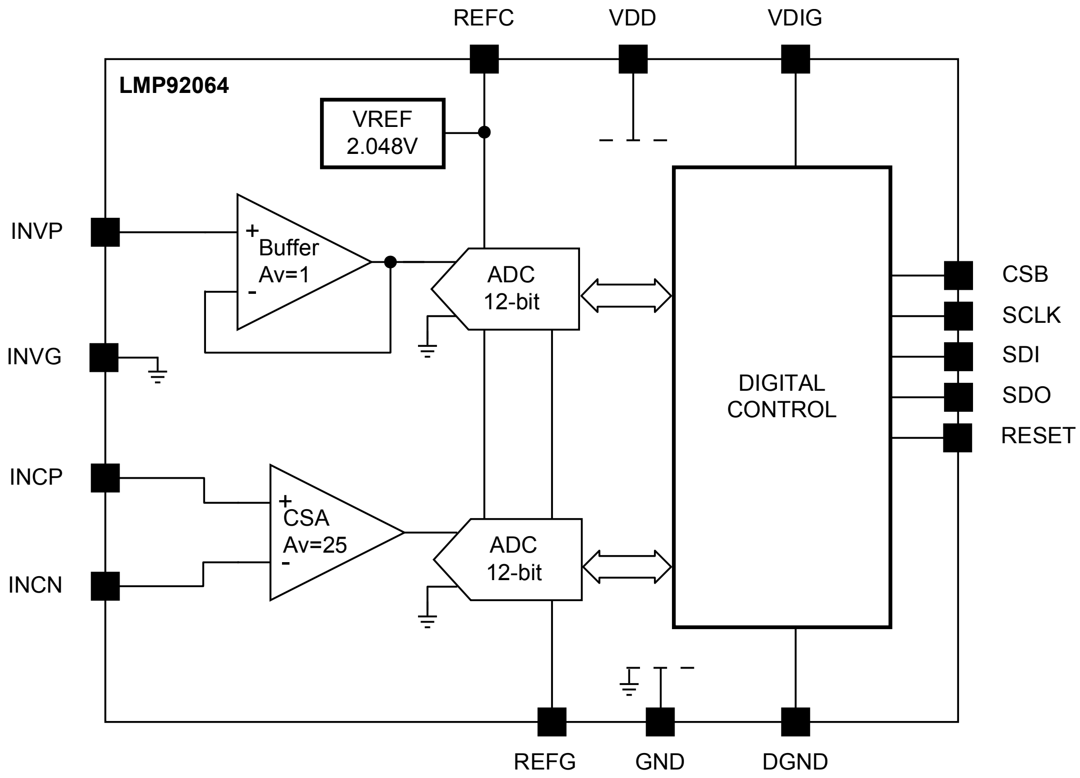
Figure 19. Gain vs Frequency (Voltage Channel)

7 Detailed Description

7.1 Overview

The LMP92064 is a precision low-side digital current sensor and voltage monitor with a digital SPI interface. The analog front-end includes a precision current sense amplifier to measure a load current across a shunt resistor and abuffered voltage channel to measure the voltage supply of the load.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Sense Input Channel

The current sensing channel of the LMP92064 has a high impedance differential amplifier followed by a 12-bit analog-to-digital converter. The binary code result of a conversion is stored as a right-justified 16-bit number as shown in Table 1, where the 4 most significant bits are always 0. Due to an offset auto-calibration feature of the current sense channel path, the top 256 codes are clipped at code 3840, denoted by the trailing zeros found in the equivalent binary code of the maximum positive input voltage.

The output data of the current sense channel is accessible on registers 0x0203 and 0x0202.

Table 1. Ideal Current Channel Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	V_{FS}= 81.92 mV	**BINARY CODE [B15:B0]**	**HEX CODE**
Least significant bit (LSB)	V_{FS} / 4096		
Maximum Positive Input Voltage	V_{FS} – 256 LSB	0000 1111 0000 0000	0x0F00
Zero	0 V	0000 0000 0000 0000	0x0000

7.3.2 Current Sense Input Channel Common-Mode and Differential Voltage Range (Dynamic Range Considerations)

The input voltage should be in the range of –0.2 V to 2 V. The input can withstand voltage up to VDD + 0.3 V absolute maximum but the operational range is limited to 2 V. Operation below –0.2 V or above 2 V on either input pin will introduce severe gain errors and nonlinearity.

The maximum differential voltage (defined as the voltage difference between INCP and INCN) for which the part is designed to work is 75 mV. Larger differential or common mode input voltages will not damage the part (as long as the input pins remain between GND – 0.3 V and VDD + 0.3 V), however, exposure for extended periods may affect device reliability. The ADC output code will not roll over and will clip at minimum or maximum scale when the maximum differential voltage is exceeded.

7.3.3 Voltage Sense Input Channel

The voltage sensing channel of the LMP92064 has a high impedance buffer amplifier followed by a 12-bit analog-to-digital converter. The binary code result of a conversion is also stored as a right-justified 16-bit number as shown in Table 2, where the 4 most significant bits are always 0.

The output data of the voltage sense channel is accessible on registers 0x0201 and 0x0200.

Table 2. Ideal Voltage Channel Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	V_{FS}= 2.048 V	BINARY CODE [B15:B0]	HEX CODE
Least significant bit (LSB)	V_{FS} / 4096		
Maximum Positive Input Voltage	V_{FS} – 1 LSB	0000 1111 1111 1111	0x0FFF
Zero Code Voltage	0 V	0000 0000 0000 0000	0x0000

7.3.4 Reference

The LMP92064 includes an internal 2.048-V band-gap reference for the ADCs, which eliminates the need of an external reference and reduces component count and board space. The REFC pin is provided to allow bypassing this internal reference for low noise operation. A 1-µF ceramic decoupling capacitor is required between the REFC and REFG pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

7.3.5 Reset

There are two methods to reset the LMP92064. A soft reset is done by setting bit7=1 in the CONFIG_A register. In a soft reset, the SPI state machine and the contents of registers 0x0000 and 0x0001 are unaffected.

A hardware reset is done by connecting the RESET pin of the LMP92064 to VDIG. If the pin is driven by a switch or a GPIO, TI recommends adding an external RC filter to prevent reset glitches.

7.3.6 Device Power-Up Sequence

The sources providing power to the analog and digital supply pins of the LMP92064, VDD and VDIG, must ramp up at the same time to have a proper power-on reset (POR) event. The easiest way to achieve it is to tie VDD and VDIG to the same power source using a star configuration.

7.4 Device Functional Modes

7.4.1 ADC Operation

The LMP92064 includes two 12-bit ADCs that are continuously running in the background. The device is configured, and data is read, using a four-wire SPI interface: CSB, SCLK, SDO and SDI. The device outputs its data on SDO, and the data for both channels is synchronized such that all data read would be from the same instant in time. New conversion data for both channels will only be made available after all registers are read in descending sequential order (addresses 0x0203-0x0200). All registers must be read otherwise new conversion data will not be available. Three different output data formats are available as detailed in Figure 20, Figure 21 and Figure 22.

Device Functional Modes (continued)

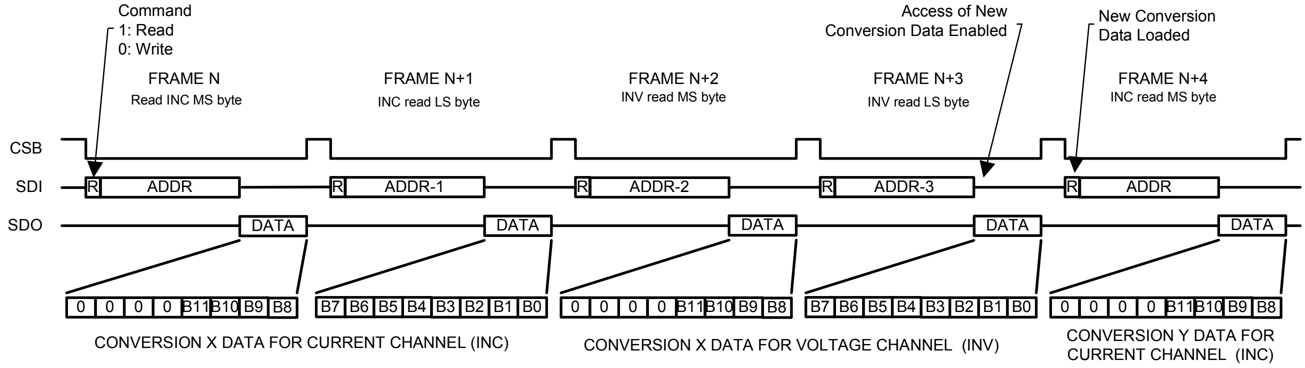


Figure 20. Timing Diagram With Byte Read Frames

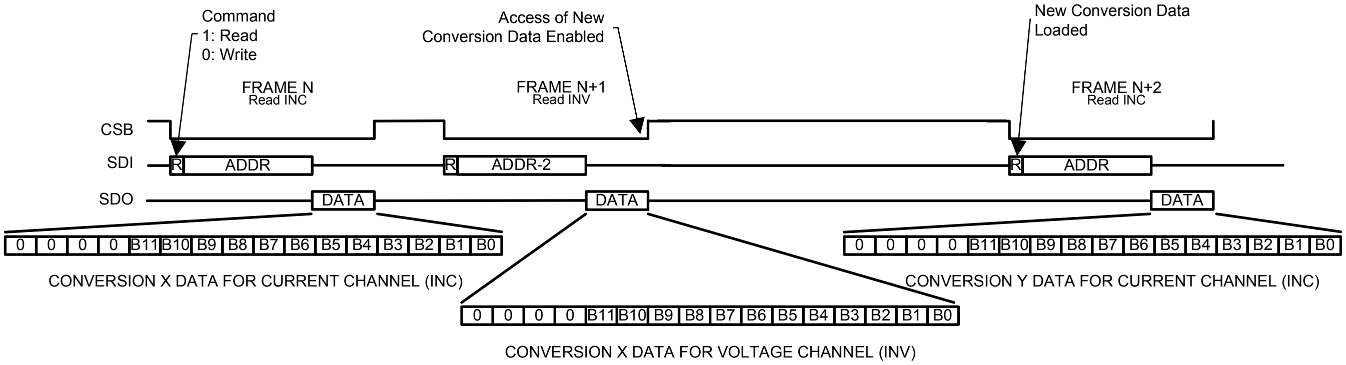


Figure 21. Timing Diagram With Word Read Frames

The register address to read can automatically decrement if the CSB line is kept low longer. For example, to read all the conversion data, keep the CSB line low for 48 SPI clock cycles (16 clocks for command/address, 8 clocks for MSB of current channel, 8 clocks for LSB of current channel, 8 clocks for MSB of voltage channel and 8 clocks for LSB of voltage channel). The read command should start from address 0x0203.

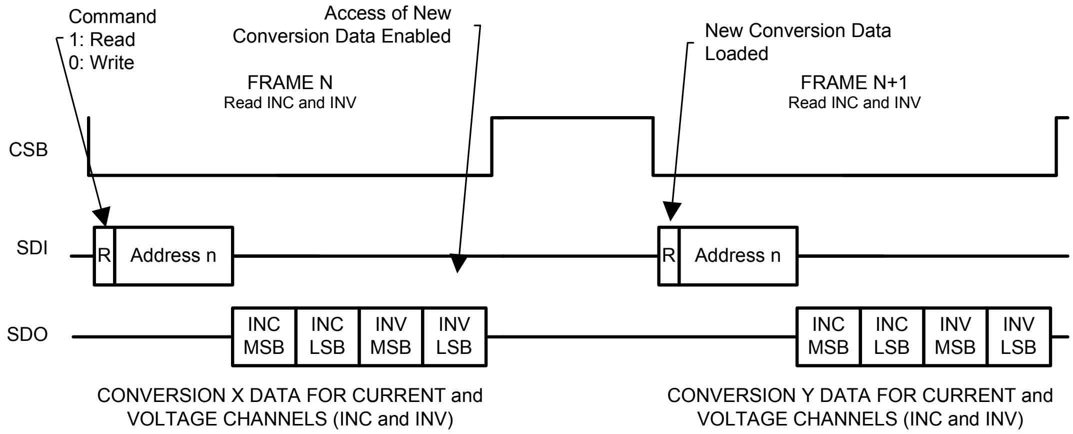


Figure 22. Timing Diagram With All Data Read Frames

7.5 Register Maps

1. If written to, Reserved bits must be written to 0, unless otherwise indicated.
2. Read back value of Reserved bits and registers is unspecified and should be discarded.
3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
4. If written to, registers indicated as Reserved must have the indicated default value as shown in the register map. Any other value can cause unexpected results.

Table 3. Register Map

REGISTER NAME	REGISTER DESCRIPTION	ADDRESS	ACCESS	DEFAULT
CONFIG_A	Interface Configuration A	0x0000	R/W	0x18
CONFIG_B	Interface Configuration B	0x0001	R/W	0x00
Reserved	Reserved	0x0002	R/W	0x00
CHIP_TYPE	Chip Type	0x0003	RO	0x07
CHIP_ID	Chip ID	0x0004 0x0005	RO	0x00 0x04
CHIP_REV	Chip Revision	0x0006	RO	0x01
MFR_ID	Manufacturer ID	0x000C 0x000D	RO	0x51 0x04
REG_UPDATE	Register Update	0x000F	R/W	0x00
CONFIG_REG	LMP92064 Specific Configuration Register	0x0100	R/W	0x00
STATUS	Status Register	0x0103	RO	N/A
DATA_VOUT	Voltage Channel Output Data	0x0200 0x0201	RO	N/A
DATA_COUT	Current Channel Output Data	0x0202 0x0203	RO	N/A

Table 4. CONFIG_A: Interface Configuration A

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0000	RESET	DDIR	ADDRDIR	SDDIR				

[7]	RESET(1)	Soft reset (self-clearing) 0: Normal (default) 1: Reset	R/W
[6]	DDIR	Data direction 0: Data is transmitted MSB first (default)	RO
[5]	ADDRDIR(2)	Multiple-read auto-address direction 0: Address auto-decrements (default)	RO
[4]	SSDIR	Serial data direction 1: Unidirectional; SDI is used for write and SDO is used for read (default)	RO
[3:0]		Bits [3:0] should always mirror [7:4] as follows: [3] = [4] [2] = [5] [1] = [6] [0] = [7]	R/W

(1) Contents of register 0x0000 and 0x0001 and SPI state machine are unaffected
(2) Address 0x0000 will wrap to 0x7FFF

Table 5. CONFIG_B: Interface Configuration B

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0001	STREAM	Reserved	BUFREG_RD	Reserved		Reserved		Reserved

[7]	STREAM	Stream 0: Streaming is on (default)	RO
[6]	Reserved	Reserved 0 (default)	RO
[5]	BUFREG_RD[1]	Active/buffered register read-back 0: Read back from active register (default) 1: Read back from buffered register	R/W
[4:3]	Reserved	Reserved 00 (default)	RO
[2:1]	Reserved	Reserved 00 (default)	RO
[0]	Reserved	Reserved 0 (default)	RO

(1) Only double-buffered register affected: 0x0100

Table 6. CHIP_TYPE: Chip Type

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0003	CHIP_TYPE							

[7:0]	CHIP_TYPE	Chip type 0x07: Precision ADC	RO

Table 7. CHIP_ID: Chip ID LSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0004	CHIP_ID_LSB							

[7:0]	CHIP_ID_LSB	Chip ID LSB 0x00 (Manufacturer defined)	RO

Table 8. CHIP_ID: Chip ID MSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0005	CHIP_ID_MSB							

[7:0]	CHIP_ID_MSB	Chip ID MSB 0x04 (Manufacturer defined)	RO

Table 9. CHIP_REV: Chip Revision

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0006	CHIP_REV							

[7:0]	CHIP_REV	Chip REV 0x01	RO

Table 10. MFR_ID: Manufacturer ID LSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x000C	MFR_ID_LSB							

[7:0]	MFR_ID_LSB	Manufacturer ID LSB 0x51	RO

Table 11. MFR_ID: Manufacturer ID MSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x000D	MFR_ID_MSB							

[7:0]	MFR_ID_MSB	Manufacturer ID MSB 0x04	RO

Table 12. REG_UPDATE: Register Update

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x000F								BUFREG_ UPDATE

[7:1]	Reserved	Reserved 0 (default)	RO
[0]	BUFREG_ UPDATE(1)	Buffered register update (self clearing) 0: No action (default) 1: Transfer buffered register contents to active register	R/W

(1) Register 0x0100 is buffered.

Table 13. CONFIG_REG: Lmp92064 Specific Configuration Register

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0100	Reserved							

[7:0]	Reserved(1)	Reserved for future use 0x00 (default)	R/W

(1) This register is double-buffered; register 0x000F must be set to 1 to transfer the contents from the buffer to the active register.

Table 14. STATUS: Status Register

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0103	0	0	0	0	0	0	0	STATUS

[7:1]	Unused	Unused Always read 7’b0	RO
[0]	STATUS	Status 0: Device is not ready for conversion 1: Device is ready for conversion	RO

Table 15. DATA_VOUT: Voltage Channel Output Data LSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0200	VOUT_DATA_LSB							

[7:0]	VOUT_ DATA_LSB	Voltage output data least significant byte	RO

Table 16. DATA_VOUT: Voltage Channel Output Data MSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0201	0	0	0	0	VOUT_DATA_MSB			

[7:4]	Unused	Unused 0000 (default)	RO
[3:0]	VOUT_ DATA_MSB	Voltage output data most significant byte	RO

Table 17. DATA_COUT: Current Channel Output Data LSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0202	COUT_DATA_LSB							

[7:0]	COUT_ DATA_LSB	Current output data least significant byte	RO

Table 18. DATA_COUT: Current Channel Output Data MSB

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0203	0	0	0	0	COUT_DATA_MSB			

[7:4]	Unused	Unused 0000 (default)	RO
[3:0]	COUT_ DATA_ MSB	Current output data most significant byte	RO

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMP92064 is a precision low-side digital current sensor and voltage monitor with a digital SPI interface. The device is typically used to measure a load current by means of a current sense resistor connected in series with a load. Use the following design procedure to select the main components of a simple current and voltage monitoring application using the LMP92064.

8.2 Typical Application

In this example, the LMP92064 is used to sense the load current flowing through the sense resistor, R1. Additionally, the voltage across R3 can be sensed to calculate the bus voltage.

The load that will be monitored is operating from a –48-V bus. Because the GND pin of the LMP92064 is connected to the –48-V bus, –48 V becomes the ground reference for the device.

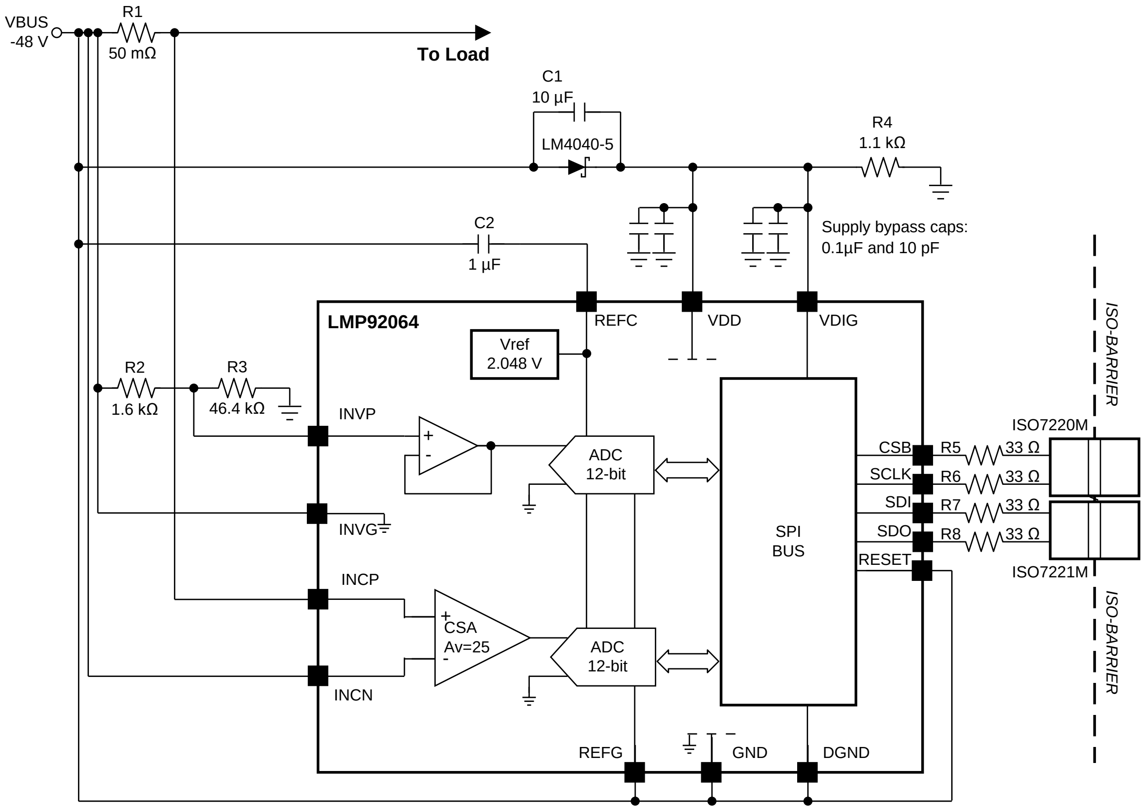


Figure 23. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 19 as the application parameters.

Table 19. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Bus Voltage	-48 V
Bus Voltage Variation	±2%
Supply Voltage	5 V
SPI Clock	12 MHz
Maximum Load Current	1 A
Resolution	1 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Digital Isolators

The ISO7220M and ISO7221M isolators are used for this example. Please refer to the ISO722x documentation for device specific information. These devices support data rates of up to 150 Mbps and provide a low propagation delay necessary for bi-directional SPI communication at 12 MHz.

8.2.2.2 Supply Voltage for the LMP92064

A 5-V supply is required for the LMP92064. The LM4040-5 reference is used to generate the required voltage from the load's –48-V supply. The LM4040-N is a precision micropower shunt voltage reference and is available in several fixed breakdown voltage options. The LM4040-5 provides the required 5-V breakdown voltage.

In a conventional shunt regulator application (Figure 24), the LM4040-5 requires a current limiting resistor connected between the positive supply voltage and the LM4040-5.

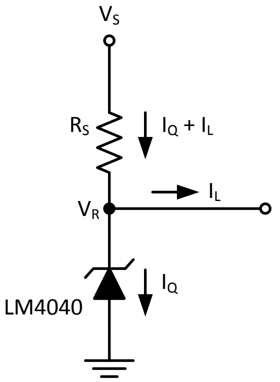


Figure 24. Shunt Regulator

The value of the resistor is determined by the positive supply voltage (V_S), the load current (I_L), the reference operating current (I_Q), and the LM4040-5's reverse breakdown voltage (V_R).

$$R_S = \frac{V_S - V_R}{I_L + I_Q} \quad (1)$$

8.2.2.3 Series Resistor for the Shunt Regulator

The selection of R_S should satisfy two main conditions:

- R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4040-5 even when the supply voltage is at its minimum and the load current is at its maximum value.
- R_S should be large enough so that the current flowing through the LM4040-5 is less than 15 mA when the supply voltage is at its maximum and the load current is at its minimum.

The minimum operating current of the LM4040AIM3-5/NOPB is 80 µA and its maximum operating current is 15 mA.

The typical supply current of the LMP92064 is 13 mA. The measured average current of the circuit, including the isolators, is 38 mA.

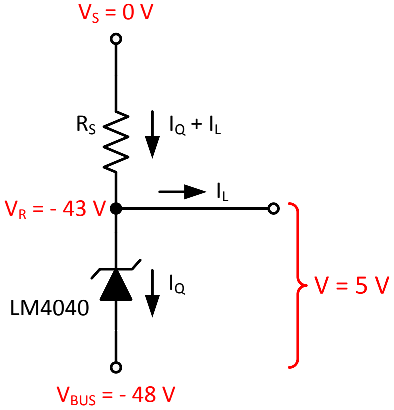


Figure 25. Shunt Regulator Voltages

From Figure 25, V_S = 0 V and V_R = –43 V. R_S can be calculated as follows:

$$R_S = \frac{0\,V - (-43V)}{38\,mA + 80\mu A} = 1129\,\Omega \tag{2}$$

Choosing a smaller resistor, like a 1.1-kΩ resistor, will result in about 39.1 mA to flowing through R_S, providing a margin of 1 mA above the required 38.08 mA.

A variation in the bus voltage (V_{BUS}) of ±2% would result in less than ±0.87 mA of current variation. Given the additional current margin obtained by the 1.1-kΩ resistor, the shunt regulator would still have more than the required 80 µA of operating current.

The power rating of the series resistor should be selected according to the expected power to be dissipated. In normal operation, the resistor would dissipate 43 V x 39 mA = 1.677 W.

Excess current not used by the LMP92064 and isolators circuits will be burned by in the LM4040-5, and this current should never exceed 15 mA.

8.2.2.4 Voltage Channel Input Resistor Divider

The input buffer amplifier of the LMP92064's voltage channel can tolerate high source impedances, which enables scaling the bus voltage with the use of an external resistor divider. The accuracy of the voltage measurements depends on the accuracy of the components used for the resistor divider as well as the impedance of the divider.

In this example, the voltage channel can sense the voltage across R2 (see Figure 23). The main voltage should be scaled to a range below 2.048V by the resistive divider. If the resistive divider is always connected to the bus voltage, the series resistance of R2 + R3 should be adjusted (while keeping their ratio constant) to limit the current across the resistors within a permissible range for the application.

For simplicity, R2 is set to 1.6kΩ and R3 is set to 46.4 kΩ. The bus voltage of 48 V results in 1.6 V across R2 and the current flowing through R2 and R3 is 1 mA.

8.2.2.5 Sense Resistor Selection

The accuracy of the current measurement depends heavily on the accuracy of the current sense resistor. Its value depends on the application and it is a compromise between signal accuracy, maximum permissible voltage loss and power dissipation in the current sense resistor. High resistance values provide better accuracy at lower currents by minimizing the effects of offset, while low resistance values of minimize voltage loss in the load supply section, but at the expense of low-end accuracy.

In this example, the maximum sense voltage at the input of the current sense channel of the LMP92064 is 75 mV. Given the maximum load current requirement of 1 A, the sense resistor should be selected to be smaller than 75 mΩ.

The resolution at the input of the current sense channel of the device is 20 µV / code. To observe a change in the output code for a 1 mA change in sense current, the sense resistor should be larger than 20 mΩ.

8.2.3 Application Curves

The data in the following curves was collected using a 50 mΩ sense resistor, which results in a conversion factor of 2.5 codes/mA. The sense current for the first curve was increased in steps of 100 mA up to 1 A. The sense current for the second curve was increased in steps of 1 mA up to 10 mA. The data was acquired asynchronously at a rate of 2000 samples per second, and each data point is the resulting average of 260 samples.

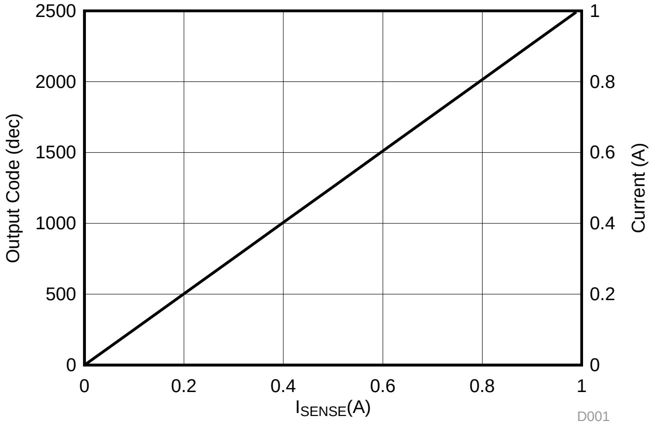


Figure 26. Output Codes in 1-A Range

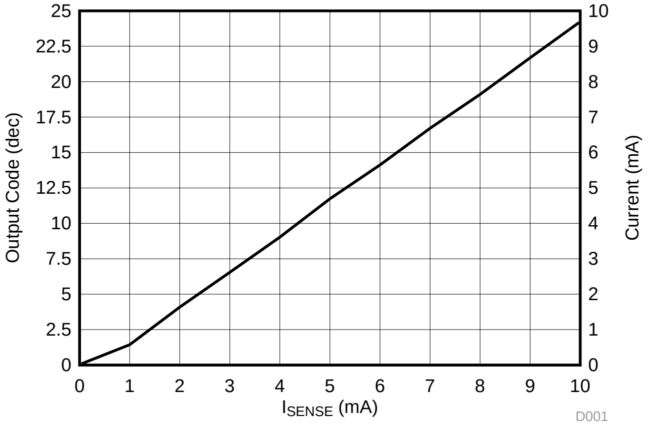


Figure 27. Output Codes in 10-mA Range

9 Power Supply Recommendations

To decouple the LMP92064 from AC noise on the power supply, it is recommended to use a 0.1-μF bypass capacitor between the VDD and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10-μF bypass capacitor may further reduce the supply noise. In addition, the VDIG power pin should also be decoupled to DGND with a 0.1-μF bypass capacitor. Do not forget that these capacitors must be rated for the full supply voltage (2x the maximum voltage is recommended for the capacitor working voltage rating).

10 Layout

10.1 Layout Guidelines

- Connect the sense resistor pads directly to the INCP and INCN inputs of the LMP92064 using “Kelvin” or “4-wire” connection techniques. See the *Current Input Error Sources and Layout Considerations* section for more information.
- Bypass capacitors should be placed in close proximity to the supply pins. It is recommended to use a 0.1-μF capacitor on each supply pin. Additional bypass capacitors can be used.
- A 1-μF ceramic bypass capacitor should be placed in close proximity to the REFC pin.
- The SPI signals traces should be routed close together.
- Series resistors should be placed at the SPI sources.

10.1.1 Current Input Error Sources

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (<100 mΩ), trace resistance shared with the load can cause significant errors. TI recommends connecting the sense resistor pads directly to the INCP and INCN inputs of the LMP92064 using “Kelvin” or “4-wire” connection techniques. An example is shown in Figure 28.

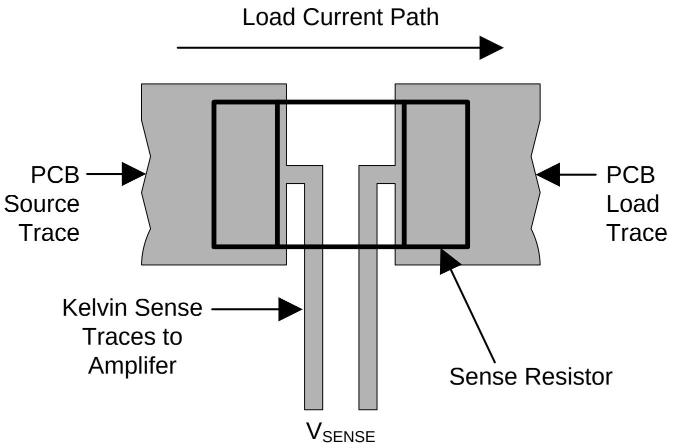


Figure 28. 4-Wire "Kelvin" Sensing Technique

Because the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. The traces should be one continuous piece of copper from the sense resistor pad to the LMP92064 input pin pad, and ideally on the same layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat. To minimize noise pickup and thermal errors, the input traces should be treated as a signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines.

10.2 Layout Example

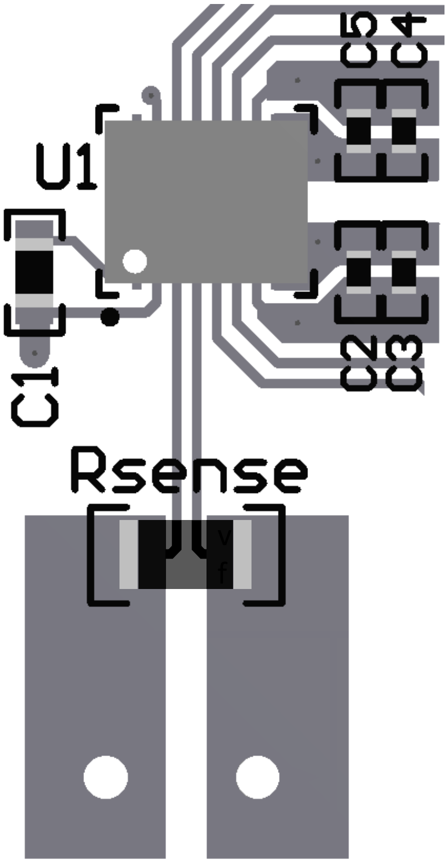


Figure 29. Layout Schematic

11 器件和文档支持

11.1 商标

All trademarks are the property of their respective owners.

11.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP92064SD/NOPB	Active	Production	WSON (NHR) | 16	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	L92064
LMP92064SD/NOPB.A	Active	Production	WSON (NHR) | 16	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	L92064
LMP92064SDE/NOPB	Active	Production	WSON (NHR) | 16	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	L92064
LMP92064SDE/NOPB.A	Active	Production	WSON (NHR) | 16	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	L92064
LMP92064SDX/NOPB	Active	Production	WSON (NHR) | 16	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	L92064
LMP92064SDX/NOPB.A	Active	Production	WSON (NHR) | 16	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	L92064

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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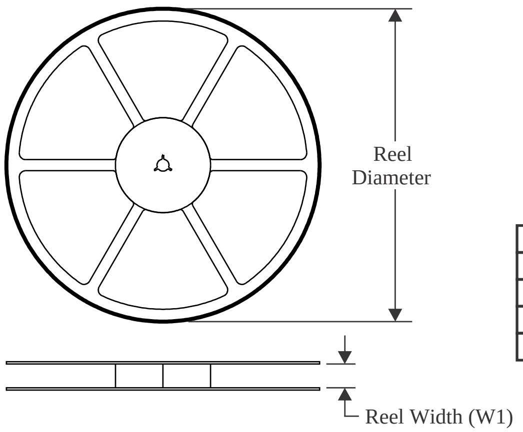
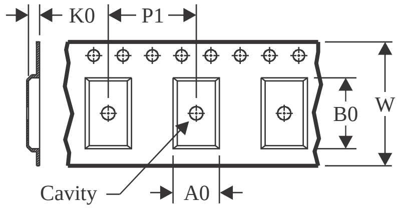
TAPE AND REEL INFORMATION

REEL DIMENSIONS

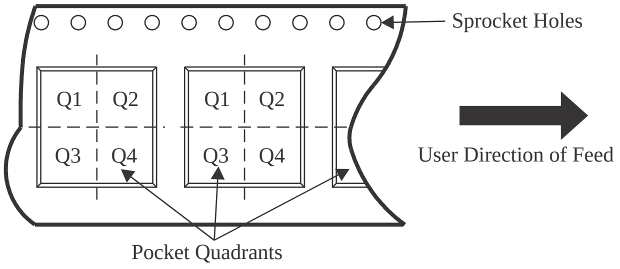


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

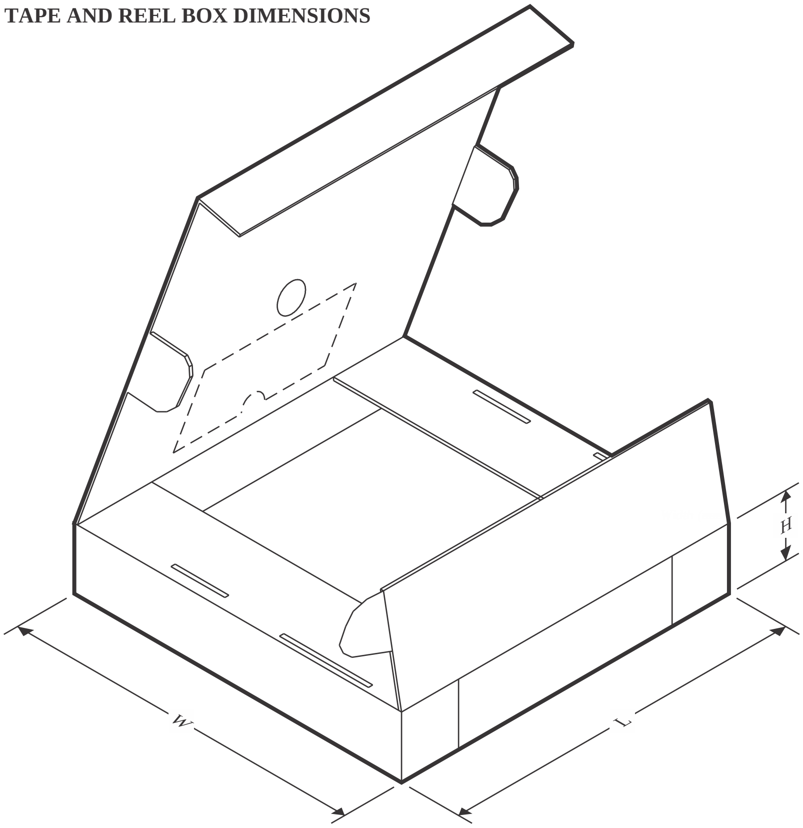
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

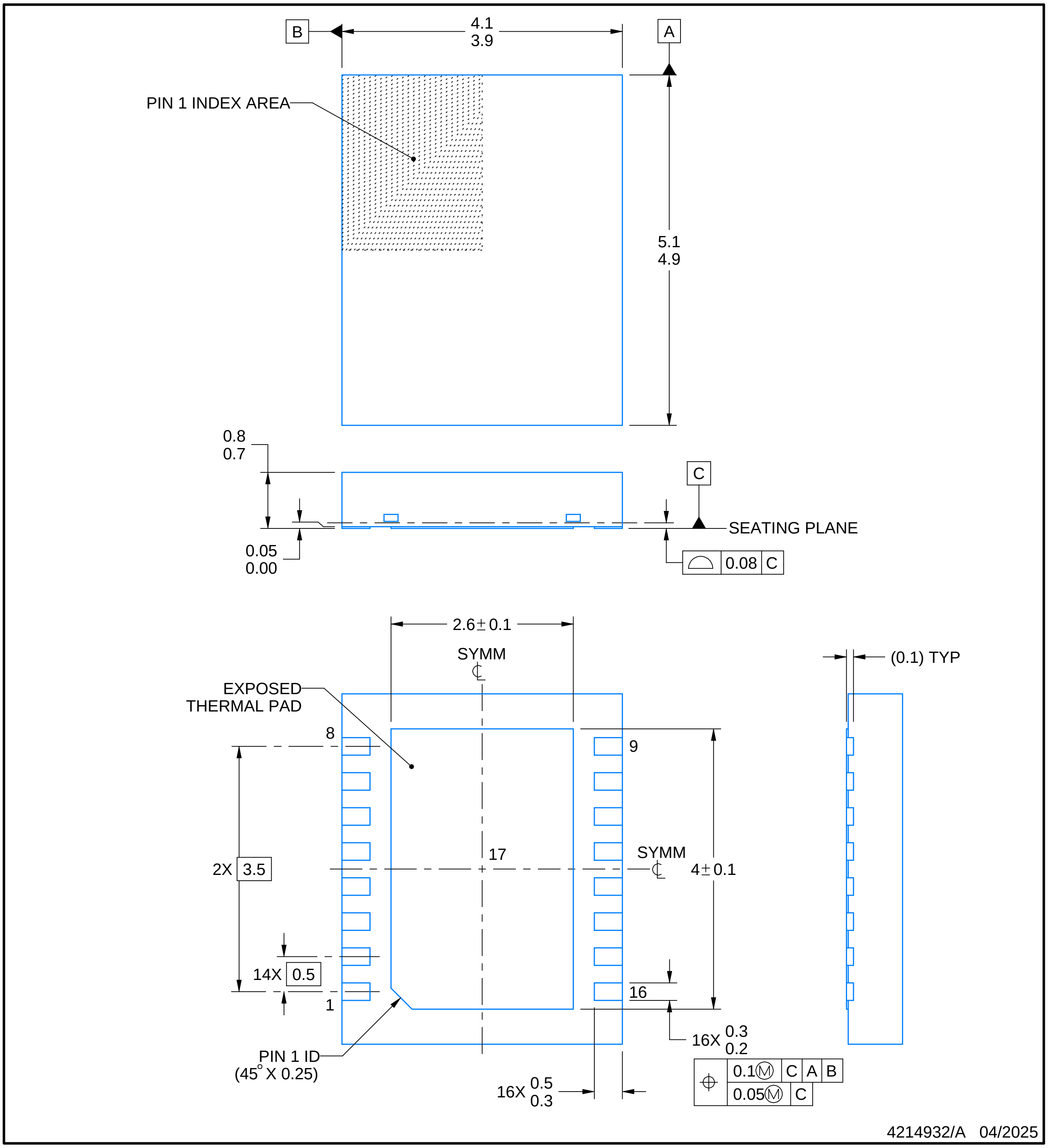
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP92064SD/NOPB	WSON	NHR	16	1000	177.8	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMP92064SDE/NOPB	WSON	NHR	16	250	177.8	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMP92064SDX/NOPB	WSON	NHR	16	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



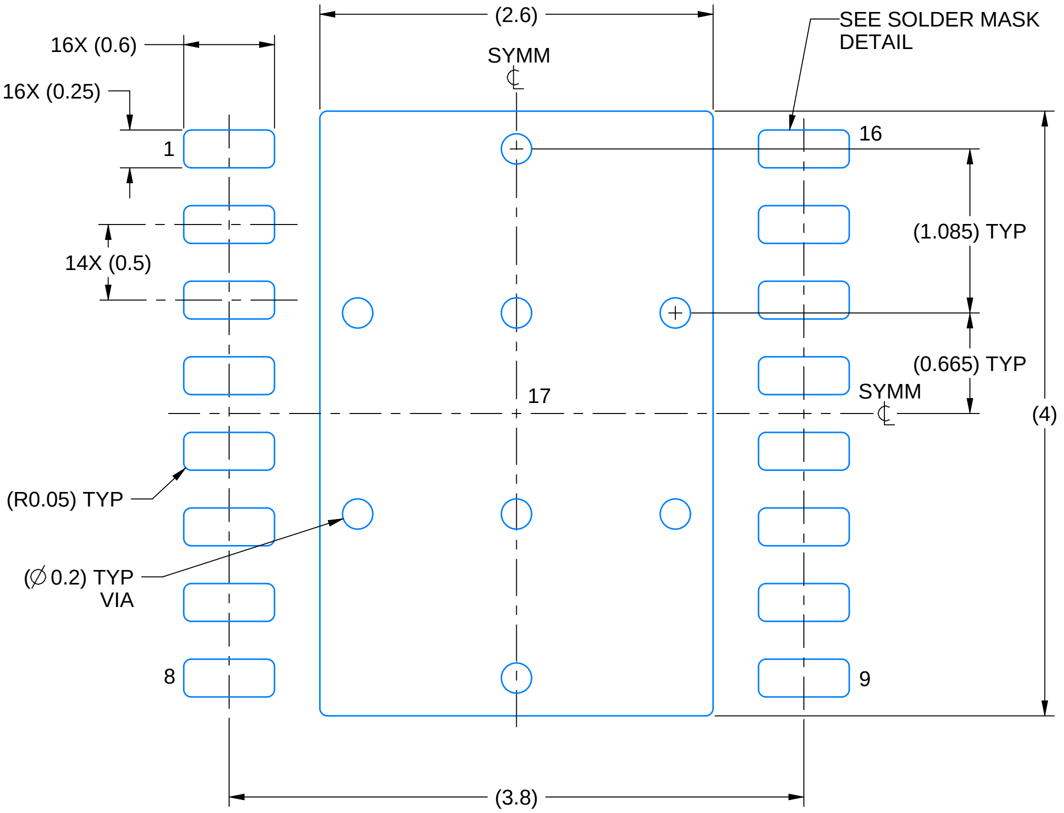
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP92064SD/NOPB	WSON	NHR	16	1000	208.0	191.0	35.0
LMP92064SDE/NOPB	WSON	NHR	16	250	208.0	191.0	35.0
LMP92064SDX/NOPB	WSON	NHR	16	4500	356.0	356.0	36.0

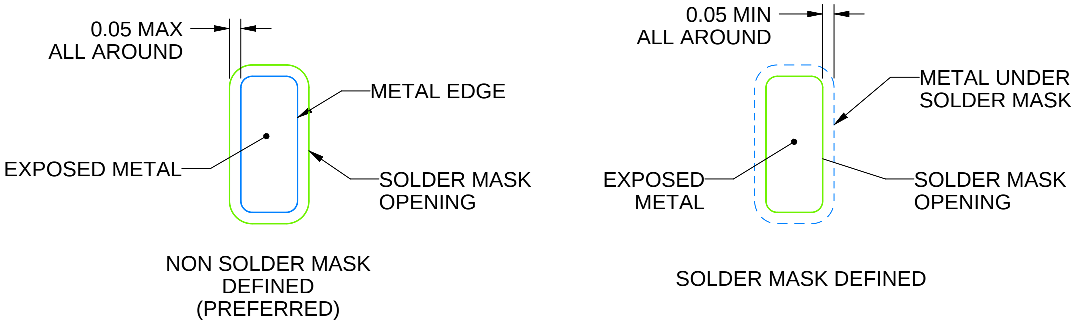


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

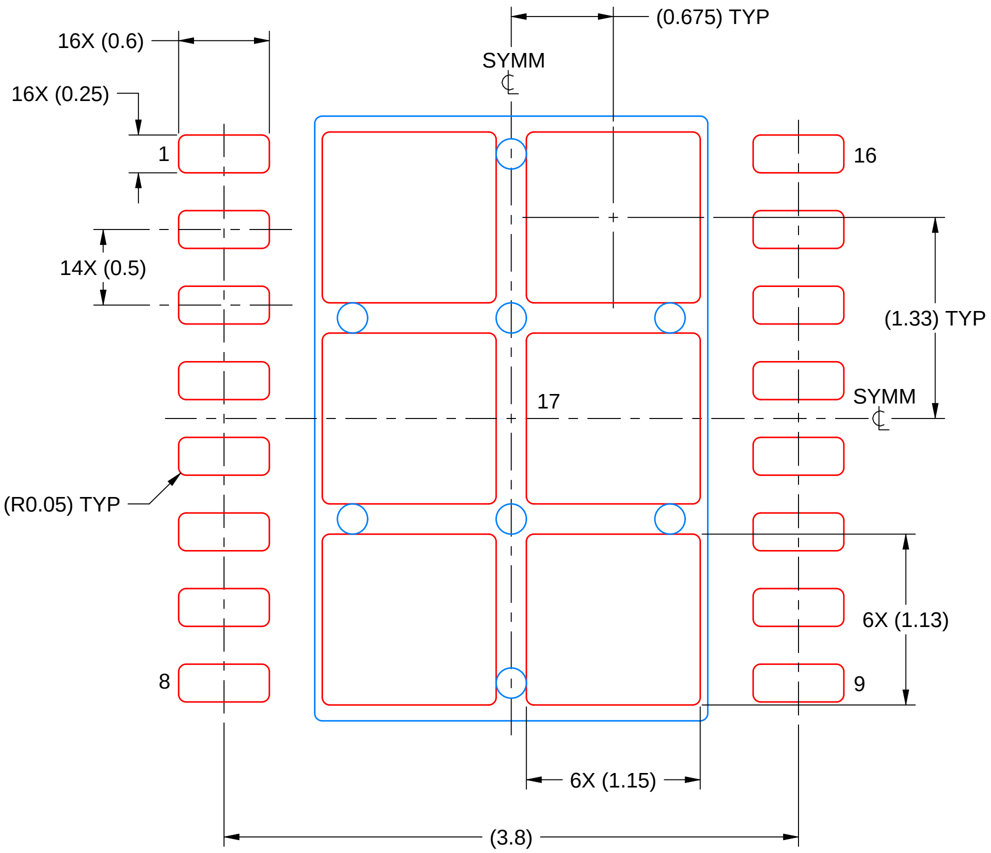


SOLDER MASK DETAILS

4214932/A 04/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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